Skanda Koppula

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ETH Zürich, Fulbright Research Fellowship

Researcher at the Systems Group, Department of Computer Science.   *Sept. 2018 - August 2019*

Massachusetts Institute of Technology

Masters of Eng. and BSc, Computer Science, MEng GPA: 5.0/5.0   *Sept. 2013 - June 2018*

Relevant courses: Hardware Architectures for Deep Learning, Applied Cryptography, Compilers, Machine Learning, Operating Systems, Computer Architecture, Computer Security, Bayesian Inference

Work Experience

NVIDIA Autonomous Driving R&D, Intern   *May 2018 - September 2018*
– Added support for multi-camera vehicle feeds on NVIDIA's training and simulation pipelines.
– Decreased training time by 16% using custom data format to reduce disk reads and CRC overhead.

Google Acoustic Modeling Research Team, Intern   *June 2017 - September 2017*
– Tested kernel factorization to improve cross-domain accuracy of neural language models.
– Developed approach to characterize memory and visualize hidden state of recurrent networks.

Yahoo, Software Engineering Intern   *June 2016 - Aug. 2016*
– Improved malicious login attempt event detection by 7% with a pruned neural network.
– Implemented online updating of the login classifier using data from a multi-company threat feed.

Square Security, Software Engineering Intern   *June 2015 - Aug. 2015*
– Built an in-production service to collect memory dumps from Square card readers
– Simplified firmware bug-fixing by parsing dumps into a human-readable source error trace.

Projects

MIT Driverless (Formula Student Racecar Team), Perception Lead   *August 2016 - Present*
– Demonstrated a 85% mAP/0.8 IoU YOLOv3-based network for racetrack landmark localization.
– Trained and tested an end-to-end driving network for a Formula Student Electric racecar.
– Developed PCBs and firmware for the first open-source automotive battery management system
– Won 2nd place at the 2017 U.S. Formula Student Electric competition (among 53 teams).

Research

MIT Energy Efficient Systems Lab, Master's Thesis   *Sept. 2016 - June 2018*
– Achieved a > 2x speed-up and > 500x decrease in estimated energy consumption for real-time speaker identification by demonstrating an FPGA design capable of neural network inferencing and mel-frequency coefficient extraction.

ETH Zürich Systems Lab, Swiss Government Excellence Scholar   *Sept. 2018 - June 2019*
– Ongoing work to demonstrate faster CNN inference using aggressive DRAM timing parameters and CNNs retrained for bit-error resilience.

Biomedical Cybernetics Lab, Student Researcher   *May 2013*
– Applied Bayesian modeling to develop a genomic-environmental prognostic models to identify patients at-risk or pre-disposed to alcoholism, schizophrenia, and lung cancer.

Skills

Embedded Systems: **C/C++**, **x86 Assembly**.

Hardware and Digital Design: **Altium PCB Designer**, **Vivado HLS**, and **Bluespec Verilog**.

Miscellaneous: **Python** (**TensorFlow, PyTorch, numpy**), **Java**, **Scala**, **bash**.

Research publication list and references are available upon request!