Sandeep Koranne

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OBJECTIVE

To utilize my expertise in large scale algorithm design, implementation, documentation and testing; bringing together diverse fields of graph theory, mathematical analysis, computational geometry, approximation algorithms and algebraic geometry to solve challenging problems.

RESEARCH INTERESTS

Graph theory, computational geometry, combinatorial algorithms, algebraic geometry, parallel programming, compiler optimizations and generic programming.

WORK EXPERIENCE

- **Chief Scientist**, Mentor Graphics Corporation, Wilsonville. (Jan 2014 – Present):
  - Leading a geographically dispersed technical team of engineers,
  - Architect for Power Grid Extraction product (full chip),
  - Responsible for Mentor's Parasitic Extraction Products
- **Software Architect: PEX**, Mentor Graphics Corporation, Wilsonville. (Jan 2011 – Jan 2014):
  - Architect and lead developer of graph theory based layout analysis product for sub-20nm,
  - Architect and lead developer of new parasitic extraction product of Mentor Graphics. Optimized for multi-million net SOC designs, our solution delivers high throughput with field-solver comparable accuracy,
  - Responsible for all aspects of high performance computing, including but not limited to, linear algebra kernels for the field solvers, SMP and distributed computing, SIMD (SSE and AVX) and theoretical research on parallel algorithms (see Research publications). The commercial product runs on 100s of cores with almost linear scaling in the parallel section.
  - Responsible for core computational geometry and graph algorithms, including segment intervalization for *in-die variation* modeling and spatial data structures.
- **Principal Engineer**, Mentor Graphics Corporation, Wilsonville. (Jan 2008 – Jan 2011),
  - Member of core Calibre DRC computational geometry and hierarchy processing team. Worked on optimizing Boolean scanline, OPC, edge-classification, DRC scanline, Boolean operations, and polygon operations. Researched and implemented several new algorithms, including entropy reduced checksum.
  - Architect of Calibre Auto-Waiver solution: designed, implemented automatic DRC error waiver solution. Reduces time-to-market by *waiving* user defined errors from IP cells,
- **Senior Staff Algorithms Developer**, Synplicity Inc., Sunnyvale. (April 2004 – Jan 2008)
  - Lead architect of Physical Synthesis solution for Altera devices: includes algorithm design, implementation, QoR analysis, framework design and product planning.
  - Theoretical analysis and implementation of various edge-disjoint path routing algorithms, placement algorithms, and other analysis to improve quality of synthesis results.
- **Senior Scientist**, Tanner Research, Inc., Pasadena. (September 2001 – April 2004)
  - Designed and implemented state-of-art computational geometry framework for hierarchical VLSI layout analysis. Implemented search structures, predicates, boolean, sizing and fracturing solutions. System capacity was designed to handle multi-million edge data-sets.

- ⋆ Optimization of layout checking rule decks using term rewriting and data flow analysis methods. Implemented support for concurrent execution of layer derivations, multi-processor support, and network-of-workstation (NoW) optimizations. Parser front end written using lex and yacc, back-end is Boost Graph Library.
- ⋆ Multi-layer density and planarization (metal fill): designed and implemented novel algorithm based on linearly separable 2d convolution kernel,
- ⋆ Designed and implemented algorithms for polygon self-intersection and orientation detection and correction, polygon fracturing (NP-complete), and interior cycle (hole) removal (NP-complete),

◇ **Project Leader (embedded core test)**, ED&T/Test, Philips Research Labs, Eindhoven, The Netherlands, (September 2000 - September 2001)

◇ **Software Engineer**, ED&T/Test, Philips Research Labs, Eindhoven (July 1999 - September 2000)

EDUCATION

◇ **Indian Institute of Technology, Delhi**
Masters in VLSI Design, Tools and Technology (interdisciplinary program), Jun 1997-Dec 1998.
Master's program supported by a Fellowship from Texas Instruments India Ltd.,
Thesis: "XPLAN: A methodology to estimate crosstalk in VLSI circuits".

◇ **Maulana Azad College of Technology, (REC), Bhopal**
Bachelor's in Computer Science and Engineering, Aug 1993-May 1997.
Received University Gold Medal and Roll of Honors,
Undergraduate thesis: Solving the VLSI standard cell placement problem using graph partitioning.
Senior year project: A compiler for Pascal subset. Generated .asm code for x86 with register allocation, developed on Linux with lex and yacc, and ported on MS-DOS.

◇ **Awards**

Texas Instruments fellowship from Aug 1997 - Dec 1998.

University Gold Medal for securing 1st position in Computer Science department,

Gold medal in National Science Aptitude Test of India (year 1990).

SKILLS

◇ C++, including C++-11

◇ Linear Algebra, sparse matrix, Intel MKL, distributed computing

◇ Algebraic geometry (polynomials and Gröbner basis methods)

◇ OASIS, GDSII, VSB, MDP, Spatial data-structures, scanline

◇ Large system design and implementation in C++

◇ Lisp, Erlang, Python, Lex, Yacc

◇ System knowledge of CUDA, LLVM, NESL, REDUCE, OpenMP

◇ Strong background in algorithms, algebra, graph theory and computational geometry

◇ System level knowledge of Linux and GNU tools, Cygwin and Visual Studio .Net

◇ Others: Qt, POSIX threads, SIMD Vectorization, OpenGL, Motif

◇ LaTeX, Documentation, fluent in spoken/written English and Hindi

INDUSTRY AWARDS

◇ Exceptional performance awards from Mentor Graphics in 2011,

◇ Winner of Sun Studio 12 Contest
http://skoranne.blogspot.com/2009/08/engineering-discrete-geometry.html

◇ Performance award from Synplicity (2004-2005),

◇ Performance award from Tanner EDA for HiPer Verify,

PUBLICATION

Book(s)

- ◇ Open Source Tools for Scientists and Engineers, Springer, 2010.
- ◇ Practical Computing on the Cell Broadband Engine, Springer, 2009.

Tanner internal publications :

- ◇ Algorithm for polygon data validation, interior cycle removal and fracturing,
- ◇ A system for performing hierarchical layout verification.

Philips internal publications :

- ◇ Architecture Specification of AMDC BistShell: describes the design and implementation of a CTAG compliant programmable BistShell delivered by AMDC (Advanced Memory Design Center, a Philips internal memory design group),
- ◇ Application note: Extending the InBIST algorithm for MFSRAM.

External publications (partial list) :

- ◇ "Online Streaming of Intersection Graph", Accepted at SIAM Conference on Discrete Math, 2014,
- ◇ "Constructing Small-Signal Equivalent Impedances Using Ellipsoidal Norms", ISQED 2014,
- ◇ "Design and Implementation of a Distributed Spatial Data Structure", Poster in SIAM PP 2014,
- ◇ "Data-Parallel Implementation of Quadrature Methods for Complex Numbers", WPEA 2013,
- ◇ "Application of Sparse Tensors for Optimizing Multi-Dimensional VLSI Electromagnetic Analysis", FEMTEC, 2013,
- ◇ "Analysis of Very Large Resistive Networks Using Low Distortion Embedding", ISQED, 2013,
- ◇ "VLSI Layout Analysis Using PGAS Programming", Partitioned Global Address Space, 2012,
- ◇ "Entropy-reduced hashing for physical IP management", with Bikram Garg, John Ferguson and Manish Khanna, ISQED 2011,
- ◇ "An innovative method to automate the waiver of IP-level DRC violations", with John Ferguson and David Abercrombie, Mentor Graphics, ISQED 2010.
- ◇ "Combinatorial Polytope Enumeration", with Anand Kulkarni, work in progress, *http://arxiv.org/abs/0908.1619*
- ◇ "On enumeration of simple polytopes", with Anand Kulkarni, SIAM DM 2010.
- ◇ "Design and Implementation of a Parallel SIMD Algorithm for Finding Complex Roots of Functions on the CELL Processor", SIAM CSE 2009, Miami, FL,
- ◇ "Design and Implementation of Real Time Quick Look SAR Image Generation System on the Cell Broadband Engine", Indian Society for Remote Sensing, Ahmedabad, December 2008.
- ◇ "Large-scale Polytope Diameter Experiments using the CBE Processor: Towards a Resolution to Hirsch's Conjecture", with Anand Kulkarni, SIAM Workshop on Combinatoric Scientific Computing, 2007,
- ◇ "A Note on System-on-Chip Test Scheduling Formulation", *Journal of Electronic Testing: Theory and Applications*, Vol. 20, No. 3, pp. 309–315.
- ◇ "A High Performance SIMD Framework for Design Rule Checking on Sony's PlayStation2 Emotion Engine Platform" (ISQED 2004, San Jose, March 2004),
- ◇ "Design of Reconfigurable Access Wrappers for Embedded Core Based SoC Test", *IEEE Trans. VLSI Systems*, Vol. 11, No. 5, October 2003, pp. 955–960,
- ◇ "Formulating SoC Test Scheduling as a Network Transportation Problem", *IEEE Trans. Computer Aided Design of Elec. Systems*, Vol. 21, No. 12, December 2002, pp. 1517–1525,
- ◇ "On the Use of $k-tuples$ for SoC Test Schedule Representation" (jointly authored with Vikram Iyengar), *Proc. International Test Conference*, 2002, Baltimore,
- ◇ "A Novel Reconfigurable Wrapper for Testing of Embedded Core-Based SOCs and its Associated Scheduling Algorithm", *Journal of Electronic Testing: Theory and Applications*, Vol. 18, No. 4, pp. 415–434. This issue of JETTA is also available as a book from Kluwer.

- ◇ "A Framework for Automatic Analysis of Geometrically Proximate Nets in VLSI Layout", (with O. P. Gangwal), Proceedings of the European Conference on Circuit Theory and Design, 2001,
- ◇ "On a Problem of Turán", Proceedings of the European Conference on Combinatorial Optimization, May 2000.
- ◇ "A Distributed Algorithm for k-way graph partitioning", Proceedings of EUROMICRO 99, pp. 446–448,
- ◇ "On Maximal Graphs with a k-Clique" (with R. Sharma and P. Limaye), Proceedings of ICECS 99, pp. 1415–1418,
- ◇ "Using Wire-length Estimation to Predict Coupling Length in VLSI Circuits", Proceedings of the 3rd IEEE Workshop on Signal Propagation in Interconnect, 1999.
- ◇ "A Bit-bucket Data Structure to Optimize Local Search for Microword Length Minimization", Proceedings of the IEEE Canadian Conference on Electrical and Computer Engineering, pp. 507–512, 1999,
- ◇ "A Distributed Algorithm for the Estimation of Average Switching Activity in Combinational Circuits", Proceedings of HPCN' 99, Lecture Notes in Computer Science, Springer-Verlag, pp. 1031–1034.

PATENTS

- ◇ Filed several US and International patents from 2008-Present.

EXTRA CURRICULAR

Indian Classical Music (Instrumental Sitar) performer and teacher. Performed in All India Radio (1990-1993)

Kukkiwon (World Taekwondo Federation) certified 1st Degree Black Belt in Taekwondo 2013

Mentor for high school students in Mathematics (Wilsonville High) for Intel Science Fair 2012, 2013.

- ⋆ "Analysis of the Erdös Distance Problem in Modular Elliptic Space", joint work with high school seniors Markus Woltjer and Richard Sala, 2013
- ⋆ "Graph Theory and Locality Sensitive Hashing for DICOM Image Analysis", joint work with Markus Woltjer, 2012.

VISA STATUS

Greencard holder. Indian citizenship.

REFERENCES

Available on request.

Some of my software in Action

Sandeep Koranne

1 xACT : Parasitic Extraction from Mentor Graphics Corporation

I am responsible for the overall architecture, research, design and implementation of parasitic extraction products within Mentor Graphics. I have implemented significant parts of the software including core computational geometry algorithms, graph algorithms, spatial data-structures and parallel implementations.

2 Drc AutoWaivers in nmDRC from Mentor Graphics Corporation

I was responsible for the research, design and implementation of *autowaivers* in nmDRC from Mentor Graphics. Please see documentation of DRC AutoWaivers for more details on this project.

3 Analysis of the Erdös Distance Problem in Modular Elliptic Space

Joint work with Markus Woltjer and Richard Sala, both high school students at Wilsonville High. Using the PARI software we showed that almost in all cases, the number of unique distances in a modular elliptic field follows a trimodal pattern. This is a non-trivial result to prove, but our experimental results are providing some interesting data for further analysis. This project won the Oregon state competition and went on to Intel International Science Fair 2013.

4 Graph Theory and Locality Sensitive Hashing for DICOM Image Analysis

This is joint work done with Markus Woltjer, a high school student at Wilsonville High.

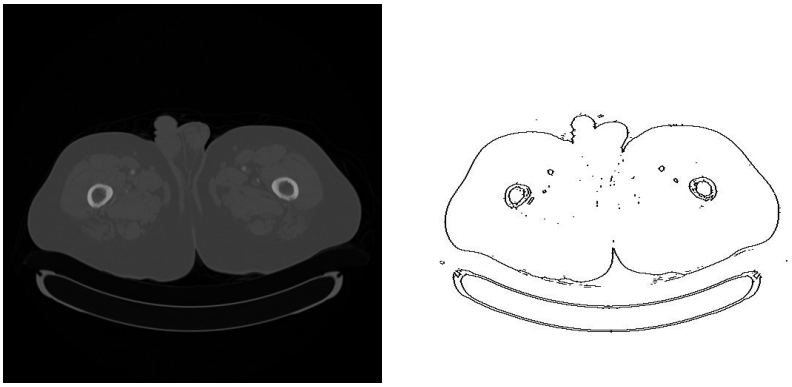

Figure 1: DICOM image of a kidney and its graph representation

The graph representation is then used to construct an *hash* function on the image which can be used for automatic classification of organs. This project won the Oregon state competition and went on to Intel Science Fair 2012, where it won 3rd place internationally.

5 Enumeration of Simple Polytopes

Alongwith Anand Kulkarni (PhD candidate at the IEOR Department at Berkeley) I have invented and implemented a method for combinatorial enumeration of simple polytopes. The produced d-regular graphs are of independent interest and I have written a graph post-processor and analyzer. The algorithm works by starting from a d-simplex, calculating vertex sets for removal using a hyperplane. The algorithm works on the combinatorial face-lattice structure of the polytope, and generates all polytopes of a given dimension, and facet count. The complete face-lattice and combinatorial structure of the polytope is output.

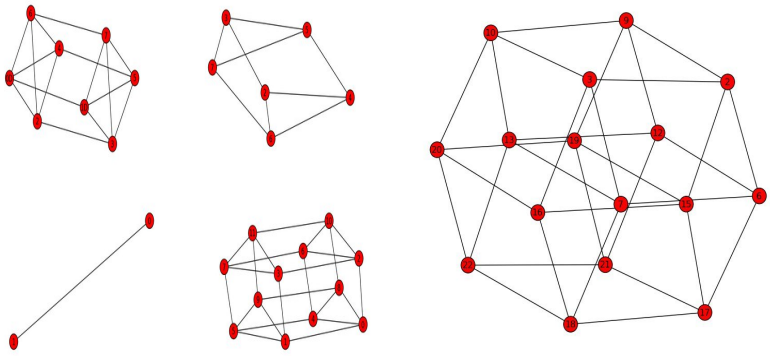

Figure 2: 4-dimensioned cube produced by our algorithm

```
VERTICES_IN_FACETS
{ 0 1 2 3 4 5 6 7} { 0 2 4 6 8 10 12 14}
{ 1 3 5 7 9 11 13 15} { 0 1 2 3 8 9 10 11}
{ 0 1 4 5 8 9 12 13} { 2 3 6 7 10 11 14 15}
{ 4 5 6 7 12 13 14 15} { 8 9 10 11 12 13 14 15}
```

Programming language: C++ and Python, OS: Linux, Solaris 10 x86,x86_64,Sparc.

6 Software written on the Cell Broadband Engine

For my book “Practical computing on the Cell Broadband Engine”, I wrote a number of compute kernels:

- Computation of complex roots of single variable complex function
- Synthetic Aperture Radar (SAR) image processing
- Moment calculation in streaming data using perfect hashing
- Structure determination of molecules using partial data functions
- Line-of-sight computation
- Merit factor of sequences and auto-correlation

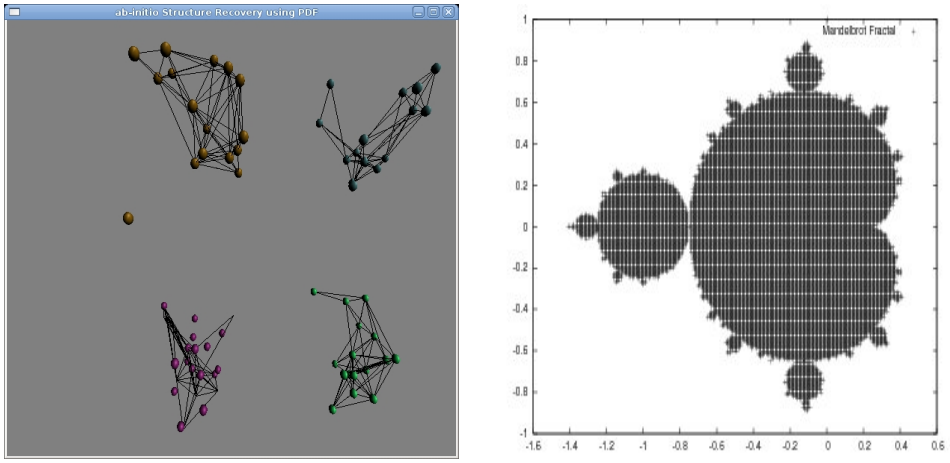

Figure 3: Structure determination using partial distance functions and Mandelbrot evaluation

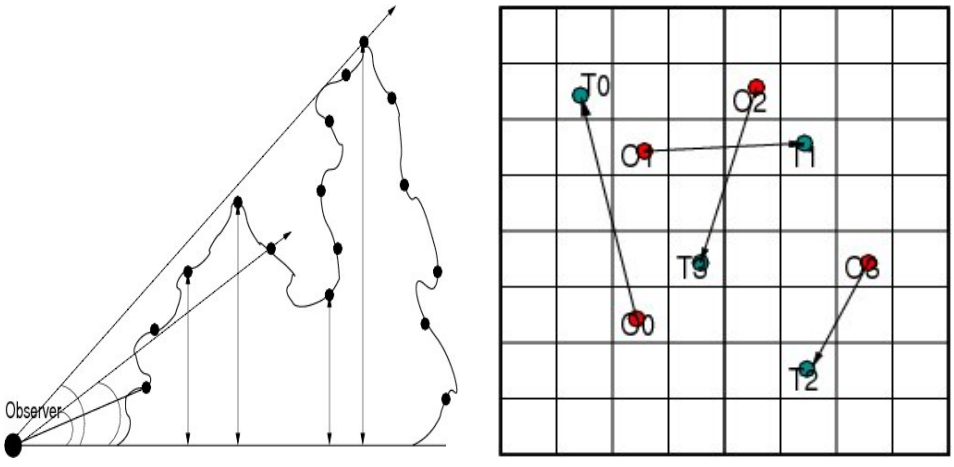

Figure 4: Landscape profile and computation of line-of-sight

7 Mask Data Preparation Toolkit, OASIS, OASIS.VSB

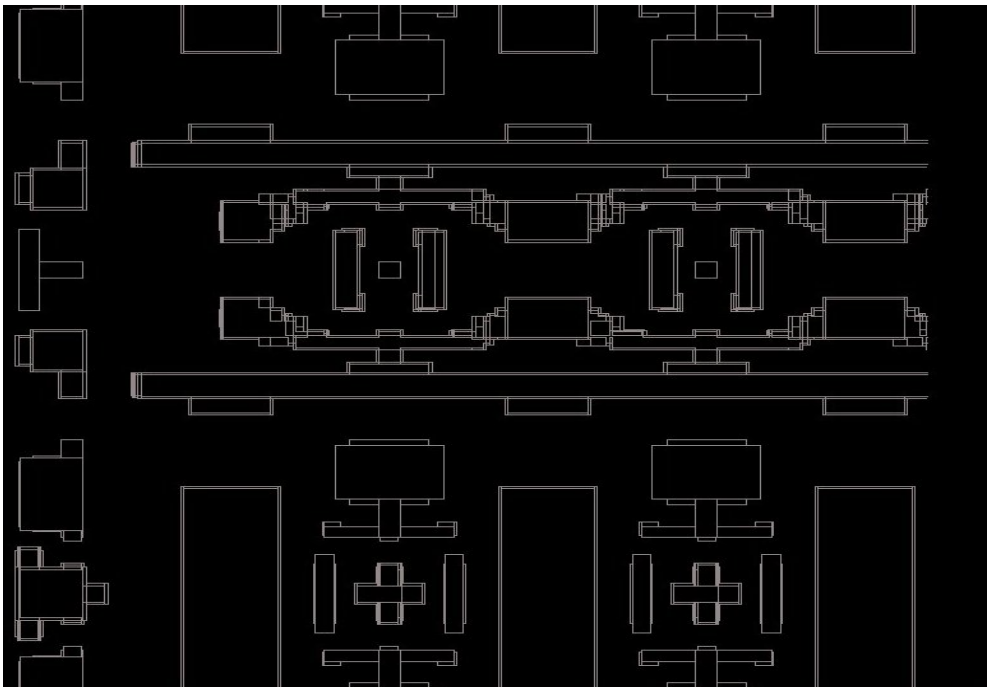

Figure 5: Trapezoidal decomposition, Boolean operations, DRC

A complete implementation of Boolean operations, including, Density and Edge decomposition on hierarchical geometry which could be input as GDSII Stream, OASIS, OASIS.VSB, CIF, Mag. This program uses novel discrete geometry formulations of computational geometry primitives to get speedup of complex Boolean operations. Rule file format is:

```
define input dataset d1 = design.oas
define output dataset o1 = c.oas
begin
    o1:46 = d1:46 + d1:100
    o1:43 = d1:43 + d1:100
    o1:49 = d1:43 * d1:46
end
```

Programming language: C++, OS: Linux, Windows, Solaris 10 x86,x86_64,Sparc.

8 Optimized VLSI Rendering Solution Using OpenGL

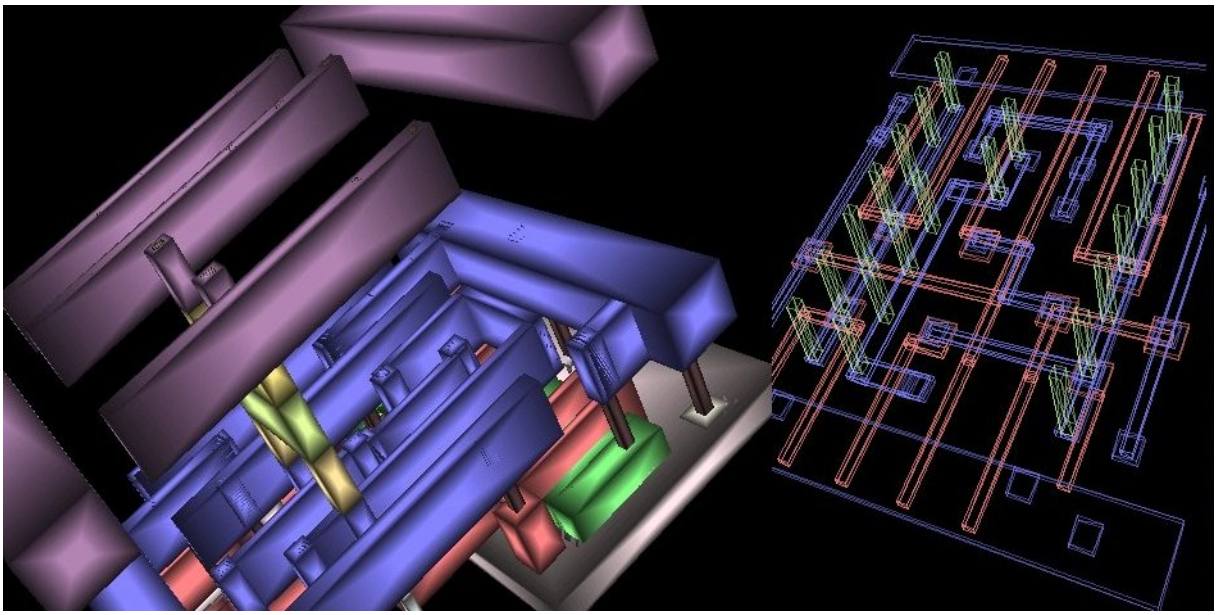

Figure 6: VLSI Layout Viewer

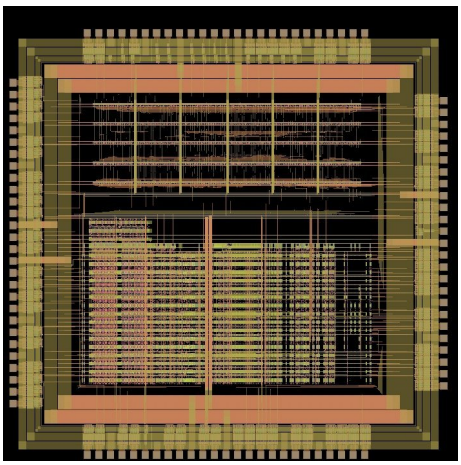

Figure 7: Full Chip VLSI Layout Viewer

A complete implementation of multi-format VLSI layout viewer optimized for Gb size layout data. Special optimizations of hierarchical and OASIS repetitions, spatial data-structures and OpenGL on modern GPU (using texture mapping). Supports on-screen measurement, color maps, mip-maps, user-specified texture map, 3d-view, wire-frame view and process simulation animation view. Programming language: C++, OS: Linux, Windows, Solaris 10 x86,x86_64,Sparc.

9 EDA and Combinatorics on CELL Broadband Engine

Large-scale Polytope Diameter Experiments using the CBE Processor: Towards a Resolution to Hirsch's Conjecture

With the release of the Cell Broadband Engine-based Playstation 3 in November 2006, a low-cost vector processor has become available to the research community for high-performance computing and combinatorial experiments. To demonstrate its effectiveness, we are using the Cell Processor to search for a counterexample to Hirsch's conjecture in its d-step form, an important open question in the theory of optimization. We present results on the generation and analysis of 2^{25} random d-regular graphs per day with up to 112 vertices.

Our implementation of the Floyd-Warshall (FW) algorithm has a peak performance of 56 GIPS (equivalent to giga-flops) on the Cell processor with almost linear speedup on the 6 vector processing elements, exceeding previous performance benchmarks by a factor of 18. This demonstrates that the CBE can be an effective supercomputing platform for attacking graph-based combinatorial challenges. Published at: The SIAM Workshop on Combinatorial Scientific Computing (CSC07), Costa Mesa, CA.February 17 - 19, 2007

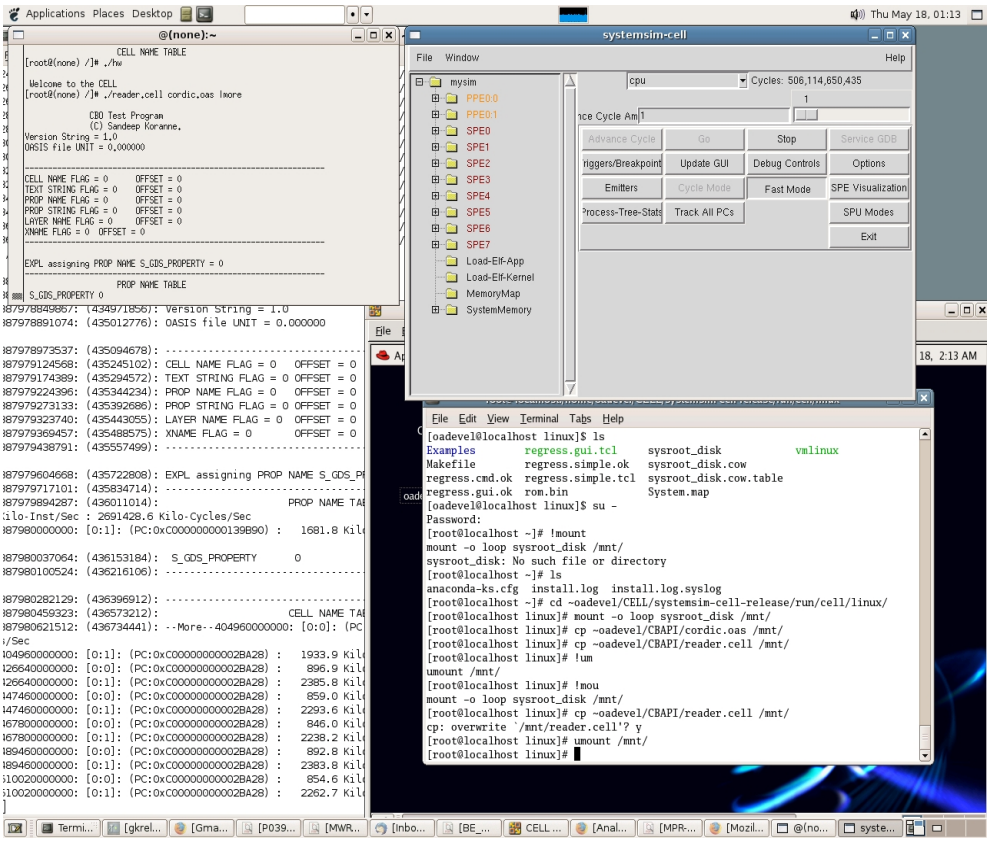

Figure 8: OASIS/GDSII geometry processing on the CELL Broadband Engine.

10 Foundry compatible DRC ©Tanner EDA, Pasadena

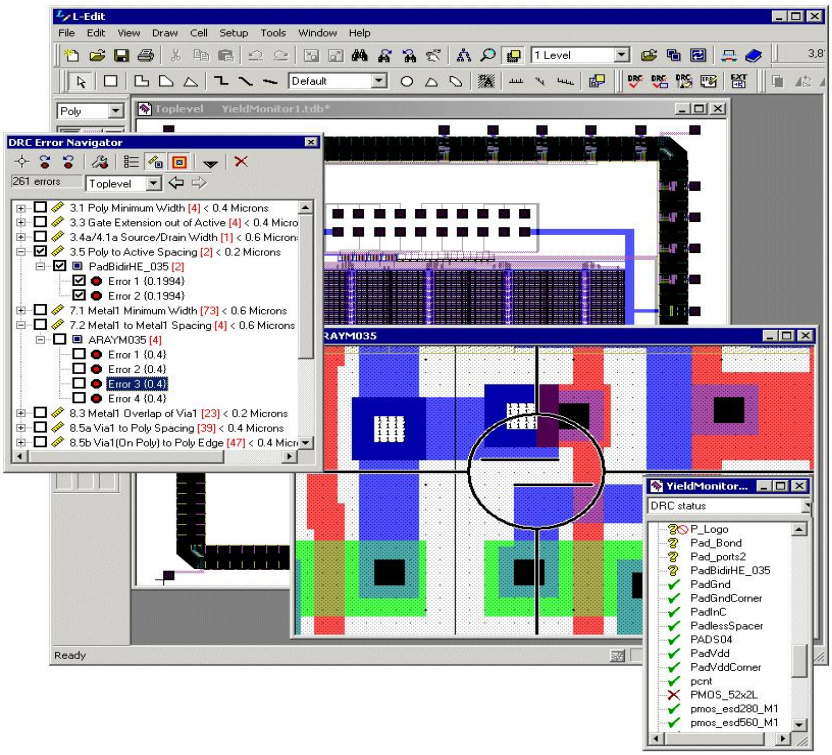

Figure 9: HiPer Verify DRC (C) Tanner EDA 2004.

This is an inset from the HiPer Verify DRC product of Tanner EDA (www.tannereda.com). I was heavily involved in the computational geometry and other algorithmic aspects of this product. I am also responsible for hierarchical connectivity representation, and the development of a high-performance hierarchical electrical rule checking product, and Extract product.

Specific skills which were very pertinent to this project included, computational geometry algorithms like plane-sweep, trapezoidal decomposition, polygon operations, hierarchical operations on VLSI data, sorting and searching (with multi-dimensioned data), Object Oriented Programming, Generic Programming, GDS/LEF/DEF/Oasis/Spice/SDF file formats and their manipulations. Since modern VLSI designs are very regular and highly hierarchical, it is my opinion that any successful EDA tool must (at least) try to utilize this repetitive nature of input. This leads to a very high performance gain, much more that can be gained by doing local optimization on a flat data set.

11 Procedural rendering of VLSI layout on PlayStation

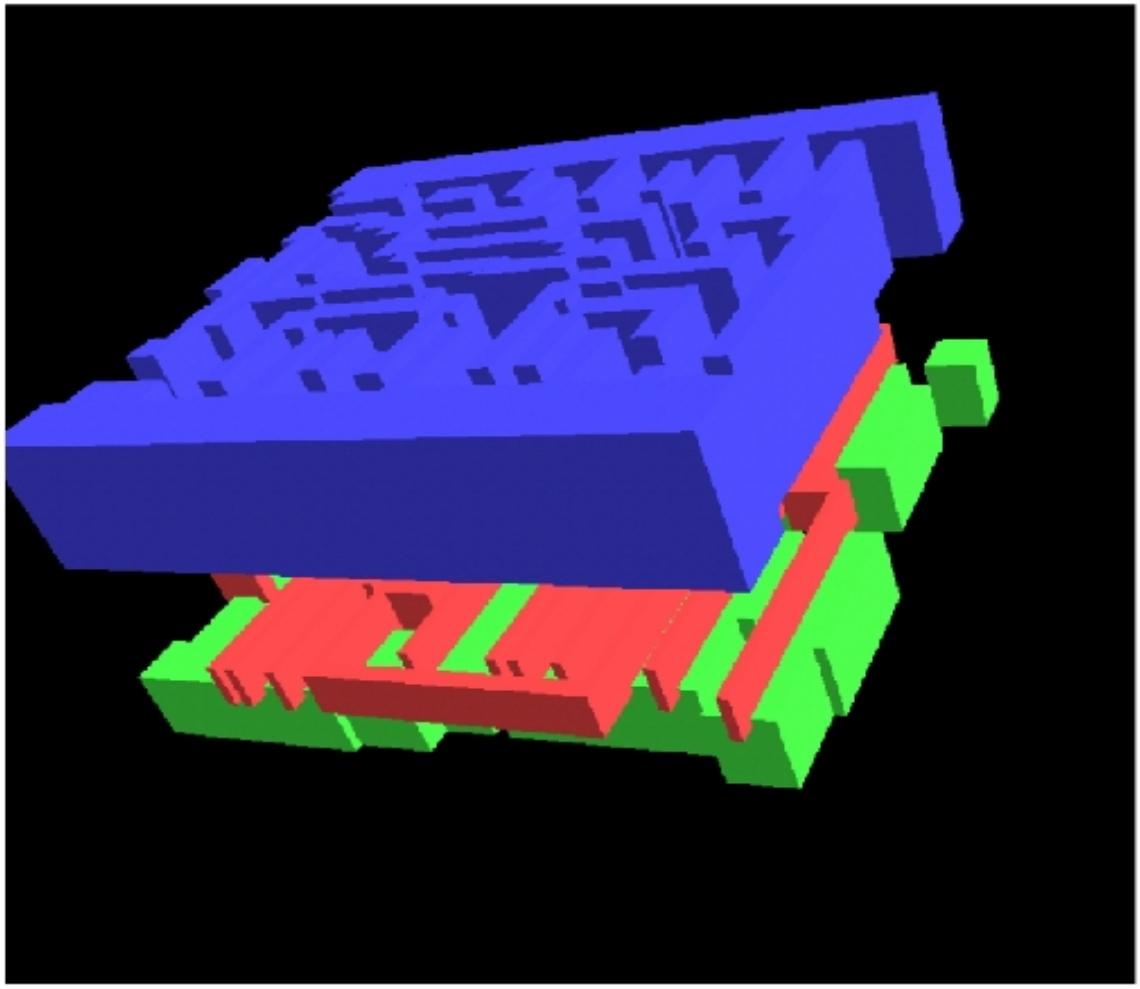

Figure 10: Procedural rendering on the PlayStation.

Ever since the release of the PlayStation Linux kit in 2002 I had wanted to use the Gigaflop category computing power of the Vector Units in the PS2 for an EDA task. I have implemented a restricted DRC on the Vector Processors, and then looking at the phenomenal graphics capabilities of the PS2, I have implemented a 3d rendering system which can be used to render VLSI layout. The user can zoom in, pan, select layers using the PS2 Dualshock controller. Initial performance tests show rendering speeds of 10-14 million triangles per second.

The rendering system uses the VLSI layout data represented as a 2d polygon, and then uses z-extrusion based on process data for layer height.

12 RICT: Randomized Incremental Construction of Trapezoids

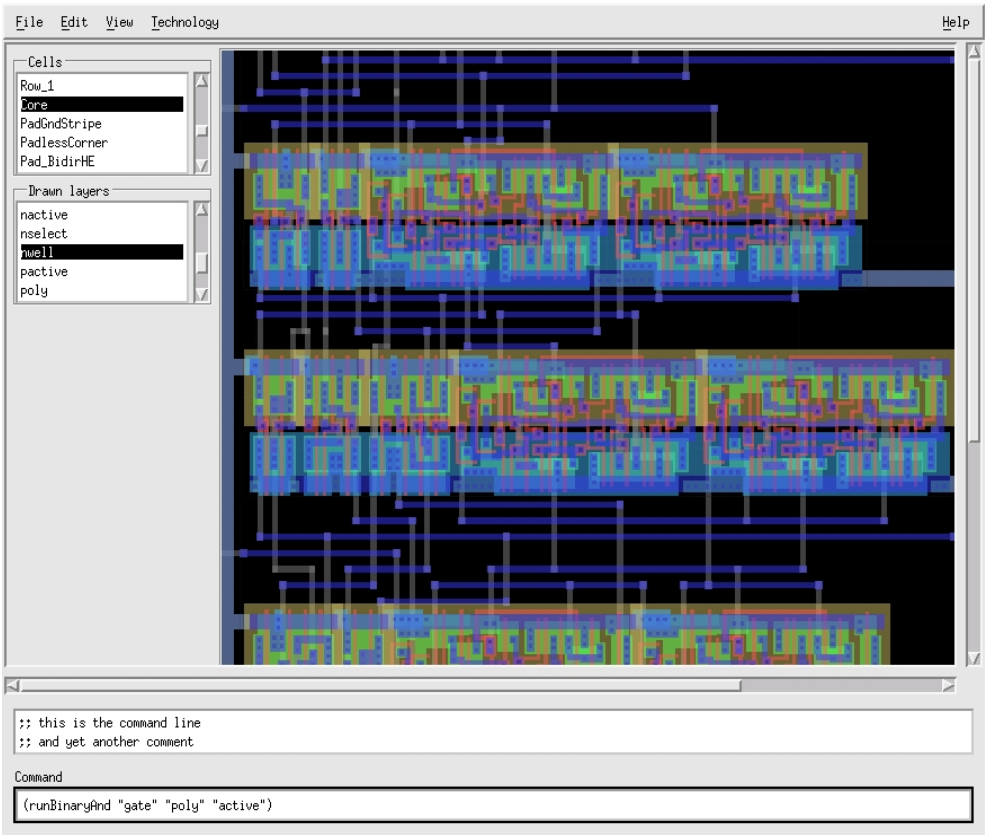

Figure 11: The OpenGL display using Motif xmDrawingAreaWidgetClass widget.

The RICT project is an implementation of Mulmuley's randomized algorithm for computing trapezoidal decompositions. The system has been written over a period of 3 years and has 35,000 lines of C++ code (all written by myself). The system sports a high performance OpenGL based visualization system for viewing VLSI layout and the decomposition. There is integrated Scheme language interface and the whole system is wrapped in a GUI developed in Motif. The low level functions are multi-threaded using the PTHREAD library.

The Scheme language interface to program internals means that once the low level algorithms were in place much of the development could be prototyped in Scheme:

```
(ReadTechFile "mycmos.tech")
(ReadDatabase "../GDS/lm.gds")
(SetRootCell "Topcell")
(if (isDatabaseValid?)
    (display "Databse read in correctly.")
    (begin
      (display "Database corrupted. Exiting") (quit)))
;; Testing the addition of a derived layer, and the DB extent operation
(runDBExtent "__db_extent__")
(RemoveLayer "metal1")
(RunBinaryAnd "gate" "poly" "active")
(vAddLayer "gate")
```

Skills gained with this project include, (i) project configuration using Autotools, (ii) CVS management (iii) in-depth knowledge of Boost C++ libraries (particularly Boost graph library), (iv) pthread, (v) OpenGL, (vi) Scheme integration and (vii) Motif.

13 SOC Toolkit: A tool for Embedded Core Test Scheduling

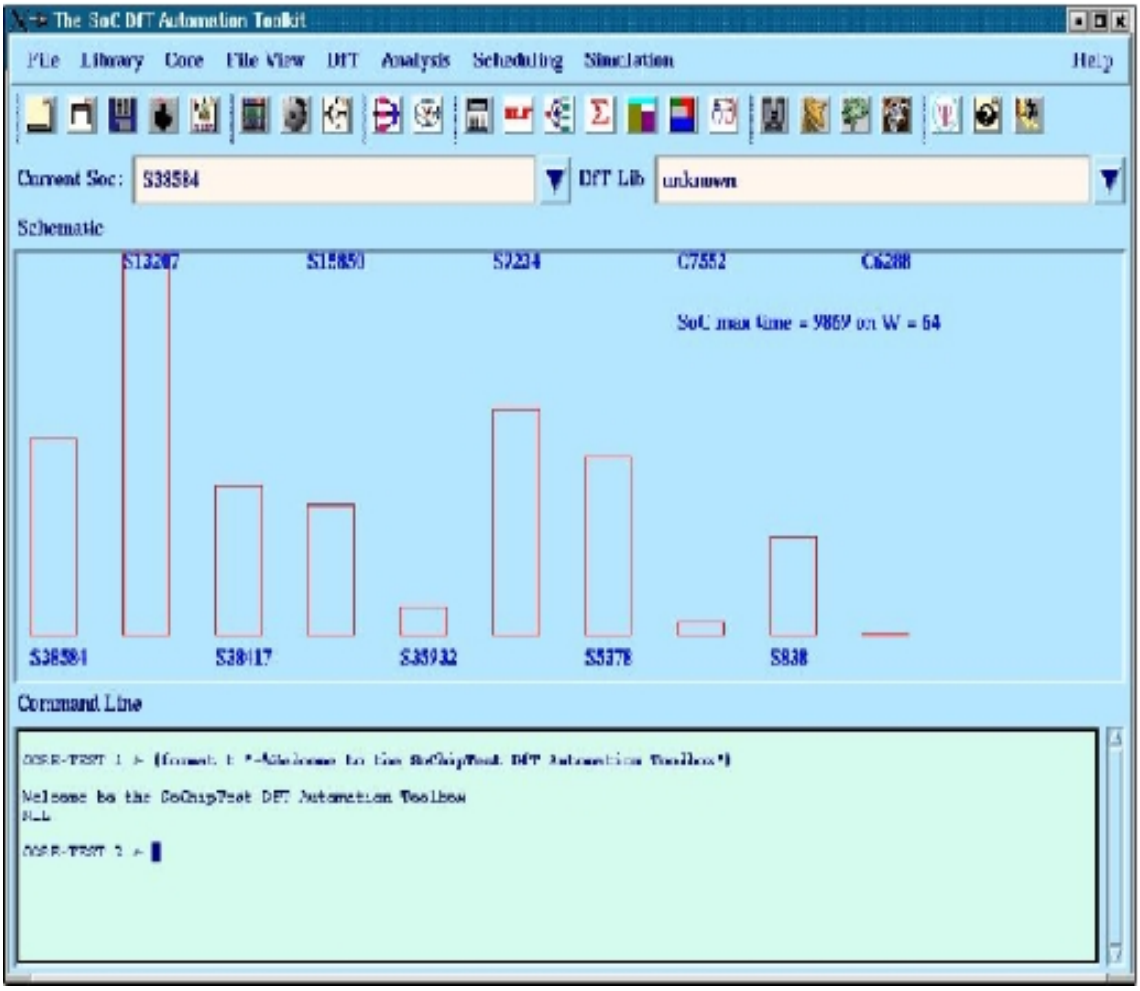

Figure 12: Embedded core test scheduling software.

The SOC Dft Automation Toolkit was developed as a companion to the papers I wrote on embedded core test scheduling problem. The system in its entirety comprises of 25,000 lines of Comman Lisp code. The Common Lisp implementation used for development was CMUCL, although the screen-shot shown above was generated using Xanalys Lispworks. The GUI sports a work pane showing the current test times for all cores in the SoC, and a command line where the user can type Lisp code and perform interactive runs. The system ran on Linux, Windows, HP-UX 11.0 and SunOS.