Sandeep Koranne

West Linn, OR 97068 (971) 276-9431 (M)
sandeep.koranne@gmail.com

WORK EXPERIENCE

- **Chief Scientist & Principal Key Expert**, Siemens EDA. (January 2008 – Present)
  - Expert in EDA flows and formats, including but not limited to, High-level Synthesis (Catapult), Logic synthesis, FPGA design, place-and-route (LEF/DEF), DRC (SVRF), GDSII, OASIS, OPC, MDP, DFT. Mixed signal design (Tanner, Virtuoso), analog design, parasitic extraction (analog and digital), SPICE simulation (AFS), Monte-Carlo (Solido), IC-design flows.
  - Veteran leader, responsible for Calibre xACT certification on multiple advanced nodes.
  - Advanced computational geometry algorithms for curvilinear data (photonics, ILT, MDP).
  - Ensure customer success; win competitive benchmarks; gain market-share; new product ideas.
  - Several key inventions, patents, publications; providing technical leadership and influence to global team. Hands-on leader, responsible for all aspects of business success for product.
- **Senior Algorithms Developer and Director**, Synplicity Inc. (April 2004 – January 2008)
  - Design, development, integration and testing of Synplicity's Amplify FPGA Physical Optimization tool using advanced graph theory algorithms and enumeration.
- **Senior Scientist**, Tanner Research, Inc. (September 2001 – April 2004)
  - Development of a high-performance foundry compatible hierarchical layout verification.
- **Project Lead**, Philips Research Labs, The Netherlands, (July 1999 - September 2001) Worked on LogicBIST, MemoryBIST, and Core ReUse.

EDUCATION

- **Oregon State University, Corvallis, OR** July 2019
  MS (Math): Thesis topic "High-Order Finite Difference Methods for Nonlinear Optical Media".
- **Indian Institute of Technology, Delhi**
  Masters in VLSI Design, Tools and Technology (interdisciplinary program), Jun 1997-Dec 1998.
  Master's program supported by a Fellowship from Texas Instruments India Ltd.,
  Thesis: "XPLAN: A methodology to estimate crosstalk in VLSI circuits".
- **Maulana Azad College of Technology, (REC), Bhopal**
  Bachelor's in Computer Science and Engineering, Aug 1993-May 1997.
  Received University Gold Medal and Roll of Honors,
  Undergraduate thesis: Solving the VLSI standard cell placement problem using graph partitioning.

AWARDS

- Winner of the Sun Studio 12 Contest 2010 (http://skoranne.blogspot.com).
- Exemplary achievement award at Synplicity and Mentor.
- University Gold Medal and Roll of Honor for securing 1st position in Computer Science.

SKILLS

- Expert in SVRF, DRC, LVS, PEX, OPC, MDP, Synthesis, Place&Route.
- Delivered tech talks, panel sessions, standardization committees.
- Expert in CMOS, VLSI, Lithography, and semiconductor manufacturing, foundry relations.
- Attention to detail, self-motivated, fast learner, team player with big picture view.
- MKL, Eigen, Ceres, SuiteSparse, LLVM, TVM, Halide, TC, XLA, AI and ML software stack.
- C++11/14, C, Julia, Common Lisp, Fortran, Python, Erlang, Lex, Yacc.
- Applied Mathematics and numerical methods, using Reduce, Maxima, and Singular.
- Author of two books and several (more than 50) peer reviewed, archived papers.
- Written large software individually. Scientific computing on Intel, Power, ARM, PS2 and PS3.