Analogue Devices
Project

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October 31, 2019

Date Performed: May 31, 2017
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1 Objective

This project requires the design of a simple current mirror, such that the current which passes through the resistor, R, is 150µA, and the minimum voltage, v_{DS}, is 0.25V. The designed circuit is simulated using PSPICE to verify the correct operating characteristics.

2 Design

The circuit topology can be seen in Figure 1. The given device characteristics are $\mu_n C_{ox} = 40\mu A$, $V_t = 2V$, and $\lambda = 0$. The design problem requires that we specify R. Additionally the parameters W and L for each of the transistors need to be determined. It is noted that since there is a resistor present in the device, size is not a critical factor when selecting transistors. At this scale micro electro-mechanical (MEM) resistors would be employed to satisfy the resistor requirement. These MEM resistors are orders of magnitude larger than the areas of the transistor devices. The implication is that low cost, larger, transistors can be used without violation of design parameters.

Further design considerations surround the decision to use identical transistors for M_1, M_2, and M_3. Selecting transistors with different footprint sizes can make the layout of the device cumbersome, and the final device awkward to implement when dealing with integrated circuits. In this instance, however, we have assumed that this device will not be part of an integrated circuit due to the physical resistor. Hence, it will be assumed that transistors will be matched for simplicities sake. Given this assumption, it is a relatively straight forward task to determine v_{GS1} and v_{GS2}. We note that $v_{GS1} = v_{GS2} = 10V$, as shown in the hand calculations. Noting that $v_{G2} = v_{G3}$ and $v_{S2} = v_{S3}$, we see that $v_{GS3} = 10V$ also.

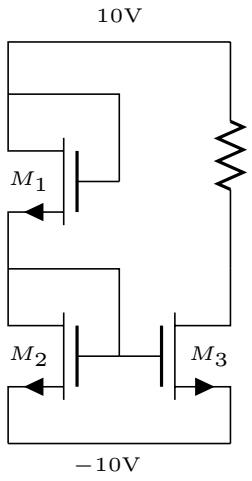

Figure 1: The circuit topology of the basic current mirror - the current I_0 flows through the resistor in the right hand branch of the circuit.

This allows the calculation of the aspect ratio, $^{W}/_{L}$, which was found to be 0.11718. This means that we can select some width of the transistor channels, W, and calculate the corresponding channel length, L. Finally, to get some insight on what resistor value we should implement we can determine an upper bound on acceptable transistor values. Analysis yields that:

$$R \leq 131.66\text{k}\Omega$$

This upper bound is a theoretical limit for which the transistor voltage v_{DS3} will remain above the 0.25V level - a specification of the design problem. Satisfying this upper bound, however, does not guarantee the transistor will remain in saturation. The upper bound for saturation for the transistor was found to be:

$$R \leq 80\text{k}\Omega$$

The channel length, L, was chosen arbitrarily to align with the commonly occurring value of 5µm. The corresponding value for the channel width, W, was calculated to be 0.5859µm. Finally the value for the resistor was chosen to be at the edge of saturation at 80kΩ.

3 Simulation

The circuit topology was implemented in OrCAD, using the values for the design parameters outlined above. The simulated circuit can be seen in Figure 2.

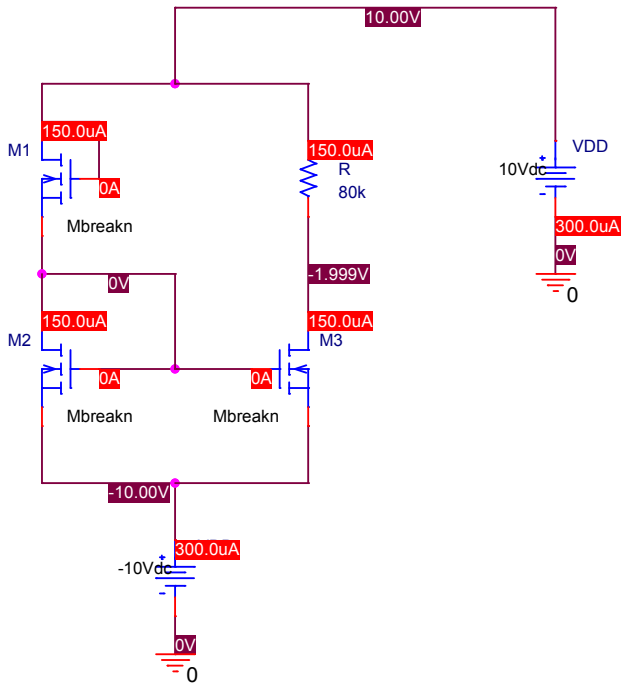

Figure 2: Simulated circuit using design parameters outlined above. The simulation was run in PSPICE.

4 Discussion

The values for the current I_0 are identical to the design specifications at 150µA. Further, we note that transistor 1, 2 and 3 all have v_{DS} values which are greater than the minimum specified value for the design. One aspect of the design worth mentioning is that selecting the resistor at 80kΩ leaves the device, $M3$, operating precariously close to the edge of saturation. Choosing a resistor value lower than 80kΩ would see an increase in the stability of the circuit performance. Power consumption for the device will not change given that there is a fixed current through both branches of the circuit, over a fixed potential difference of 20V.

5 Conclusion

The design criteria were met with no exceptions, and the device performed in simulation as expected.