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Certificate no: UC-c1c37d8a-5059-4d09-a296-18be048bc0bd
Certificate url: ude.my/UC-c1c37d8a-5059-4d09-a296-18be048bc0bd
Reference Number: 0004

CERTIFICATE OF COMPLETION

# ASIC Design & Verification using Verilog HDL +Project Demo

Instructors **VLSI Mentor**

## Shaik Sardar Basha

Date **Sept. 24, 2025**
Length **16 total hours**