Krishna Savant Syreddy
Electrical Engineering
Indian Institute of Technology, Bombay

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UG Third Year(B.Tech)
Male
DOB: 19-06-1993

Examination	University	Institute	Year	CPI / %
Graduation	IIT Bombay	IIT Bombay	2012	8.59
Intermediate/+2	BIE, AP	SR Junior College	2010	90.50
Matriculation	CBSE	Warangal Public School	2008	93.00

Research Interests

- Robotics (Planning and Localization), Artificial Intelligence
- VLSI Design, High Level Synthesis, VLSI CAD

Current Projects

- **AUVSI Robosub 2013, San Deigo, CA** *(September 2012 to Present)*
  Designing and developing an unmanned autonomous underwater vehicle (AUV) that localizes itself and performs realistic missions based on feedback from visual, inertial, acoustic and pressure sensors using thrusters/propellers. [`http://auv-iitb.org`]
  (Guided by Prof. Hemendra Arya and Prof. Leena Vachhani)
  - Working on the navigation system consisting of planning, localizing and accurate maneuvring of the vehicle.
  - Developing algorithms for fusing and filtering data from various sensors and control the vehicle. Working on ROS (Robot Operating System), an opensource software framework providing hardware abstraction and Inter Process Communication mechanism.
- **Robotic Sniffer Dog** *(Guided by Prof. J. John and D. Sharma, EE318 - Spring 2013)*
  - Building a working prototype of a robotic control system which can be controlled from a considerable distance (using repeaters) through WLAN, Zigbee protocol relying on visual data from cameras.
  - Consists of a sensor board which can detect explosive vapors in parts per billion.

Google Summer of Code - GSoC'12

Worked on a FOSS project **Gnucap plugin for schematic files** *(May 2012 to August 2012)*

- Worked with the organisation 'GNU Project' on the project 'Gnucap' (GNU Circuit Analysis Package) under the mentorship of Albert Davis. [`http://gnucap.org`]
- Implemented a schematic parser which provides interchange of data between simulatable Verilog-AMS netlist and gEDA/gschem schematic format.

Key Academic Projects

- **epsilon-to-verilog: An Educational Hardware Compiler** *(Guided by Prof. S. Patkar, Sep-Nov, 2012)*
  - epsilon-to-verilog synthesizes programs written in a new custom minimalistic high level language epsilon to hardware description languages
  - The tool parses the cfg (control flow graph) generated by epsilon and does scheduling and allocation to generate hardware description in verilog.

- **Technology Mapping - VLSI CAD** *(Guided by Prof. S.Patkar, EE677 - Autumn 2012)*
  - Modeling the problem of technology mapping as a tree covering problem using pattern trees of the library gates.
  - Implementing using python graph-tool library
- **Traveling Message Display** *(Guided by Prof. M.B.Patil and J.John, EE214- Spring 2012)*
  - Worked in a team of 3 members
  - Display a scrolling message taken using keypad on an LED Array
  - Used an FPGA board: DE0 NANO and programmed using Verilog-HDL
  - My work involved writing verilog modules for taking input from the keypad and processing
- **Simulation of Micromouse** *(Guided by Prof.Deepak B. Phatak, CS101 - Autumn 2010)*
  - Led the team of 12 members with 3 subteams of 4 members each
  - Designed n×n mazes, Solved them for the shortest path using Bellman-ford algorithm in C++ and Simulated the solution using EzWindows GUI.
  - My work involved programming the display over GUI and interlinking the different parts

Scholastic Achievements

- **All India Rank 61** in IIT-JEE (Joint Entrance Examination) - 2010 of 0.455 million students
- Awarded **Certificate of Merit** by Central Board of Secondary Education (**CBSE**) for being among **top 0.1 %** in 'Science' and 'Social Science' in All India Secondary School Examination - 2008.
- Secured **All India Rank 15** in 10th National Science Olympiad (NSO) - 2007 conducted by Science Olympiad Foundation(SOF).

Technical Skills

- **Programming Languages**: C++,Java,Python,Ruby **Operating Systems**: Linux, Windows
- **Tools**: Latex, Scilab, Mathematica, Photoshop **Web development**: HTML, CSS, JS, Django
- **EE tools**: ngspice, gnucap, gEDA tools, Eagle, Verilog-HDL, Verilog-AMS, Icarus verilog Bluespec System Verilog (BSV), Modelsim, Altera Quartus

Extra Curricular Activities

- Participated in **Unnati**, the **NSS** (National Service Scheme) group of IIT Bombay.
  - Has been involved with the **GRA** (Group for Rural Activities) as part of curriculum in I year
  - Went to Village trips in Autumn 2010 and Spring 2011.
  - Continued as a voluntary member of the NSS Team in the subsequent year.
- Participated in the Inter-hostel Hockey GC.

Additional Courses taken / currently taking

Electronic Design Lab
Computer Networks
Artificial Intelligence
Discrete Structures
Introduction to Quantum Mechanics
Processor Design
Foundations of VLSI CAD
Data Structures and Algorithms
First Course in Optimisation