EE 674 Projects – Fall 2024

Report due by December 10, 2024

In this project you will be determining the optimum location and values (RLC) of a decoupling capacitor (maximum 5) to reduce voltage noise between a power and ground plane in a 5 layer board.

Cadence Sigrity

Guide to installation located at

https://docs.google.com/document/d/19mCAR2YfwvplPLo1_ipDft8VabcYndrY3BfVrZvxIhM/edit?usp=sharing2

Inside the Sigrity Suite Manager you will find the tool PowerSI

PowerSI (a frequency domain tool using the Method of Moments to solve Maxwell's equations in integral form)

1. You will design a 5 layer board with 1 power plane and 1 ground plane. The second layer will be a ground net, and the 4th layer will be a power net (VDD). The layer stackup of the motherboard is shown below. Each group will submit a project report and a 3-minute screen-capture video of all simulation steps. **The dielectric constant and board size may be different for each group.**

Layer Manager -> Stackup

Stackup | Pad Stack

Layer #	Color	Layer Icon	Layer Name	Thickness (mm)	Material	Conductivity (S/m)	Fill-in Dielectric	Frequency (Hz)	Er	Loss Tangent
1			Signal02	0.03556		5.800000e+07	[AIR]	1e+09	[1]	[0]
			Medium03	0.5		0			4	0
2			Plane02	0.03556		5.800000e+07	[FillPlane02_Averag	1e+09	[4]	[0]
			Medium04	0.5		0			4	0
3			Signal03	0.03556		5.800000e+07	[FillSignal03_Avera	1e+09	[4]	[0]
			Medium02	0.1		0			4	0
4			Plane01	0.03556		5.800000e+07	[FillPlane01_Averag	1e+09	[4]	[0]
			Medium01	0.1		0			4	0
5			Signal01	0.03556		5.800000e+07	[AIR]	1e+09	[1]	[0]

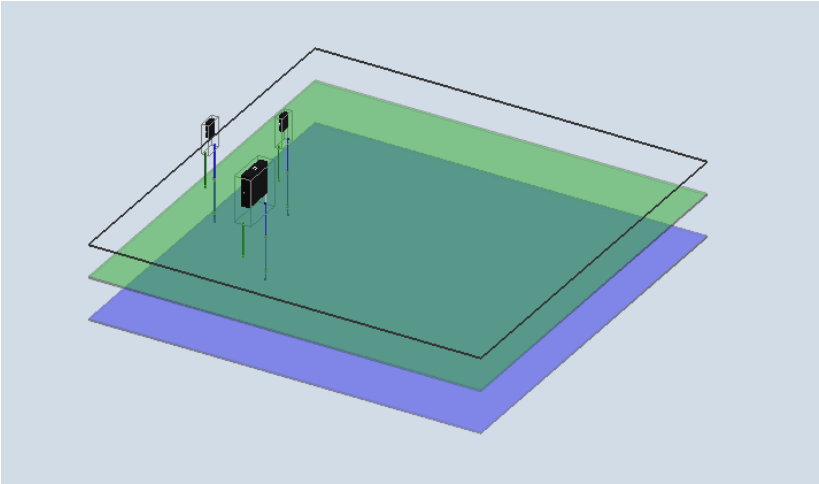
   A. You will define a via pad stack with a via diameter of .4 mm, a pad diameter of .5 mm and an anti-pad diameter of .6 mm and make it the default via.
   B. You will add vias for signal and power and ground connections as per the tutorial.
2. You will start with the Noise Coupling Analysis workflow.
3. You will create two excitation current source models to represent the active components in your design.
   a. Sink 1
      i. I1 1 2 AC=100m
   b. Sink 2
      i. I1 1 2 AC=75m

4. You will create two components, S1 and S2, that reference these two models and connect them to the layout.

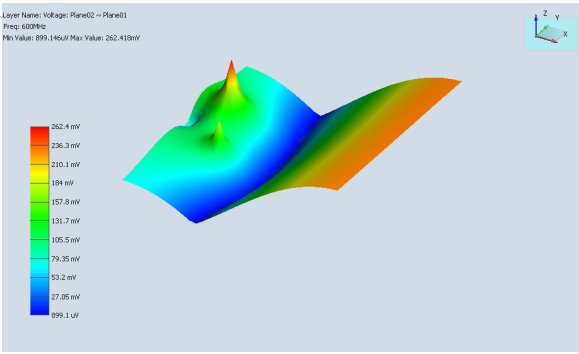
5. You will use the short circuit response of a VRM. This means you will create a spice model of a resistor having a value of 0.01 mOhm to connect at the VRM power and ground nodes

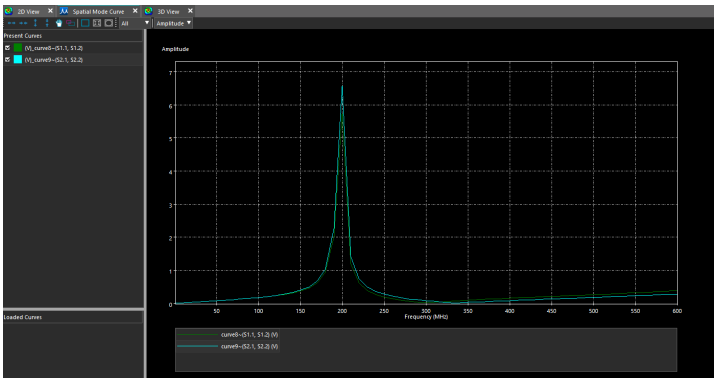
6. You will create a component of the model, T1 and connect its circuit nodes to the layout nodes representing the VRM.

   3D model of base model without decoupling caps is shown below



7. You will visualize the 2D and 3D spatial voltage distribution between power and ground plane layers to identify hotspots on the PCB and then place decoupling capacitors (max number 5) at appropriate locations on PCB to optimize the power/ground noise voltages at sink locations.





8. You will derive values for decoupling capacitors, build a model and components for decap, and place on layout at 'hotspots' for re-simulation.
9. You will change workflow to extraction mode. Deactive decaps, simulate and view pwr/gnd impedance Z11.

10. You will reactivate decaps for re-simulation to examine effects on pwr/gnd impedance.