EE 674 PROJECT-2

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Introduction:

In modern electronic design, ensuring power and signal integrity is critical for the reliable performance of high-speed circuits. Voltage noise between the power (VDD) and ground (GND) planes in a printed circuit board (PCB) can cause severe issues, such as signal distortion, timing errors, and overall system instability. To address these challenges, it is essential to design a robust power delivery network (PDN) that minimizes voltage fluctuations and maintains consistent power flow to active components. This project focuses on optimizing the PDN of a 5-layer PCB by strategically placing decoupling capacitors to reduce voltage noise and impedance between the power and ground planes.

To achieve these objectives, we utilized **Cadence PowerSI**, a state-of-the-art tool for power and signal integrity analysis. PowerSI employs full-wave electromagnetic simulation, solving Maxwell's equations in the frequency domain to provide precise results. By leveraging its advanced capabilities, we conducted comprehensive analyses to identify voltage noise hotspots, simulate spatial voltage distributions, and evaluate impedance characteristics. Throughout the project, we employed both **Spatial Mode** and **Extraction Mode** workflows in PowerSI to systematically address the challenges of power integrity.

Our process began with the setup of a detailed PCB model. We designed a 5-layer stack-up that includes dedicated power and ground planes, ensuring a realistic representation of a high-speed PCB design. Within this setup, we defined excitation sources to emulate active components and introduced a short-circuit response model for the voltage regulator module (VRM). This step allowed us to simulate realistic operating conditions and gain insights into how power and ground noise affect the system's performance.

Using the **Spatial Mode** workflow, we visualized the 2D and 3D voltage distributions across the PCB to identify noise-prone areas or "hotspots." This analysis guided us in determining the optimal locations for placing decoupling capacitors, which are critical for reducing resonant noise peaks. We then proceeded to calculate the appropriate RLC values for the decoupling capacitors and modeled them within PowerSI. By simulating the system with and without these capacitors, we observed a significant reduction in voltage noise at the identified sink locations, confirming the effectiveness of our approach.

In the next phase, we used the **Extraction Mode** workflow to further analyze the PCB's power integrity. We simulated the impedance characteristics of the power and ground planes, first without the decoupling capacitors and then with them. This analysis allowed us to compare the system's performance before and after optimization. By strategically placing a maximum of five decoupling

capacitors, we achieved a marked reduction in impedance, which translates to improved power delivery and reduced susceptibility to noise.

The results of our simulations, coupled with a systematic design approach, demonstrated the effectiveness of decoupling capacitors in mitigating power and ground noise issues. We successfully reduced voltage noise from its initial peaks and improved the overall impedance profile of the PCB. These improvements are crucial for ensuring stable and reliable operation in high-speed electronic systems.

In this report, we detail each step of our process, including PCB model creation, workflow implementation, and the analysis of simulation results. We also provide a comparative evaluation of the system's performance with and without decoupling capacitors, highlighting the significance of our design modifications. Furthermore, we have included simulation visualizations and metrics to support our findings.

Through this project, we have not only gained valuable insights into power integrity optimization but also demonstrated the practical application of advanced tools like Cadence PowerSI in solving real-world engineering challenges. The knowledge and skills acquired during this project underscore the importance of a methodical approach to PCB design and its role in addressing power integrity issues in modern electronic devices.

Project Objective:

Reduction of Voltage Noise:
To minimize the voltage noise between the power (VDD) and ground (GND) planes of a 5-layer PCB using strategically placed decoupling capacitors.

Hotspot Identification:
To identify high-voltage noise regions ("hotspots") across the PCB through 2D and 3D spatial voltage distribution analysis using Cadence PowerSI.

Impedance Optimization:
To analyze and reduce the impedance of the power delivery network, ensuring stable and efficient power delivery to active components.

Decoupling Capacitor Placement:
To determine the optimal locations and values (RLC parameters) for up to five decoupling capacitors that can effectively suppress voltage noise and mitigate resonances.

Workflow Integration:
To implement and compare the **Spatial Mode** and **Extraction Mode** workflows of Cadence PowerSI for noise reduction and impedance analysis.

Simulation and Validation:
To simulate the PCB design with and without decoupling capacitors to validate their effectiveness in reducing noise and improving the power delivery network.

Report Preparation:
To document the methodology, simulations, and findings in a comprehensive report and screen-capture video for effective presentation of the project outcomes.

Cadence SI:

Cadence PowerSI is a cutting-edge tool for power and signal integrity analysis, designed specifically for integrated circuit packages and printed circuit boards (PCBs). It addresses the challenges posed by high-speed design issues, such as power-ground noise, signal degradation, and electromagnetic interference.

This project explores the reduction of power and ground voltage noise in a 5-layer printed circuit board (PCB) using Cadence PowerSI, a powerful tool for power and signal integrity analysis. Noise and impedance mismatches in PCBs can severely impact performance and reliability, particularly in high-speed designs. By strategically optimizing decoupling capacitor placement and values, the project aims to minimize noise and improve power delivery network (PDN) stability.

Advanced Simulation Technology:
PowerSI employs full-wave methods to simulate electromagnetic field phenomena, offering highly accurate solutions by directly solving Maxwell's equations without approximations.

Frequency-Domain Analysis:
The tool operates in the frequency domain, enabling detailed insights into the frequency-dependent behavior of power delivery networks (PDNs).

Comprehensive Applications:
PowerSI is widely used in the design and analysis of:

- ➔ Integrated circuit packages (e.g., chip carriers)
- ➔ Multi-layer PCBs
- ➔ Power-ground systems and their impedance profiles

Power and Signal Integrity Solutions:

- ➔ Fast and precise modeling of PDNs and signal transmission paths
- ➔ Identification and mitigation of high-speed design issues, including noise hotspots and resonant frequencies
- ➔ Extraction of electrical parameters (S, Z, and Y) for system-level integration

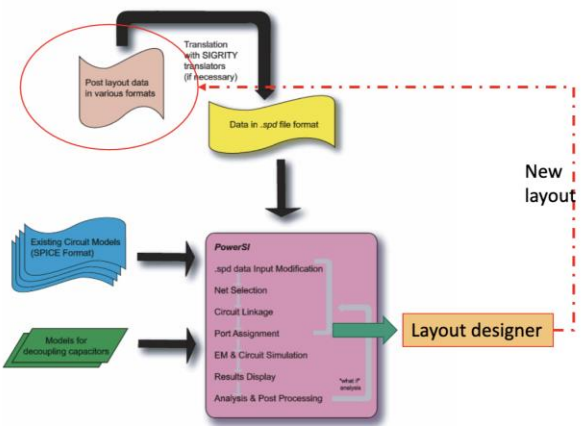
PowerSI Modes-Extraction:

Extraction Mode is used to compute electrical properties like **Scattering (S), Impedance (Z),** and **Admittance (Y)** parameters for multi-port networks. These parameters are vital for understanding the electrical behavior of structures like PCBs and PDNs.

The mode outputs these parameters in a Touchstone format, a widely accepted file type used in electrical simulations. This makes it easy to incorporate the results into broader system-level analyses.

When paired with Sigrity Broadband SPICE, Extraction Mode produces SPICE-compatible models that are accurate over a wide frequency range. These models can be used for time-domain (transient) simulations involving complex circuit designs.

PowerSI Modes-Extraction Mode Flow:



Layout designer -> New layout

Add multiple ports for analysis

Define frequency range

Run simulation -> Extract S, Z, Y parameters

PowerSI Modes-Spatial:

Spatial Mode focuses on analyzing AC voltage and current distributions across the physical structure of the PCB, considering multiple sources.

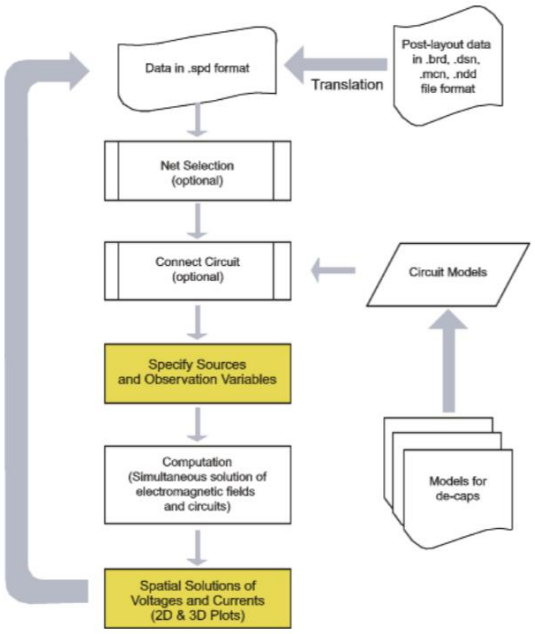
This mode maps how voltages vary across the power and ground planes, offering a spatial perspective of the circuit's electrical behavior.

It supports the addition of multiple input sources, allowing designers to simulate different scenarios involving power delivery and signal integrity.

This mode enables visualization of voltage distribution, helping to identify "hotspots" where noise or voltage fluctuations are significant.

Spatial Mode pinpoints areas with high voltage noise (hotspots) and the frequencies at which these occur, guiding mitigation efforts.

Using the information from hotspots and voltage distributions, designers can decide where to place decoupling capacitors for maximum noise reduction



PowerSI Modes-Spatial Mode Flow:

➔ Add sources to the layout.

➔ Define observation points and set up field observations.

➔ Run a simulation and observe results.

➔ Identify hotspots and calculate resonant frequencies.

➔ Optimize decoupling capacitors and rerun simulation.

PCB Design Parameters:

- **Dielectric Constant (εr):** 5
- **Metal Layer Thickness:** 0.03556 mm
- **Dielectric Layer Thicknesses:**
  - Layer 1: 0.5 mm
  - Layer 2: 0.5 mm

    - Layer 3: 0.1 mm
    - Layer 4: 0.1 mm
- **Plane Dimensions (x-y):** 100 mm x 100 mm

Setup of a 5 layer PCB model in PowerSI-Steps

Step 1: Launch PowerSI

- Open the PowerSI tool from the Cadence Systems Analysis suite.
- From the Windows Start Menu, navigate to **All Apps > Cadence Systems Analysis > PowerSI 2024.0** and double-click the PowerSI icon.
- This initializes the workspace for creating a new PCB model.

Step 2: Start a New Project

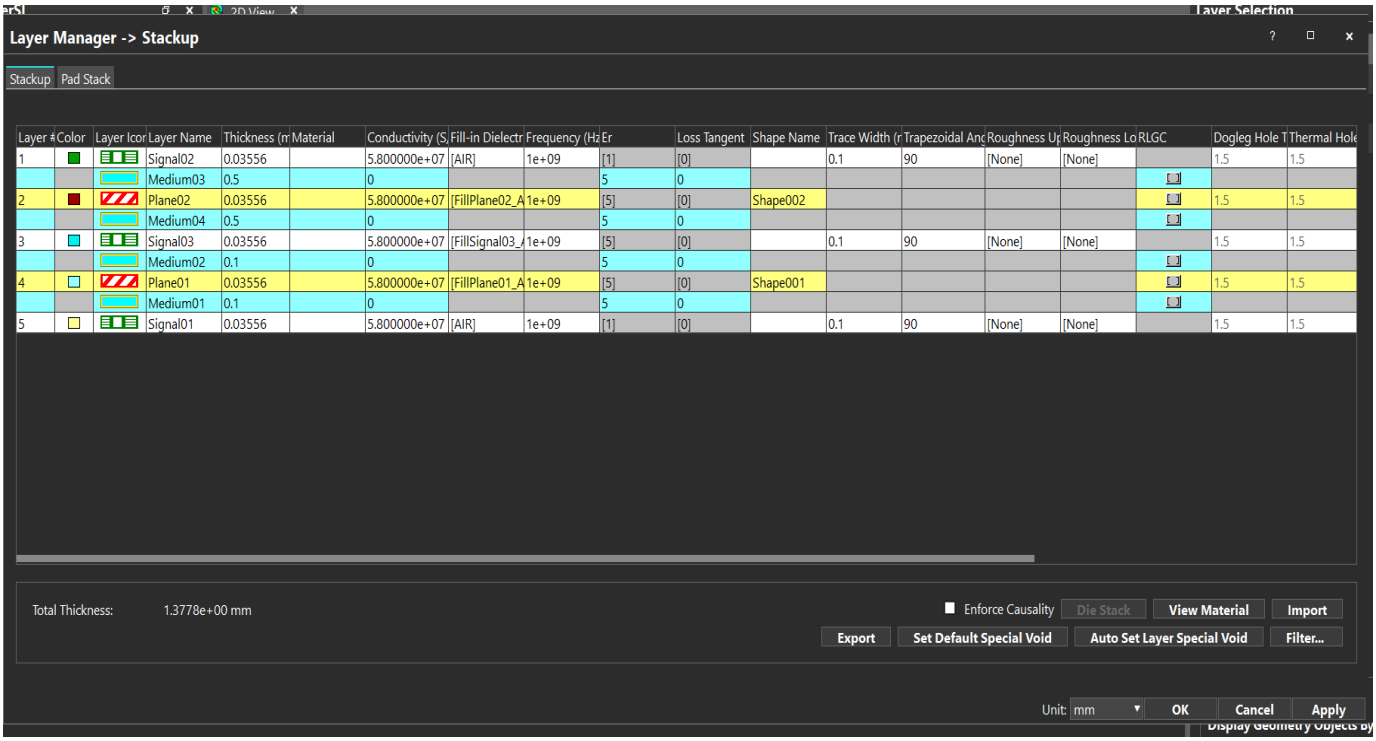
1. Click on the File Menu in the toolbar.
2. Select New to create a new project.
3. This opens a default 4-layer square PCB design with a 100 mm x 100 mm layout.

Workspace Components:

- **Menu Bar (A):** Contains file and tool options.
- **Toolbars (B):** Provides quick access to commonly used functions.
- **Workflow Pane (C):** Guides the user through each step of the modeling process.
- **Show Area (D):** Visualizes the PCB design and changes.
- **Output/Folder Browser/TCL Reader Pane (E):** Displays messages and logs.
- **Layer Selection, Net Manager, or Component Manager (F):** Manages layers, nets, and components in the design.

Step 3: Modify the Layer Stackup

1. In the Workflow Pane, select Check Stackup to access the Layer Manager.
2. Right-click on Layer 2 in the stackup and select Insert.
3. Choose Signal Layer to add a new layer between Plane01 and Plane02.
4. Review the stackup, which now consists of 5 layers. Click OK to finalize.

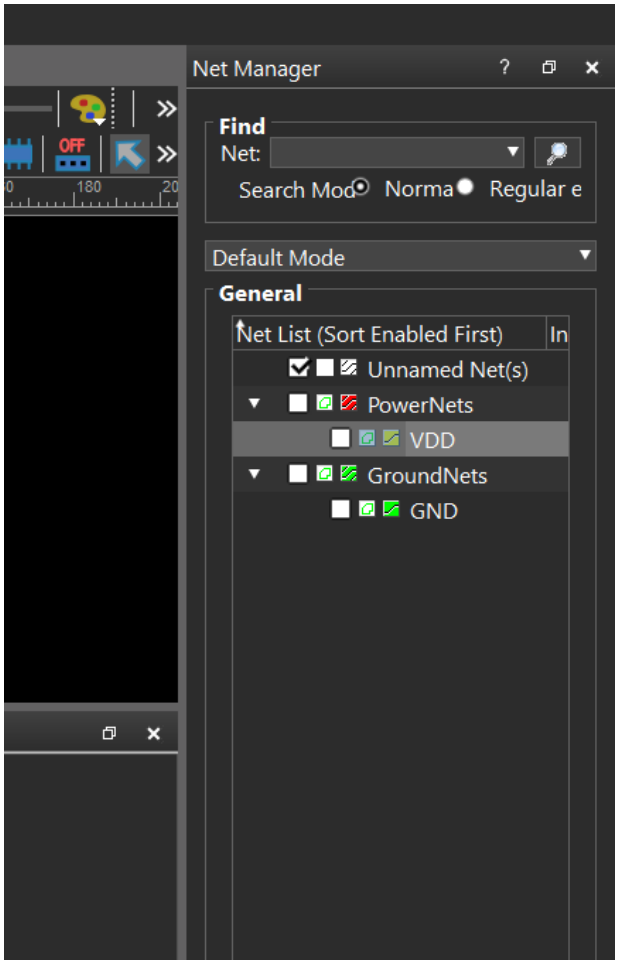


Final Layer Details:

- The layers include dielectric and metal layers with thicknesses as specified:
  - Layer 1: 0.5 mm
  - Layer 2: 0.5 mm
  - Layer 3: 0.1 mm
  - Layer 4: 0.1 mm

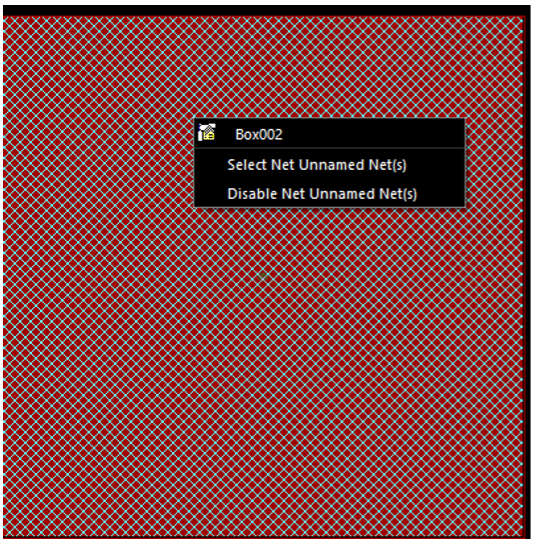
Step 4: Define Nets

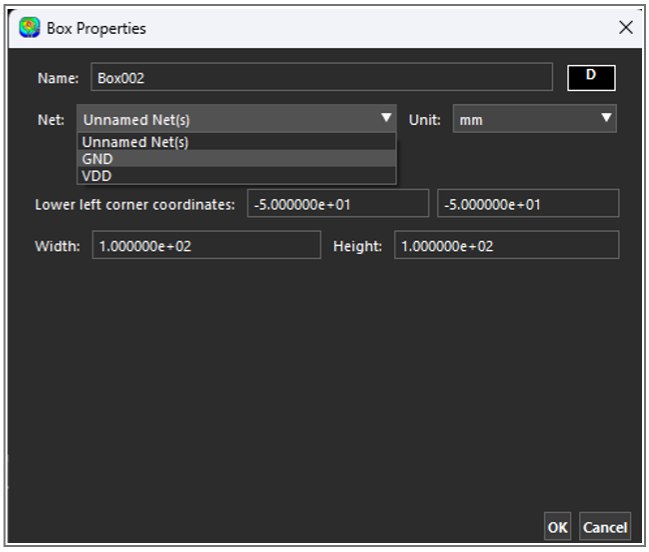
1. Open the Net Manager pane.
2. Right-click to select New and create two nets named GND and VDD.
3. Assign a color for each net (e.g., green for GND and yellow for VDD).
4. Classify the nets:
   - Right-click on GND and select Classify as GroundNet.
   - Right-click on VDD and select Classify as PowerNet.



Step-5: Assign Plane02 to GND net:

Assigning **Plane02 to the GND net** is an essential step in PCB design to establish a dedicated ground plane. The ground plane acts as a reference point for all voltage levels within the circuit and provides a low impedance return path for currents. This minimizes noise, reduces electromagnetic interference (EMI), and improves signal integrity by ensuring stable and consistent grounding across the board. By assigning Plane02 to the GND net, we enhance the overall power and signal integrity of the system, critical for high-speed electronic designs.





Step-6: Assign Plane01 to VDD net:

Assigning **Plane01 to the VDD net** is done to create a dedicated power plane that distributes the supply voltage uniformly across the PCB. This ensures consistent power delivery to all active components, reduces voltage drops, and minimizes noise caused by fluctuating currents. A dedicated power plane also improves the overall power integrity and enhances the performance of high-speed circuits by providing a stable power source.

Step-7: Create a new padstack for model vias:

Creating a **new padstack for model vias** is necessary to define the physical and electrical properties of the vias used in the PCB design. Vias are critical for establishing connections between different layers of the PCB, such as linking the power (VDD) and ground (GND) planes or signal layers. By customizing a padstack, we can specify parameters like via diameter, plating thickness, and clearance, ensuring optimal performance, manufacturability, and minimal signal or power integrity issues in the PCB design.

Step-8: Padstack Configuration for "trainingPad":

Entering **pad dimensions for DefaultLibLayer for the new padstack "trainingPad"** is done to define the size, shape, and other attributes of the pad used in the PCB design. This step ensures that the via or component pad aligns with the required specifications for both electrical performance and manufacturability. By setting the correct pad dimensions, we can optimize the design for signal integrity, minimize impedance mismatches, and ensure compatibility with the fabrication process. Properly defined padstack dimensions are crucial for the reliable connection of components and layers, contributing to the overall performance and quality of the PCB.

Steps for Configuring and Setting Default Padstack:

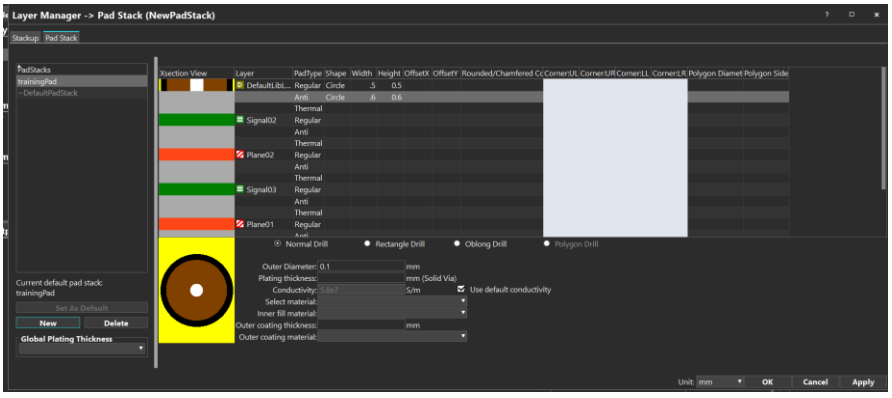
1. **Select the New Padstack ("trainingPad")**
   Begin by selecting the newly created padstack named "trainingPad" from the library, which will be used for the vias in the design.

2. **Choose Circle for Pad Shape**
   Set the pad shape to "Circle" with a width of **0.5 mm** for the DefaultLibLayer. This defines the geometry of the via pad on the PCB layer.

3. **Choose Circle for Anti-Pad Shape**
   Similarly, set the Anti-Pad shape to "Circle" with a width of **0.6 mm** for the DefaultLibLayer. The Anti-Pad ensures that the via does not create a short between the layers by leaving an area free of copper.

4. **Set the Outer Diameter**
   Enter an **outer diameter of 0.4 mm** for the via. This determines the overall size of the via hole and ensures the via fits within the desired specifications for the design.

5. **Set as Default Padstack**
   Finally, click the **Set As Default** button to make "trainingPad" the default padstack for all vias in the design. This ensures consistency across the design and simplifies the process of assigning vias to the appropriate layers.



Step-9: Creating Vias for VDD and GND Connections from Signal02 Layer

Creating vias for **VDD** and **GND** connections from the **Signal02 Layer** is done to establish reliable electrical paths between different layers of the PCB. Vias are used to connect the power (VDD) and ground (GND) planes with the signal layers, ensuring that all components receive stable power and return current. By creating these vias, we maintain

the integrity of the power delivery network and minimize noise and signal interference across the board. This step is essential for improving power integrity, reducing voltage fluctuations, and optimizing the overall performance of the PCB.

Steps for Adding Vias for VDD and GND Connections

1. **Select the Add Via Icon**
   Left-click on the **Add Via** icon in the tool palette to begin the via creation process. This prepares the tool to add vias to the PCB design.

2. **Left-Click on the PCB Area**
   Left-click at the desired location on the **Signal02 Layer** in the PCB layout. This is where the via will be placed to establish the electrical connection between layers.

3. **Via Editing Window: Select Upper Layer**
   In the **Via Editing** window, select the **upper layer** to define the starting point of the via. For the VDD connection, this will be **Signal02** (the signal layer).

4. **Select Lower Layer to Complete the Via**
   Choose the **lower layer** to complete the via creation. For **VDD vias**, select **Plane01** (the power plane) as the destination. For **GND vias**, select **Plane02** (the ground plane).

5. **Create the Via Using the Default Padstack**
   The via will automatically be created using the **Default padstack** configuration, ensuring consistent via dimensions and placement across the design.

6. **Click Add to Insert the Via**
   After defining the layers for the via, click **Add** to insert the via into the PCB design. The via will now establish a connection between the Signal02 layer and either Plane01 (for VDD) or Plane02 (for GND).

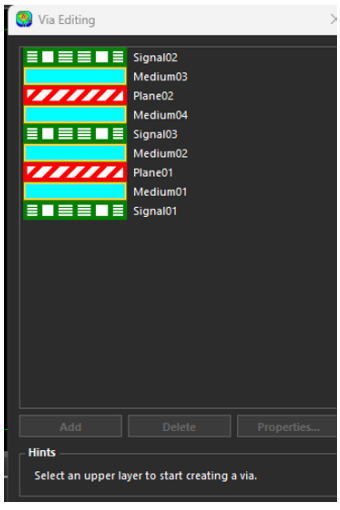
7. **Repeat the Process for Multiple Vias**
   Add additional vias as required for the VDD and GND connections using the same process. Refer to the table below for the locations and number of vias to be placed.

Via	X coordinate	Y coordinate	Layer connection
VDD	-35	12	Signal02 to Plane01(VDD)
VDD	-47.5	1.5	Signal02 to Plane01(VDD)
VDD	-25	-15	Signal02 to Plane01(VDD)
GND	-35	8	Signal02 to Plane21(GND)
GND	-47.5	-2.5	Signal02 to Plane21(GND)
GND	-25	-25	Signal02 to Plane21(GND)

Note:

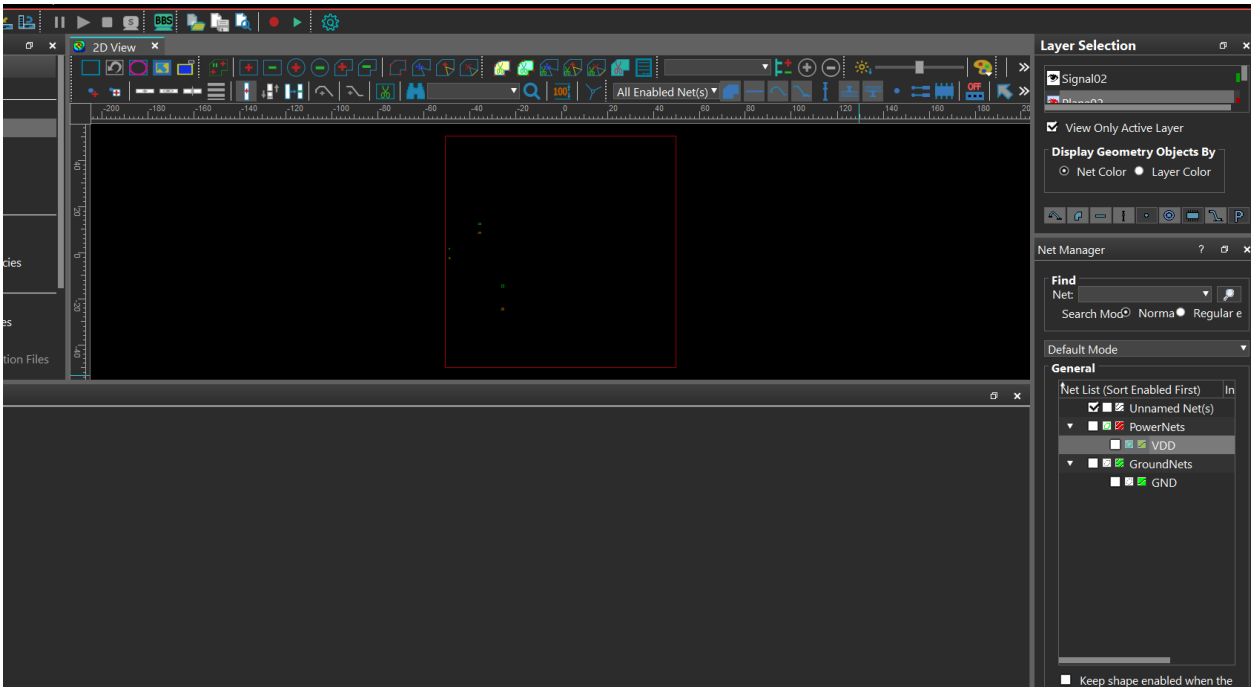
- **VDD vias** will connect **Signal02** to **Plane01** (VDD plane).
- **GND vias** will connect **Signal02** to **Plane02** (GND plane).

This process ensures the proper routing of power and ground connections, facilitating stable power delivery and signal integrity across the PCB.



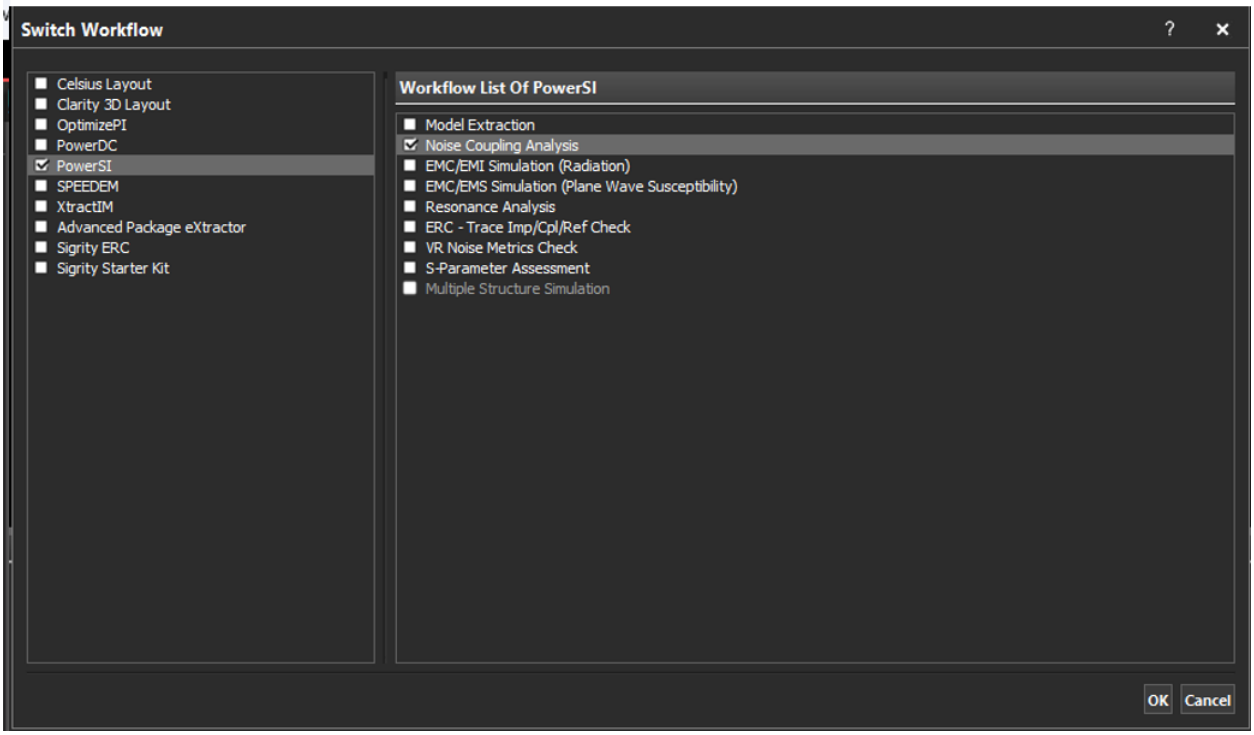
Post-Via Placement and Labeling:

After placing the vias, the **PCB should resemble the image below**, showing the completed via connections between the Signal02 layer and the power/ground planes (Plane01 and Plane02). It's crucial to note the **via labeling** for both the **devices** and **Voltage Regulator Modules (VRM)**. Proper labeling ensures that the vias are easily identifiable, aiding in troubleshooting and ensuring correct connections for efficient power and ground distribution.



Setup for Simulating with Spatial Workflow:

Setting up for simulation with **Spatial Workflow** is crucial for accurately analyzing and predicting the performance of the PCB design, especially for signal integrity and power delivery. This setup enables the simulation of how signals and power flow through the various layers and components of the PCB. By using the Spatial Workflow, we can model the physical and electrical interactions in the design, ensuring that the vias, trace routes, and planes are optimized for minimal signal loss, cross-talk, and other potential issues. This step is essential for identifying and mitigating design flaws before manufacturing, leading to a more reliable and efficient final product.



Adding Excitation Sources to the Layout:

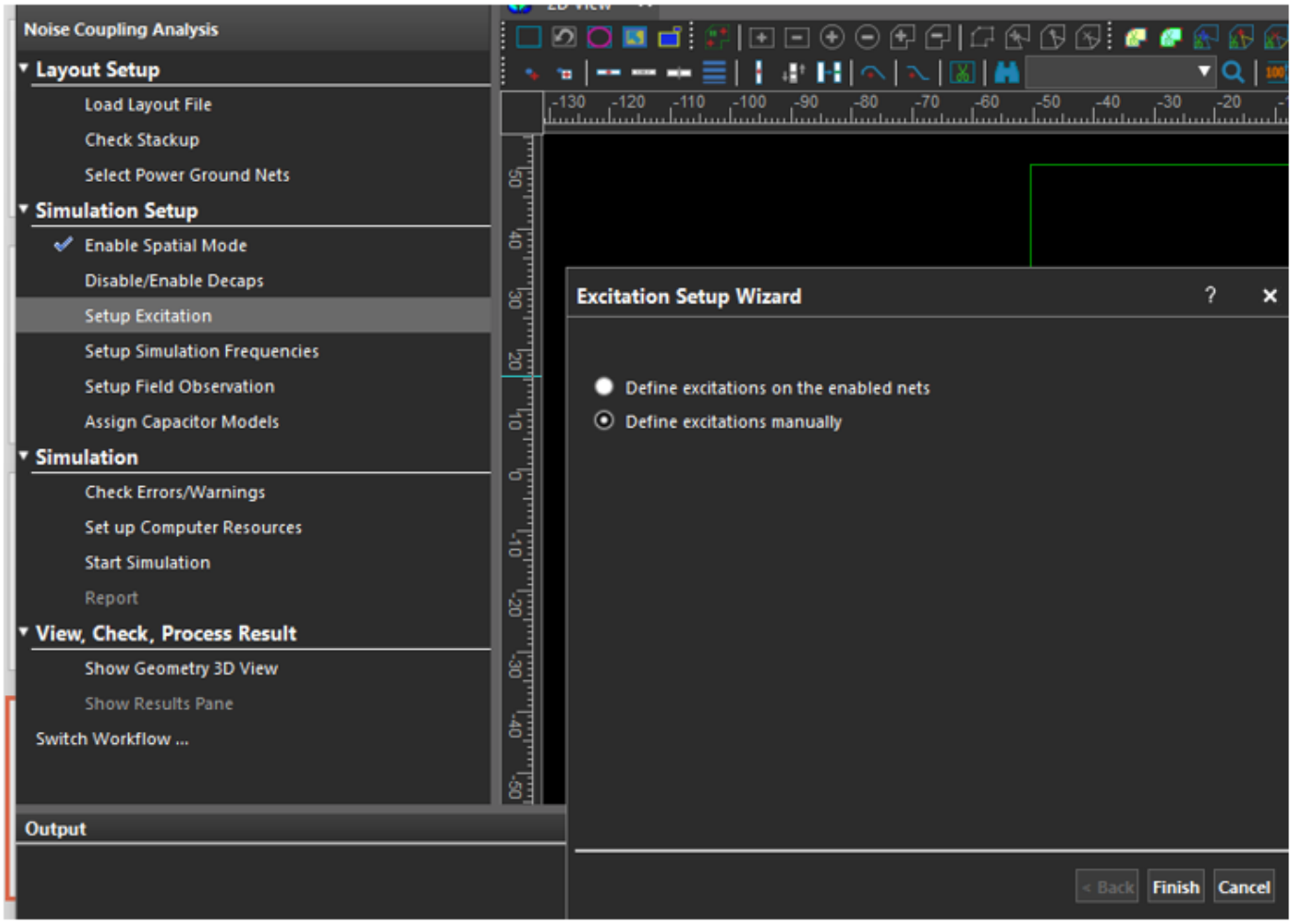
Adding **excitation sources** to the layout is necessary to simulate the behavior of active components in the design, such as chips or other circuit elements that draw current. These sources represent the power consumed by the components during operation, and their placement helps in simulating the voltage and current distribution across the PCB. This allows us to analyze how power and ground noise affect the components and identify hotspots or areas of high voltage fluctuation that may need optimization with decoupling capacitors.

Steps to Add Excitation Sources:

1. **Click on Setup Excitation**
   Open the setup menu for excitation sources by clicking on the **Setup Excitation** option. This prepares the layout for defining the current sources representing active components.

2. **Click on Define Excitations Manually**
   Choose the **Define Excitations Manually** option. This allows to manually specify the characteristics of the excitation sources, such as their location, current value, and direction, simulating the current draw from active components.

3. **Click on Finish**
   After defining the excitation sources, click **Finish** to complete the process. The sources will now be added to the layout, and the simulation will include their effects on the power and ground planes, allowing for a detailed analysis of the system's behavior under load.



Defining the Sinks:

Defining **sinks** is crucial for representing the active components or devices in the PCB that consume power. These sinks act as load models, simulating the current drawn by the active components during operation. By defining sinks with specific current values (e.g., 100 mA or 75 mA), we can accurately simulate the behavior of the PCB under realistic conditions and analyze the power distribution and voltage fluctuations at various locations. This is vital for optimizing the power delivery network (PDN) and ensuring stable performance.

Steps to Define Sinks:

1. **Click New Button in the Component Manager to Select New Model Definition**
   Open the **Component Manager** and click the **New** button to create a new model definition for the sink component. This step allows us to define the characteristics and behavior of the sink in the layout.

2. **Select New Model Definition**
   After clicking the New button, select the **New Model Definition** option to define the specific parameters of the sink model. This step ensures that the sink is modeled with the appropriate current and voltage requirements.

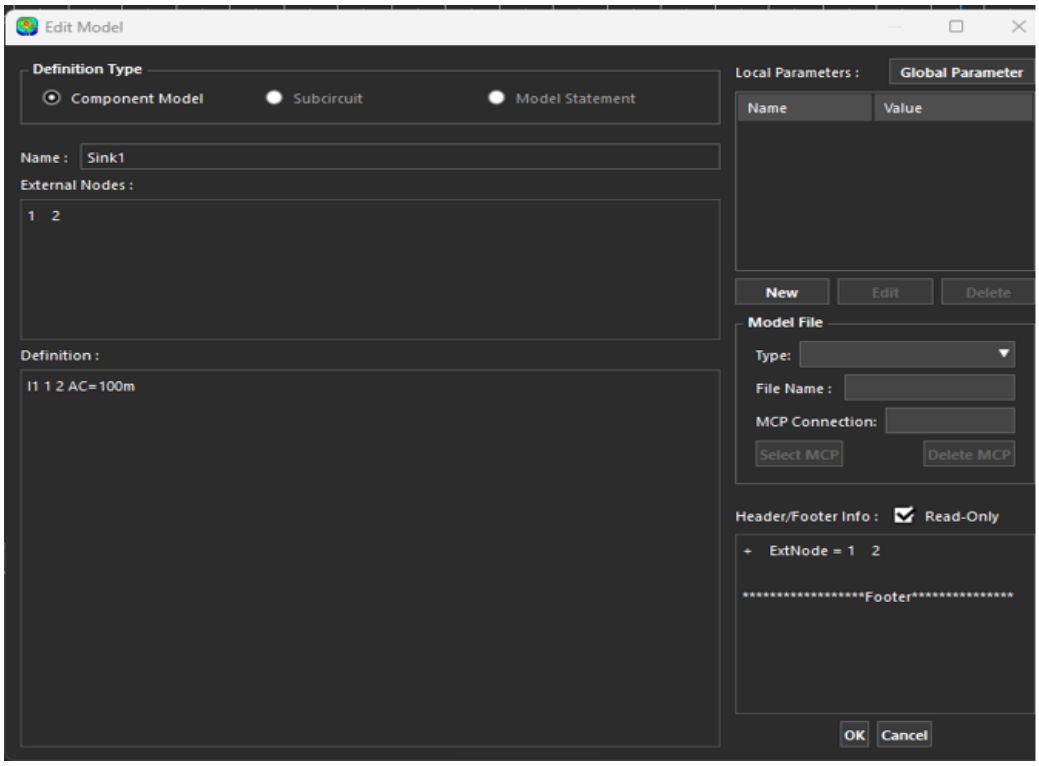
3. **Click OK**
   After selecting the new model definition, click **OK** to finalize the creation of the sink model.

4. **Name the New Model Sink1**
   Assign the name **Sink1** to the model to uniquely identify it in the simulation. This helps in organizing and referencing the various components in the design.

5. **Provide Two External Nodes (1 and 2)**
   Define two external nodes (1 and 2) that will connect the sink to the PCB layout. These nodes represent the input and output points for the current source, ensuring the sink is properly connected to the power/ground network.

6. **Define an AC Source of 100 mA for Sink1**
   Specify that Sink1 will draw **100 mA** of AC current. This models the power consumption of the active component or device represented by Sink1.

7. **Define the Second Sink (Sink2) with a 75 mA AC Source**
   Similarly, create a second sink (Sink2) and define it with a **75 mA AC current source**. This represents another active component in the design with different power requirements.


Edit Model
Definition Type
Component Model
Subcircuit
Model Statement
Name : Sink1
External Nodes :
1 2
Definition :
I1 1 2 AC=100m
Local Parameters :
Global Parameter
Name
Value
New
Edit
Delete
Model File
Type:
File Name :
MCP Connection:
Select MCP
Delete MCP
Header/Footer Info :
Read-Only
+ ExtNode = 1 2
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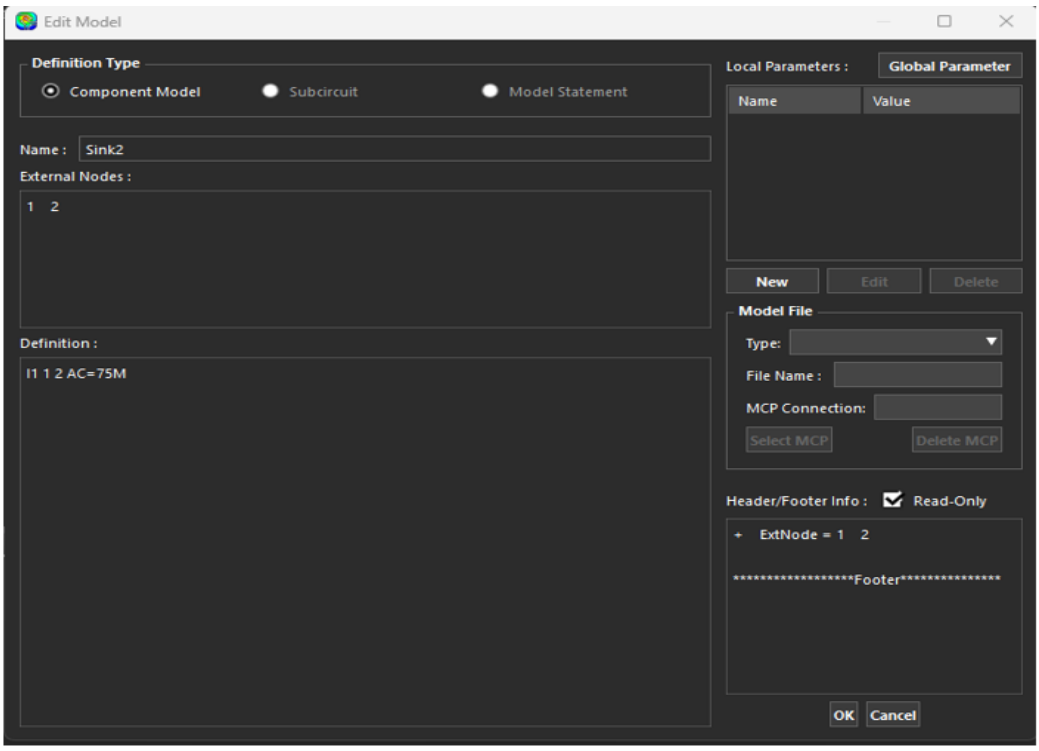
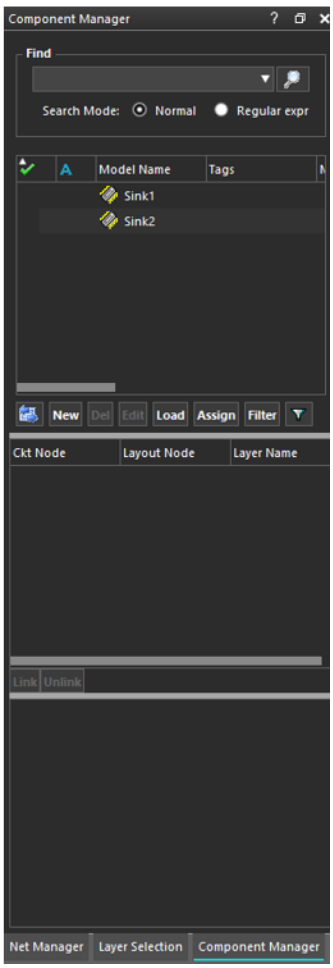
OK
Cancel


Edit Model
Definition Type
Component Model
Subcircuit
Model Statement
Name : Sink2
External Nodes :
1 2
Definition :
I1 1 2 AC=75M
Local Parameters :
Global Parameter
Name
Value
New
Edit
Delete
Model File
Type:
File Name :
MCP Connection:
Select MCP
Delete MCP
Header/Footer Info :
Read-Only
+ ExtNode = 1 2
**********Footer**********
OK
Cancel



Creating Components Referenced by Models Sink1 and Sink2

Creating components that are referenced by the sink models (Sink1 and Sink2) is essential to establish the physical presence and connection points of these active loads within the PCB design. These components represent the actual devices consuming current and ensure that the simulation reflects the power draw at specific locations. By assigning reference designators to these components (S1 for Sink1 and S2 for Sink2), we can track and manage their roles in the layout, facilitating better analysis and validation of the power delivery network.

Steps to Create Components Referenced by Models Sink1 and Sink2:

1. **Click New Button in the Component Manager**
   Open the **Component Manager** and click the **New** button to start creating a new component. This step allows us to define the properties and behavior of the component, including its association with the sink model.

2. **Select New Component Definition**
   Choose the **New Component Definition** option to define the specific attributes of the component. This ensures the component will be properly linked to the existing sink model and will participate in the simulation.

3. **Click OK**
   After selecting the new component definition, click **OK** to finalize its creation. The component is now set up for linking to a sink model.

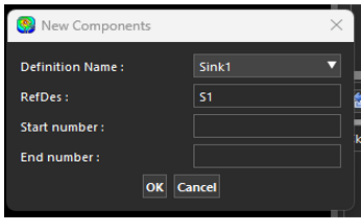
4. **Select Sink1 for the Model Definition Name**
   Choose **Sink1** as the model definition for the component, indicating that this component will represent the first active load (with the 100-mA current).

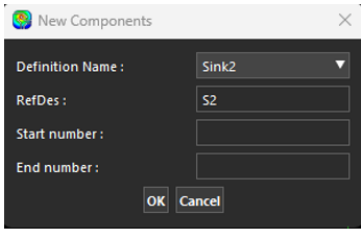
5. **Give Component Reference Designator of S1 and Click OK**
   Assign the reference designator **S1** to this component. This reference helps identify the component within the layout and the simulation. After entering the designator, click **OK** to complete the process.

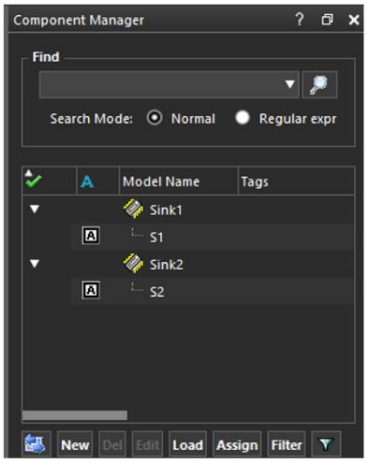
6. **Repeat Steps 1-3 for Sink2**
   Repeat the process from steps 1 to 3 to create a second component, this time referenced by **Sink2**, which corresponds to the second active load (75 mA).

7. **Select Sink2 for the Model Definition Name**
   Choose **Sink2** as the model definition for this new component, indicating that it represents the second active load in the design.

8. **Give Second Component Reference Designator S2 and Click OK**
   Assign the reference designator **S2** to this component, distinguishing it from S1. Once done, click **OK** to finalize the creation of the second component.







Connecting Components to VDD and GND Nodes in the Layout:

Connecting the components (S1 and S2) to the **VDD** and **GND** nodes in the layout is essential for completing the power and ground distribution network of the PCB. By linking the active components to these nodes, we ensure that they receive the correct supply voltage (VDD) and have a proper return path (GND) for current flow. This connection reflects the actual operating conditions of the PCB, allowing for accurate simulation of power delivery and voltage fluctuations at the components. Properly connecting the components ensures the stability and functionality of the entire system by maintaining consistent power integrity.

Steps to Connect Components to VDD and GND Nodes:

1. **Left-click on Component S1 in the Component Manager**
   Select **S1** from the Component Manager to begin the connection process.

2. **Left-click on S1 Ckt Node 1**
   Click on **S1 Ckt Node 1**, which represents the first node of the component.

3. **Right-click on VDD Via Node**
   Right-click on the **VDD via node** where the power connection should be made.

4. **Left-click Link**
   Left-click **Link** to establish the connection between **S1 Ckt Node 1** and the **VDD via node**.

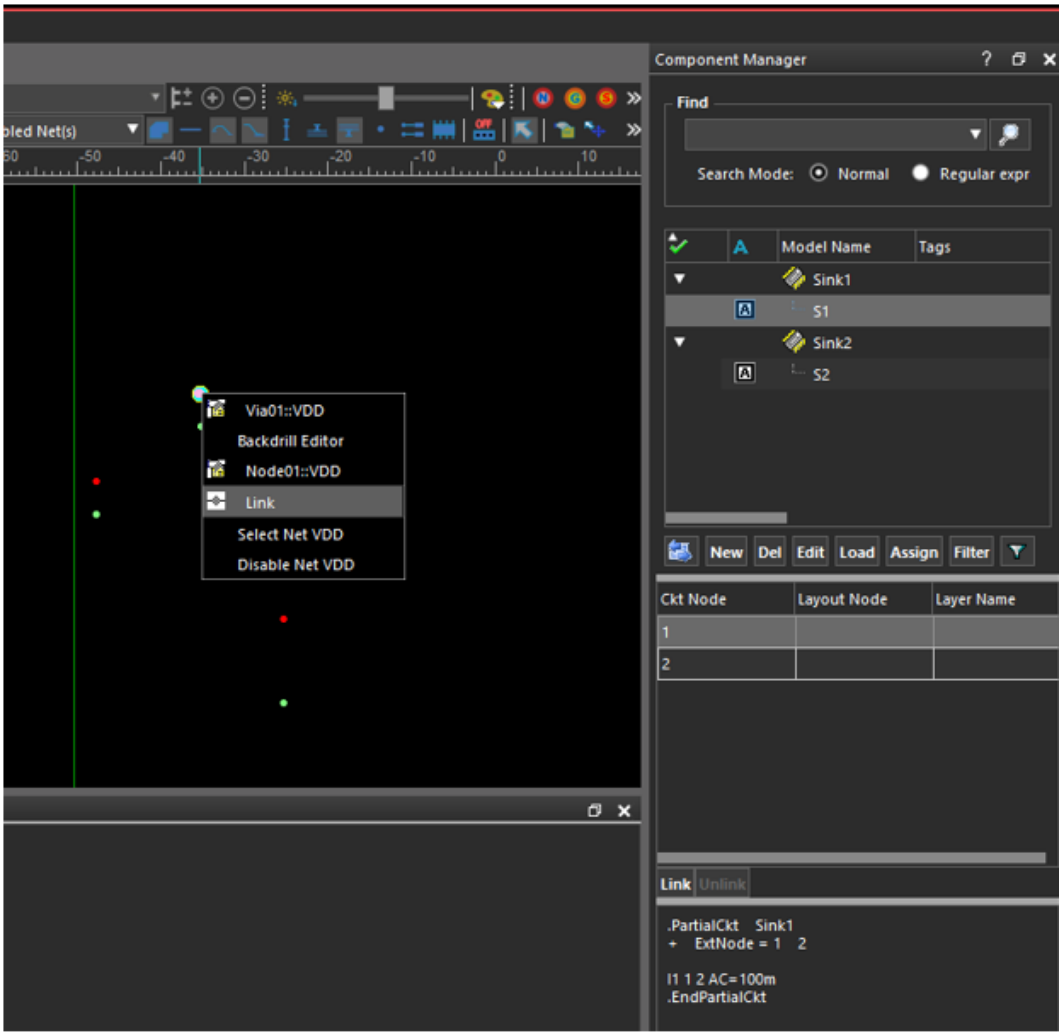
5. **Left-click on S1 Ckt Node 2**
   Click on **S1 Ckt Node 2**, representing the second node of the component.

6. **Right-click on GND Via Node**
   Right-click on the **GND via node** to establish the ground connection.

7. **Left-click Link**
   Left-click **Link** to connect **S1 Ckt Node 2** to the **GND via node**.

8. **Repeat Steps 2-7 for Component S2**
   Repeat the same process for **S2**, connecting its nodes to the **VDD** and **GND** via nodes.

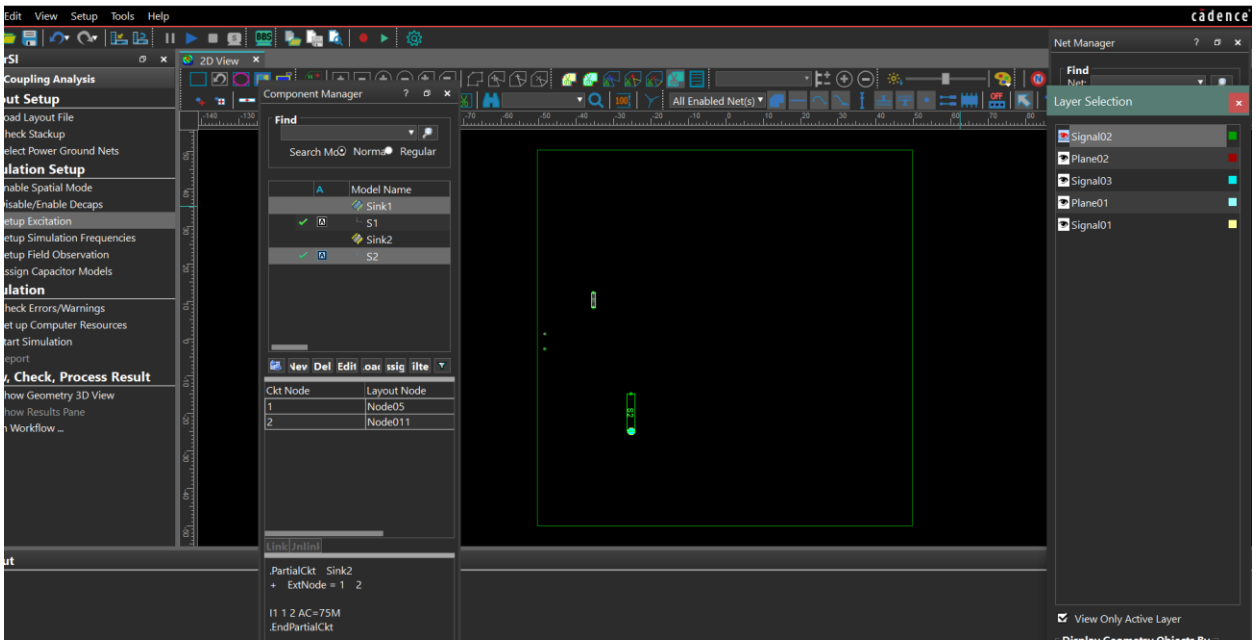
9. **Click on View > Show > Components**
   After connecting both components, click **View > Show > Components** to visualize the components on the layout.



After linking

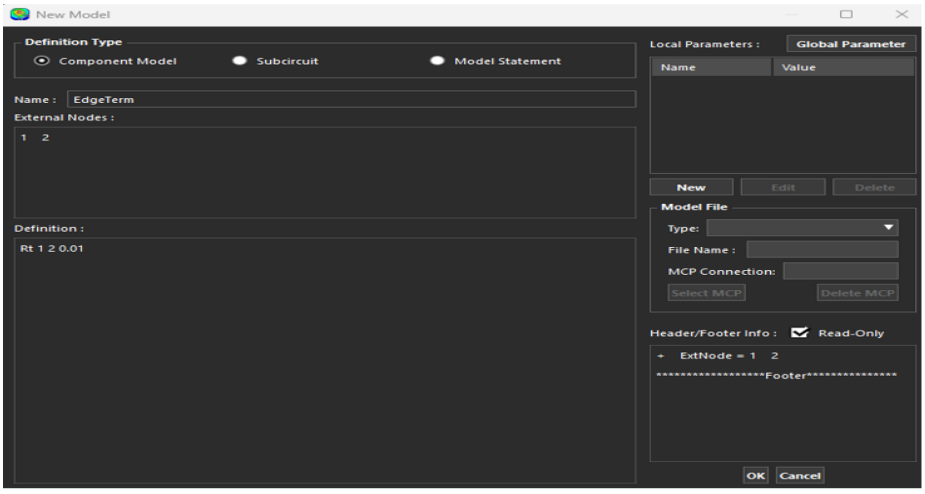
Ckt Node	Layout Node	Layer Name
1	Node01::VDD	Signal02
2	Node07::GND	Signal02

Components visible on the layout:



Creating VRM Terminating Model as a Resistor of 0.01 Ohm:

Creating a **VRM terminating model** as a **0.01 ohm resistor** is done to simulate the short-circuit response of the **Voltage Regulator Module (VRM)**. The resistor represents the internal resistance of the VRM, which plays a critical role in modeling how the power supply interacts with the PCB. By using this resistor, we can accurately simulate the voltage drop and power dissipation at the VRM's power and ground nodes, ensuring that the power delivery network's behavior is properly accounted for during simulation. This helps optimize the design for efficient power distribution and minimizes potential voltage noise or instability.



Creating and Linking the Edgeterm Model to the Layout:

Creating a component using the **Edgeterm model** and linking it to the layout represents the **voltage regulator module (VRM) termination** in the power delivery network. The Edgeterm model helps simulate the response of the VRM's power connection, typically modeled as a resistor, allowing us to understand how the VRM interacts with the power and ground planes. Linking this model ensures that the VRM termination is correctly integrated into the simulation, affecting voltage distribution and impedance characteristics, which are crucial for power integrity.

Steps to Create and Link the Edgeterm Model:

1. **Click the New Button**
   Click the **New** button to create a new component in the **Component Manager**.

2. **Select New Component Type and Click OK**
   Choose **New Component Type** and click **OK** to define the component for the Edgeterm model.

3. **Select Name "EdgeTerm"**
   Name the new component **EdgeTerm** to represent the VRM termination model.

4. **Give Component Reference Designator of "Rt" and Click OK**
   Assign the reference designator **Rt** to the component, indicating it represents the VRM termination. Click **OK** to finalize the component creation.

5. **Click Ckt Node 1 of Rt**
   Select **Ckt Node 1** of the **Rt** component to begin the connection process.

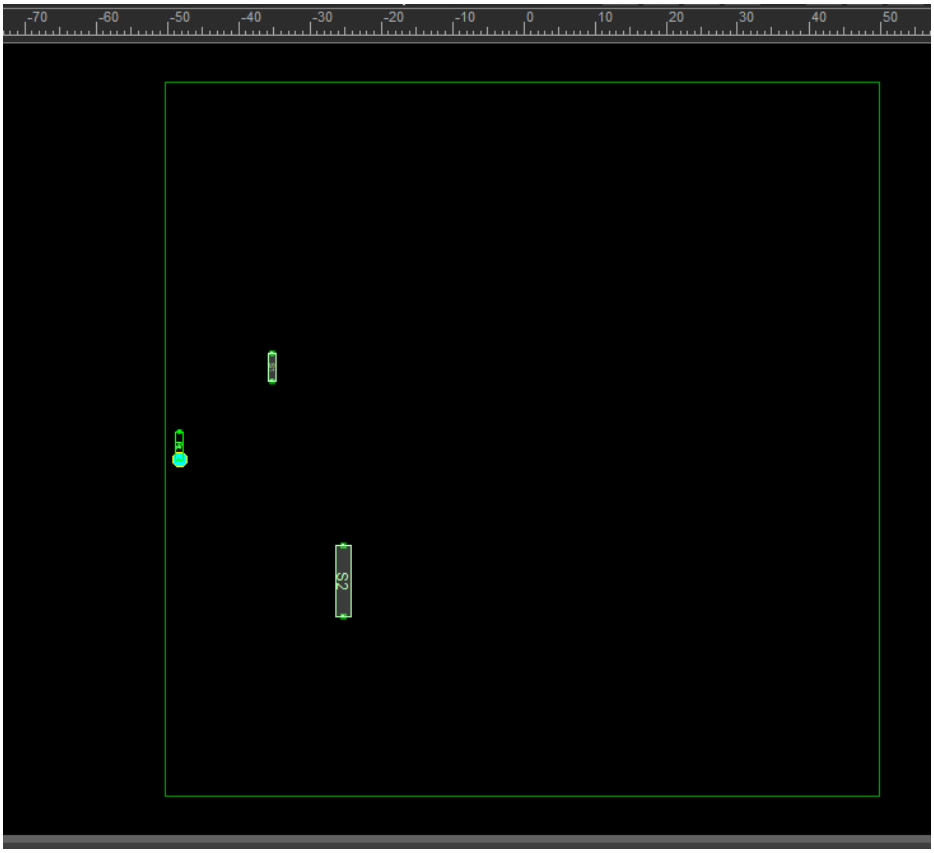
6. **Right-click on VDD Node**
   Right-click on the **VDD node** to link it to the power plane.

7. **Select Link**
   Click **Link** to connect **Ckt Node 1** of the **Rt** component to the **VDD node**.

8. **Click Ckt Node 2 of Rt**
   Select **Ckt Node 2** of the **Rt** component to complete the connection.

9. **Select Link**
   Click **Link** again to connect **Ckt Node 2** to the appropriate power or ground node, ensuring proper termination.

Layout after Linking:

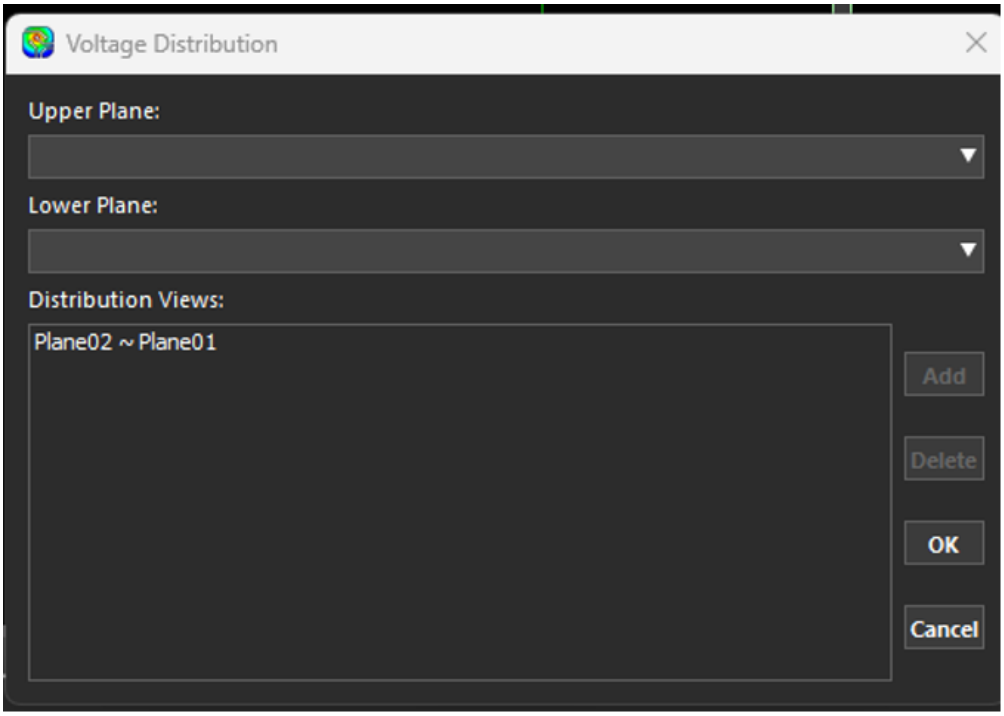


Setting Up Simulation Frequencies:

Setting up **simulation frequencies** is essential for analyzing the behavior of the PCB across a range of frequencies. Different components and signals on the PCB behave differently at various frequencies, and power delivery networks can show resonance or impedance issues at specific frequencies. By defining the frequency range for the simulation, we ensure that the system is evaluated under realistic operating conditions, allowing us to identify critical frequency points, such as peak voltage or resonance frequencies, and optimize the design for stable performance across the full operating spectrum.

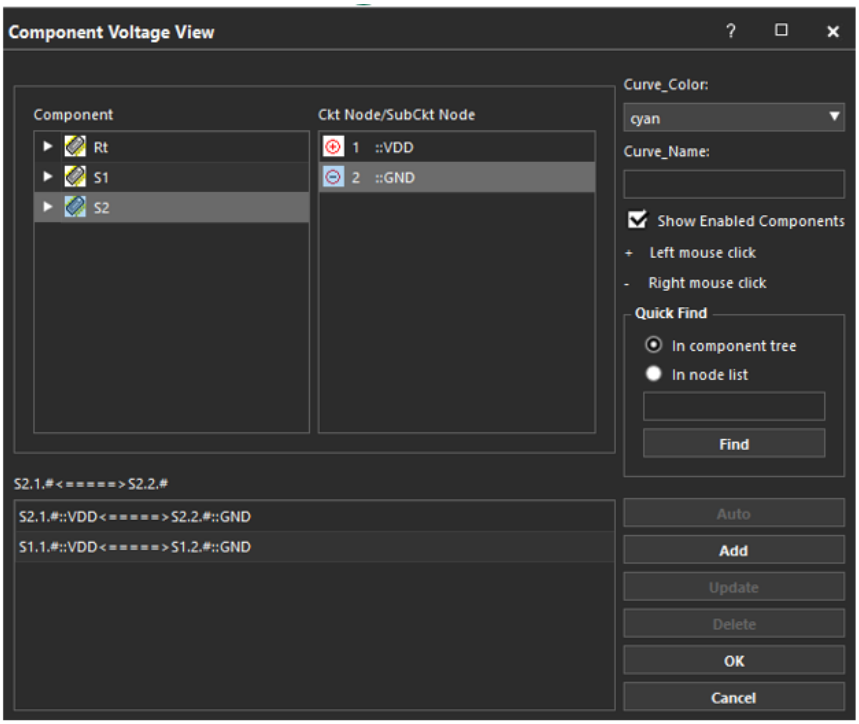
Specifying Plane Layers to Observe Voltage Distributions:

Specifying the **plane layers** to observe voltage distributions allows us to analyze how voltage varies across the power (VDD) and ground (GND) planes in the PCB. This is important for identifying areas with high voltage fluctuations or noise, which could affect the performance and stability of the circuit. By observing voltage distributions between the power and ground planes, we can pinpoint **hotspots** of potential problems, such as resonance or voltage dips, and take corrective actions, like adding decoupling capacitors, to improve the power integrity of the design.



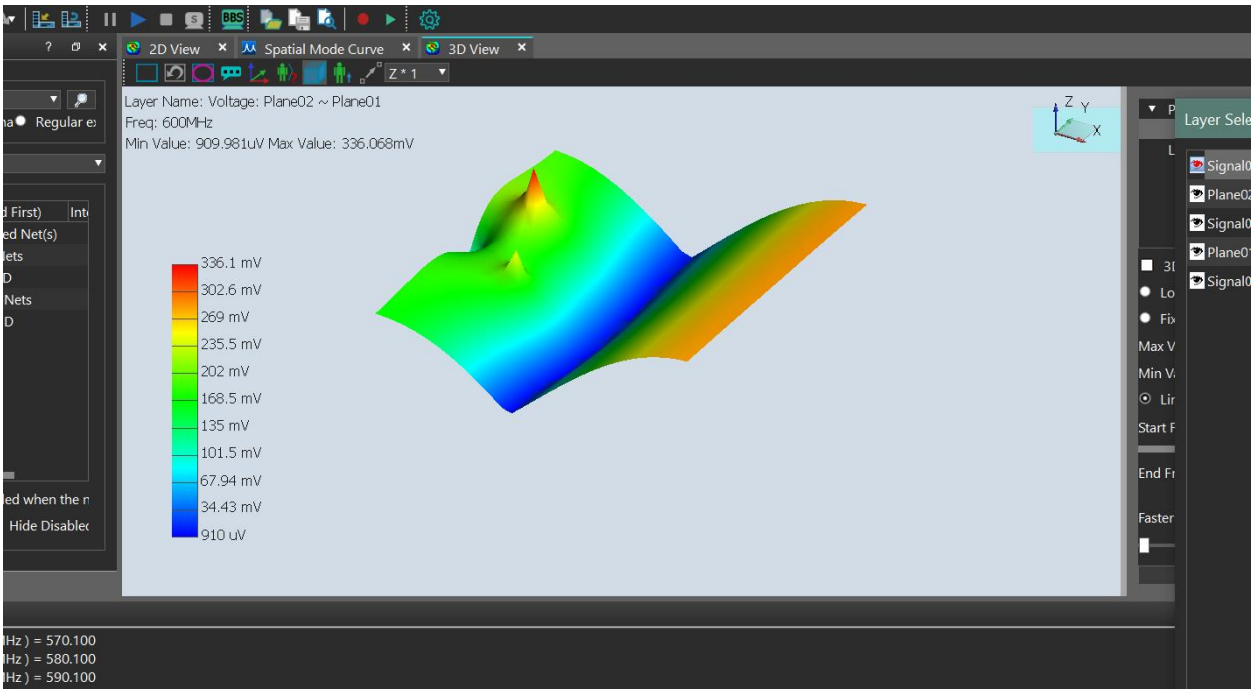
Setting Up Observation of Voltages at Components S1 and S2:

Setting up observation of voltages at components S1 and S2 allows us to monitor the voltage levels at critical points in the design, specifically at the active components (S1 and S2) that are consuming power. By observing these voltage levels, we can ensure that the components are receiving stable voltage and identify any fluctuations or irregularities that could impact their performance. This observation helps in evaluating the effectiveness of the power delivery network, ensuring that the design is optimized for reliable operation and minimal noise or voltage dips at the component level.

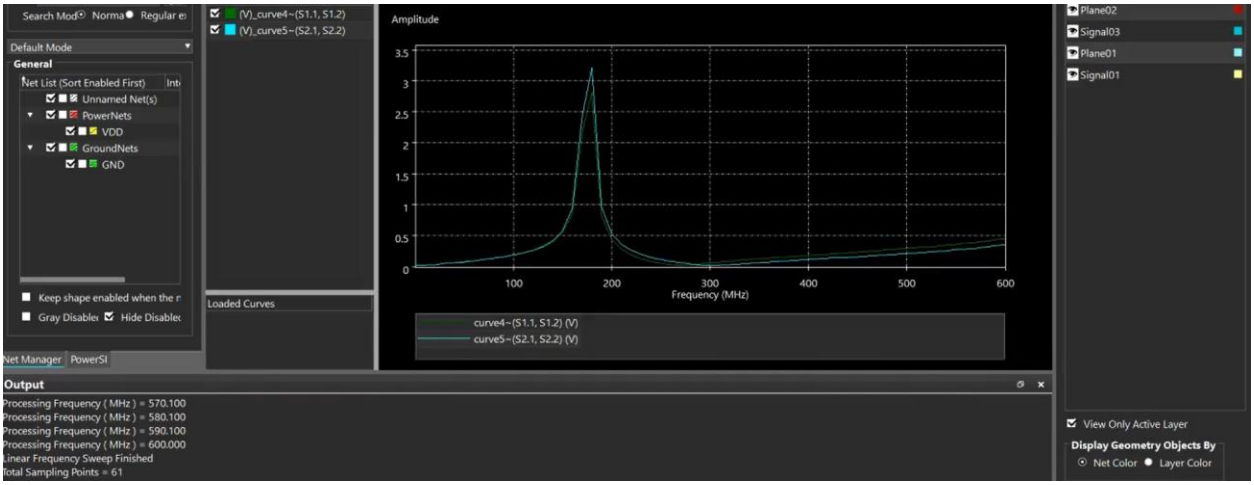


Start the Simulation:

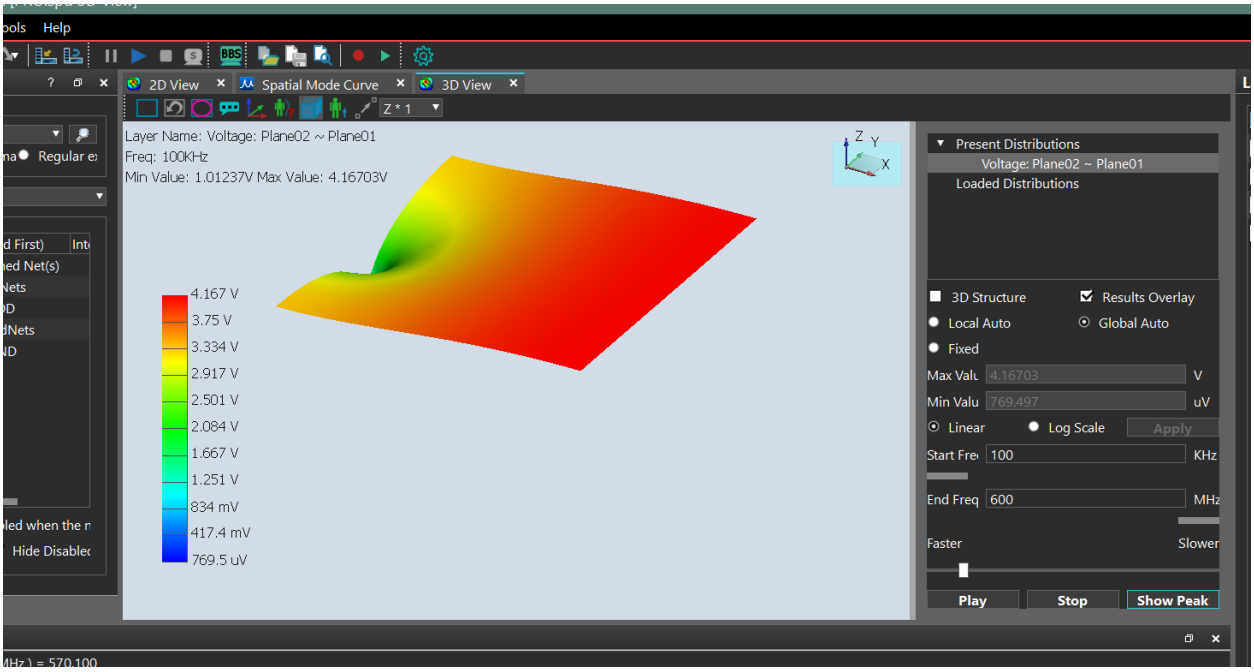
3d-plot



Peak Voltage level:



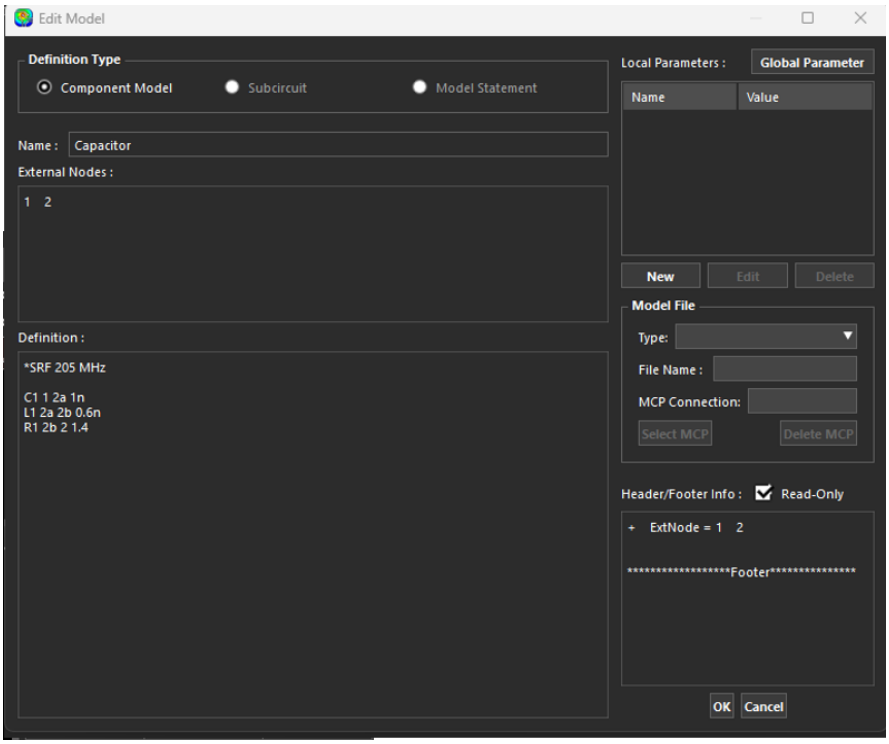
Peak Voltage 3d image:



Adding Decoupling Capacitors to Reduce Peak Voltages:

Adding decoupling capacitors is essential to reduce the peak voltages at sink locations and across the entire layout. Decoupling capacitors help stabilize the power supply by filtering out high-frequency noise and mitigating voltage spikes caused by rapid current changes. These capacitors act as local energy reservoirs, providing a quick supply of current during

transient conditions and preventing voltage fluctuations that could otherwise affect the performance of sensitive components. By placing decoupling capacitors at strategic locations, especially at voltage noise hotspots, we enhance the overall power integrity, reduce noise, and ensure stable operation of the PCB.



Adding Decoupling Capacitors to Reduce Peak Voltages:

Adding decoupling capacitors helps to reduce peak voltages at sink locations and across the layout by filtering high-frequency noise and stabilizing the power supply. These capacitors act as local energy buffers, providing current during transient conditions and preventing voltage fluctuations that can affect component performance. This step ensures improved power integrity, reduced noise, and a more stable operating environment for active components.

Steps to Add Decoupling Capacitors:

1. **Create 5 Decoupling Capacitors from Capacitor Model**
   To start, we will create 5 decoupling capacitors based on a predefined Capacitor model to ensure uniformity across the design.

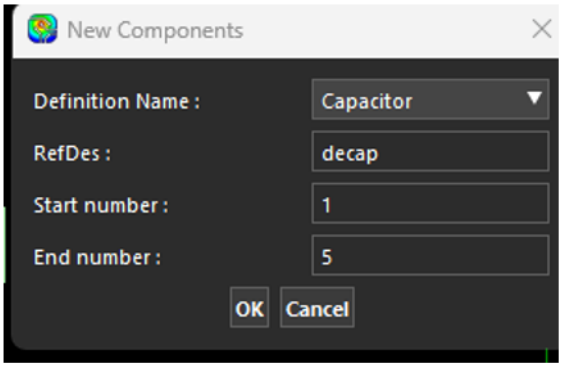
2. **Click New Button in the Component Manager**
   Open the Component Manager and click the New button to start creating the decoupling capacitors.

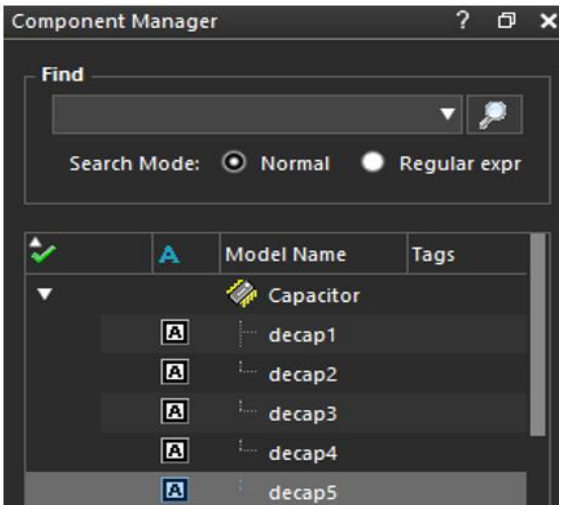
3. **Select New Component**
   Choose the New Component option to define the new capacitor components that will be added to the layout.

4. **Give Reference Designator Name ‘decap’**
   Assign the reference designator ‘decap’ to the decoupling capacitors. This name will identify all capacitors used for decoupling in the design.

5. **Enter 1 for Start Number and 5 for End**
   Set the range for the decoupling capacitors by entering 1 as the start number and 5 as the end number. This will create 5 references for the capacitors, each of which will be placed at different locations in the design.

6. **Note 5 Decap References are Created for Capacitor Model**
   The above steps will create 5 distinct references for the decoupling capacitors, each based on the defined Capacitor model. These references will be placed at critical points in the layout to reduce peak voltages and improve power delivery network stability.





Adding Decoupling Capacitors and Connecting Vias:

Adding **decoupling capacitors** at specific locations (next to sinks and voltage hotspots) helps to reduce peak voltages and stabilize the power delivery network. By placing the capacitors in areas with high voltage fluctuations, we can filter out noise and prevent resonant voltage spikes that could adversely affect the performance of the components. This process ensures that the system operates more efficiently and reliably. After placing the capacitors, rerunning the simulation allows us to confirm the effectiveness of the changes by observing the reduction in peak voltage levels.

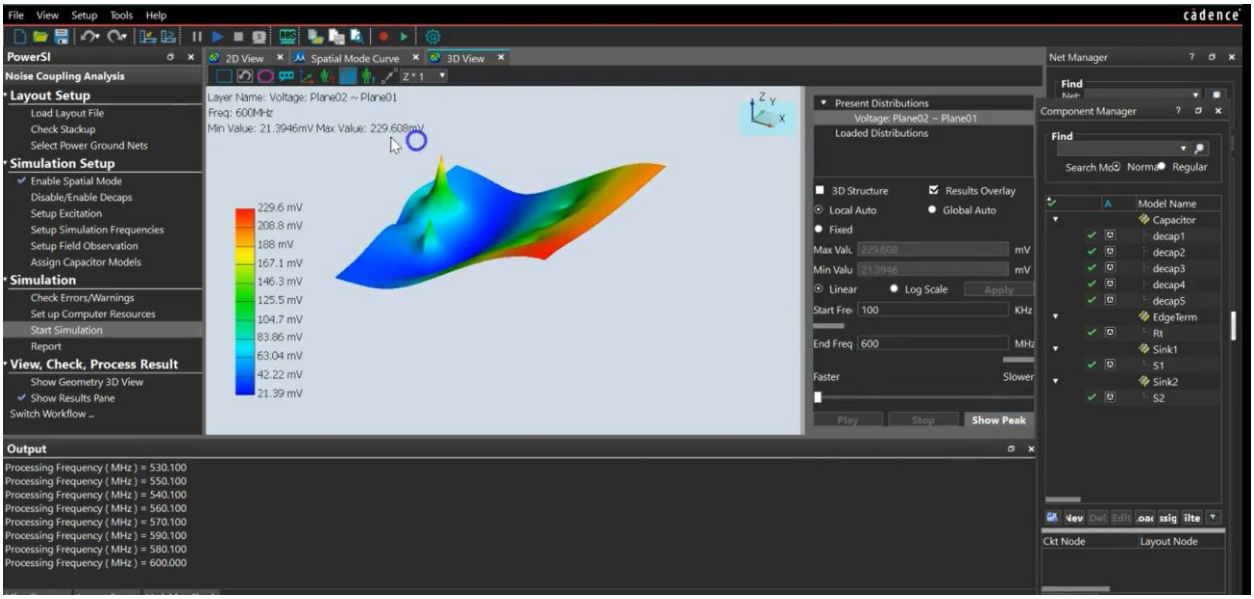
Steps:

1. **Create VDD/GND Vias Next to Sinks and in Hotspots**
   Vias are created next to the **sinks** (active components) and in the **voltage hotspots**, which are the areas of high noise or fluctuating voltage. These vias ensure that the decoupling capacitors can be connected to both the **VDD** and **GND** planes.

2. **Connect Decoupling Capacitors at These Locations**
   Place the decoupling capacitors at the identified hotspots and near the sinks. The capacitors are connected to the VDD and GND planes via the vias, allowing them to stabilize voltage levels and reduce noise.

3. **Rerun Simulation to See Reduction in Peak Voltage Distribution**
   After placing the decoupling capacitors, rerun the simulation to observe the impact on voltage distribution across the layout. The decoupling capacitors should reduce the peak voltages at the sink locations and throughout the layout, improving power integrity.

4. **Observe Reduction in Peak Voltage**
   The simulation should show a significant reduction in the peak voltage levels at the hotspots. In the project the peak voltage drops from **336.427mV** to **229.608mV**, indicating that the decoupling capacitors are effectively reducing noise and stabilizing the voltage. This reduction confirms the effectiveness of the capacitors in improving power integrity and reducing voltage fluctuations.



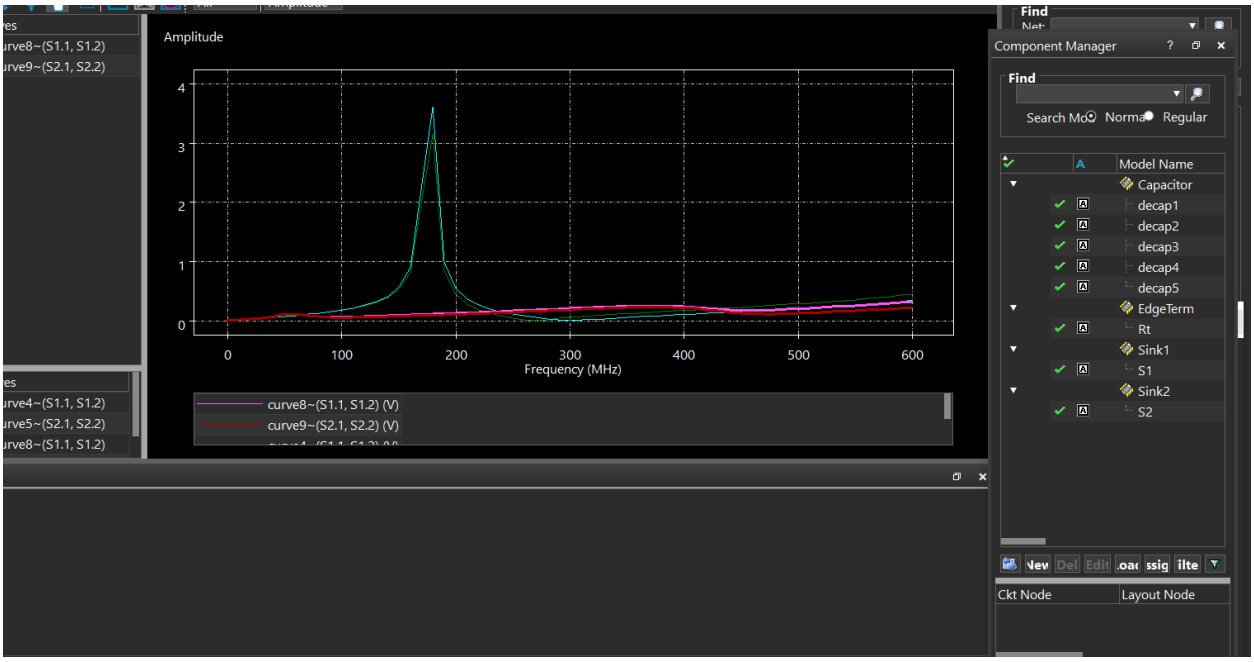
Comparison of Peak Voltage Distribution With and Without Decoupling Capacitors

How Decoupling Capacitors Are Reducing Voltages:

Without decoupling capacitors, the simulation shows higher peak voltages, as seen in the initial value of **336.427mV**. This higher voltage indicates fluctuations and noise in the power delivery network, typically caused by rapid current transients in the circuit.

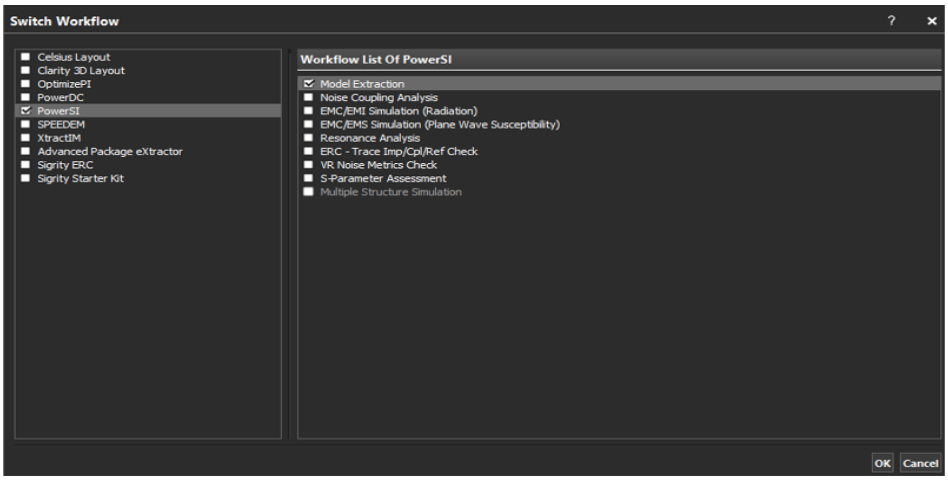
After placing the decoupling capacitors near the **sinks** and **hotspots**, the peak voltage drops to **229.608mV**. The decoupling capacitors effectively filter out high-frequency noise and mitigate voltage spikes by acting as local energy reservoirs. They provide quick bursts of current to maintain voltage stability, reducing the voltage fluctuations at critical points. This results in a more stable power delivery system and improved overall performance of the PCB.

The reduction in peak voltage demonstrates the capacitors' ability to minimize power and ground noise, ensuring that the active components receive a clean, stable power supply.



Changing to Workflow to Model Extraction:

Changing to the **Model Extraction workflow** is done to analyze and extract the impedance characteristics of the power and ground planes, specifically the **Z11 impedance**. This workflow allows for a more detailed investigation of the electrical properties of the PCB, focusing on the frequency-dependent behavior of the power delivery network. By switching to this workflow, we can evaluate the effects of the decoupling capacitors on the impedance and ensure that the power delivery system is optimized for stable operation. The extraction workflow helps us generate more accurate models of the PCB, which can be used for further analysis and comparison with real-world performance.



Using Ports for Extraction Workflow:

In the **Model Extraction workflow**, we use **ports** to define the electrical boundaries of the system and to extract impedance parameters (such as **Z11**). By setting up ports, we can measure and analyze the power/ground impedance, ensuring that the power delivery network is optimized and stable. Ports represent the input and output points of the system where the electrical signals or currents enter and exit. Setting the reference impedance to **1 ohm** helps simulate a realistic scenario and ensures the system's impedance is matched properly for accurate extraction of the parameters.

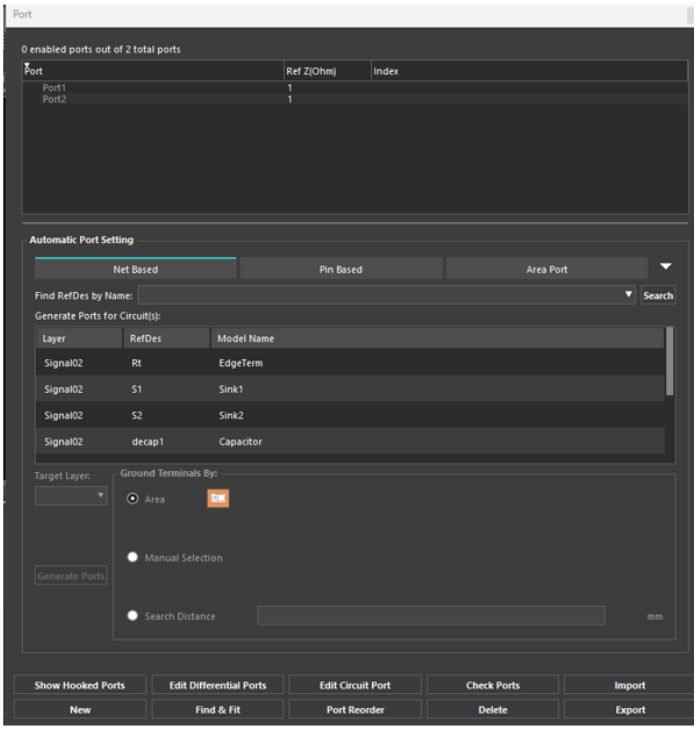
Steps to Set Up Ports for Extraction:

1. **Go to Setup > Port...**
   Navigate to the **Setup** menu and select **Port** to access the settings for defining the ports in the model.

2. **Click New Button Twice**
   Click the **New** button twice to create two ports. These ports will be used to connect the system for extracting impedance values.

3. **Change Reference Z (Ohm) to 1 Ohm**
   In the Port settings, change the **Reference Z (Ohm)** to **1 ohm**. This sets the reference impedance to 1 ohm, which is typically used in simulations for impedance matching to ensure accurate extraction of power and ground plane behavior.

4. **Select Port1 in the Menu Bar Pulldown Menu**
   From the menu bar, select **Port1** from the **pulldown menu**. This connects Port1 to the system and prepares it for impedance extraction. We are using this port to define one boundary for extracting impedance parameters.



Hooking the Ports:

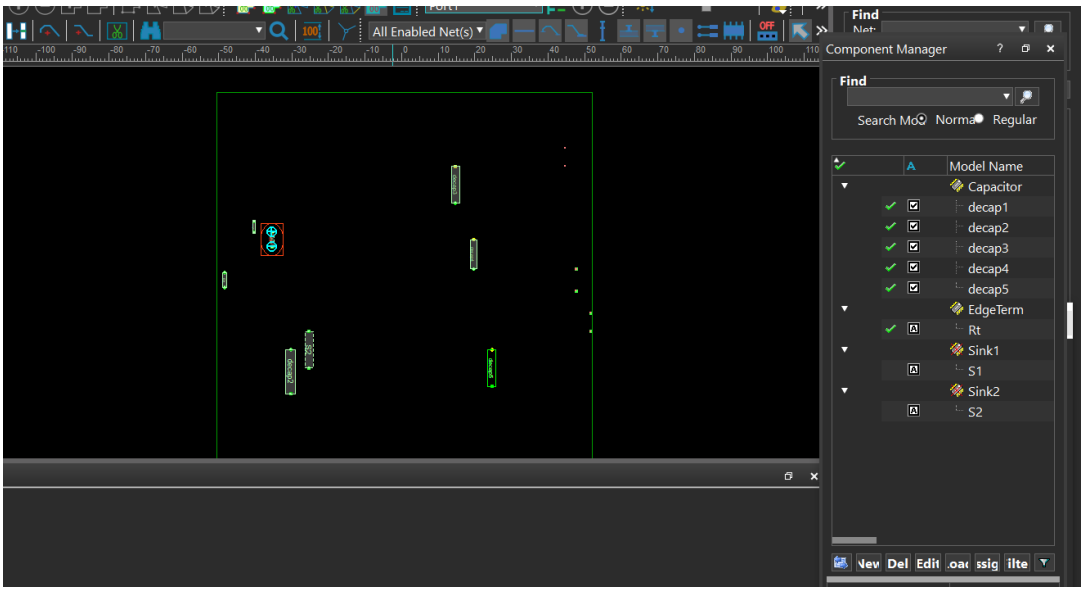
Hooking ports is an essential step in the **Model Extraction workflow** to define the electrical boundaries of the system and enable the extraction of impedance parameters, such as **Z11**. Ports serve as the interface points where signals or currents enter or exit the system. By hooking the ports to specific nodes, such as **VDD** and **GND**, we establish where the electrical behavior is measured and simulated.

Hooking ports allows us to:

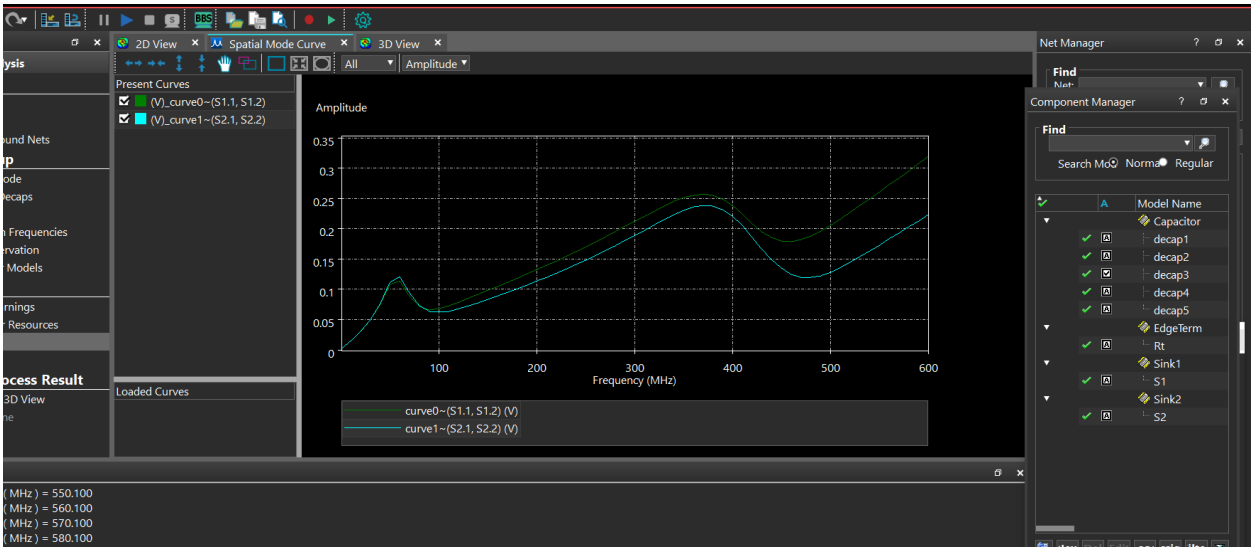
1. **Extract Impedance Parameters**: Ports enable the measurement of parameters like **Z11**, which helps assess the power/ground impedance and the overall efficiency of the power delivery network.

2. **Define System Boundaries**: Ports act as connection points, setting the boundaries of the model so that we can accurately analyze the interaction between the power/ground planes and active components.

3. **Enable Realistic Simulations**: Properly hooked ports ensure that the simulation reflects realistic operating conditions by representing how the power and ground systems connect to external loads or components.



Activating Decoupling Capacitors and Running simulation:

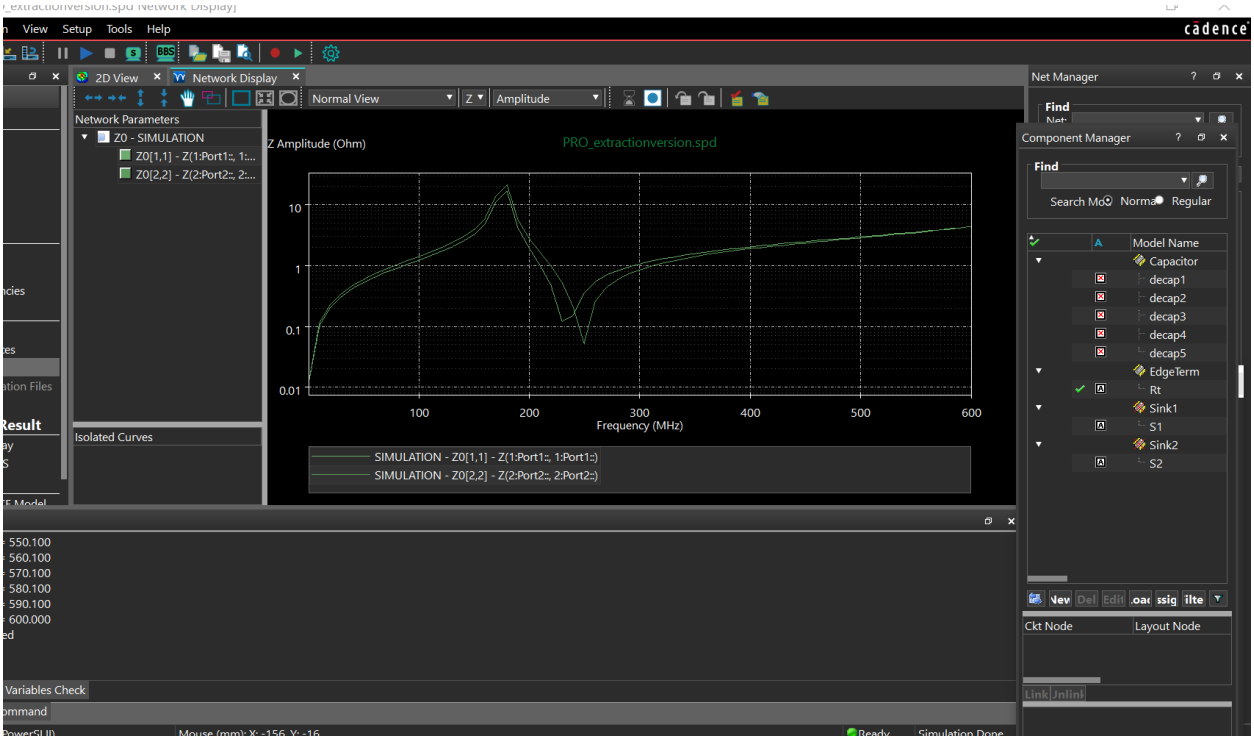


Deactivating Decoupling Capacitors and Running Extraction Simulation:

1. **Go to Component Manager and Deactivate Decoupling Capacitors**
   Open the **Component Manager** and locate the **decoupling capacitors** (decaps) in the model. To deactivate the decoupling capacitors, click the box next to each component twice. A **red X** will appear next to the component, indicating that it has been deactivated. This step ensures that the decoupling capacitors are not included in the simulation for impedance extraction.

2. **Start the Simulation**
   After deactivating the decoupling capacitors, begin the simulation by clicking on the **Start Simulation** button. This will run the extraction simulation to analyze the power and ground impedance without the influence of the decoupling capacitors.

3. **Select Z Parameters from the Extraction Menu Options**
   Once the simulation has started, go to the **Extraction menu** and select the **Z parameters** (impedance) options. This allows the simulation to focus on extracting the **Z11 impedance** of the power/ground planes, which is essential for assessing the power delivery network's integrity and stability.



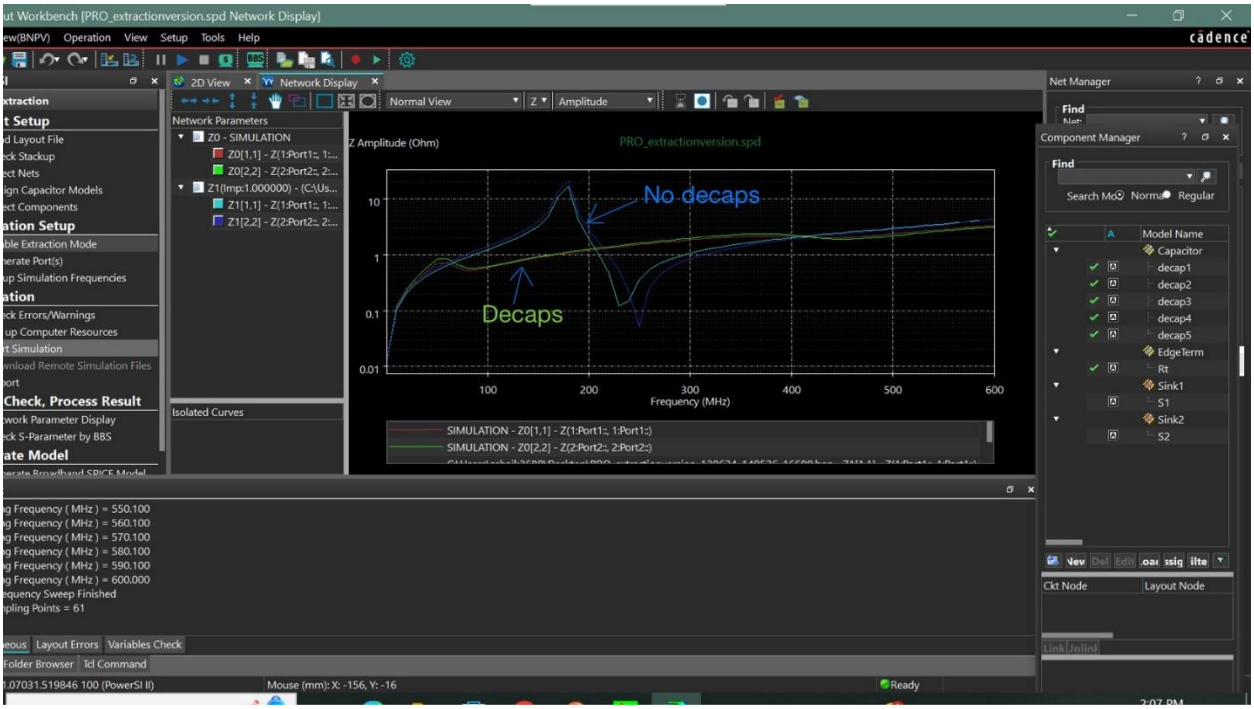
Reactivating Decoupling Capacitors and Running Extraction Simulation:

1. **Go to Component Manager and Reactivate Decoupling Capacitors**
   Open the **Component Manager** and locate the **decoupling capacitors** (decaps) in the model. To reactivate the decoupling capacitors, click the box next to each component once. The **red X** will disappear, indicating that the decoupling capacitors are now active and included in the simulation.

2. **Go to the Toolbar and Click Start Simulation**
   After reactivating the decoupling capacitors, go to the **Toolbar** and click the **Start Simulation** button (blue arrow) to begin the extraction simulation with the capacitors now included.

3. **Select Z Parameters from the Extraction Menu Options**
   Once the simulation starts, go to the **Extraction menu** and select the **Z parameters** options. This step focuses the simulation on extracting the **Z11 impedance** of the power/ground planes with the decoupling capacitors in place.

4. **Right-click in the Network Parameters Panel and Load Simulation Without Decaps for Comparison**
   After running the simulation with the decoupling capacitors, right-click in the **Network Parameters panel** and load the previous simulation results (without decoupling capacitors) for comparison. This allows you to evaluate the effect of the decoupling capacitors on the impedance and overall power delivery network performance.



Conclusion:

In this project, we successfully utilized **Cadence PowerSI** to analyze and optimize the power delivery network (PDN) of a 5-layer PCB. Through the careful placement of **decoupling capacitors** at strategic locations, we were able to reduce voltage noise and stabilize the power/ground planes, leading to improved power integrity across the design. By leveraging both **Spatial Mode** and **Extraction Mode**, we performed detailed simulations to identify **voltage hotspots**, optimize impedance characteristics, and verify the effectiveness of our modifications.

The results clearly demonstrated the importance of decoupling capacitors in mitigating voltage fluctuations, as evidenced by the reduction in peak voltage from **336.427mV** to **229.608mV**. The comparison of impedance values before and after capacitor placement confirmed a significant enhancement in power delivery, providing a more stable and efficient operating environment for the active components.

This project not only highlights the critical role of power integrity in high-speed PCB design but also emphasizes the effectiveness of **Cadence PowerSI** in identifying and addressing power-related challenges. The insights gained from this work will contribute to the design of more reliable, efficient, and stable electronic systems, ensuring optimal performance in real-world applications.

The successful implementation of decoupling capacitors and impedance optimization demonstrates the value of detailed simulations in ensuring the reliability and efficiency of power delivery networks, marking a significant step toward the creation of robust and high-performance PCBs.