# Shaheed Basha Shaik

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**Portfolio:** skshaheed-34.github.io/portfolio


## PROFESSIONAL SUMMARY


Computer Engineering master's student with strong hands-on experience across **ASIC/SoC design, RTL development, and design verification**. Proven background in **System Verilog/UVM-based verification**, assertion-driven validation, and coverage closure, complemented by **RTL design, FPGA prototyping, and ASIC flow exposure** including synthesis, STA, and formal verification. Solid hardware foundation spanning **digital systems, low-power design concepts, and mixed-signal awareness**, supported by Python/Tcl-based automation and rigorous debugging through waveform analysis and lab-based validation. Seeking full-time roles in **ASIC Design, RTL Development, or SoC Design Verification**.


## TECHNICAL SKILLS

**Design Verification & RTL:** SystemVerilog, Verilog, UVM testbench development, constrained-random testing, directed testing, assertions (SVA), functional coverage, coverage closure, debugging & waveform analysis

**ASIC / SoC Design & Flow:** RTL design & integration, synthesis, static timing analysis (STA), gate-level simulation (GLS), equivalence checking, formal verification (JasperGold exposure), low-power design concepts, clocking & reset strategies, SoC architecture fundamentals, memory-mapped interfaces

**Automation & Scripting:** Python, Tcl, Bash, regression automation, log analysis, test infrastructure & workflow development

**FPGA & Prototyping:** FPGA prototyping (Vivado), hardware–software co-design, RTL bring-up & validation on FPGA

**Hardware, Lab & Validation:** Oscilloscope, logic analyzer, signal generator, multimeter, measurement-driven debug, root-cause analysis, post-silicon debug fundamentals

**Tools & Environment:** VCS / Questa, Cadence JasperGold, Vivado, Linux, Git, GitHub, JIRA

## PROJECTS

**SoC Subsystem Verification using SystemVerilog/UVM** **Spring 2026**

- Developed a UVM-based verification environment for a SoC-level subsystem including bus interface, control registers, and memory-mapped peripherals
- Implemented constrained-random stimulus, functional coverage, and assertion-based checks to verify corner cases and drive coverage closure
- Debugged RTL issues through waveform analysis and coverage feedback; automated regressions using Python/Tcl

**FPGA-Based ALU Design, Integration, and Verification** **Fall 2025**

- Designed a 32-bit ALU in Verilog supporting arithmetic and logical operations; integrated and synthesized for FPGA implementation
- Built SystemVerilog testbenches with directed and randomized tests, achieving 100% functional coverage
- Analyzed timing and resource utilization using Vivado and validated correct operation on FPGA hardware

**Formal Property Verification of Control Logic** **Spring 2026**

- Authored SystemVerilog Assertions (SVA) to verify protocol behavior, FSM correctness, and clock-gating conditions
- Applied formal verification using Cadence JasperGold to explore corner cases and unreachable states
- Identified and optimized inefficient state transitions, improving robustness and power-awareness

**Low-Power Memory Controller Design** **Spring 2025**

- Architected and implemented an SRAM controller in Verilog with clock-gating and low-power operating modes

- Balanced latency, power, and timing constraints through iterative RTL refinement and STA-driven analysis
- Achieved ~20% improvement in power efficiency without impacting memory access performance

**Digital System Integration & Timing Validation** **Fall 2024 – Spring 2025**

- Integrated multiple RTL blocks within a system-level design, ensuring clean interfaces and timing-safe connectivity
- Performed synthesis and static timing analysis to resolve setup/hold violations on critical paths
- Supported gate-level simulation and equivalence checking to validate post-synthesis correctness

**Phase-Locked Loop (PLL) Design & Simulation** **Mar 2025 – May 2025**

- Designed and simulated a full PLL architecture including VCO, PFD, charge pump, and passive loop filter using LTspice and MATLAB
- Analyzed loop stability, lock time, and frequency behavior; performed FFT-based spectral analysis
- Evaluated design tradeoffs relevant to mixed-signal and clocking systems in SoC environments

## PROFESSIONAL EXPERIENCE:

**Graduate Teaching Assistant – Engineering Electronics Laboratory (EE 330L)**
**San Diego State University, CA | Jan 2026 – Present**

- Supported laboratory instruction covering semiconductor devices, amplifiers, oscillators, and frequency-domain behavior, reinforcing theory-to-hardware correlation
- Guided students in systematic debugging of circuit-level failures using oscilloscopes and signal generators, emphasizing root-cause analysis
- Assisted in validating gain, bandwidth, and timing-related measurements, ensuring consistency between analytical predictions and measured results

**Graduate Teaching Assistant – Electronic Circuits Laboratory (EE 430L)**
**San Diego State University, CA | Aug 2025 – Dec 2025**

- Mentored students on MOSFET-based circuit design including current mirrors, differential amplifiers, and multistage amplifiers
- Supported verification of op-amp characteristics such as bandwidth, CMRR, and stability using measurement-driven validation
- Assisted in identifying and resolving measurement mismatches and functional discrepancies, strengthening debugging discipline

**Junior Software Engineer**
**ACS Solutions, Hyderabad, India | Sep 2023 – Jun 2024**

- Developed and maintained modular software components, applying structured programming and version control practices (Git, JIRA)
- Performed systematic debugging and root-cause analysis to resolve functional issues, improving overall system reliability
- Built automation scripts to streamline testing, data analysis, and reporting workflows, strengthening skills applicable to verification infrastructure
- Collaborated within Agile teams, supporting cross-functional development and disciplined engineering processes

## Education

**Master of Science in Computer Engineering** San Diego State University, California
**Expected June 2026** GPA: **3.5 / 4.0**

## Relevant Coursework:

VLSI Circuit Design, VLSI Testing, Analog Integrated Circuits, RF Systems, Cyber-Physical Systems, Embedded Systems