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**Dear Hiring Manager,**

I am a Computer Engineering master's student at San Diego State University with hands-on experience across ASIC/SoC design, RTL development, and design verification, and I am writing to express my interest in entry-level roles within your hardware engineering team. My background combines strong fundamentals in digital design with practical experience in System Verilog/UVM-based verification, RTL implementation, and automation-driven validation workflows.

Through academic and project-based work, I have developed UVM verification environments for SoC subsystems, implementing constrained-random stimulus, functional coverage, and assertion-based checks to validate control logic, memory-mapped interfaces, and corner cases. I have extensive experience debugging RTL issues through waveform analysis and coverage feedback, and I am comfortable iterating between design and verification to achieve functional completeness and closure.

In parallel, I have worked on RTL design and integration, including a 32-bit ALU and a low-power SRAM controller, gaining exposure to synthesis, static timing analysis, gate-level simulation, equivalence checking, and formal verification using industry-standard tools. These projects strengthened my understanding of timing, power-performance tradeoffs, and clean interface design in ASIC and SoC environments.

I also bring a solid hardware foundation supported by FPGA prototyping, mixed-signal coursework, and lab-based validation. My experience designing and simulating a PLL provided insight into clocking systems, stability analysis, and real-world design tradeoffs that impact SoC reliability. Additionally, I regularly use Python and Tcl to automate regressions, analyze simulation logs, and improve verification efficiency.

Beyond technical skills, my experience as a Graduate Teaching Assistant has reinforced a disciplined approach to debugging, documentation, and clear technical communication. I am comfortable working in collaborative engineering environments, quickly learning new tools and flows, and contributing across both design and verification tasks.

I am highly motivated to contribute to teams developing advanced semiconductor systems and would welcome the opportunity to apply my skills in ASIC design, RTL development, or SoC design verification. Thank you for your time and consideration. I look forward to the opportunity to discuss how my background aligns with your team's goals.

**Sincerely,**
**Shaheed Basha Shaik**