ECE-593, Winter-2024
Fundamentals of Pre-Silicon Validation

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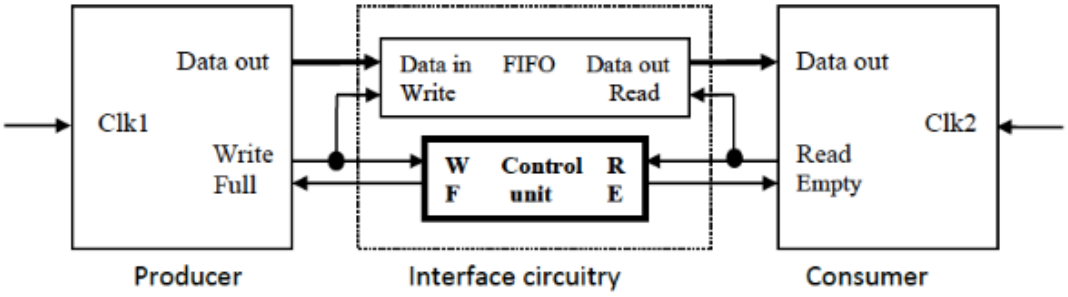
Project: Develop Specification, Implementation and Verification of Asynchronous FIFO

For this project your group will write the HLDS, Implement the Async-FIFO in SystemVerilog and Verify the design using UVM testbench architecture.



Following activities needs to be completed by each group:

Use your google-doc as your work-pad and regularly update your progress.

A. Tasks:

1. Complete the Design Specification document (HLDS), based on the consumer demands. (I will provide the top-level specs)
    a. This should include a schedule of your completion plan and ownership.
2. Implement and successfully compile the design based on requirements presented in HLDS.
3. Verify your implemented Async-FIFO design using various functional verification strategies:
    a. Must include well established Verification Plan documentation.
    b. 100% coverage goals for both code coverage and functional coverage by writing covergroups with different coverpoints and bins(i.e. for functional coverage), provide a detailed

explanation.. If in any case you are not able to achieve, provide a detailed explanation.

c. You must use SVA (SystemVerilog assertions) and covergroups with different coverpoints and bins.
d. You must showcase the usage of targeted tests, constrained-random test.
e. Before building up UVM test architecture, start with class based conventional testbench.

B. Verification Plan to clearly include:

a. Verification Requirements
    i. Verification Levels
    ii. Functions
    iii. Specific test and methods used.
        1. Type of Verification
        2. Verification Strategy
        3. Abstraction Level
        4. Driving principles
        5. Checking methods
    iv. Coverage
    v. Scenarios
b. Management Details
    i. Tools and Methodologies
    ii. Risks and Dependencies
    iii. Resources
    iv. Schedule

C. Deliverables:

a. Your completed HLDS document. Must include groups members name and email. Acknowledgements, citations, references.
b. Your completed Verification Plan (V-PLAN) document
c. HDL codes for your implementation design, follow the good naming practices for each module, interfaces, packages.
d. Test bench and other related codes
e. Make separate directory for conventional/class based and UVM testbenches files.

f. Ensure you rename your transcript-files according to what you are trying to show. All transcripts must be included.
g. Include waveform snapshots of import events and clearly showcasing and highlighting them.

Use Makefile for running simulations.

All the deliverables should be zipped into one file and submitted in Canvas. Please name the zipped file as: **<team_#>_ece593w24_final_project.zip**

Spec and Group Assignments:

Team Number	Specification Option
1, 3, 5	A
2, 4, 6	B
7, 9, 11	C
8. 10, 12, 18	D
13, 17	E
15	Multi-CPU System

Option	Producer Freq (Mhz)	Consumer Freq (Mhz)	Write Idle Cycles	Read idle Cycles	Burst Length
A	250	100	0	2	150
B	500	250	2	0	200
C	500	500	0	4	450
D	250	500	2	3	150
E	750	250	0	2	500

Producer Freq = Writing Frequency
Consumer Freq = Reading Frequency
Write Idle Cycle= Number of idle cycles between successive writes
Read Idle Cycle= Number of idle cycles between successive reads
Burst Length = Number of data items to be transferred
Duty-cycle= Assume 50:50