DSD LAB

LAB 1

Q1)

Write Verilog code to describe the following functions
f1 =ac'+bc+b'c'
f2 = (a+b'+c)(a+b+c')(a'+b+c')
Check whether f1 and f2 in question 1 are functionally equivalent or not.

Source Code :

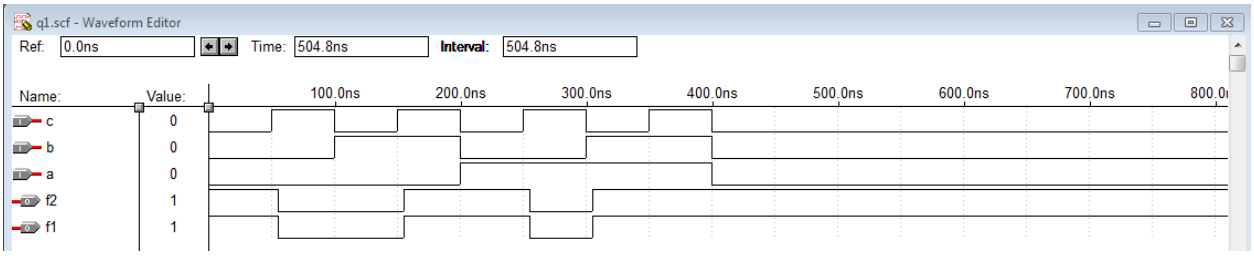
```
module q1(a, b, c, f1, f2);
input a, b, c;
output f1, f2;

not(a1, a);
not(b1, b);
not(c1, c);

and(fa1, a, c1);
and(fb1, b, c);
and(fc1, b1, c1);
or(f1, fa1, fb1, fc1);

or(fa2, a, b1, c);
or(fb2, a, b, c1);
or(fc2, a1, b, c1);
and(f2, fa2, fb2, fc2);
endmodule
```

Output Waveform:



From the graph it is clear that f1 and f2 are functionally equivalent.

Q2)
Simplify the following functions using K-map and implement the circuit using logic gates. Write Verilog code and simulate the circuit
a) f(A,B,C,D) = Σm(1,3,4,9,10,12) + D(0,2,5,11)
b) f(A,B,C,D) = ΠM(6,9,10,11,12) + D(2,4,7,13)

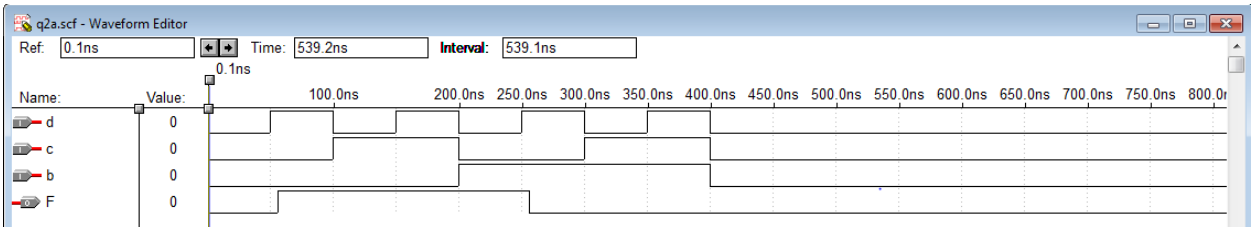
a)

The expression Σm(1,3,4,9,10,12) + D(0,2,5,11) simplifies to the following expression:
F = BC'D' + B'D + B'C

Source Code:

```
module q2a(a, b, c, d, F);
input a, b, c, d;
output F;
assign F = (b & ~c & ~d) | (~b & d) | (~b & c);
endmodule
```

Output Waveform:



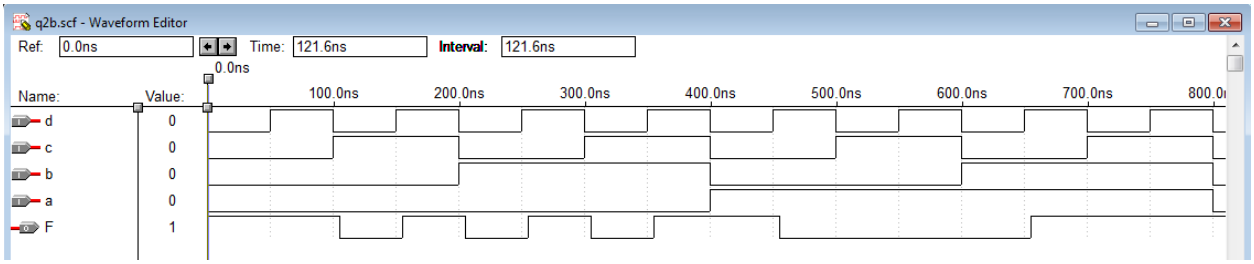
b)

The expression f(A,B,C,D) = ΠM(6,9,10,11,12) + D(2,4,7,13) evaluates to:
F = (A' + B + D')(A' + B + C')(A + C' + D)(B' + C + D)

Source Code:

```
module q2b(a, b, c, d, F);
input a, b, c, d;
output F;
assign F = (~a | b | ~d) & (~a | b | ~c) & (a | ~c | d) & (~b | c | d);
endmodule
```

Output Waveform:



Q3)
Minimize the following expression using K-map and simulate using only NAND gates.
f(A,B,C,D)= πM(2,6,8,9,10,11,14)

The expression f(A,B,C,D)= πM(2,6,8,9,10,11,14) simplifies to:
F = A'C' + A'D + BC' + BD

Source Code:

```
module q3(a, b, c, d, F);
input a, b, c, d;
output F;

assign F = ~(~(~a & ~c) & ~(~a & d) & ~(b & ~c) & ~(b & d));
endmodule
```

Output Waveform: