DSD LAB

Lab 4

Q1)

Source Code:

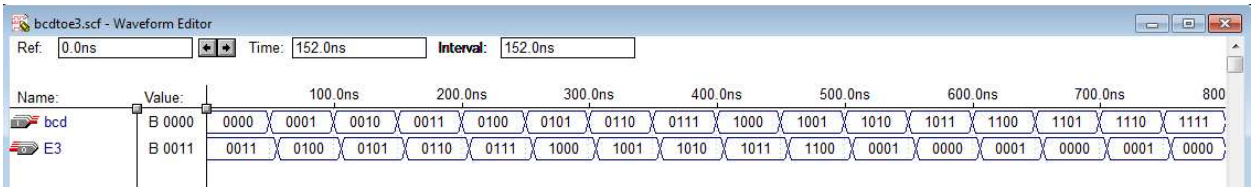
```
module bcdtoe3(bcd, E3);
input [3:0] bcd;
output [3:0] E3;
reg [3:0] E3;
wire e3, e2, e1, e0;
mux8to1 m3({1'b0, 1'b0, 1'b0, 1'b1, 1'b1, bcd[0], 1'b0, 1'b0},bcd[3:1], e3);
mux8to1 m2({1'b0, 1'b0, 1'b0, bcd[0], 1'b0, ~bcd[0], 1'b1, bcd[0]},bcd[3:1], e2);
mux8to1 m1({1'b0, 1'b0, 1'b0, ~bcd[0], bcd[0], ~bcd[0], bcd[0], ~bcd[0]},bcd[3:1], e1);
assign e0 = ~bcd[0];
always @(bcd)
begin
E3[0] = e0;
E3[1] = e1;
E3[2] = e2;
E3[3] = e3;
end
endmodule

module mux8to1(W, S, out);
input [7:0]W;
input [2:0]S;
wire [7:0]W;
wire [2:0]S;
output out;
reg out;

always @(W or S)
begin
case(S)
0: out = W[0];
1: out = W[1];
2: out = W[2];
3: out = W[3];
4: out = W[4];
5: out = W[5];
6: out = W[6];
7: out = W[7];
endcase
end
```

endmodule

Output Waveform:



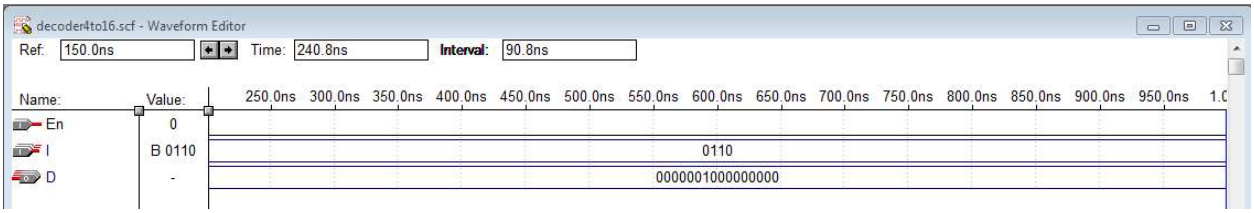
Q2)

Source Code:

module decoder4to16(I, En, D);
input [3:0]I;
input En;
output [0:15]D;
wire [0:3]En_temp;
wire [0:15]Dout;
decoder2to4 d1(I[3:2], En, En_temp[0:3]);
decoder2to4 d2(I[1:0], En_temp[0], Dout[0:3]);
decoder2to4 d3(I[1:0], En_temp[1], Dout[4:7]);
decoder2to4 d4(I[1:0], En_temp[2], Dout[8:11]);
decoder2to4 d5(I[1:0], En_temp[3], Dout[12:15]);
assign D = ~Dout;
endmodule

module decoder2to4(I, En, D);
input [1:0] I;
input En;
output [0:3] D;
reg [0:3] D;
always @(I or En)
begin
D = 4'b1111;
if(En == 0)
case(I)
0: D = 4'b0111;
1: D = 4'b1011;
2: D = 4'b1101;
3: D = 4'b1110;
endcase
else
D = 4'b1111;
end
endmodule

Output Waveform :



Q3)

Source Code:

```
module priorityen16to4(I, PE, z);
input [15:0] I;
output [3:0] PE;
reg [3:0] PE;
output z;
reg z;
integer i;

always @(I)
begin
z = 0;
if(I == 0)
PE = 0;
else
begin
for(i = 0; i<16; i = i+1)
begin
if(I[i] == 1)
PE = i;
end
z = 1;
end
end
endmodule
```

Output Waveform: