**Assignment for CSE VI semester (Compiler Design)**

Marks : 10

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Sub: CSE VI 2016 Roll No.: XXXX Topic

**Format for submission**

1. Introduction
2. Description
3. Operational Function with example
4. Conclusion
5. Reference

**Topics and Roll numbers**

1. Cache interference in optimization (10)
2. Iteration spaces for nesting loop (15)
3. Affine and non affine practices during compilation (16)
4. Self spatial reuse of data (20)
5. Space partition constraints (29)
6. Inter procedural analysis for compiler design (45)
7. Dynamic loading and reflection for context sensitive interprocedural analysis (47)
8. Data flow values for variable and constant propagation framework (59)
9. Custom propagation framework and transfer function (96)
10. Redundancy elimination technique for compiler design (135)
11. Lazy code motion problem (144)
12. Data flow analysis schema (147)
13. Analysis of live variables (152)
14. Semilattice and data flow analysis (154)
15. Iterative algorithm for general framework (160)
16. Region based analysis and reducible flow graph (163)
17. Speed of convergence of iterative data flow algorithm (166)
18. Importance of back edge and reducibility in flow graph (176)
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20. Dead code elimination (223)
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22. Role of quick sort in machine independent optimization (241)
23. Handling of non reducible flow graph (242)
24. Affine expression and reference variables (245)
25. Instruction pipelines and branch delays (248)
26. Multiple instruction issues and parallelism (249)
27. Code scheduling constraints and data dependence (259)
28. Concept of parallelism with respect to register usage (262)
29. Register allocation and code scheduling for instruction level parallelism (264)
30. Block scheduling with respect to prioritized topological order (280)
31. Scheduling cyclic dependency graph for software pipelining (156)
32. Hardware support for software pipeline (163)
33. Optimization for parallelism with respect to data locality (195)