浙江大学

本科实验报告

Cache Controller

课程名称：计算机组成与设计

姓　　名：箫宇

学　　院：信息与电子工程学院

　　系：

专　　业：信息工程

学　　号：

指导老师：刘鹏

2023 年 7 月 2 日

目录

一 有限状态机设计

1. 状态编码设计

如图??所示，我参考教材 5.9 节设计了一共四个状态，分别是：空闲状态 IDLE，Tag 位比较状态 CompareTag，写回状态 WriteBack 以及分配状态 Allocate，各个状态作用如下

(1) IDLE：等待来自 CPU 的控制信号 ld 以及 st，当这两个信号有效时，转移到 CompareTag 状态。

(2) CompareTag：比较来自 Cache 的对应 Block 的 Tag 位与来自 CPU 的地址 Addr 的 [31:11] 位，同时根据对应 Block 的 Valid 与 Dirty 位判断是 Hit 或者 Miss，以及转移到对应的状态。

(3) WriteBack：在此状态将 Cache 中的 Block 写回 L2 Cache 中，当接收到来自 L2 的写回完成信号 write_done 后，写回完成，状态转移到 Allocate。

(4) Allocate：此状态用于在 L1 Cache miss 时将 L2 Cache 中的值加载到 L1 Cache 中，当得到写入完成信号 l2_ack 后，说明写入完成，状态切换到 CompareTag。

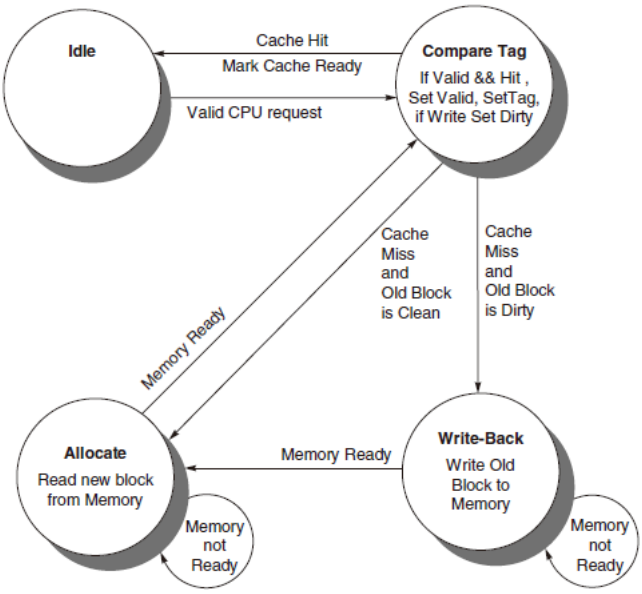

图 1: state diagram

各个状态的状态编码如表??所示

状态编码	
IDLE	00
CompareTag	01
WriteBack	10
Allocate	11

表 1: 状态编码

2. 状态转换表

状态转移表如表**??**所示，‘–’表示在当前状态转移情况下不关心该信号。

state	**ld**	**st**	**tag==addr[31:11]**	**dirty**	**valid**	**l2_ack**	**write_done**	**nextstate**
IDLE	0	0	–	–	–	–	–	IDLE
	0	1	–	–	–	–	–	CompareTag
	1	0	–	–	–	–	–	
	1	1	–	–	–	–	–	
CompareTag	–	–	–	0	0	–	–	Allocate
	–	–	–	1	0	–	–	WriteBack
	–	–	–	–	1	–	–	IDLE
WriteBack	–	–	–	–	–	–	1	Allocate
	–	–	–	–	–	–	0	WriteBack
Allocate	–	–	–	–	–	1	–	CompareTag
	–	–	–	–	–	0	–	Allocate

表 2: 状态转移表

3. FSM 图

FSM 图如图**??**所示。

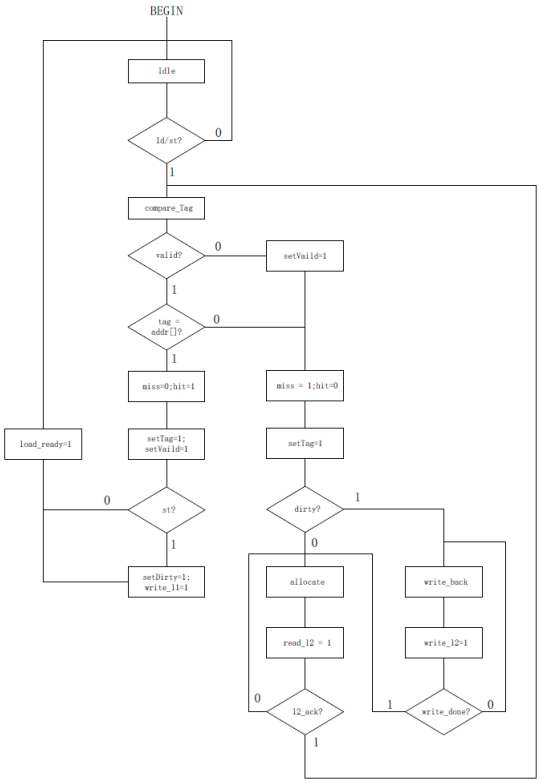

图 2: FSM 图

二 电路设计

我通过 Vivado 软件进行了电路设计，电路图如图**??**所示。

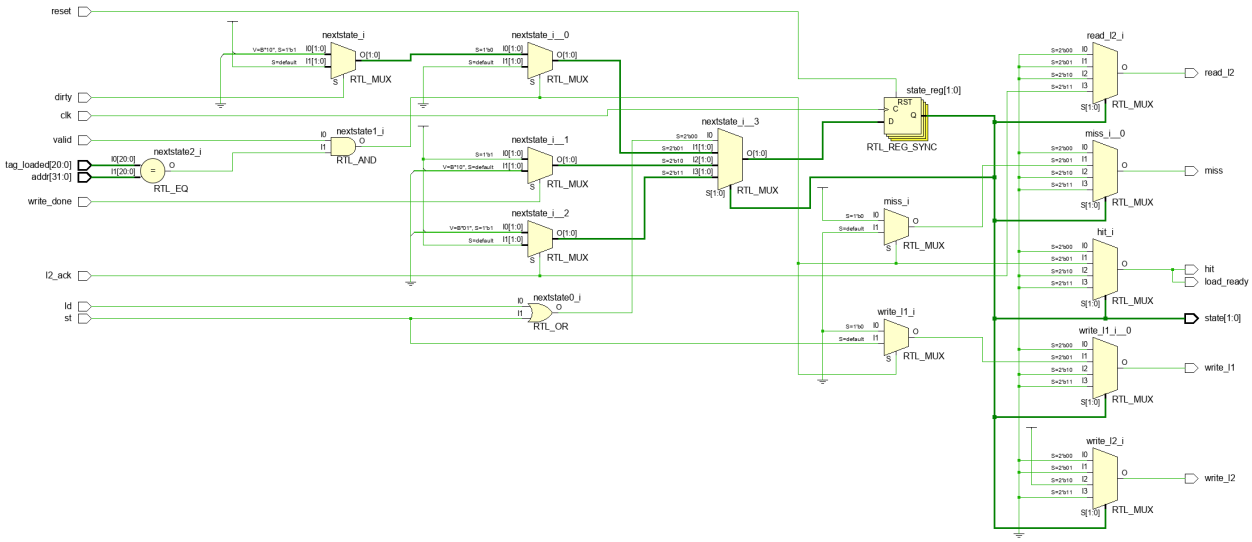

图 3: 电路图

三 Verilog 实现

1. 信号含义详细阐释

(1) clk: 时钟信号

(2) reset: 重置信号

(3) ld: 数据由 L1 加载到 CPU

(4) st: 数据由 CPU 写入 L1

(5) addr: 数据所在地址

(6) valid:L1 的有效位

(7) dirty:L1 的脏位

(8) tag_loaded:L1 对应位置的 Tag

(9) l2_ack: 数据是否完成从 L2 写入 L1 的过程

(10) write_done: 数据是否完成从 L1 写回 buffer 的过程

(11) hit:hit 信号

(12) miss:miss 信号

(13) load_ready:L1 数据是否准备就绪

(14) write_l1: 使能 L1 的写入功能

(15) read_l2: 发向 L2 的 load 指令

(16) write_l2: 使能 L1 写回 buffer

2. Verilog 代码

Cache 控制器的代码 Listing **??**所示。

3. 测试样例

所用测试代码如 Listing **??**所示。

4. 测试结果

Cache Controller 测试结果如图**??**所示，各个控制信号正确，功能能够正常实现

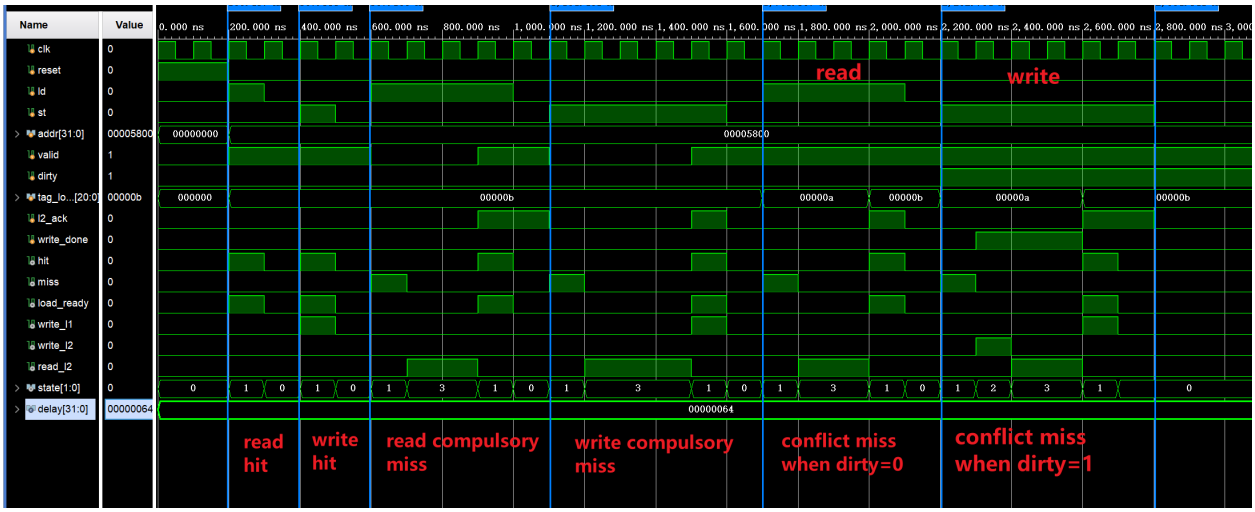

图 4: 测试结果

四 心得体会

通过本次实验，我对 Cache 的整个控制机制有了一个更加具体的理解，同时也补足了自己在学习 Cache 相关内容时所遗漏的知识点。

除此之外，这次实验也是我第一次编写 testbench 文件，对于 Verilog 语言的测试方式有了一个更加透彻的掌握。

五 附录

1. cache 代码

Listing 1: Cache 控制器代码

```
%%
%% This is file `.tex',
%% generated with the docstrip utility.
%%
%% The original source files were:
%%
%% fileerr.dtx  (with options: `return')
%%
%% This is a generated file.
%%
%% The source is maintained by the LaTeX Project team and bug
%% reports for it can be opened at https://latex-project.org/bugs/
%% (but please observe conditions on bug reports sent to that address!)
%%
%%
%% Copyright (C) 1993-2022
%% The LaTeX Project and any individual authors listed elsewhere
%% in this file.
%%
%% This file was generated from file(s) of the Standard LaTeX `Tools
   Bundle'.
%%
   ------------------------------------------------------------------------

%%
%% It may be distributed and/or modified under the
%% conditions of the LaTeX Project Public License, either version 1.3c
%% of this license or (at your option) any later version.
%% The latest version of this license is in
%%    https://www.latex-project.org/lppl.txt
%% and version 1.3c or later is part of all distributions of LaTeX
%% version 2005/12/01 or later.
%%
%% This file may only be distributed together with a copy of the LaTeX
%% `Tools Bundle'. You may however distribute the LaTeX `Tools Bundle'
%% without such generated files.
%%
%% The list of all files belonging to the LaTeX `Tools Bundle' is
%% given in the file `manifest.txt'.
%%
 \message{File ignored}
```

```
\endinput
%%
%% End of file `.tex'.
```

2. 测试代码

Listing 2: Cache 控制器测试文件

```
%%
%% This is file `.tex',
%% generated with the docstrip utility.
%%
%% The original source files were:
%%
%% fileerr.dtx  (with options: `return')
%%
%% This is a generated file.
%%
%% The source is maintained by the LaTeX Project team and bug
%% reports for it can be opened at https://latex-project.org/bugs/
%% (but please observe conditions on bug reports sent to that address!)
%%
%%
%% Copyright (C) 1993-2022
%% The LaTeX Project and any individual authors listed elsewhere
%% in this file.
%%
%% This file was generated from file(s) of the Standard LaTeX `Tools
   Bundle'.
%%
   ------------------------------------------------------------------------

%%
%% It may be distributed and/or modified under the
%% conditions of the LaTeX Project Public License, either version 1.3c
%% of this license or (at your option) any later version.
%% The latest version of this license is in
%%    https://www.latex-project.org/lppl.txt
%% and version 1.3c or later is part of all distributions of LaTeX
%% version 2005/12/01 or later.
%%
%% This file may only be distributed together with a copy of the LaTeX
%% `Tools Bundle'. You may however distribute the LaTeX `Tools Bundle'
```

```
%% without such generated files.
%%
%% The list of all files belonging to the LaTeX `Tools Bundle' is
%% given in the file `manifest.txt'.
%%
 \message{File ignored}
\endinput
%%
%% End of file `.tex'.
```