

Lab2. Wang Junfei 33006896

Two tristate inverters

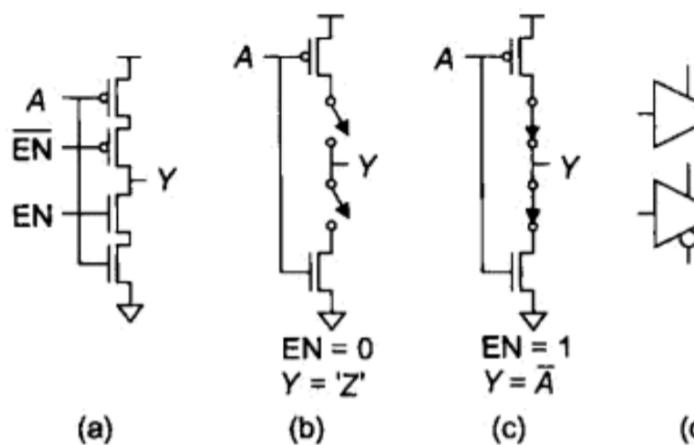
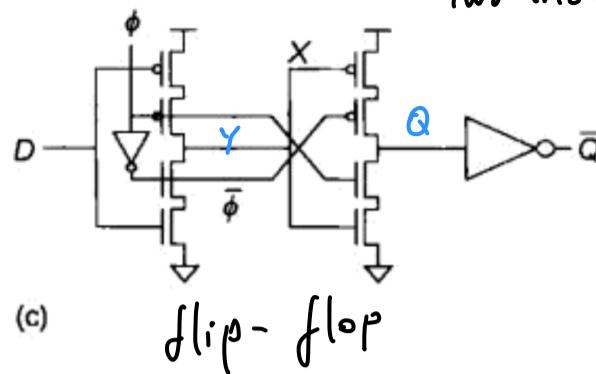


图 1.27 三态反相器

$\overline{EN}/\overline{\overline{EN}}$	A	Y
0 / 1	0	X
0 / 1	1	X
1 / 0	0	1
1 / 0	1	0

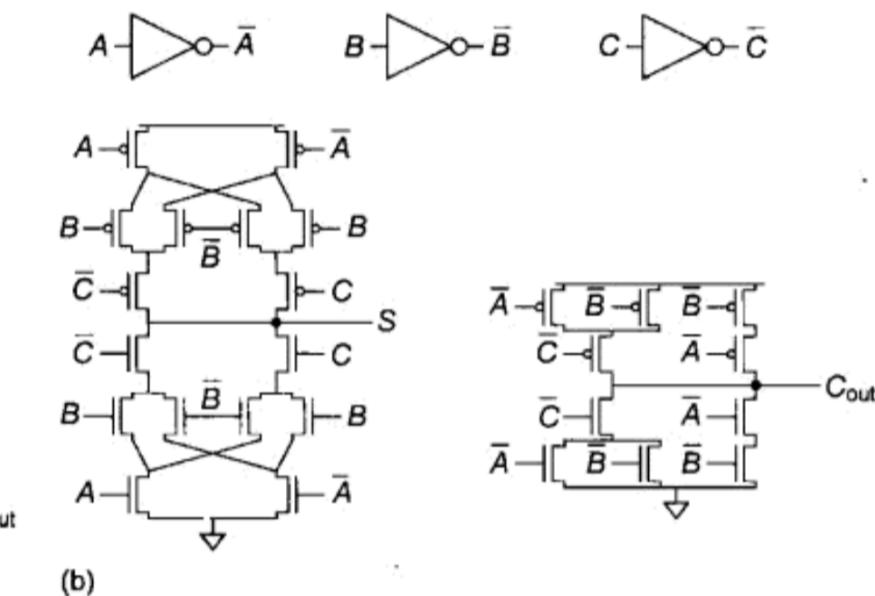


图 11.3 全加器设计 $S = A \oplus B \oplus C_{in}$

C_{in}	A	B	C_{out}	S	$C_{out} = AB + A C_{in} + B C_{in}$
0	0	0	0	0	
0	0	1	0	1	
0	1	0	0	1	
0	1	1	1	0	
1	0	0	0	1	
1	0	1	1	0	
1	1	0	1	0	
1	1	1	1	1	

Truth Table active-low reset signal

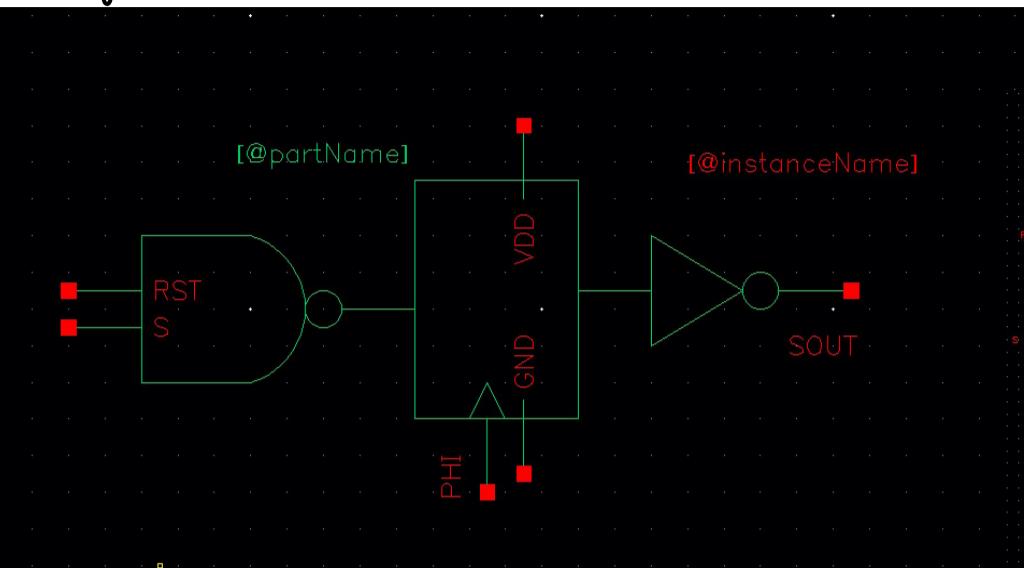
Step 1:

<u>CIN</u>	A	Q	\bar{Q}	COUT	S	RST	D
0	0	0	1	0	1	1	0
0	0	1	0	0	0	1	1
0	1	0	1	1	0	1	1
0	1	1	0	0	1	1	0
1	0	0	1	1	0	1	1
1	0	1	0	0	1	1	0
1	1	0	1	1	1	1	0
1	1	1	0	1	0	1	1
0	0	0	1	0	1	0	1
0	0	1	0	0	0	0	1
0	1	0	1	1	0	0	1
0	1	1	0	0	1	0	1
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	1	0	1	1	1	0	1
1	1	1	0	0	0	0	1

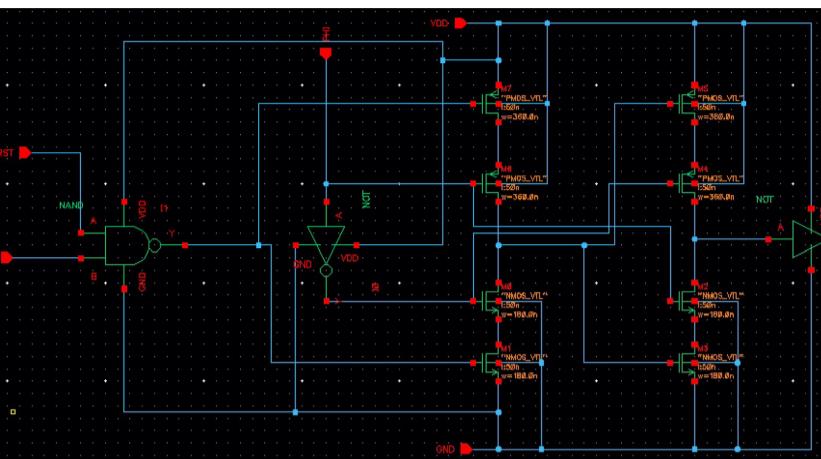
In order to convenient draw the truth table, I add two variables : \bar{Q} and S.

Step 2.

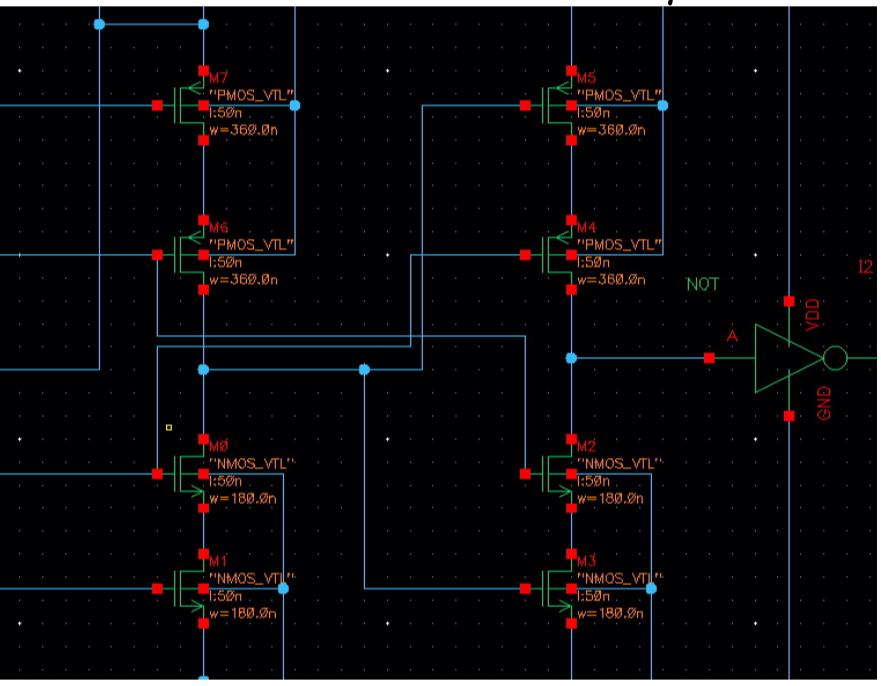
the symbol of flip-flop with reset signal :



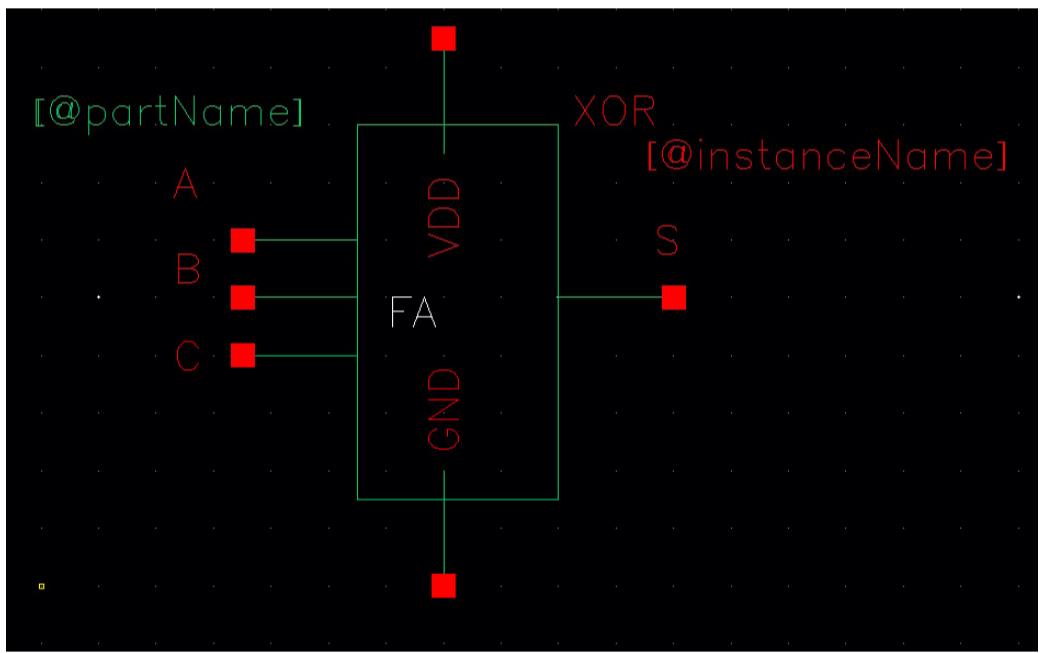
transistor-level schematics for flip-flop :



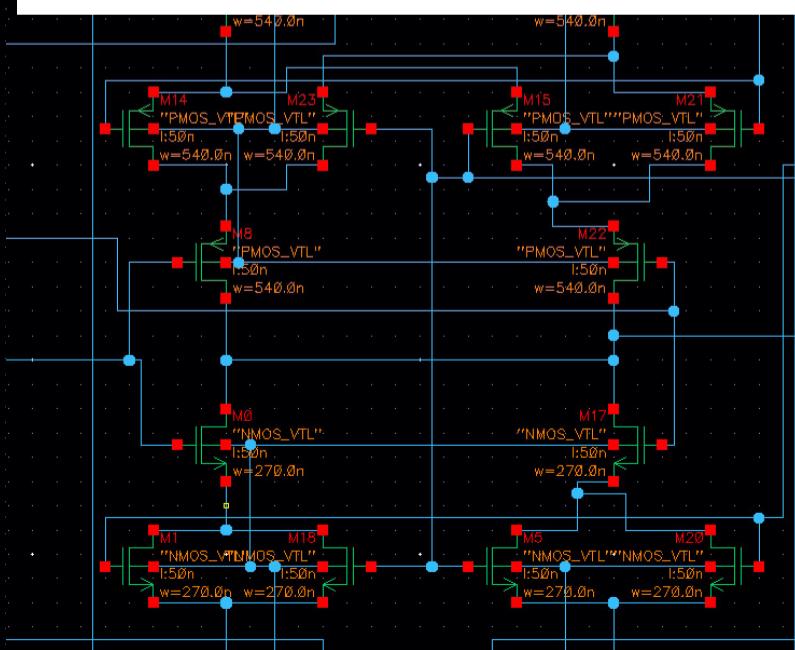
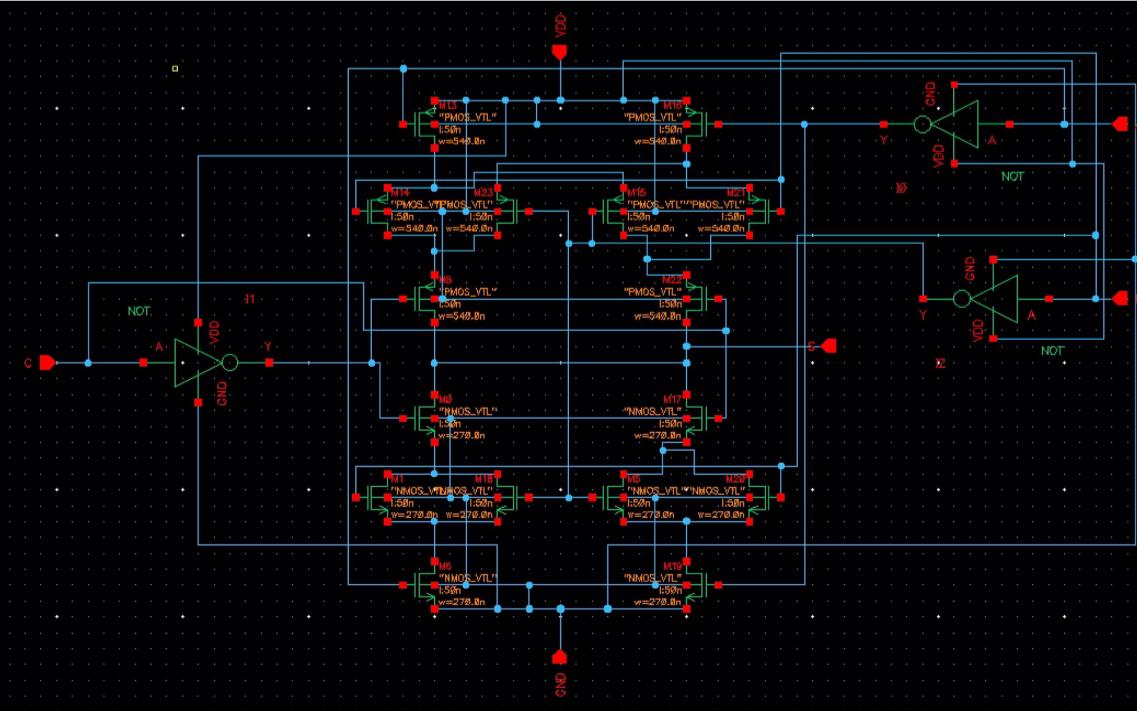
for flip-flop , the pmos width / nmos width
 $= 360 \text{ nm} / 180 \text{ nm}$



the symbol of full adder XOR part :

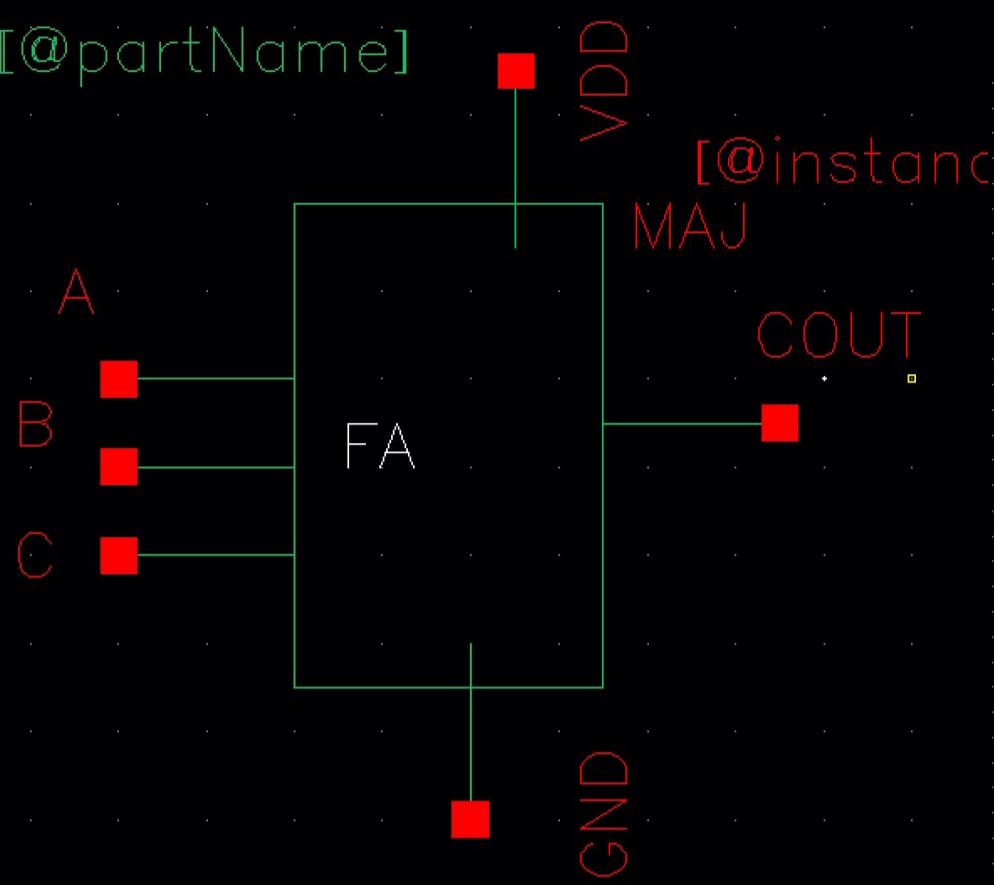


transistor-level schematics for full adder XOR part for full adder XOR part , pmos width / nmos width
 $= 540 \text{ nm} / 270 \text{ nm}$



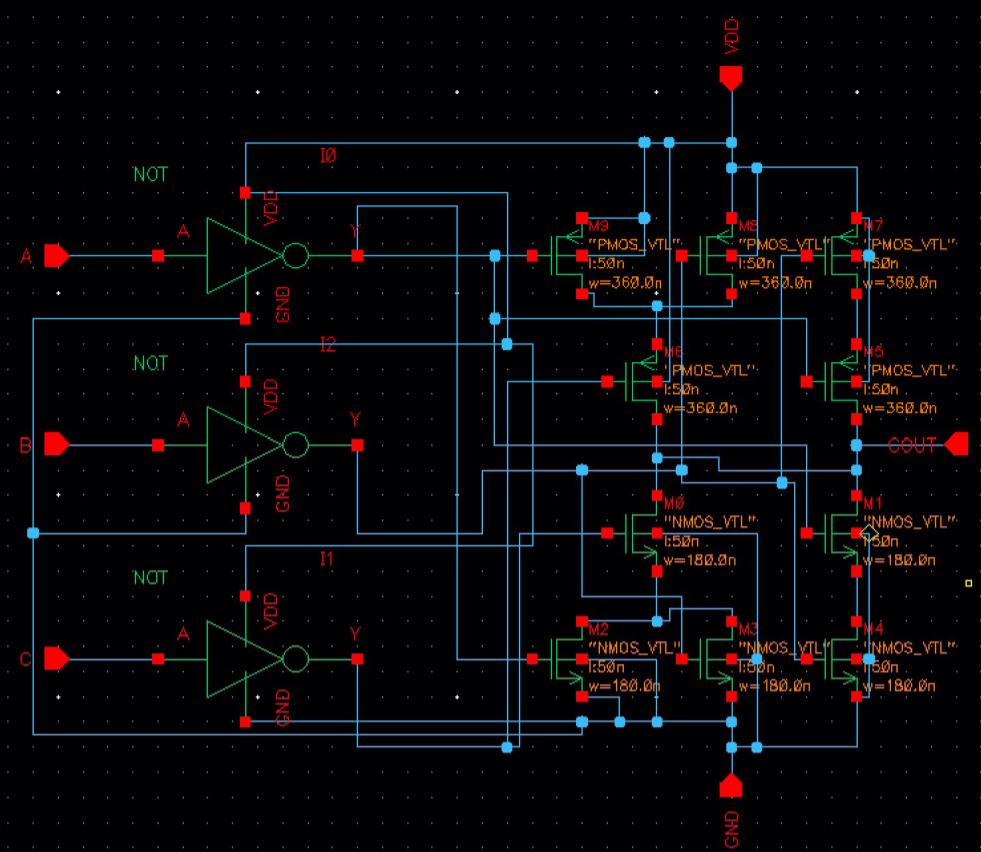
symbol of full adder MAJ part

[@partName]

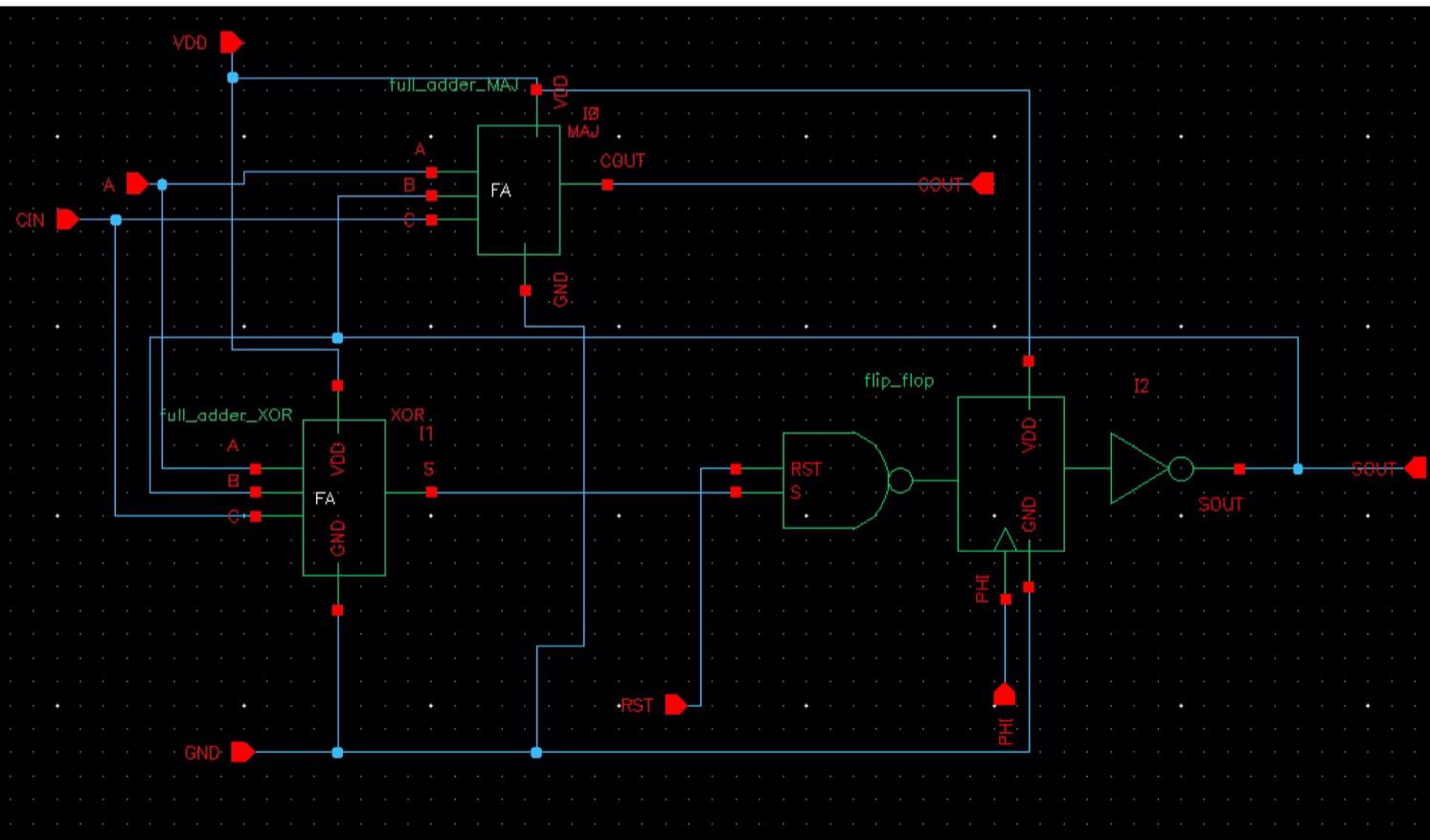


transistor-level schematics of full adder MAJ part

pMOS width / NMOS width = 360nm / 180nm



gate-level schematic for the entire accumulator:



Step 3

Each line of the table represents 1 clock cycle, $\sqrt{4}$ clock rising in every row.

RST	CIN	A	SOUT	COV7	S	D	Q	
0	0	0	0	0	0	1	1	$\frac{1}{2} \text{clock}$ present state = Output
0	0	1	0	0	1	1	1	$\frac{1}{2} \text{clock}$ Next State logic = Present
0	1	0	0	0	1	1	1	$\frac{1}{2} \text{clock}$ Stage + input
0	1	1	0	1	0	1	1	$\frac{1}{2} \text{clock}$ $S_{out} = \bar{Q}$
1	0	0	0	0	0	1	1	$S = CIN \oplus A \oplus \bar{Q}$
1	0	0	1	0	1	0	0	$\frac{1}{2} \text{clock}$ $D = \overline{S \cdot RST}$
1	0	1	0	0	1	0	1	$\frac{1}{2} \text{clock}$
1	0	1	1	1	0	1	0	$\frac{1}{2} \text{clock}$
1	0	1	0	0	1	0	1	$\frac{1}{2} \text{clock}$
.....								
repeat {								
1	1	1	0	1	0	1	1	$\frac{1}{2} \text{clock}$
1	1	1	1	1	1	0	0	$\frac{1}{2} \text{clock}$

if and only if variable CIN and A have different value (0,1 or 1,0), the present state (Q) and next state (D) will make a difference,

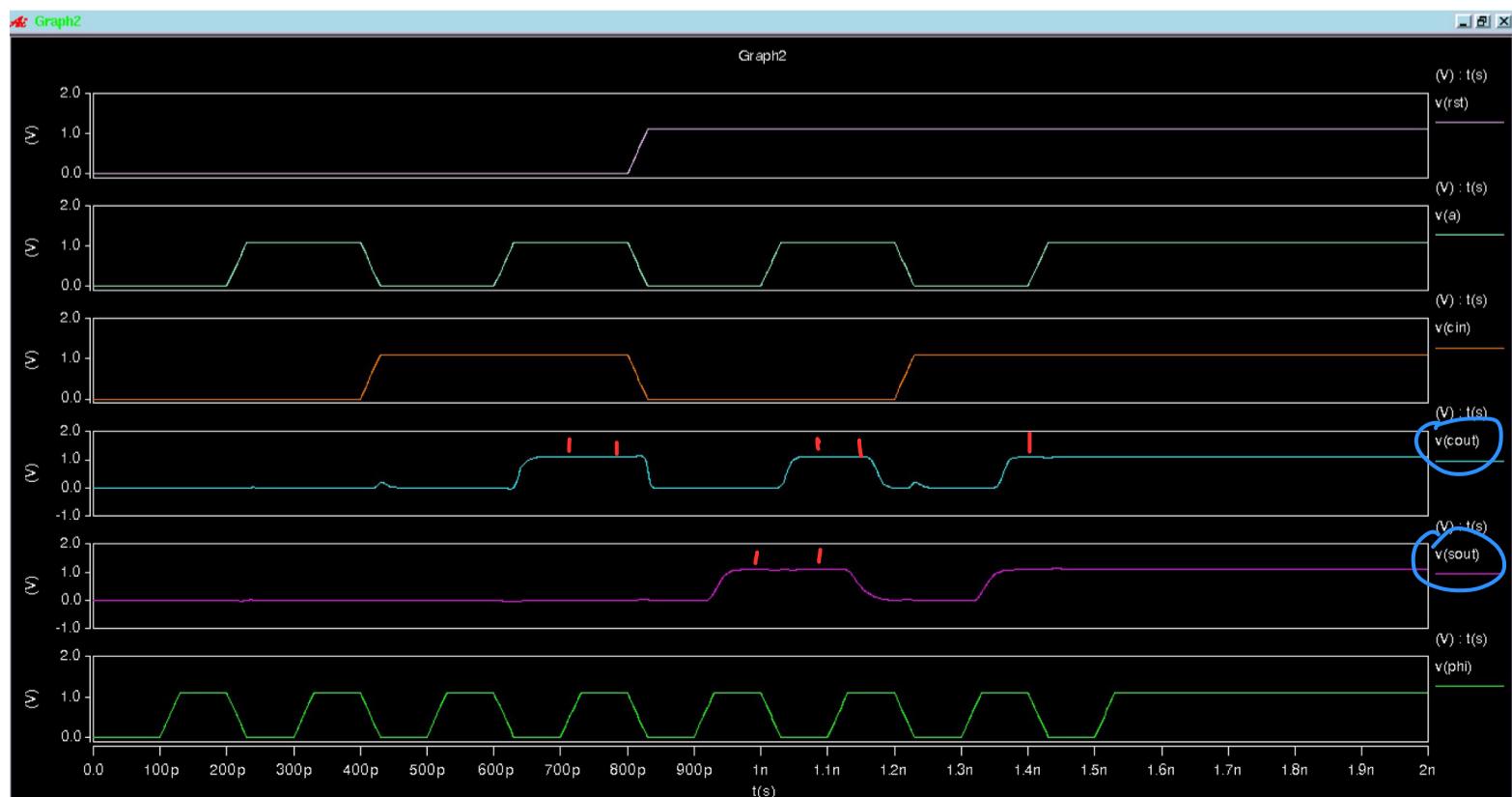
For waveform input :

	RST	CIN	A	SOUT	COUT	S	D	Q	\overrightarrow{Q}
0	0	0	0	0	0	0	()	clock
0	0	0	1	0	0	1	()	clock
0	1	0	0	0	0	1	1)	clock
0	1	1	0	0	1	0	1)	clock
1	0	0	0	0	0	0	1)	clock
1	0	0	1	0	0	1	0	1	clock
1	0	1	1	1	1	0	1	0	
1	1	0	1	1	0	1	1	0	clock
1	1	0	0	0	1	0	1	1	
1	1	1	1	0	1	0	1	1	clock
1	1	1	1	0	1	0	1	1	

Waveform for above truth table :

clock period is 200ps.

Sout just change when Cin and A are different value (0,1 or 1,0)

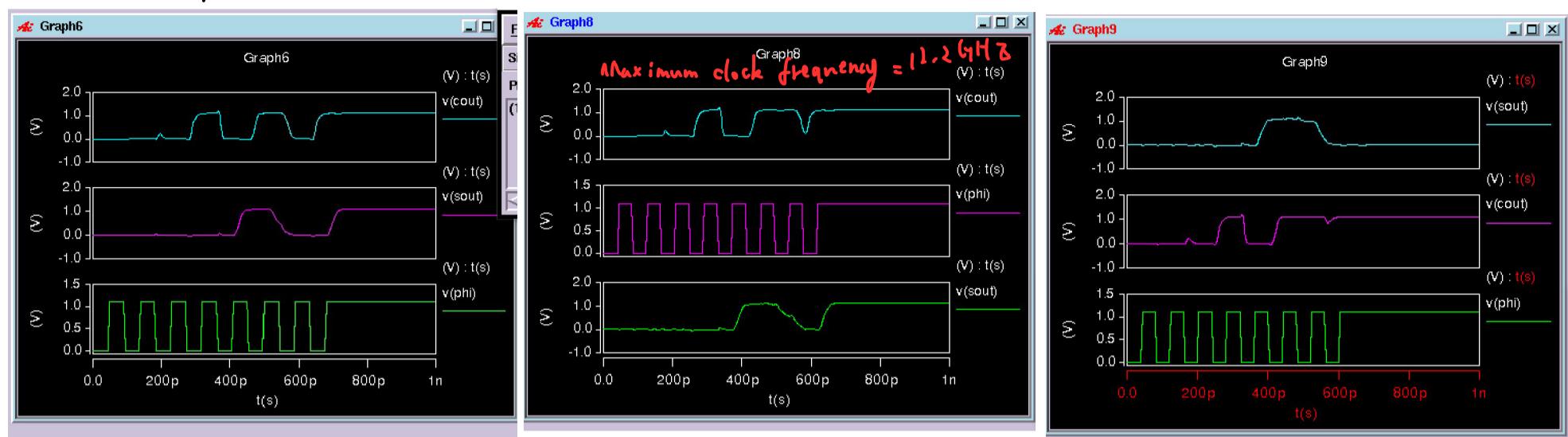


Step 4.

when period = 84 ps :

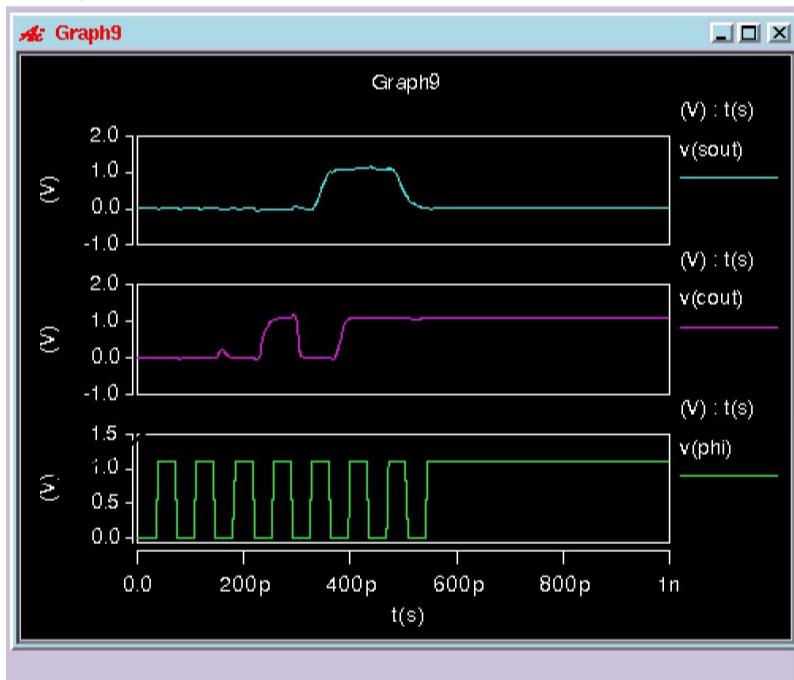
when period = 82 ps :

when period = 80 ps :



obviously, when period = 80 ps, the output becomes incorrect. so the minimum clock period is 82 ps, which means the maximum clock frequency = $\frac{1}{82 \text{ ps}} = 12.2 \text{ GHz}$

when period = 74 ps, the incorrect output;



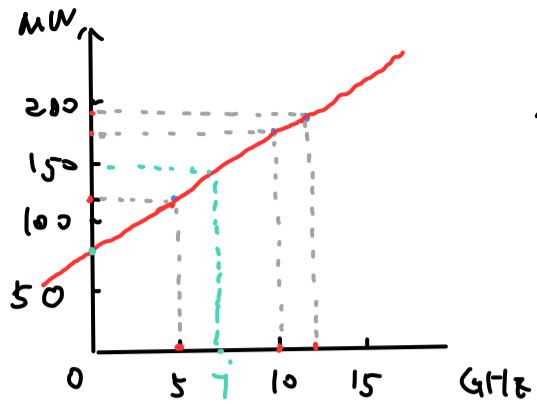
Step 5

Static power = leakage current × supply voltage

dynamic power = average power - static power

Frequency	Period	time period	average power	switching power
12.2 GHz	82 ps	656 ps	189.3 mW	0.0155 mW/MHz
10 GHz	100 ps	800 ps	176.9 mW	0.01764 mW/MHz
5 GHz	200 ps	1600 ps	120.7 mW	0.2414 mW/MHz

so the power from the three frequencies to be consistent if there are the same static power.



\therefore the static power is about 75 mW when frequency is 0 Hz.
 \therefore dynamic power = avg power - static power

Frequency	Period	time period	avg power	switching power	dynamic power	static power
Maximum frequency → 12.2 GHz	82 ps	656 ps	189.3 mW	0.0155 mW/MHz	114.3 mW	75 mW
10 GHz	100 ps	800 ps	176.4 mW	0.01764 mW/MHz	101.9 mW	75 mW
5 GHz	200 ps	1600 ps	120.7 mW	0.2414 mW/MHz	45.7 mW	75 mW

when static and dynamic power are equal, the avg power = 150 mW.
from the plot, we can estimate the clock frequency is about 7 GHz.

Step 6:

the RVE Rtot

min width of poly 0.05 : poly 没对齐.

min spacing of gate poly 0.1μ : 相邻 poly gate 离小 0.1μ 距离.

minimum width of metal 0.065 : metal 1 没对齐

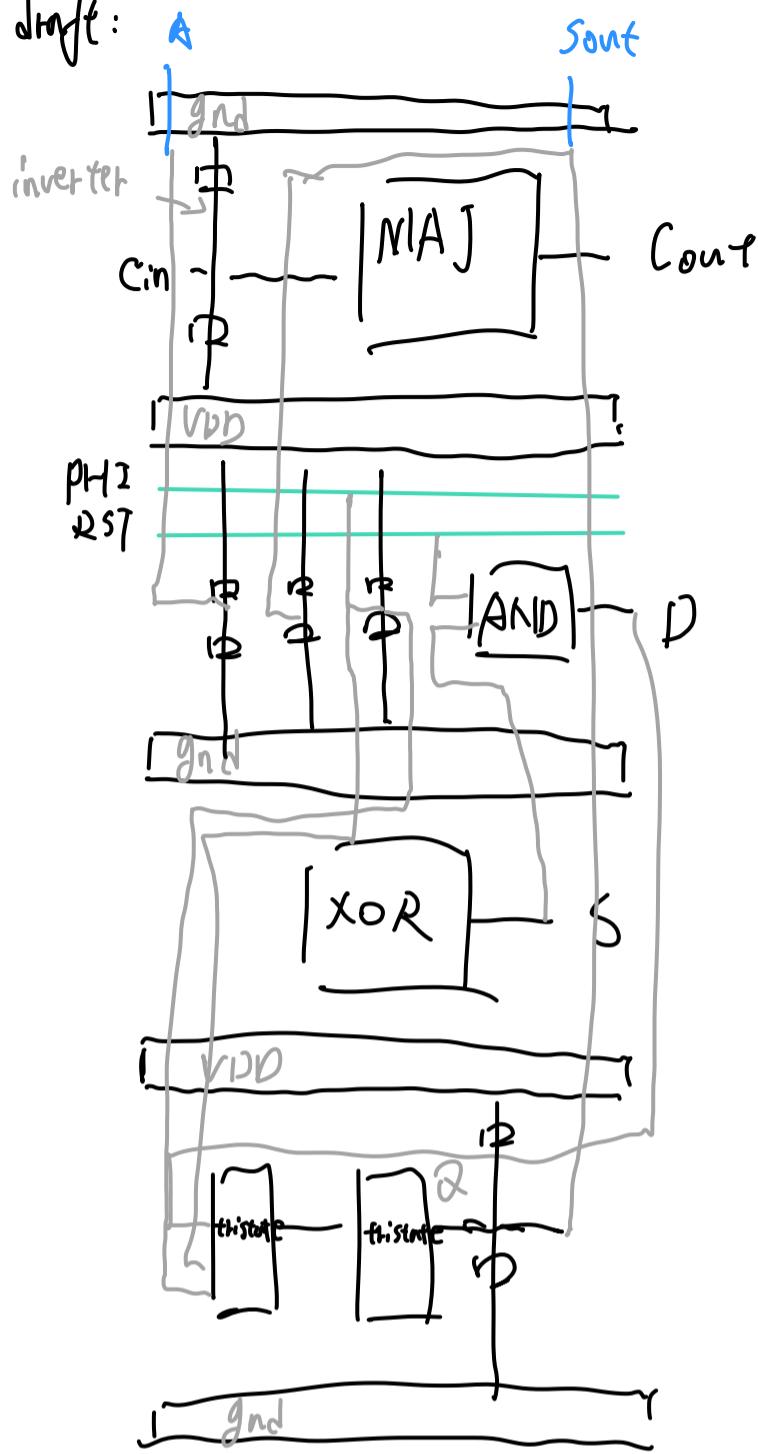
minimum spacing of metal 1 = 0.065 : 相邻 m1 金属 离小 0.065 距离

minimum width of metal 2 = 0.07 : metal 2 没对齐

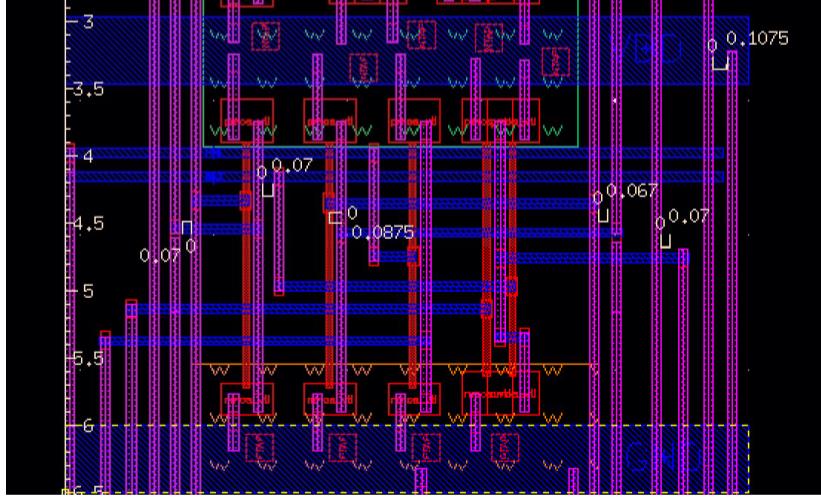
minimum spacing of metal 2 = 0.07 : 相邻 m2 金属 离小 0.07 距离

I just span multiple row vertically, so there are 3 gnd and 2 vdd rail vertical in my layout and total 4 cells. Every cell I just put some device and fit the layout well.

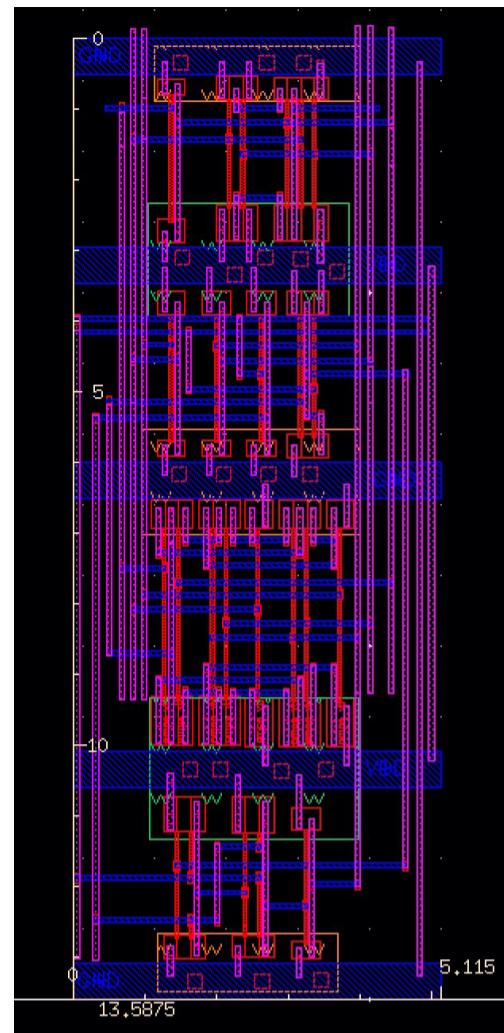
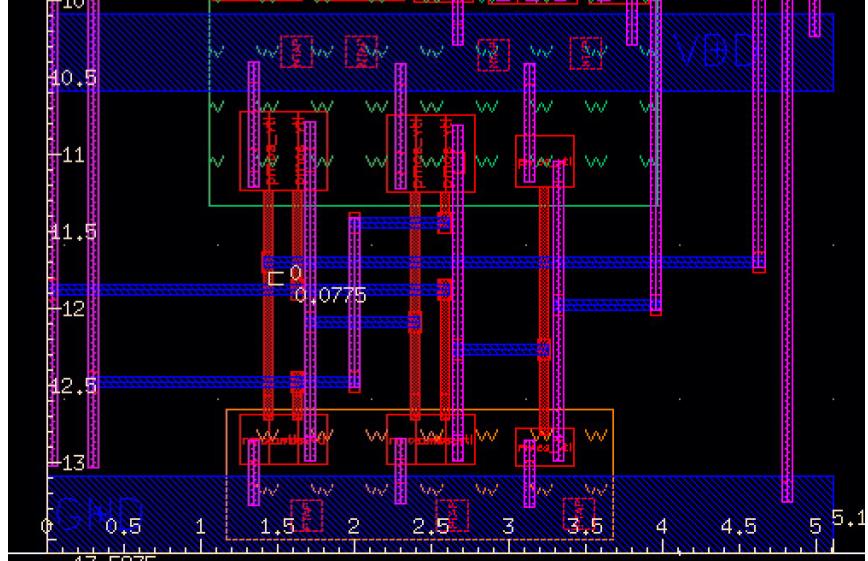
Simple draft:



Second cell: three inverters and one AND gate

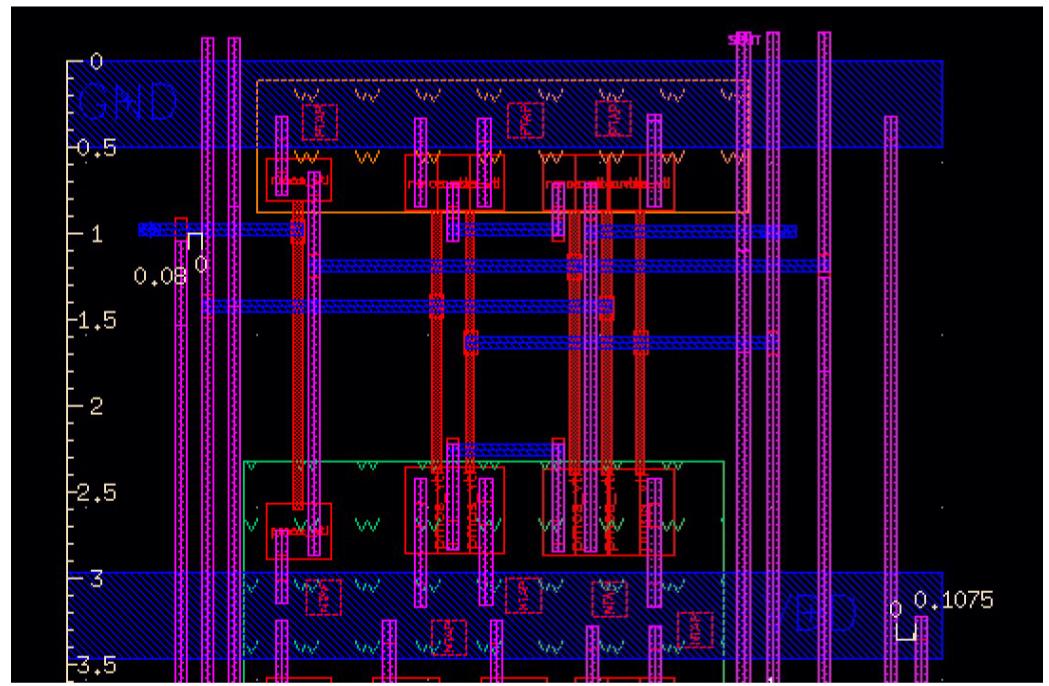


Last cell: flip-flop and inverter

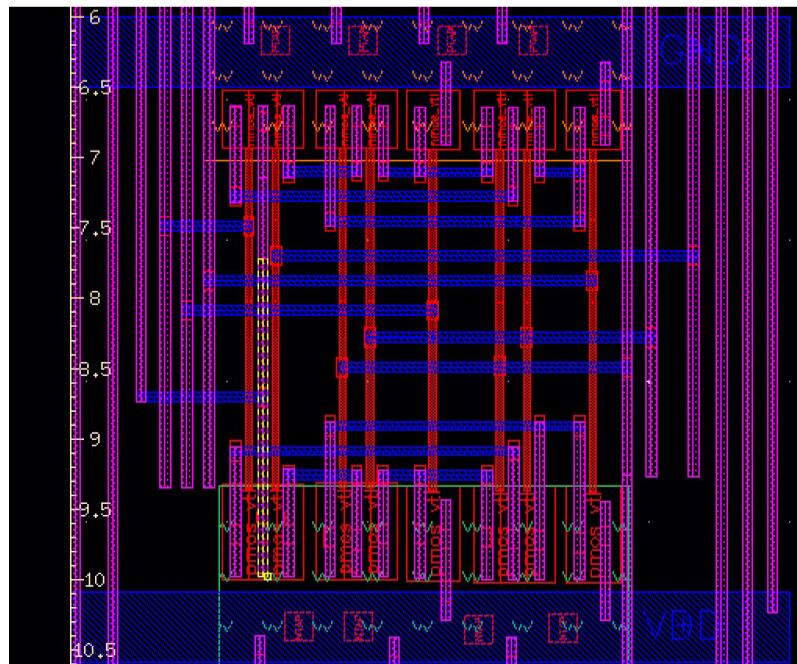


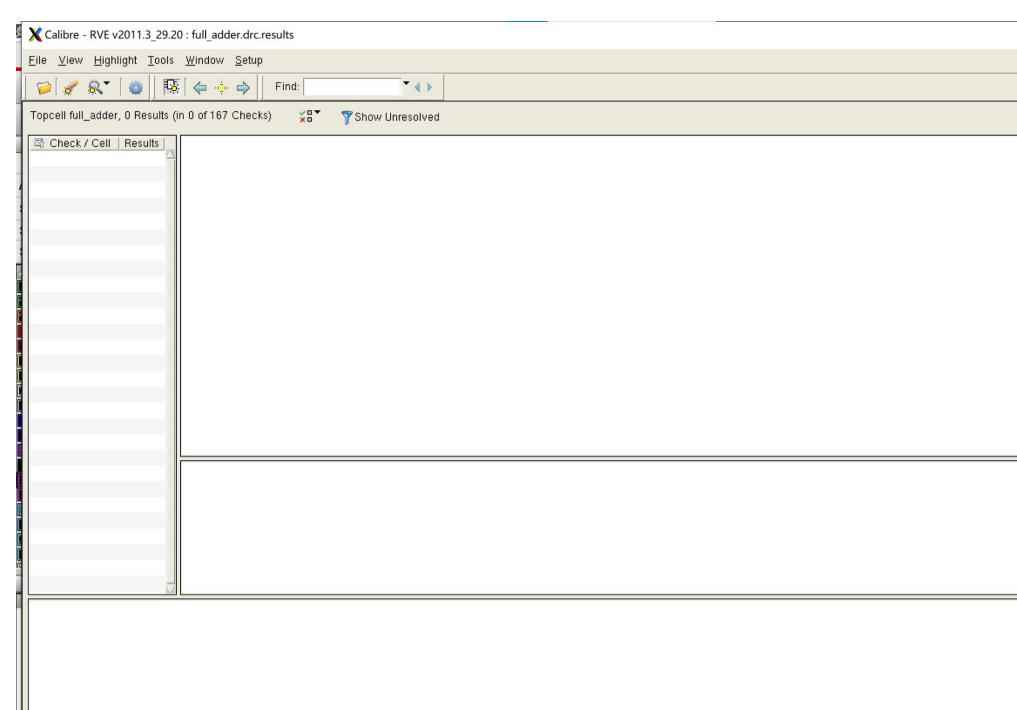
height : 13.5875 μm
width : 5.115 μm

first cell: one inverter and full-adder-MAJ.



third cell: full-adder-XOR





LVS Report File - full_adder.lvs.report

```

Set File Edit Options Windows
TRACE PROPERTY mn(nmos_thkox) 1 1 4e-09 ABSOLUTE
TRACE PROPERTY mn(nmos_thkox) w w 4e-09 ABSOLUTE
TRACE PROPERTY mp(pmos_thkox) 1 1 4e-09 ABSOLUTE
TRACE PROPERTY mp(pmos_thkox) w w 4e-09 ABSOLUTE

CELL COMPARISON RESULTS < TOP LEVEL >

# # #####
# # # INCORRECT #
# # #####
Error: Different numbers of nets (see below).
Error: Different numbers of instances (see below).
Error: Connectivity errors.

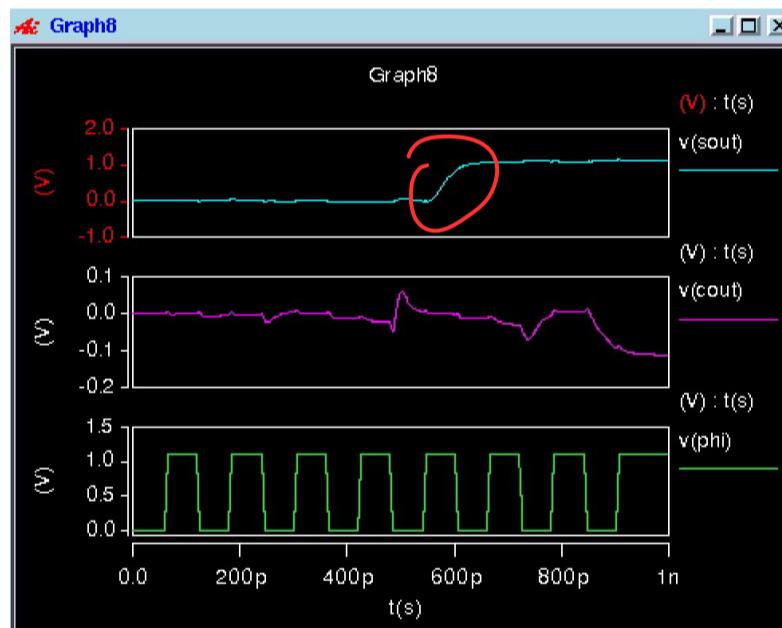
LAYOUT CELL NAME: full_adder
SOURCE CELL NAME: full_adder

INITIAL NUMBERS OF OBJECTS

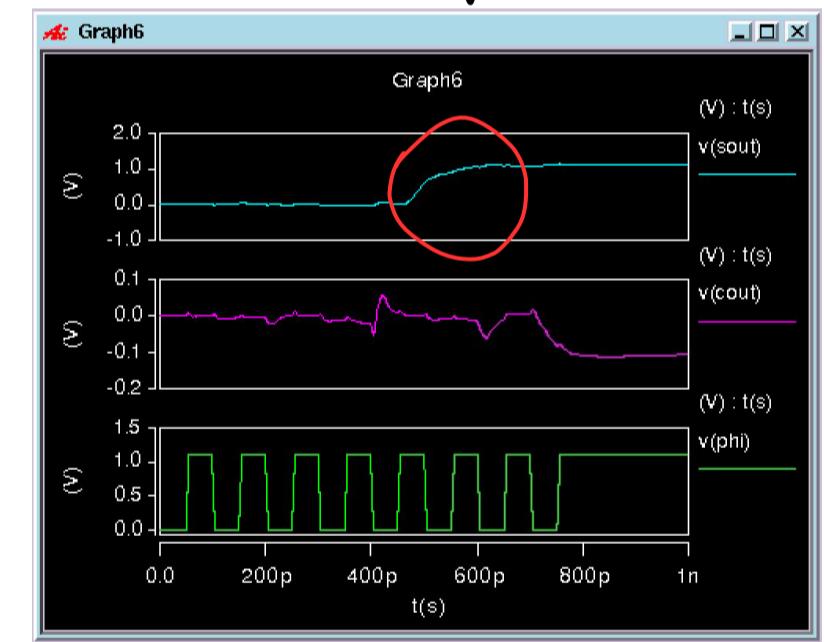
```

the maximum frequency I test from netlist with parasitic information is 10 GHz, which means around 100 ps. When adding parasitic information, the maximum obviously decrease

100 ns :



90 ns (10% higher frequency):



Step 7a:

$$C_{\text{load}} = 20 + 9 + 6 = 35 \text{ fF}$$

parasitic inverter delay: $\tau = 3RC$

$$\text{propagation delay}_{\text{no driver}} = (1 \times \frac{35 \text{ fF}}{3C} + 1) \tau$$

$$= (1 \times \frac{35}{0.54} + 1) \tau \approx 66 \tau$$

$$90 \text{ nm} = 0.09 \mu\text{m}$$

$$C_y = C_{\text{permicron}} \cdot W \quad C = 2fT / \mu\text{m} \times 0.09 \mu\text{m}$$

$$C_{\text{permicron}} = 2 \text{ fF}/\mu\text{m} = 0.18 \text{ fF}$$

$$\therefore 3C = 0.54 \text{ fF}$$

$$G = 1 \times 1 \times 1 = 1$$

$$B = 1 \quad 35fF$$

$$H = 65 = \frac{35}{0.548} fF$$

$$F = GBH = 65$$

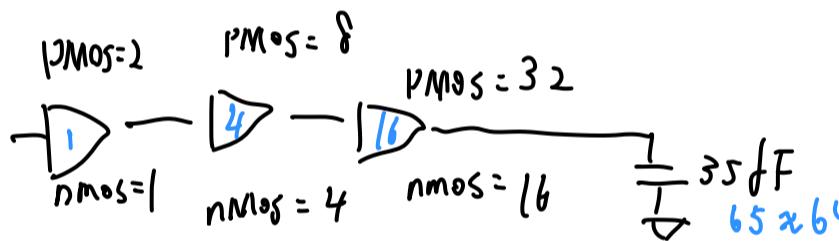
$$\hat{f} = \sqrt[3]{65} \approx 4$$

$$P = 1 + 1 + 1 = 3$$

$$\text{optimal total delay } D = 4 \times 3 + 3 = 15\tau$$

$$C_2 = \frac{65 \times 1}{4} \approx 16 \quad \because \text{ratio PMOS:nMOS} = 2:1 \\ \therefore \text{PMOS width} = 32 \quad \text{nMOS width} = 16$$

$$C_1 = \frac{6 \times 1}{4} \approx 4 \quad \because \text{ratio PMOS:nMOS} = 2:1 \\ \therefore \text{PMOS width} = 8 \quad \text{nMOS width} = 4$$



every stage take up the same effort
and get the minimum delay.

$$d_1 = g_1 h_1 + p_1 = \frac{1}{4} \times 1 \times 1 + 1 = 5\tau$$

$$d_2 = g_2 h_2 + p_2 = \frac{64}{16} \times 1 \times 1 + 1 = 5\tau$$

Step 7b:

```
lab2_inverter.mt0 - 记事本
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)
$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'
.TITLE '** generated for: hspiced'
tpdr temper alter#
1.208e-12 2.500e+01 1
```

```
lido2_inverter_load.mtw - 10 事半
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)
$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'
.TITLE '** generated for: hspiced'
tpd t1 t2 t3
temper alter#
3.693e-11 1.194e-11 1.095e-11 1.339e-11
2.500e+01 1
```

actual $t = 1.2 \mu s$

for circuit with driver and capacitance ; $t_{pd} = 37 \mu s$ $t_1 = 12 \mu s$ $t_2 = 11 \mu s$ $t_3 = 13 \mu s$
 $1.2 \times 15 = 18 \mu s \neq 37 \mu s$, obviously my assumption of Cpernicron don't fit the fact.

almost equal
 $37 \approx 12 + 11 + 13$

by inverse calculation:

$$\left\{ \begin{array}{l} f = \frac{37 \text{ ps}}{1.2 \text{ ps}} - 3 \rangle / 3 \\ F = (f)^3 = \frac{350 \text{ fF}}{3 \text{ C}} \end{array} \right. \Rightarrow C_{\text{permition}} = 0.16 \text{ fF/mm}$$

$$C = C_{\text{permition}} \times 0.09 \text{ mm}$$

If $C_{\text{permition}} = 0.16 \text{ fF/mm}$, then agree with my analysis from step 7a.

Step 7C :

As a assumption, 1st stage size decrease and 2nd stage size increase in every combination. So $\left\{ \begin{array}{l} 0.18 \times 16 \\ 0.09 \times 16 \end{array} \right. \downarrow$ and $\left\{ \begin{array}{l} 0.19 \times 4 \\ 0.09 \times 4 \end{array} \right. \uparrow$.

```
m0 net10 a vdd vdd PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9 PS=390e-9 M=1
m5 y net12 gnd gnd NMOS_VTL L=50e-9 W=1.44e-6 AD=151.2e-15 AS=151.2e-15 PD=1.65e-6 PS=1.65e-6 M=1
m4 net12 net10 gnd gnd NMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15 PD=570e-9 PS=570e-9 M=1
m3 net10 a gnd gnd NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9 PS=300e-9 M=1
c0 y gnd 35e-15
.tran 1p 1n
.MEASURE TRAN tpd TRIG=v(a) VAL='1.1/2' fall=1 TARG=v(y) VAL='1.1/2' RISE = 1
.alter
m2 y net12 vdd vdd PMOS_VTL L=50e-9 W=2.70e-6 AD=302.4e-15 AS=302.4e-15 PD=3.09e-6 PS=3.09e-6 M=1
m5 y net12 gnd gnd NMOS_VTL L=50e-9 W=1.35e-6 AD=151.2e-15 AS=151.2e-15 PD=1.65e-6 PS=1.65e-6 M=1
m1 net12 net10 vdd vdd PMOS_VTL L=50e-9 W=900e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9 PS=930e-9 M=1
m4 net12 net10 gnd gnd NMOS_VTL L=50e-9 W=450e-9 AD=37.8e-15 AS=37.8e-15 PD=570e-9 PS=570e-9 M=1
.alter
m2 y net12 vdd vdd PMOS_VTL L=50e-9 W=2.52e-6 AD=302.4e-15 AS=302.4e-15 PD=3.09e-6 PS=3.09e-6 M=1
m5 y net12 gnd gnd NMOS_VTL L=50e-9 W=1.26e-6 AD=151.2e-15 AS=151.2e-15 PD=1.65e-6 PS=1.65e-6 M=1
m1 net12 net10 vdd vdd PMOS_VTL L=50e-9 W=1080e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9 PS=930e-9 M=1
m4 net12 net10 gnd gnd NMOS_VTL L=50e-9 W=540e-9 AD=37.8e-15 AS=37.8e-15 PD=570e-9 PS=570e-9 M=1
.alter
m2 y net12 vdd vdd PMOS_VTL L=50e-9 W=2.36e-6 AD=302.4e-15 AS=302.4e-15 PD=3.09e-6 PS=3.09e-6 M=1
m5 y net12 gnd gnd NMOS_VTL L=50e-9 W=1.17e-6 AD=151.2e-15 AS=151.2e-15 PD=1.65e-6 PS=1.65e-6 M=1
m1 net12 net10 vdd vdd PMOS_VTL L=50e-9 W=1260e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9 PS=930e-9 M=1
m4 net12 net10 gnd gnd NMOS_VTL L=50e-9 W=630e-9 AD=37.8e-15 AS=37.8e-15 PD=570e-9 PS=570e-9 M=1
.alter
m2 y net12 vdd vdd PMOS_VTL L=50e-9 W=2.18e-6 AD=302.4e-15 AS=302.4e-15 PD=3.09e-6 PS=3.09e-6 M=1
m5 y net12 gnd gnd NMOS_VTL L=50e-9 W=1.08e-6 AD=151.2e-15 AS=151.2e-15 PD=1.65e-6 PS=1.65e-6 M=1
m1 net12 net10 vdd vdd PMOS_VTL L=50e-9 W=1440e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9 PS=930e-9 M=1
m4 net12 net10 gnd gnd NMOS_VTL L=50e-9 W=720e-9 AD=37.8e-15 AS=37.8e-15 PD=570e-9 PS=570e-9 M=1
.alter
m2 y net12 vdd vdd PMOS_VTL L=50e-9 W=2.00e-6 AD=302.4e-15 AS=302.4e-15 PD=3.09e-6 PS=3.09e-6 M=1
m5 y net12 gnd gnd NMOS_VTL L=50e-9 W=0.99e-9 AD=151.2e-15 AS=151.2e-15 PD=1.65e-6 PS=1.65e-6 M=1
m1 net12 net10 vdd vdd PMOS_VTL L=50e-9 W=1620e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9 PS=930e-9 M=1
m4 net12 net10 gnd gnd NMOS_VTL L=50e-9 W=810e-9 AD=37.8e-15 AS=37.8e-15 PD=570e-9 PS=570e-9 M=1
.alter
m2 y net12 vdd vdd PMOS_VTL L=50e-9 W=1.82e-6 AD=302.4e-15 AS=302.4e-15 PD=3.09e-6 PS=3.09e-6 M=1
m5 y net12 gnd gnd NMOS_VTL L=50e-9 W=0.90e-6 AD=151.2e-15 AS=151.2e-15 PD=1.65e-6 PS=1.65e-6 M=1
m1 net12 net10 vdd vdd PMOS_VTL L=50e-9 W=1800e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9 PS=930e-9 M=1
m4 net12 net10 gnd gnd NMOS_VTL L=50e-9 W=900e-9 AD=37.8e-15 AS=37.8e-15 PD=570e-9 PS=570e-9 M=1
```

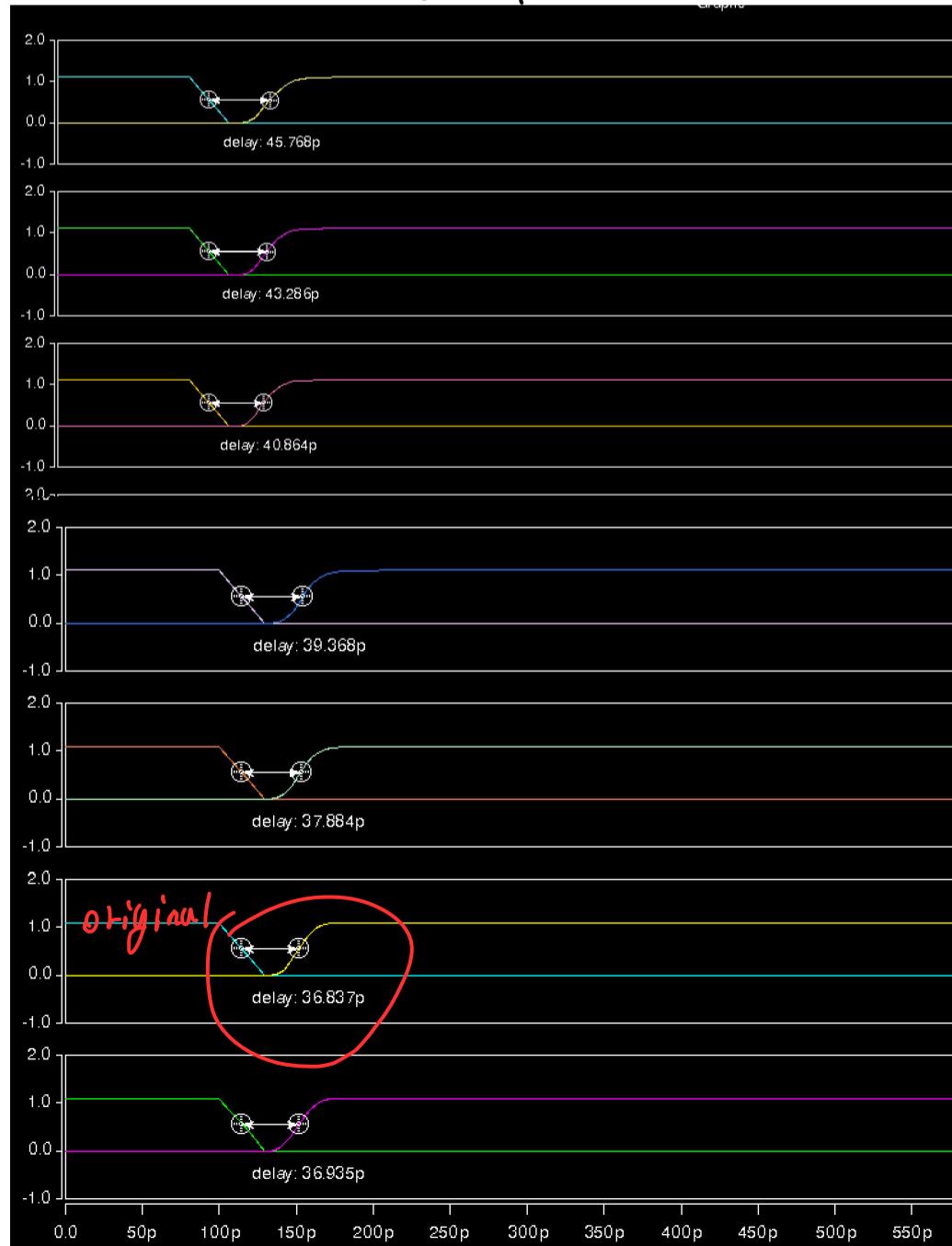
obviously, the original stage size has the minimum delay because $\frac{\text{Stage size } i}{\text{Stage size } i-1} > \frac{\text{Stage size } i-1}{\text{Stage size } i-2}$

$$\frac{4}{1} = \frac{16}{4}$$

$$= \frac{\text{Stage size } i-1}{\text{Stage Size } i-2}$$

which make the same effort (gh).

so any change will increase the delay



Step 7d:

$$\text{assump} \quad C_{\text{permiction}} = 2 \text{ fF}/\mu\text{m}$$

for two-stage driver: $-D-D-D-\overbrace{D}^{\frac{1}{2}T}$ optimal delay: 15τ
 $\therefore 35 \text{ fF}$

for four-stage driver: $-D-D-D-D-D-\overbrace{D}^{\frac{1}{4}T} a$

$$a = \frac{C}{0.54 \text{ fF}} \quad F = GBT = 1 \times 1 \times a \quad \therefore 3C = 3 \times 2 \text{ fF}/\mu\text{m} \times 0.09 \mu\text{m} \\ = 0.54 \text{ fF}$$

$$\hat{f} = \sqrt[5]{a}$$

$$P = \sqrt[5]{a} + N = \sqrt[5]{a} + 5 < \sqrt[3]{a} + 3$$

$$\rho = 3.59 \quad \hat{N} = \log_e F = \log_{3.59} a = \log_{3.59} \frac{C}{0.54 \text{ fF}} = 5$$

$$C \approx 322 \text{ fF} \quad a \approx 596$$

,; when $C = 322 \text{ fF}$, the four-stage driver has the optimal delay, which is 22.95τ .

$$\text{Size}_4 = 3.59^4 = 166 \quad \text{Size}_3 = 3.59^3 = 46 \quad \text{Size}_2 = 3.59^2 \approx 13$$

$$\text{Size}_1 = 3.95 \quad \therefore D = \sqrt[5]{596} + 5 = 22.95 \tau$$

$$-D-\overbrace{D}^{3.59}-\overbrace{D}^{13}-\overbrace{D}^{46}-\overbrace{D}^{166}-\overbrace{D}^{\frac{1}{4}T} \approx 596$$