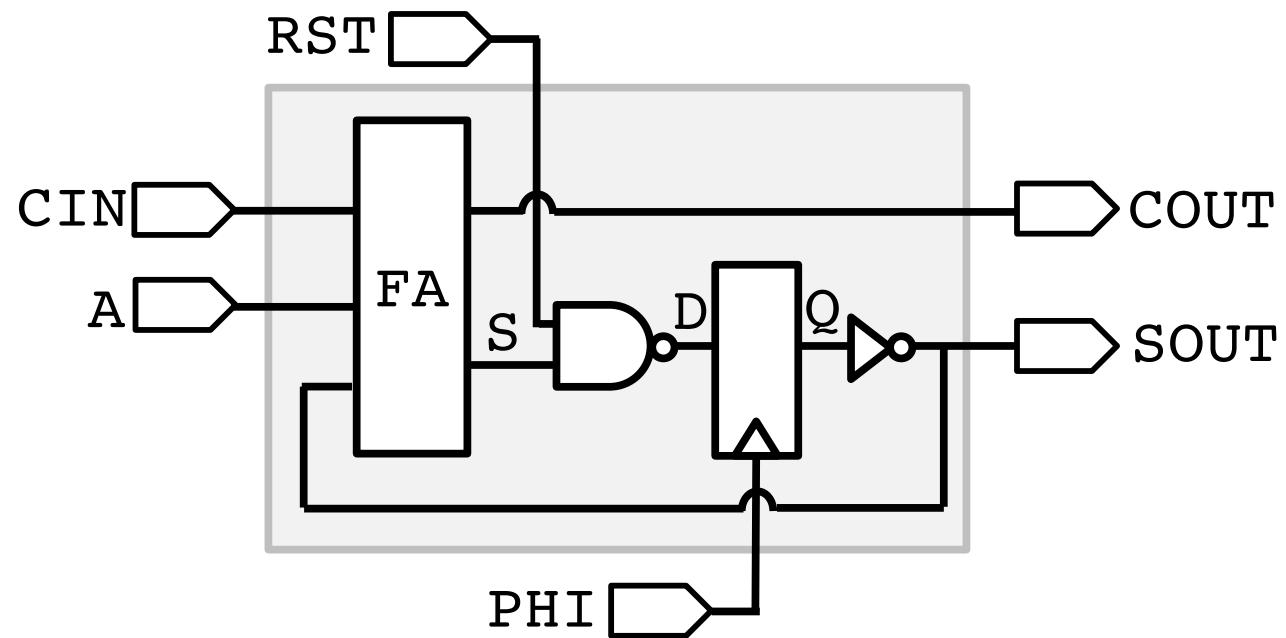
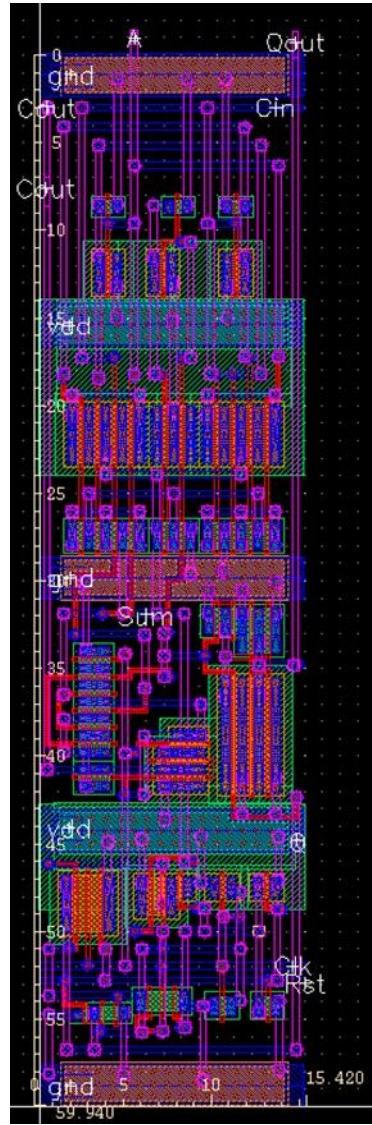


**Intro to Lab 2:
accumulator bitslice
covered in 10/12/2020 lecture**

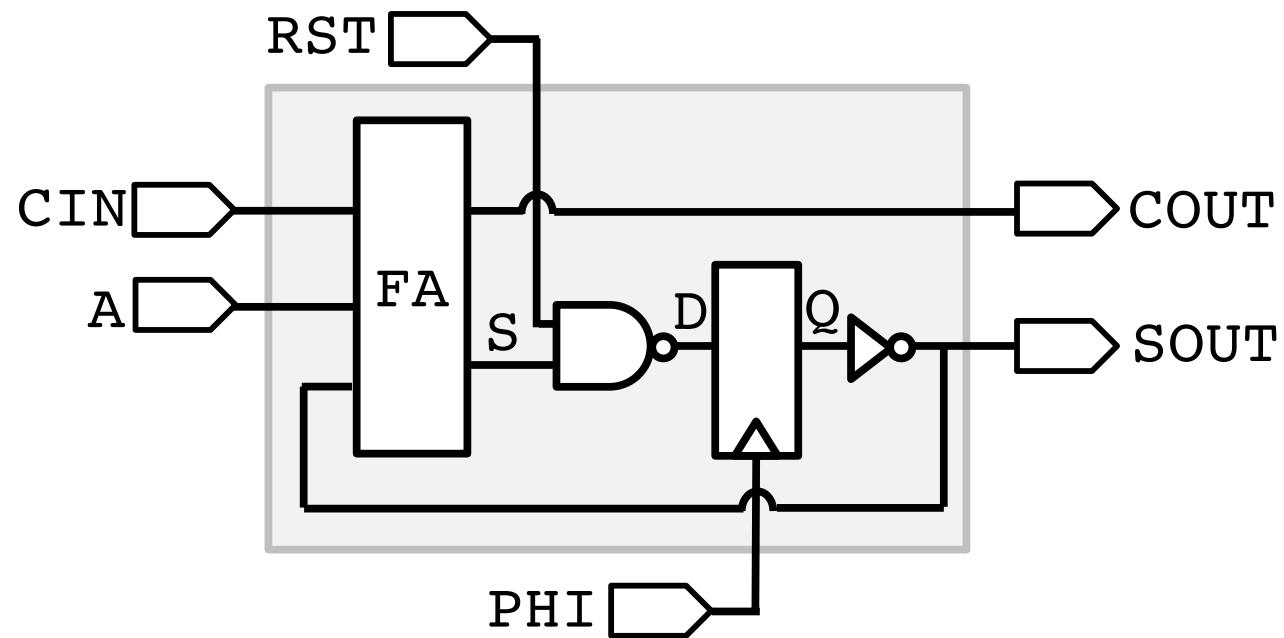
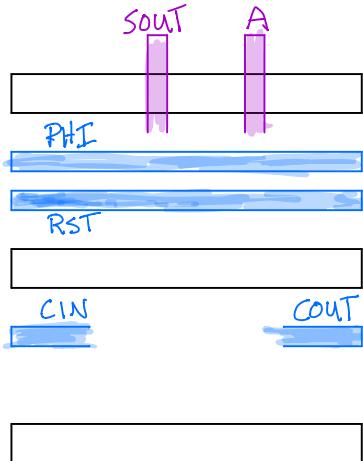
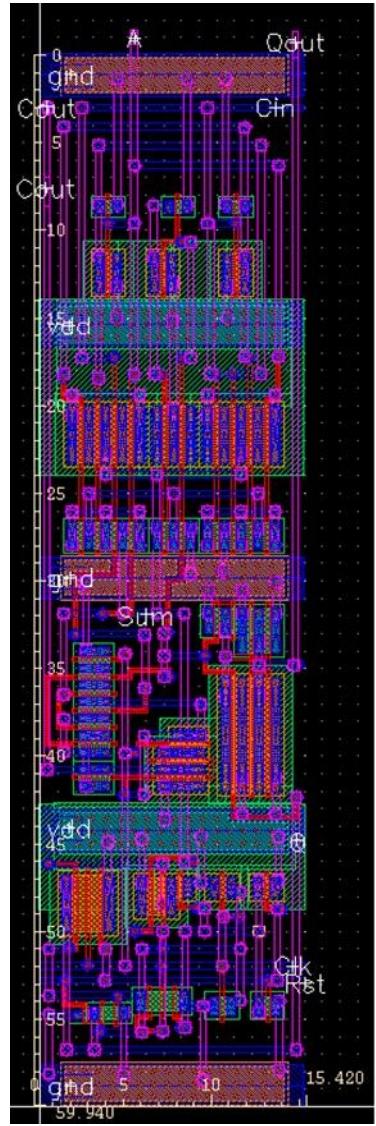
General Lab Feedback

- ❑ Plot annotations must be readable
- ❑ Submit as pdf with name and ECE558/658 at top
- ❑ Read instructions carefully
- ❑ Check spelling
- ❑ Inputs:
 - ❑ Voltage of logic 1 should match supply
 - ❑ Rise and fall times are 20% to 80%
 - ❑ Transitions should start from 0 or supply
- ❑ Get in habit of trying to judge whether numbers are reasonable. Unreasonable numbers may reveal bugs

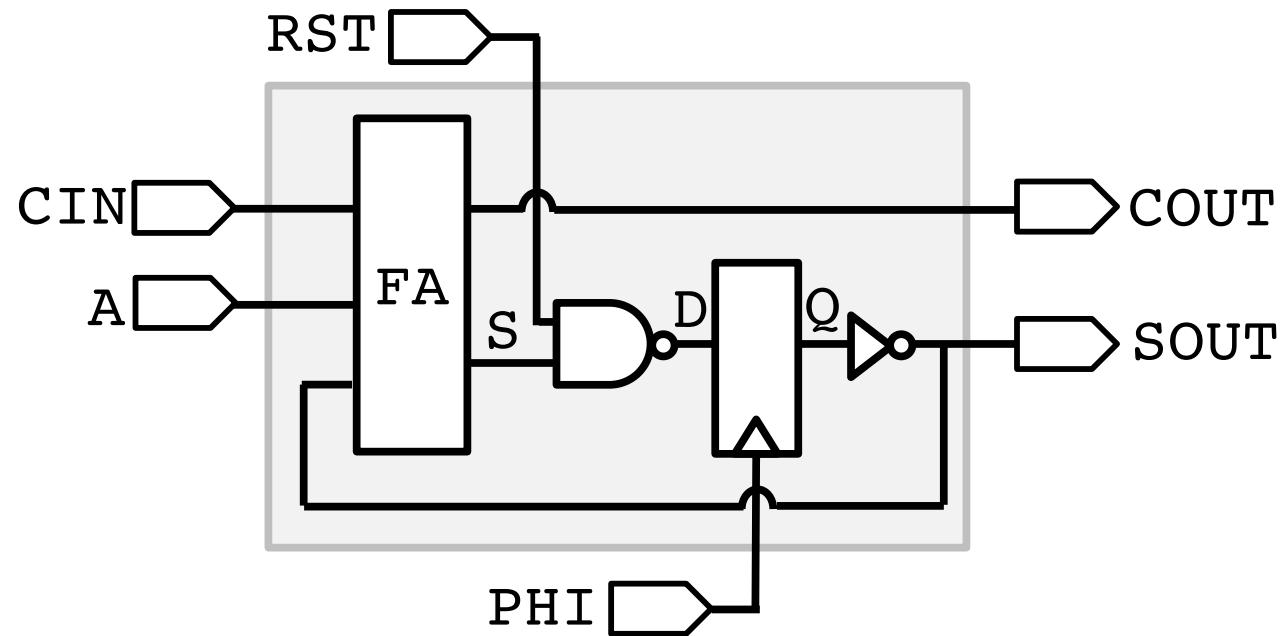
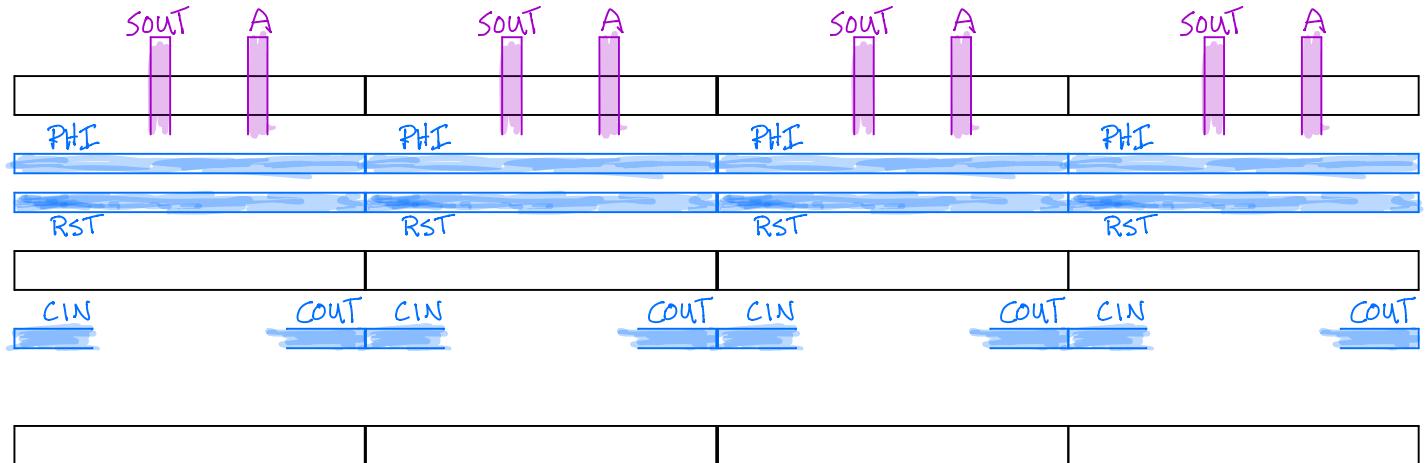
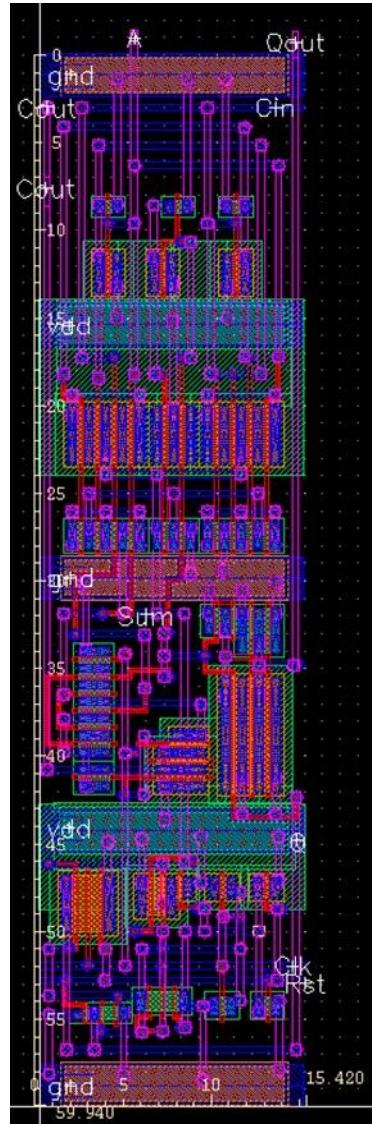
Bitsliced Design and Layout



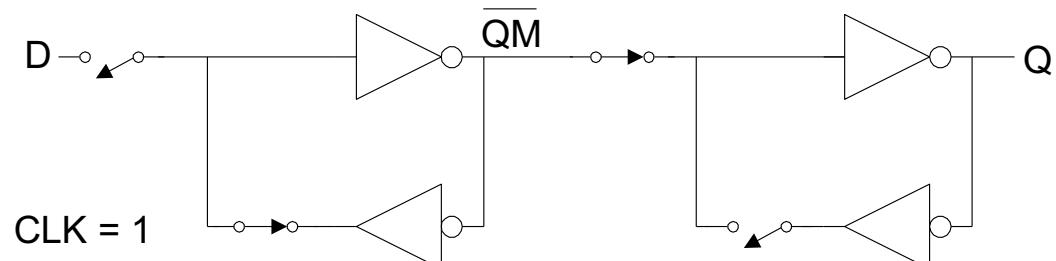
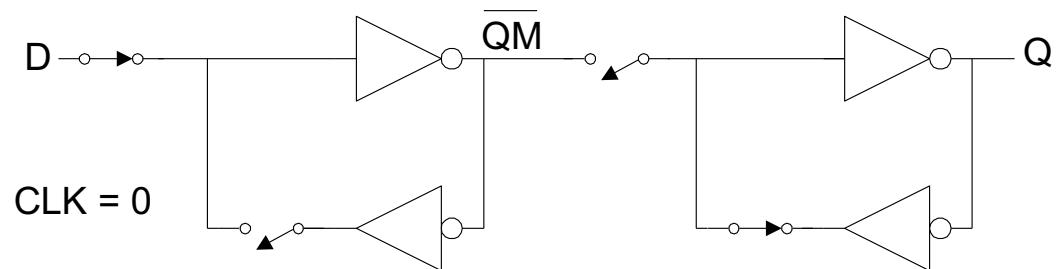
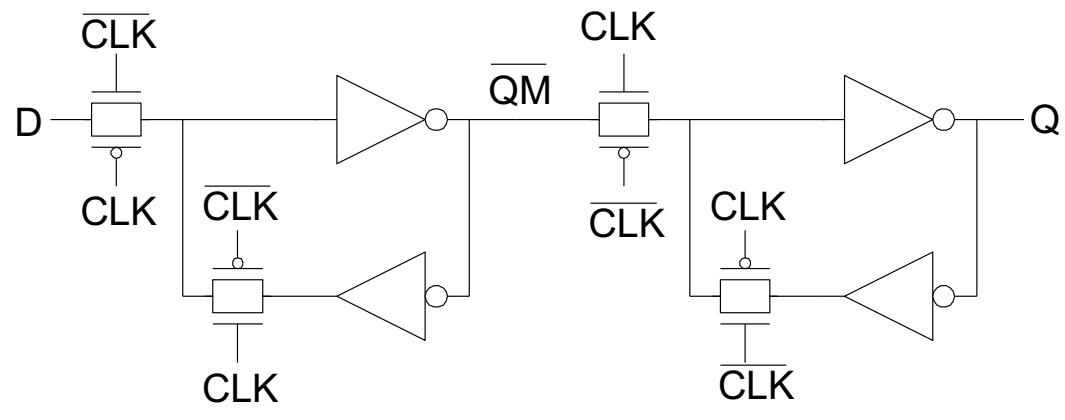
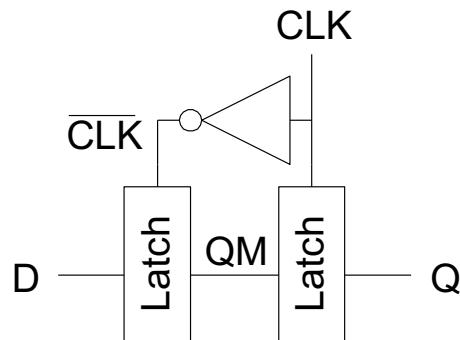
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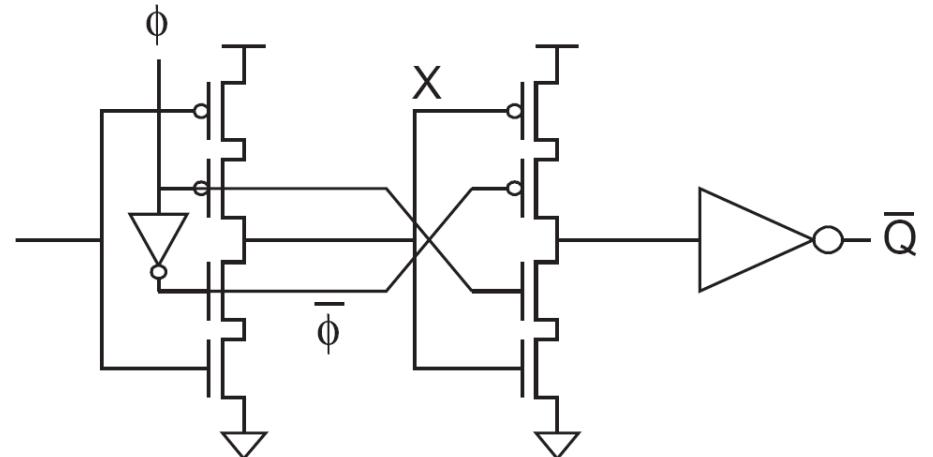


Review Static Flip-flop



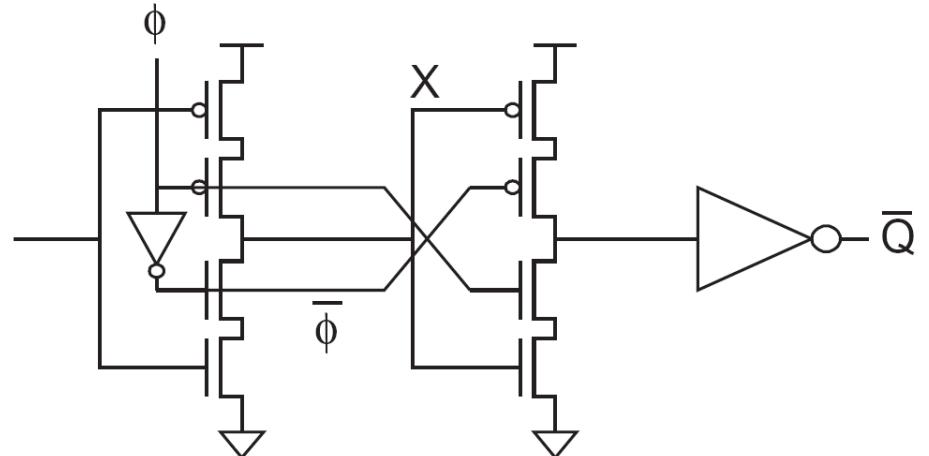
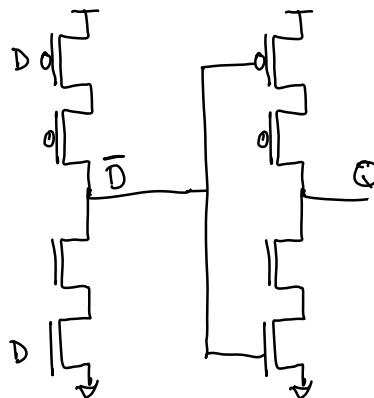
C²MOS Flip-Flop for Lab 2

- ❑ Two tristate inverters. Transparent on opposite clk phases
- ❑ Dynamic — undriven nodes hold state capacitively for 1 phase



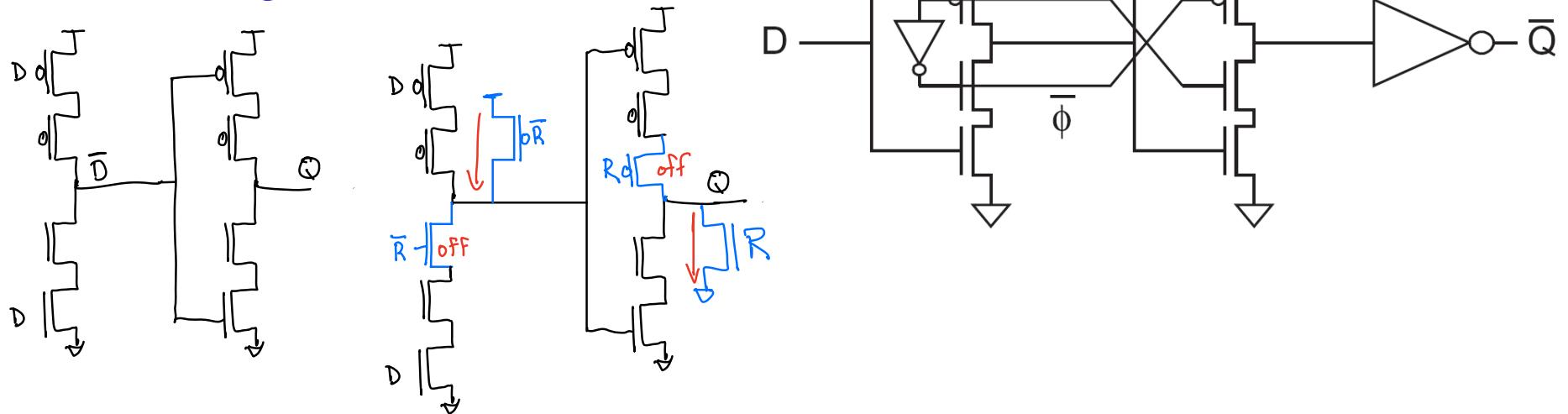
C²MOS Flip-Flop for Lab 2

- ❑ Two tristate inverters. Transparent on opposite clk phases
- ❑ Dynamic — undriven nodes hold state capacitively for 1 phase
- ❑ How to reset asynchronously without current flowing from Vdd to ground?



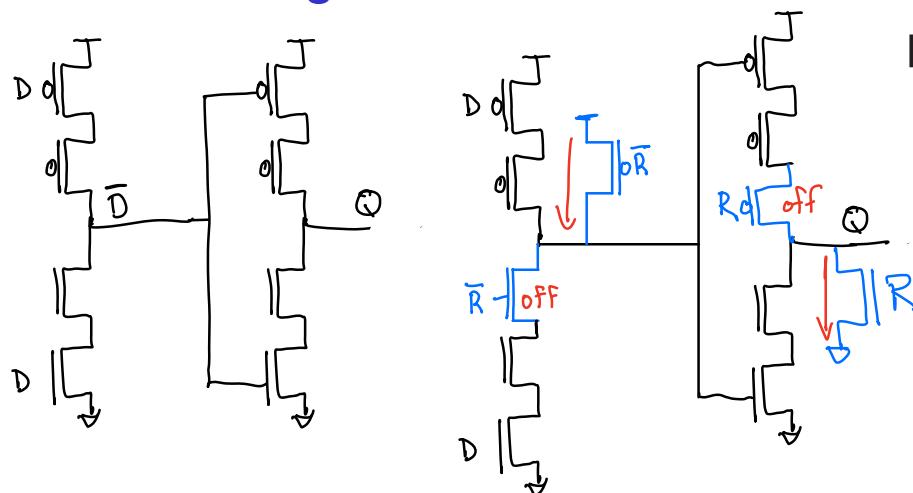
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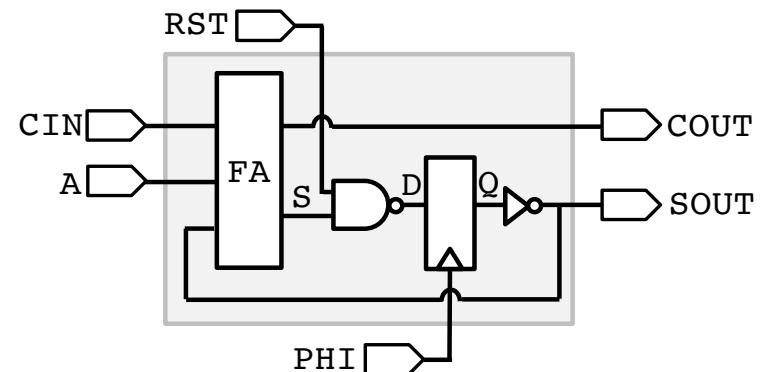
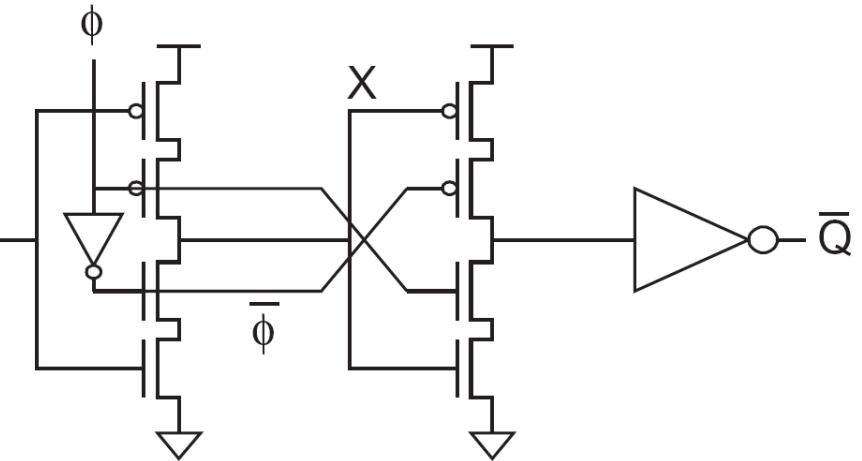


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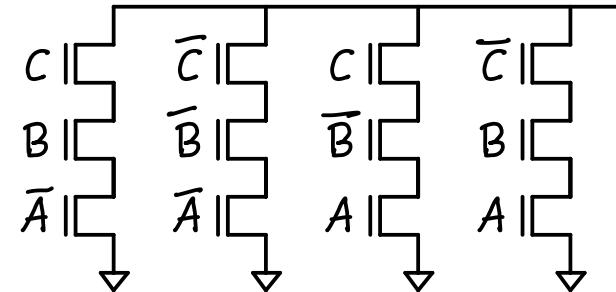


- You will instead use synchronous reset in this lab (see NAND gate)
- NAND/INV both invert.
SOUT polarity matches S



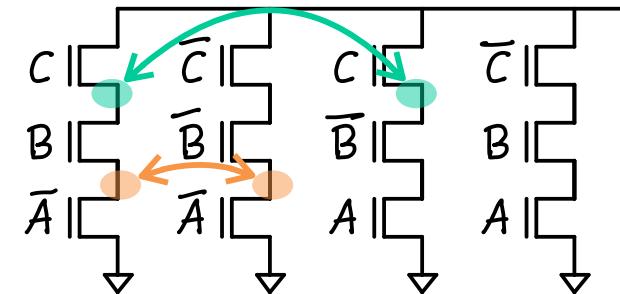
Discuss XOR gate

- ❑ XOR output always depends on all inputs
 - ❑ Contrast to NAND
 - ❑ Pull-up/down stacks of n-input static CMOS XOR must have n transistors
 - ❑ Merge redundant nodes in stacks
- ❑ Need inverted inputs



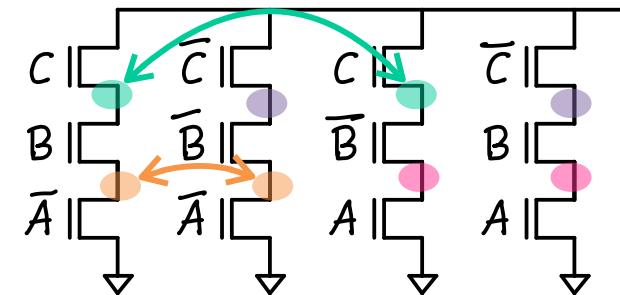
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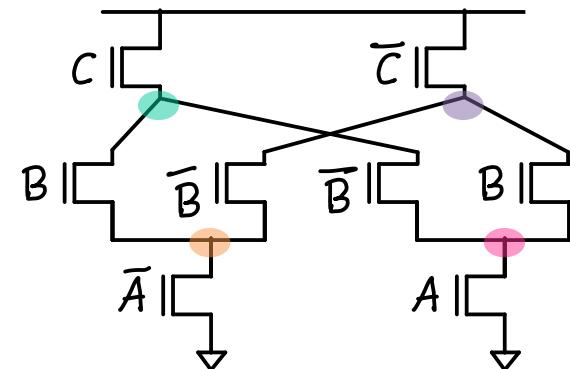
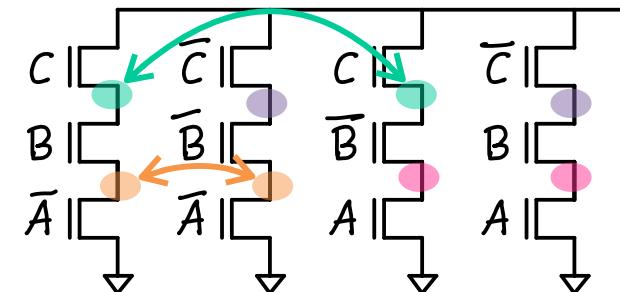
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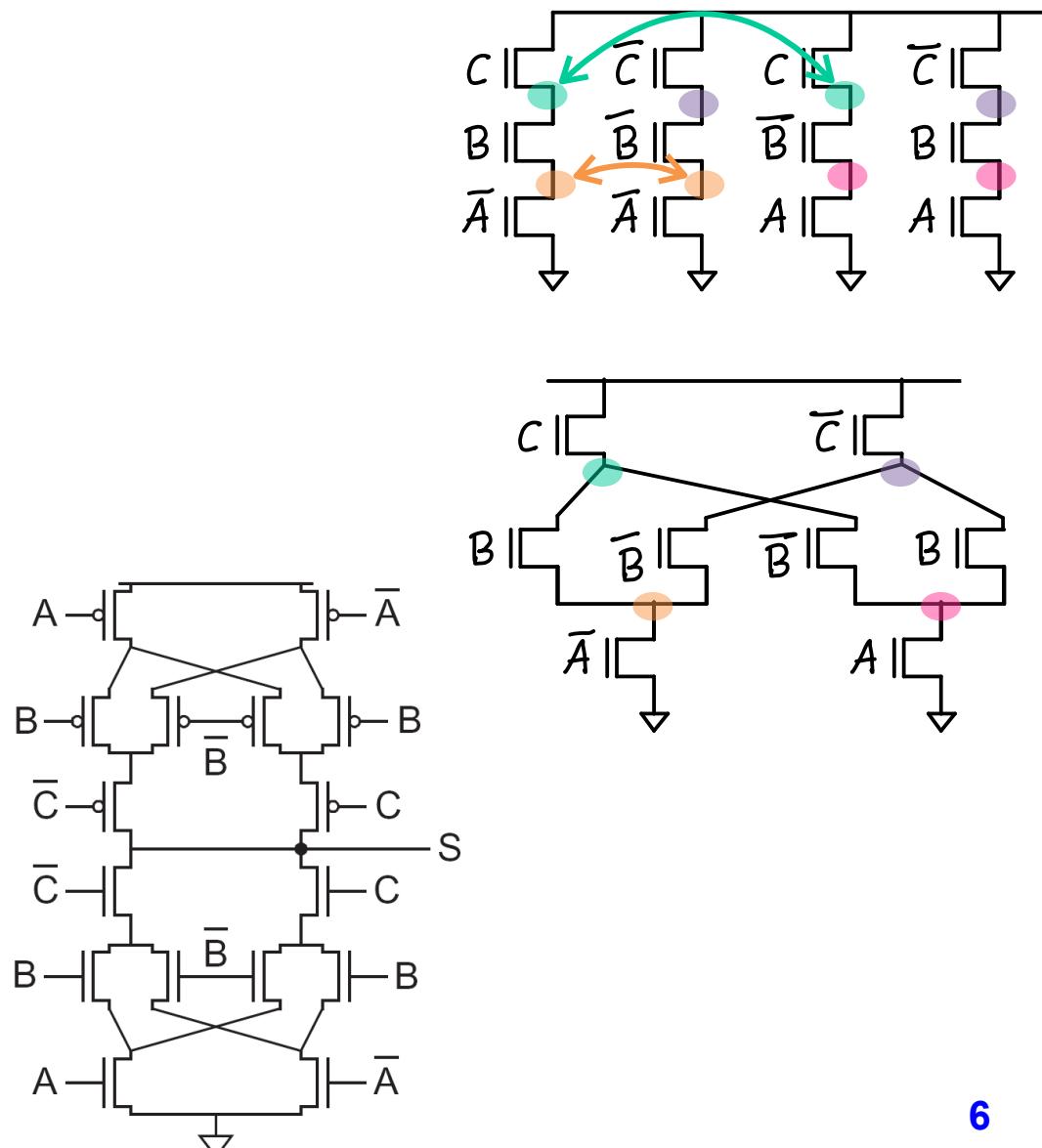
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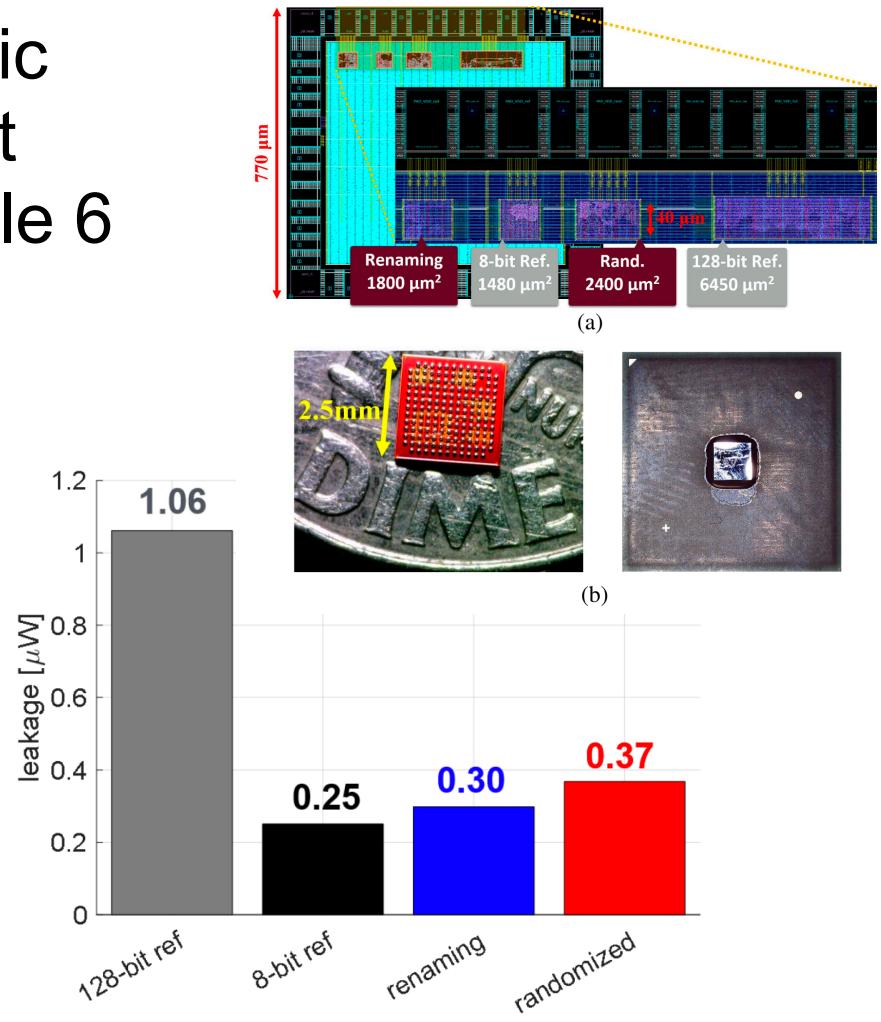
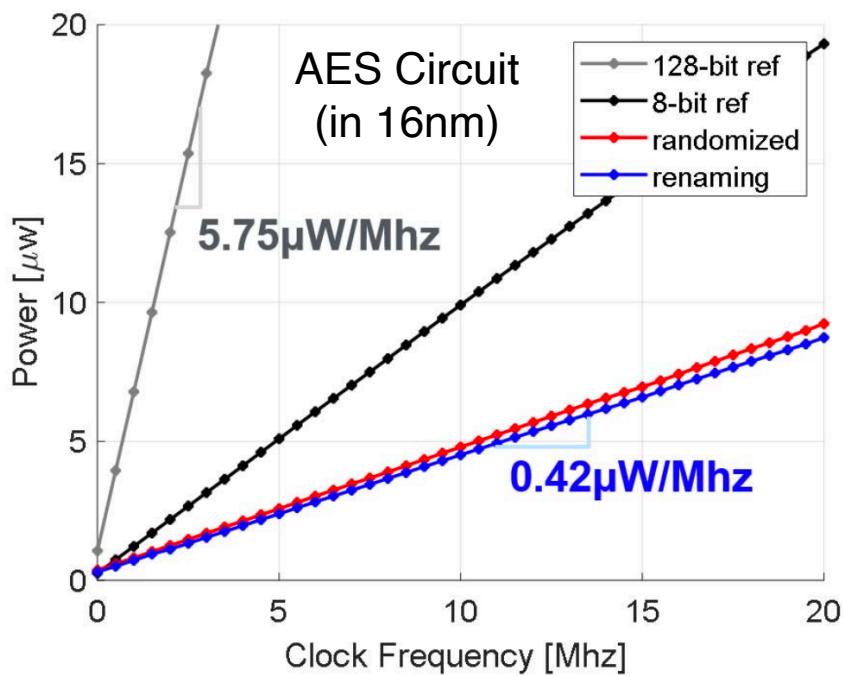
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Power Measurement Technique

- Infer both dynamic and static power from overall power at different frequencies. Module 6 will cover power in lecture.



S. N. Dhanuskodi, S. Allen and D. E. Holcomb, "Efficient Register Renaming Architectures for 8-bit AES Datapath at 0.55 pJ/bit in 16-nm FinFET," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 8, pp. 1807-1820, Aug. 2020, doi: 10.1109/TVLSI.2020.2999593.

Power Measurement Example

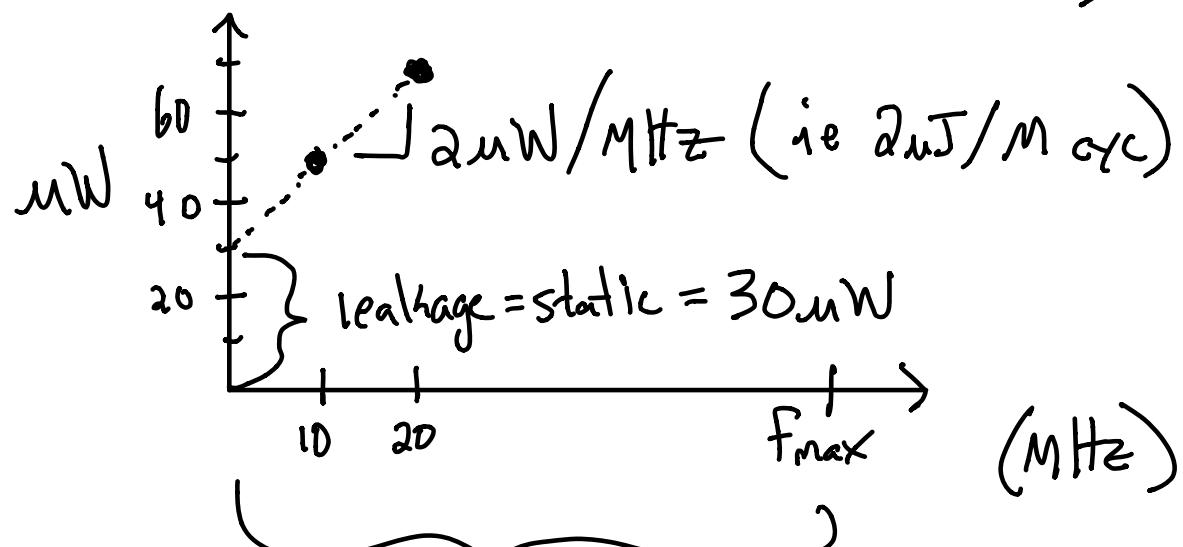


Power Measurement Example

$$W = \frac{J}{s} \quad Hz = \frac{cyc}{s}$$

10 MHz : 50 μW ($= 50 \mu J / 10 M cyc$)

20 MHz : 70 μW ($= 70 \mu J / 20 M cyc$)



if f_{max} = 100 MHz

$$\text{Power} = 30 \mu W + \frac{100 \text{ MHz}}{\text{MHz}} \cdot \frac{2 \mu W}{\text{MHz}} = 230 \mu W$$