

Lab 1 Report

student name: Wang Junfei (ECE 658)

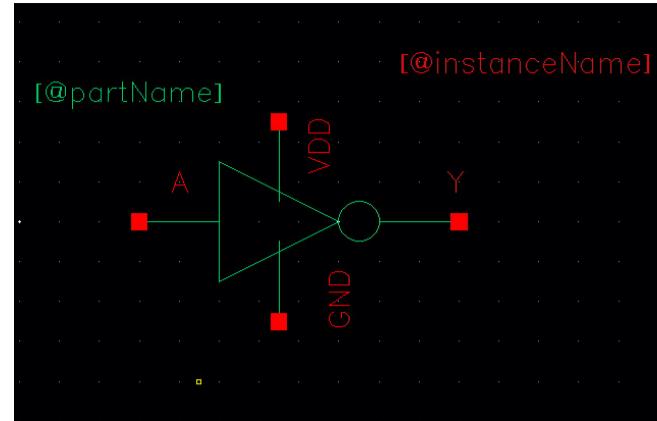
ID : 33006896

Step 1:

Truth Table for Multiplexer

S \bar{S}	B	A	Y
0 / 1	X	0	0
0 / 1	X	1	1
1 / 0	0	X	0
1 / 0	1	X	1

image of transistor-level NOT symbol:



Step 2:

image of transistor-level NAND schematic:

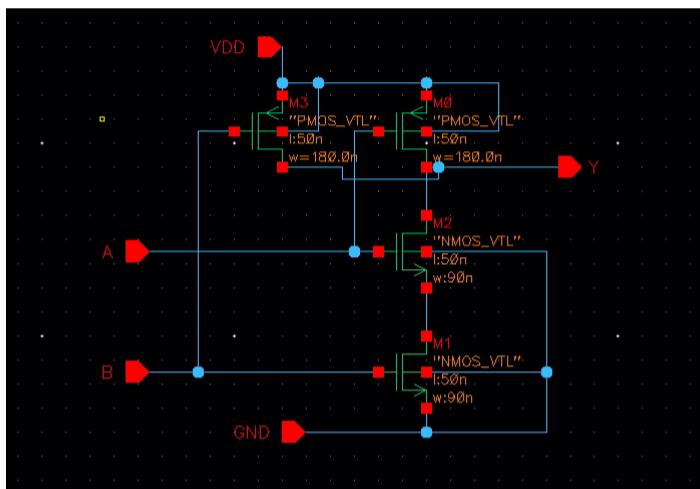


image of transistor-level NAND symbol:

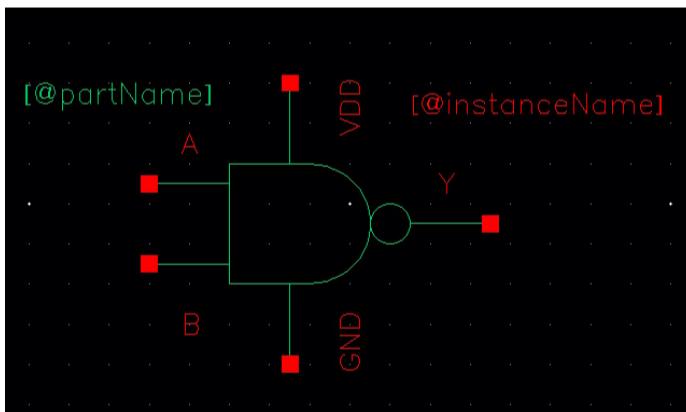
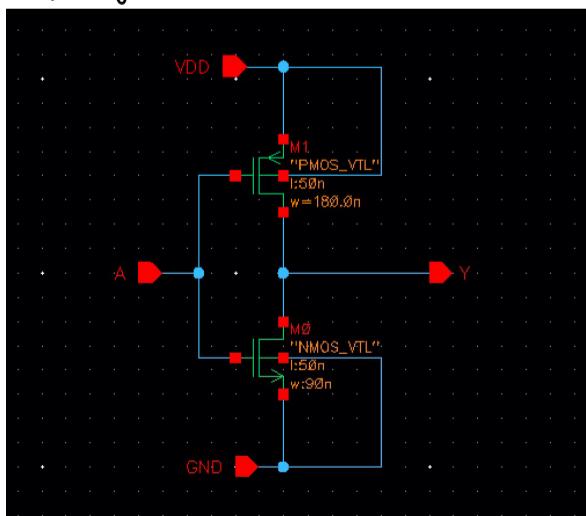
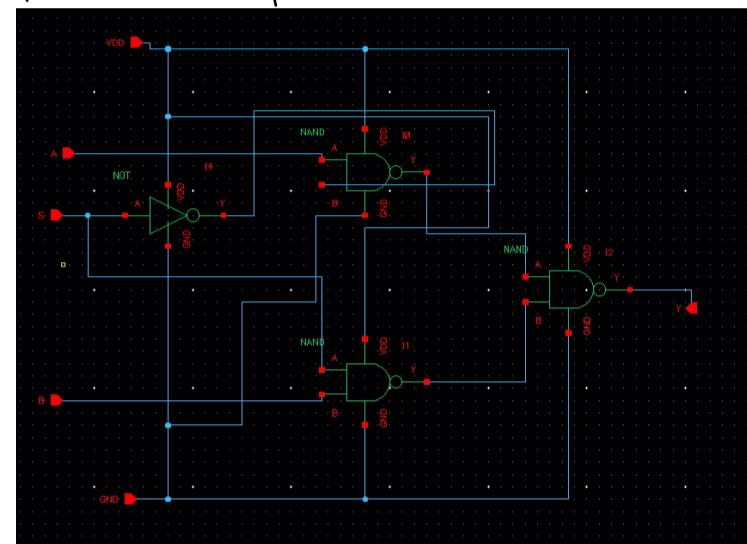


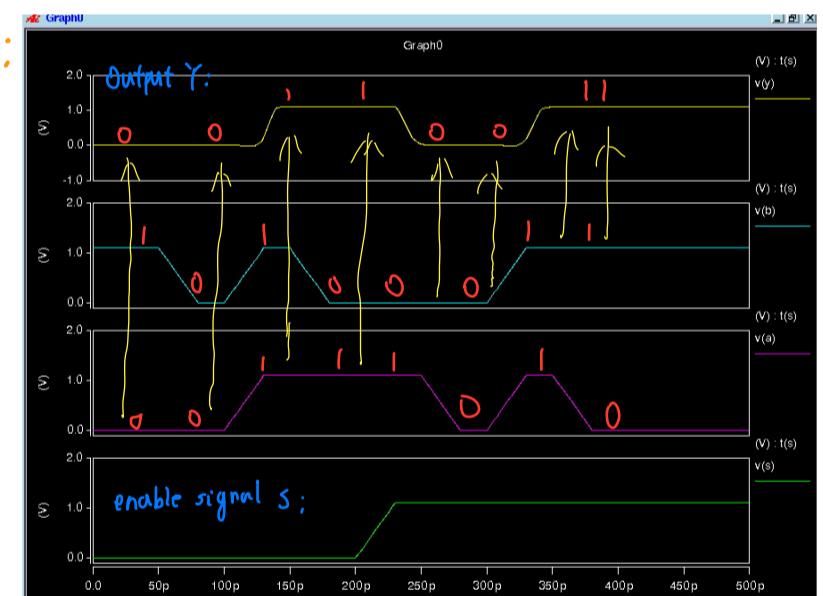
image of transistor-level NOT schematic:



Cyber level multiplexer schematic:



Step 3 :



This is my input order
and output order:

S	b	a	Y	execution order
0	1	0	0	↓ order
0	0	0	0	
0	1	1	1	
0	0	1	1	
1	0	1	0	
1	0	0	0	
1	1	1	1	
1	1	0	1	

I set up the switching period is 50 ps and transient time is 500ps.

Step 4:

Since step 4, I change transient time to 1ns
and switching period is 100ps.

Input before → after	Output before → after	$t_{pd़}$	t_r	t_{pdf}	t_f
SBA	y				
$000 \rightarrow 001$	$0 \rightarrow 1$	$1.870e^{-11}$	$7.669e^{-12}$		
$010 \rightarrow 011$	$0 \rightarrow 1$	$1.869e^{-11}$	$7.668e^{-12}$		
$010 \rightarrow 110$	$0 \rightarrow 1$	$2.000e^{-11}$	$8.212e^{-12}$		
$101 \rightarrow 111$	$0 \rightarrow 1$	$1.583e^{-11}$	$2.520e^{-11}$		
$101 \rightarrow 001$	$0 \rightarrow 1$	$2.367e^{-11}$	$6.718e^{-12}$		
$100 \rightarrow 110$	$0 \rightarrow 1$	$1.583e^{-12}$	$2.520e^{-11}$		
$001 \rightarrow 000$	$1 \rightarrow 0$			$1.606e^{-11}$	$9.389e^{-12}$
$011 \rightarrow 010$	$1 \rightarrow 0$			$1.605e^{-11}$	$9.392e^{-12}$
$110 \rightarrow 010$	$1 \rightarrow 0$			$1.704e^{-11}$	$8.372e^{-12}$
$111 \rightarrow 101$	$1 \rightarrow 0$			$1.866e^{-11}$	$8.507e^{-12}$
$001 \rightarrow 101$	$1 \rightarrow 0$			$2.383e^{-11}$	$8.765e^{-12}$
$110 \rightarrow 100$	$1 \rightarrow 0$			$1.863e^{-11}$	$8.466e^{-12}$

Step 5:

Input before → after

Output before → after

P_{dyn}

$t_{pd़}$

t_r

t_{pdf}

t_f

SBA: $000 \rightarrow 001$

$001 \rightarrow 000$

$0 \rightarrow 1$

$3.988e^{-05}$

$1.419e^{-04}$

$6.910e^{-11}$

$7.904e^{-11}$

$1.231e^{-10}$

$1.799e^{-10}$

$1 \rightarrow 0$

$7.550e^{-05}$

$1.862e^{-04}$

$0 \rightarrow 1$

$2.146e^{-04}$

$9.561e^{-04}$

$4.354e^{-11}$

$4.797e^{-11}$

$7.064e^{-11}$

$1.059e^{-10}$

$1 \rightarrow 0$

$3.916e^{-04}$

$1.283e^{-03}$

$0 \rightarrow 1$

$4.608e^{-05}$

$1.546e^{-04}$

$8.982e^{-11}$

$9.221e^{-11}$

$1.373e^{-10}$

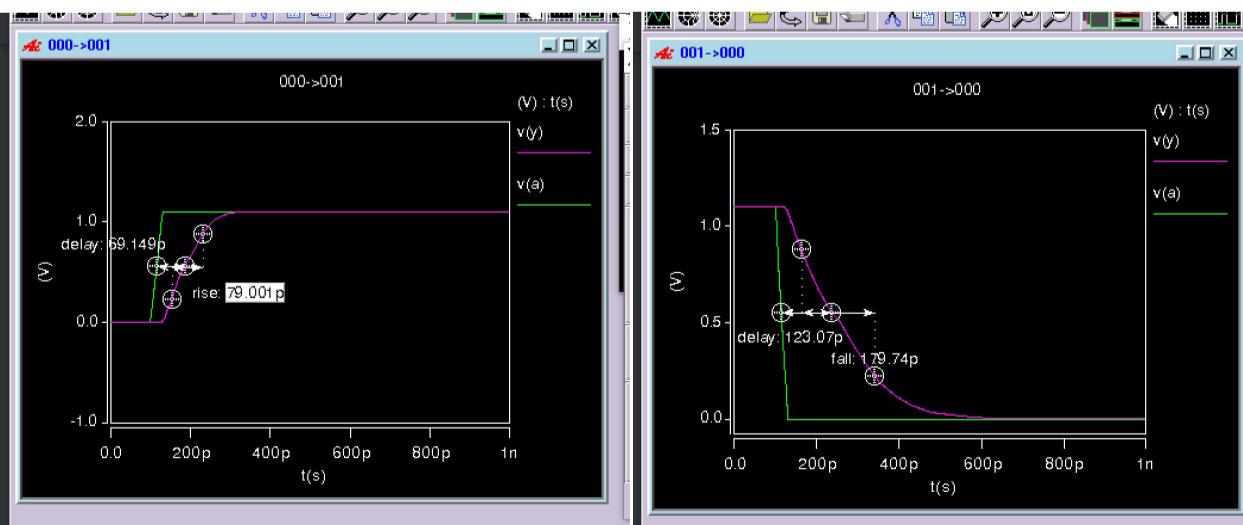
$1.941e^{-10}$

$1 \rightarrow 0$

$8.108e^{-05}$

$1.914e^{-04}$

Simulation waveforms with $t_{pd़}, t_{pdf}, t_r, t_f$:



Difference between time measurement in Step 4 and in Step 5: after adding the load on the output, the $t_{pd़}, t_{pdf}, t_f, t_r$ are all larger. In my opinion, I guess more load means more capacitance. The more capacitance, the more time to charge and discharge, So the variable t increases.

how to measure P_{stat} and P_{dyn} :

I just add two line in .spice file to measure P_{stat} and P_{dyn} :

- measure tran dynpower avg power from On to In

- measure tran leakage-current rms $I(vSupply)$ from On to In

* (Static power = leakage-current \times supply voltage)

For dynamic power:

Dynamic power consumption consists of two parts: switching current and short-circuit current,

The switching current accounts for about 80% of the total power consumption.

Step 6:

$6+2 = 8$ times So I need make transistor 8 times wider than original
∴ for NMOS: wide = $90 \times 8 = 720$ for PMOS: wide = $180 \times 8 = 1440$

```
lab1_load2.spice 記事本
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)
* Digital vector file for input
.vec 'input.vec'

** Library name: demo
** Cell name: NOT
** View name: schematic
.subckt NOT a gnd vdd y
m0 y a gnd gnd NMOS_VTL L=50e-9 W=720e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9 PS=300e-9 M=1
m1 y a vdd vdd PMOS_VTL L=50e-9 W=1440e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9 PS=390e-9 M=1
.ends NOT
** End of subcircuit definition.

** Library name: demo
** Cell name: NAND
** View name: schematic
.subckt NAND a b gnd vdd y
m2 y a W=50e-9 NMOS_VTL L=50e-9 W=720e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9 PS=300e-9 M=1
m1 net12 b gnd gnd NMOS_VTL L=50e-9 W=720e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9 PS=300e-9 M=1
m3 y b vdd vdd PMOS_VTL L=50e-9 W=1440e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9 PS=390e-9 M=1
m0 y a vdd vdd PMOS_VTL L=50e-9 W=1440e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9 PS=390e-9 M=1
.ends NAND
** End of subcircuit definition.
```

I modify the size directly from netlist.

I add the measurement in Step 5.

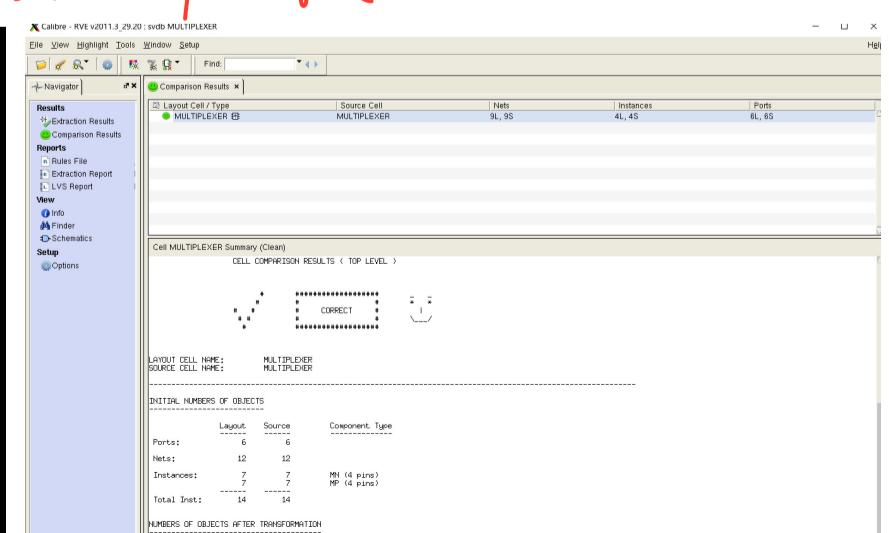
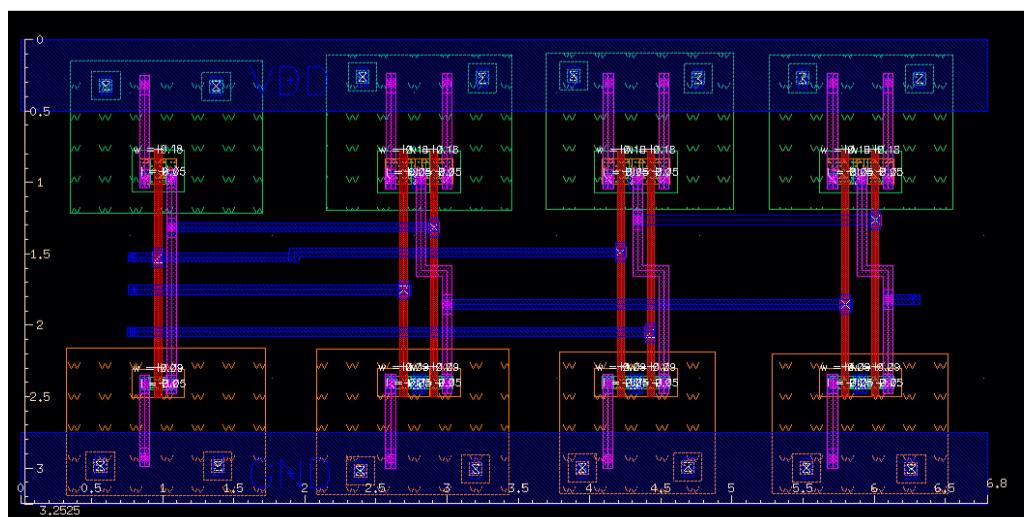
Difference between Step 5 and Step 6:

Compared with Step 5, the $t_{pd}\text{, } t_{pdf}\text{, } t_r\text{, } t_f$ decrease and $P_{stat}\text{, } P_{dyn}$ increase.

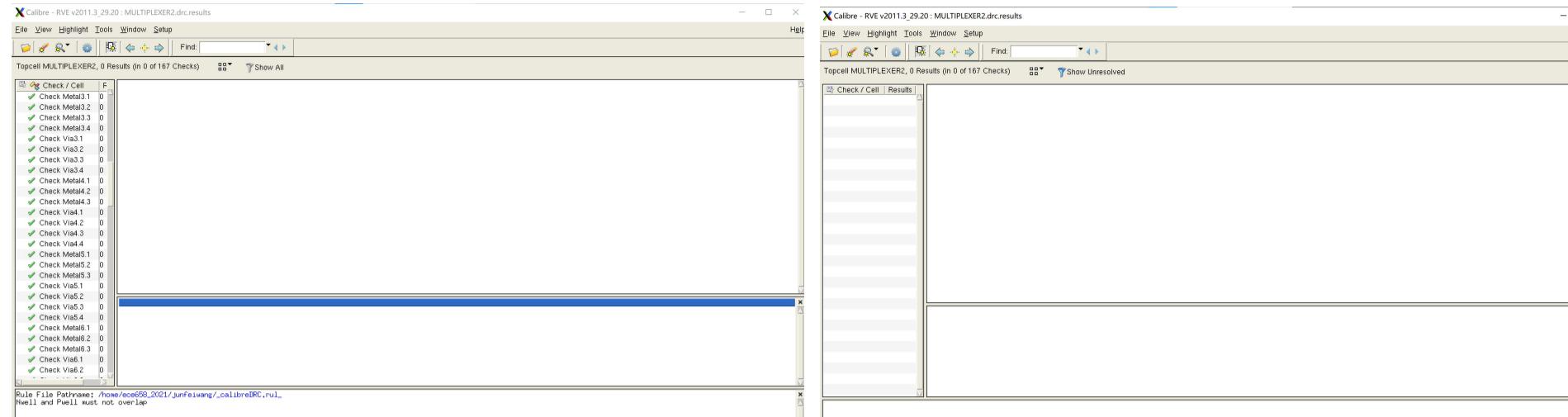
In circuit mechanism, the wider CMOS, the channel between source and drain is wider, which means more electrons or holes we can transmit. Because of $P=VI$, the P_{stat} and P_{dyn} will increase.

Step 7: Layout:

Screen capture of LVS:



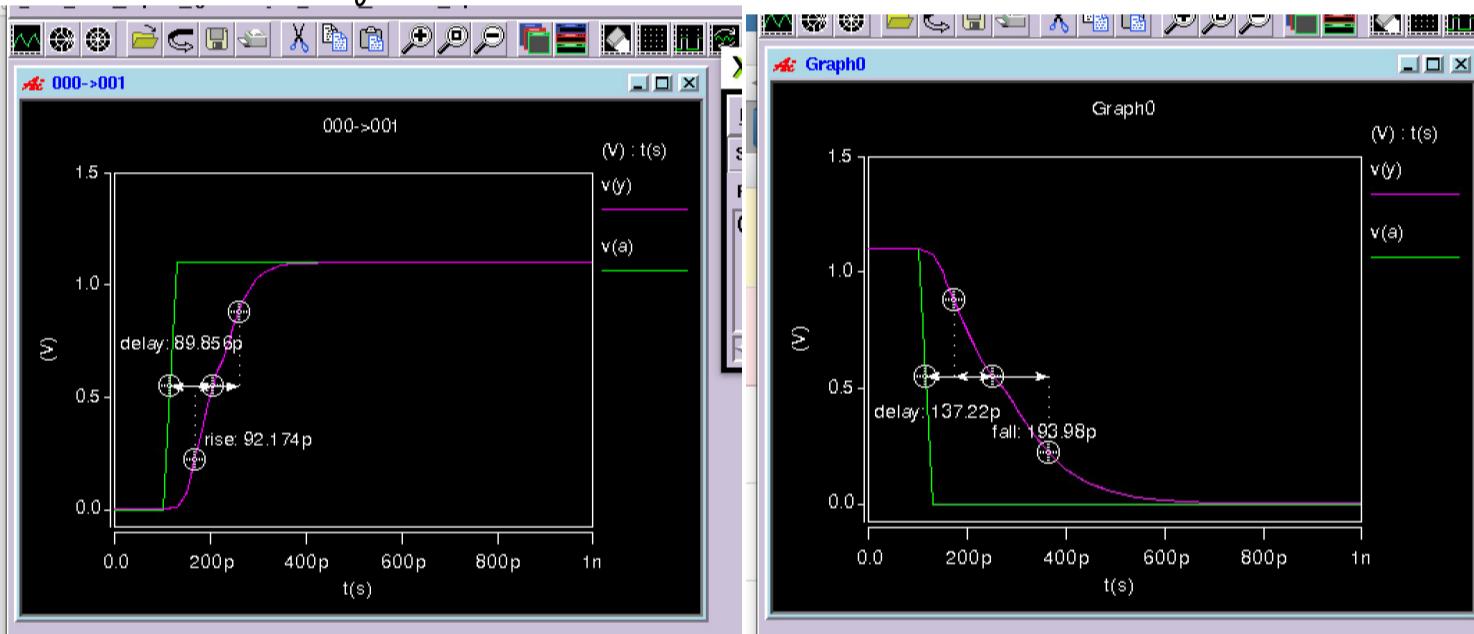
Screen capture of DRC:



Step 8:

I add the measurement row in Step 5.

Simulation Waveform with t_{pdR} , t_{pdf} , t_r , t_f :



Difference between step 5 and Step 8:

Compared with Step 5, the value of t_{pdR} , t_{pdf} , t_r , t_f , P_{stat} and P_{dyn} are all slightly increase from simulation the netlist with extracted parasitics. In my opinion, because of parasitics physics effects, the signals in one line will couple to adjacent lines, which could interfere the circuit and make propagation time and power arise.

This is a general description for 'parasitics':

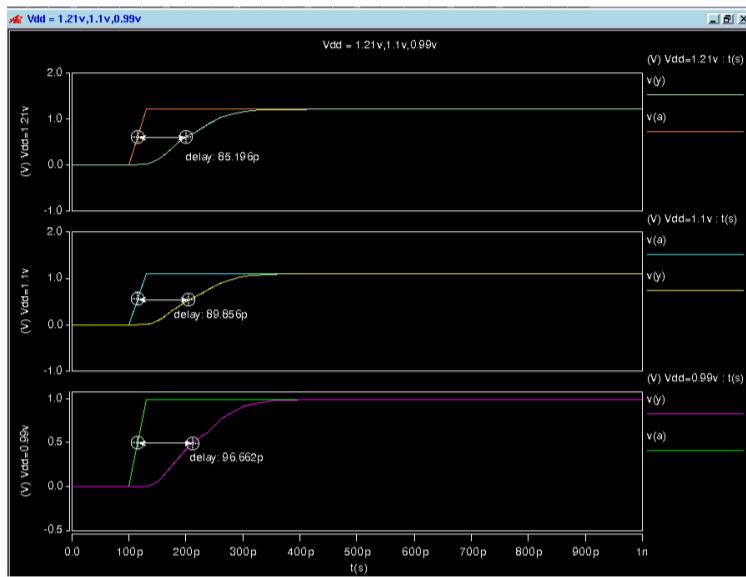
Basically, parasitics occur when you have multiple conductors in close proximity. Due to effects such as electric fields originating on one conductor and terminating on others, or magnetic fields passing around multiple conductors, charges excited on one conductor will result in induced charges excited on others.

This is a generally considered a problem, since we want signals to stay on one line and not couple to adjacent lines. Reducing them is also a challenge. Spacing out the conductors will generally be the simplest and most effective solution, but there are other options, depending on your topology.

So in order to reduce the effects of parasitics, We can increase the distance between metals, which will reduce the electric and magnetic fields . But I do not think it is a good idea , simply because the bigger areas means higher cost .

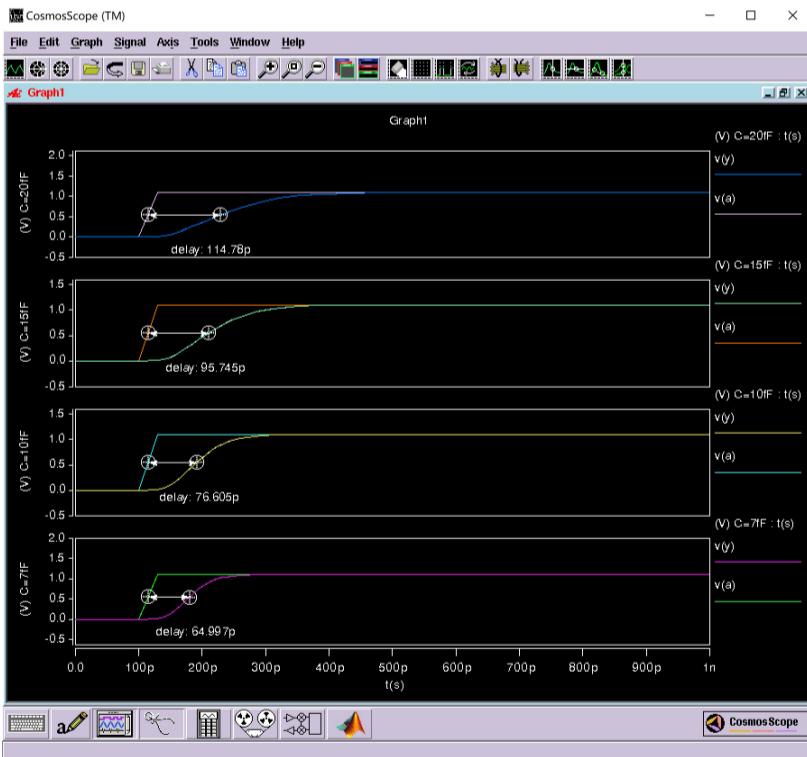
Step 9:

Step 9a:



with the increase of V_{dd} , $t_{pd़}$ declines .

Step 9b :



when $C = 7fF$, the $t_{pd़} = 64.997p$, from Step 8 I can know the $t_{pd़}$ with adding load(inverters and capacitance) is $89.82p$,

\downarrow
per 1fF means adding 3.87ps $t_{pd़}$

$$\therefore \frac{(76.605 - 64.997)ps}{3fF} = 3.87 ps/fF \quad \therefore C_{16 \text{ inverters}} = 6.414 fF$$

$$\therefore \frac{(89.82 - 64.997)ps}{3.87 ps} = 6.414 fF \quad \leftarrow 16 \text{ fanout inverters capacitance}$$