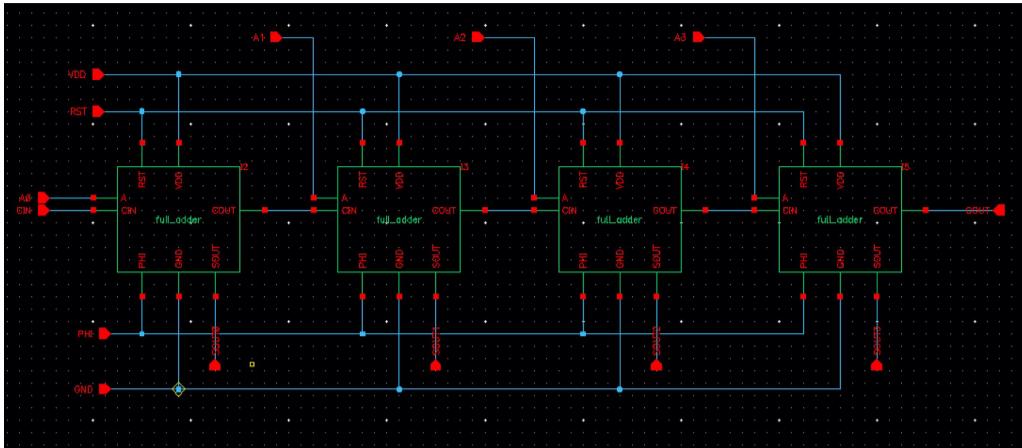


Step 1.

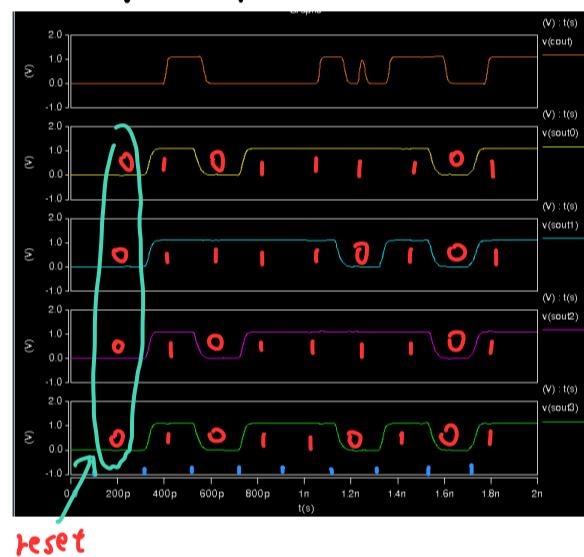
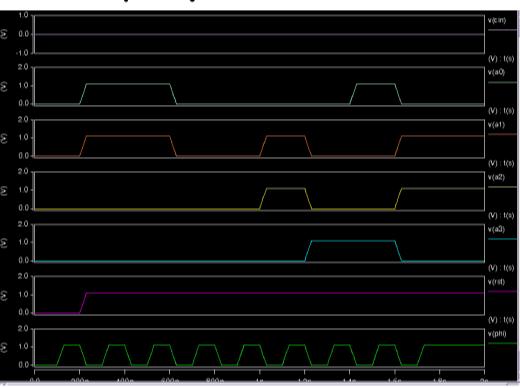


## Step 2:

in order to complete the table, I add some elements column.  
 the carry bit is CIN, C2N1, CIN2, C2N3 and COUNT. The sum of full adder before AND gate is S3, S2, S1, SO.

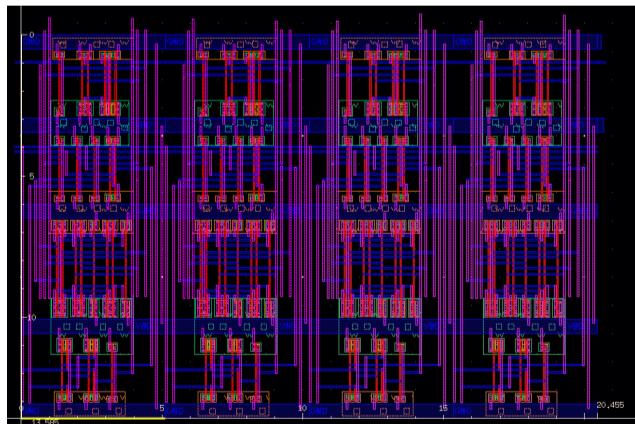
	A	B	C	D	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1	RST	A3	A2	A1	AI	COUT	CIN0	CIN1	CIN2	S3	S2	S1	S0	D3	D2	D1	D0	S1OUT2	T1OUT2	U1OUT2	V1OUT2	Q1	Q2		
2	0	0	0	0	1	0	0	0	0	X	X	X	X	1	1	1	x	x	x	x	x	x	x	x	
3	1	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	
4	1	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	
5	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	1	
6	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	
7	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	
8	1	1	0	1	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	
9	1	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	1	
10	1	0	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	0	1	1	0	0	0	1	

The seven input: phi, tSt, u3, u2, u1, u0, Cin      The five output: sout3, sout2, sout1, sout0, cout



## These

### Step 3:



height : 13.585 mm

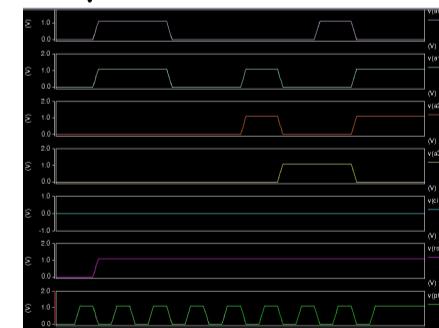
width: 29.955 μm

no too much change,

I just label the input and output pins and ground. Add pins to the accumulator layout, totally 14 ports.

## Step 4:

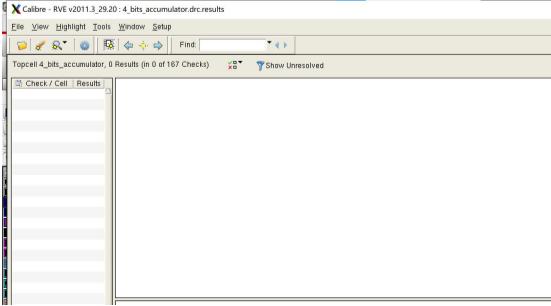
7 input: phi, tSt, C2N, a3, a2, a1, a0



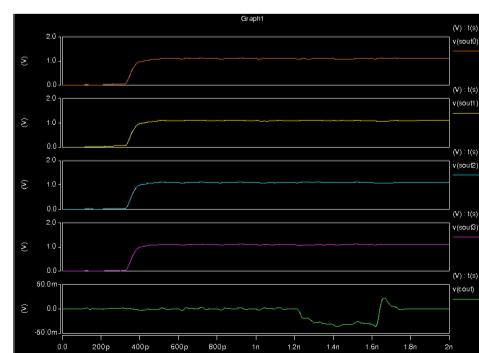
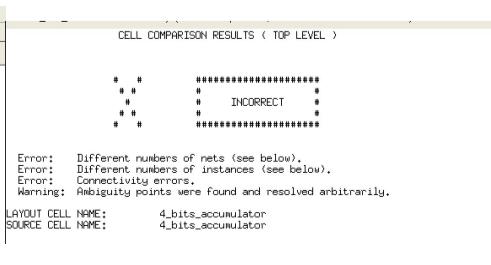
Output: cont, sent3, sent2, sent1, sent0.

## Step 4:

UFC!

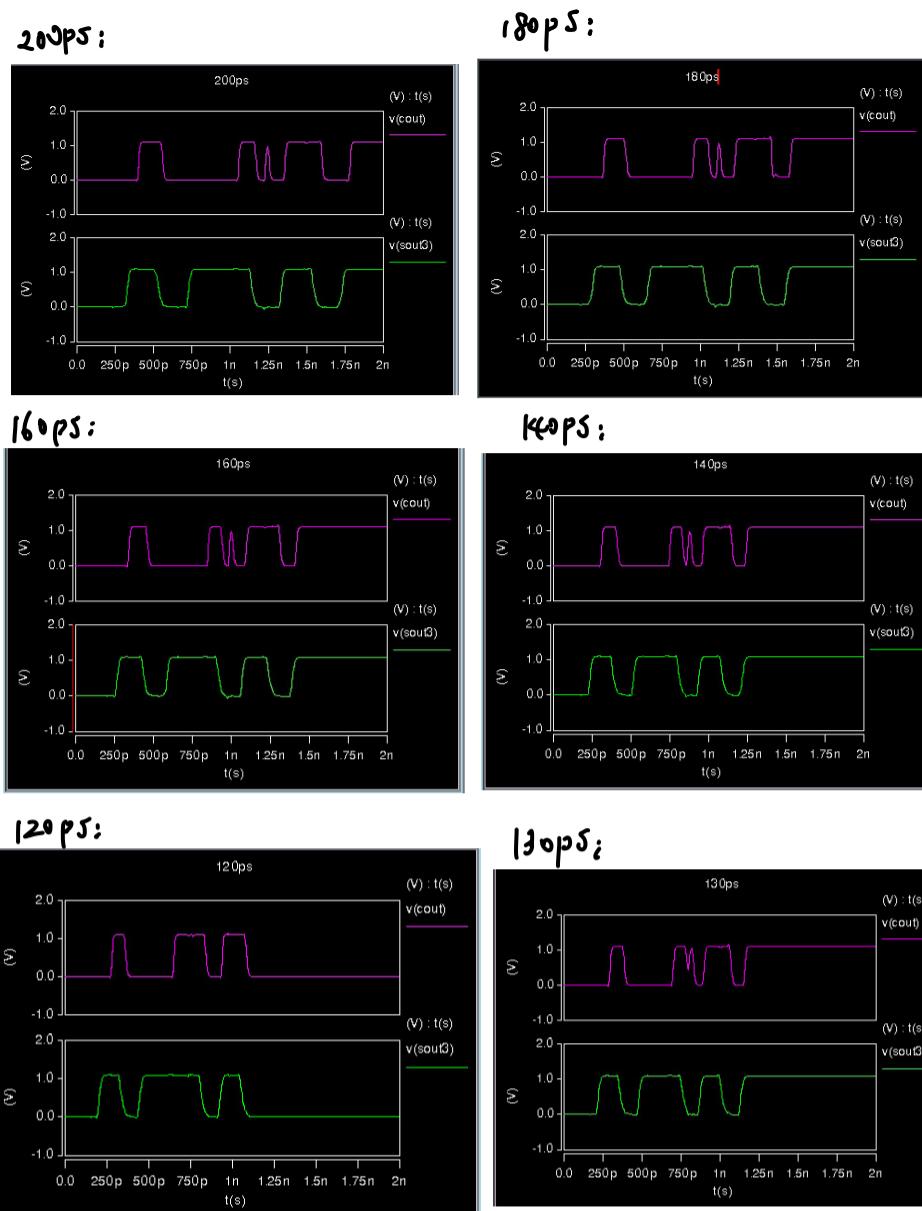


LVS :



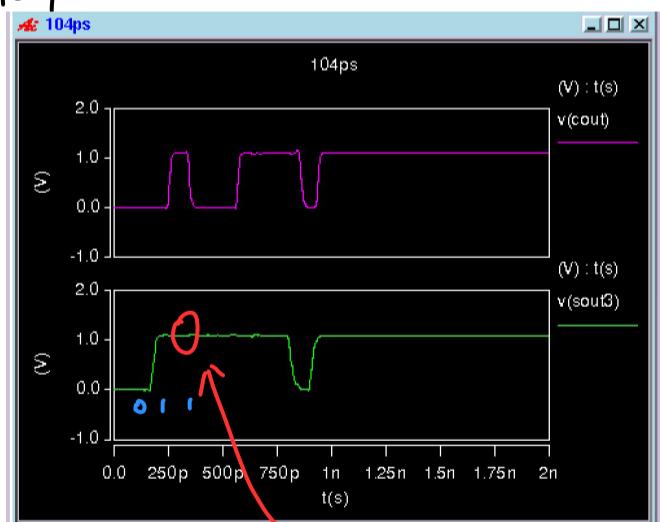
Step 5 : because clock must be slow enough for all stages to work properly. Critical path is the longest latency of stages that must be completed to successfully conclude a project from start to finish. In this layout, the critical path is from CIN to sout3, which will through combination logic (propagation delay) and sequential logic (D-flip flop : sequential overhead). Obviously, the latency will be maximum.

clock period	clock rate	rise and fall time
200 ps	5 GHz	20 ps
180 ps	5.56 GHz	18 ps
160 ps	6.25 GHz	16 ps
140 ps	7.14 GHz	14 ps
130 ps	8.33 GHz	13 ps
130 ps	7.69 GHz	13 ps



obviously, when clock period = 130 ps, the output has distortion.  
the minimum clock period should be 130ps, which means the maximum clock frequency should be around 7.69 GHz.

$$130\text{ps} \times (1-20\%) = 104\text{ps}$$

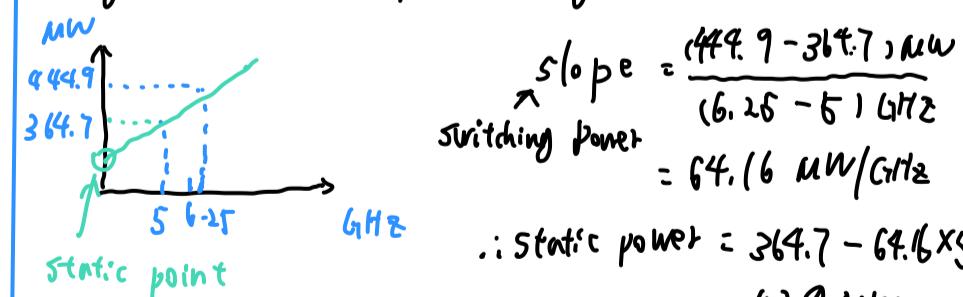


in third clock cycle, the incorrect value appears.  
obviously, which be caused by the critical path.  
simply because the clock is not slow enough to make all stage work properly.

### Step 6 :

clock period	clock rate	average power
200ps	5GHz	364.7 mW
160ps	6.25GHz	444.9 mW
120ps	8.33GHz	562.3 mW
104ps	9.62GHz	643.2 mW

$$\text{avg power} = \text{static power} + \text{dynamic power}$$



$$\begin{aligned} \text{slope} &= \frac{(444.9 - 364.7)}{(6.25 - 5) \text{ GHz}} \\ \text{switching power} &= 64.16 \text{ mW/GHz} \end{aligned}$$

$$\therefore \text{static power} = 364.7 - 64.16 \times 5 \text{ GHz} = 43.9 \text{ mW}$$

$$\begin{aligned} \therefore \text{dynamic power} &= \text{avg power} - \text{static power} \\ &= 643.2 \text{ mW} - 43.9 \text{ mW} \\ &= 599.3 \text{ mW} \end{aligned}$$

by add measure statement in netlist is easy to get avg power.

.measure then avgpower avg power from On to Xn .