

Step A1

3.① set modname accumulator-fa

=> accumulator-fa.

define modname as accumulator-fa

\$modname = accumulator-fa.

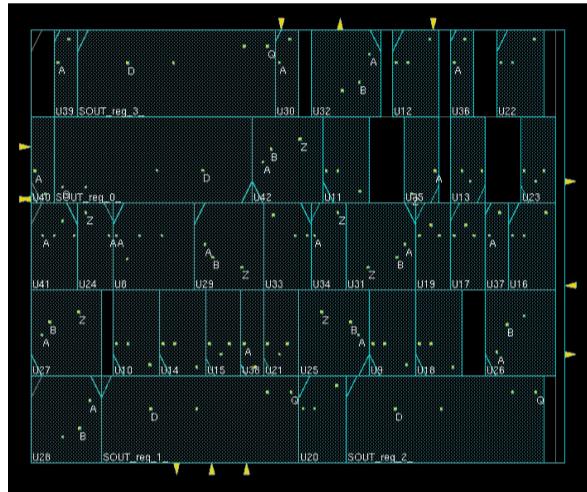
Cell	Reference	Library	Area	Attributes	U26	XNOR2_X1	NangateOpenCellLibrary	
SOUT_reg[0]	DFF_X1	NangateOpenCellLibrary	4.5220 n		U27	XOR_X1	NangateOpenCellLibrary	
SOUT_reg[1]	DFF_X1	NangateOpenCellLibrary	4.5220 n		U28	XNOR2_X1	NangateOpenCellLibrary	
SOUT_reg[2]	DFF_X1	NangateOpenCellLibrary	4.5220 n		U29	XOR_X1	NangateOpenCellLibrary	
SOUT_reg[3]	DFF_X1	NangateOpenCellLibrary	4.5220 n		U30	INV_X1	NangateOpenCellLibrary	
U8	AND2_X1	NangateOpenCellLibrary	1.0640		U31	XOR_X1	NangateOpenCellLibrary	
U9	AND2_X1	NangateOpenCellLibrary	1.0640		U32	XNOR2_X1	NangateOpenCellLibrary	
U10	AND2_X1	NangateOpenCellLibrary	1.0640		U33	AND2_X1	NangateOpenCellLibrary	
U11	AND2_X1	NangateOpenCellLibrary	1.0640		U34	CLKBUF_X1	NangateOpenCellLibrary	
U12	INV_X1	NangateOpenCellLibrary	0.5320		U35	CLKBUF_X1	NangateOpenCellLibrary	
add_1_root.add_15_2/U1_0	FA_X1	NangateOpenCellLibrary	4.2560 mo, r		U36	INV_X1	NangateOpenCellLibrary	
add_1_root.add_15_2/U1_1	FA_X1	NangateOpenCellLibrary	4.2560 mo, r		U37	INV_X1	NangateOpenCellLibrary	
add_1_root.add_15_2/U1_2	FA_X1	NangateOpenCellLibrary	4.2560 mo, r		U38	INV_X1	NangateOpenCellLibrary	
add_1_root.add_15_2/U1_3	FA_X1	NangateOpenCellLibrary	4.2560 mo, r		U39	INV_X1	NangateOpenCellLibrary	
				Total 13 cells	39.9000			
						U41	OAI2I_X1	NangateOpenCellLibrary
						U42	XOR2_X1	NangateOpenCellLibrary

which means when frequency

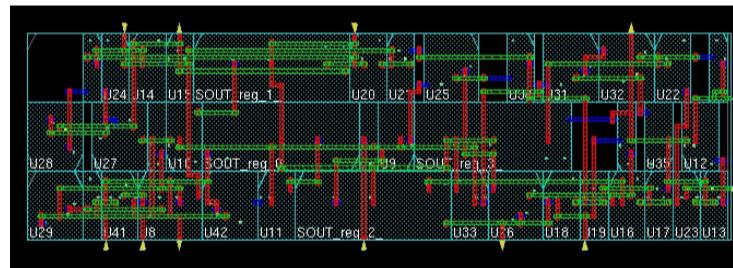
higher, the design have to add more cells in order to meet timing constrain, and accordingly the area will increase.

Step A2

1). ①



13. ① aspect ratio = 0.5.



③ 104 Average module density = 0.916.
105 Density for the design = 0.916.
106 = stdcell area 206 (55 um^2) / alloc area 225 (60 um^2).

∴ silicon area utilization = 91.6%

Step B1.

	Lab 3	Lab 4
- maximum frequency	7.69 GHz	0.5 GHz
power	537.29 mW	26.8 mW
area	278 mm ²	225 mm ²
cell height	13.6 mm	5.75 mm
number of metal layers	224	199

Maybe the use of different cells, the routing and placing accounts for the difference, these difference will affect the power consumption and limit the max frequency, and decide the area.

② the estimated area is 39.9

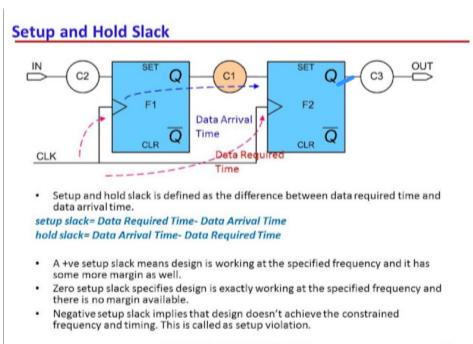
4 flip-flops the circuit use.

③ primitive: FA-X1, DFF-X1, ADD2-X1, INV-X1.

the primitives are part of the standard Verilog language, but User-Defined Primitive (UDP) can be designed by user.

8.① when CLK-PER = 2 ns ($f = 0.5\text{GHz}$), the slack = 0.0015, area estimation = 54.796.

⑤ second target frequency = 0.25 GHz (CLK-PER = 4 ns). the slack = 1.4766, area estimation = 39.9



in the file, the slack (MET) is 17.446. so the design is working at the specified frequency, no timing violations.

Step 82.

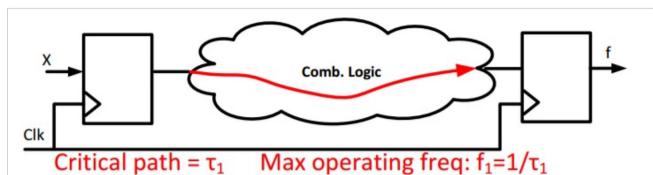
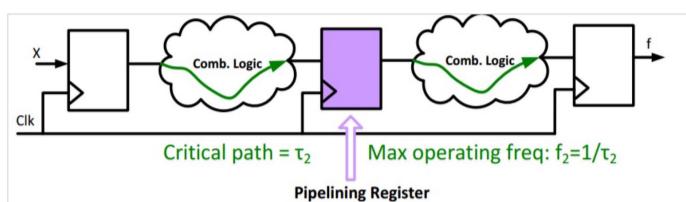


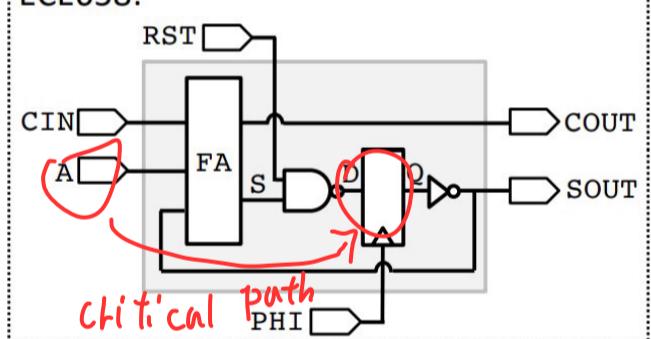
Figure 4. Long combinational logic path. Image courtesy of the Sharif University of Technology (PDF)



The critical path is the longest path with slowest time in the circuit and limits the clock speed. I find critical path from D-flip flop because data required time is very important for critical path. Data required time is the time taken for the clock to traverse through clock path. If face a very long critical path due to an extensive combinational circuit. In such cases, our data required time will increase to ensure that the delays associated with the critical path do not lead to set up time violations.

Yes, it begin and end at the same place as my critical path from lab3.

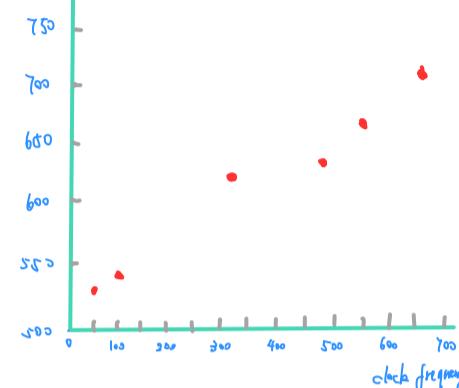
ECE658:



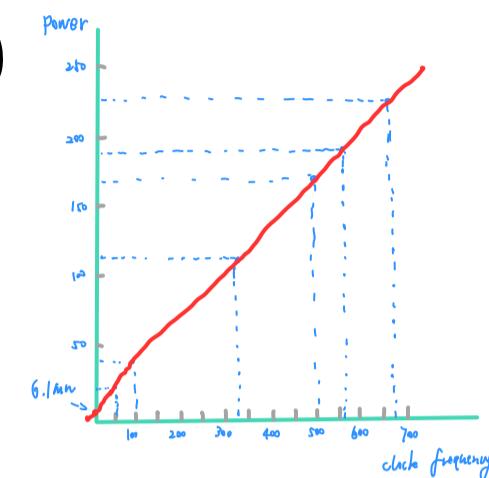
	target clock periods	cell area	total power
670MHz	1.5 ns	713.7	230.8 mW
556MHz	1.8 ns	655.7	188.4 mW
500MHz	2.0 ns	629.4	170.8 mW
333MHz	3.0 ns	628.0	114.7 mW
100MHz	10.0 ns	537.1	40.9 mW
50MHz	20.0 ns	529.1	23.5 mW

②

cell area



③



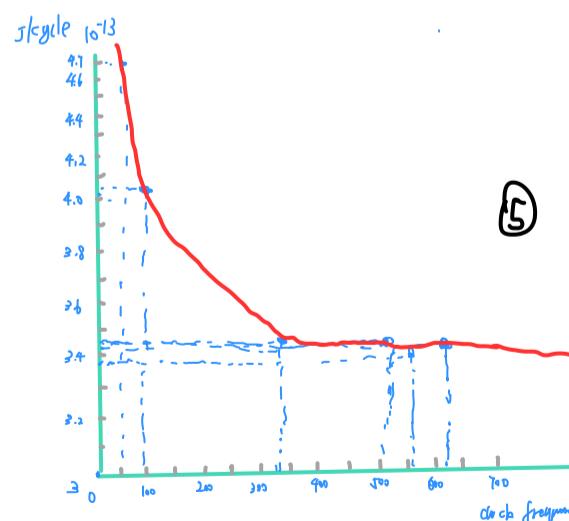
$$\text{slope} = \frac{40.9 - 3.5}{100 - 50} = 0.348$$

$$23.5 - 50 \times 0.348 = 6.1 \text{ mW}$$

frequency clock period total power J/cycle

670MHz	1.5 ns	230mW	3.45×10^{-13}
556	1.8	188.4	3.3912×10^{-13}
500	2.0	170.8	3.416×10^{-13}
333	3.0	114.7	3.441×10^{-13}
100	10.0	40.9	4.09×10^{-13}
50	20.0	23.5	4.70×10^{-13}

④



⑤ report-qor :

Information: Updating graph... (UID-83)
Information: Updating design information... (UID-85)

Report : qor
Design : accumulator ha
Version: E-2010.12-SP5-2
Date : Sun Nov 21 18:20:32 2021

Timing Path Group 'PHI'

Levels of Logic: 64.0000
Critical Path Length: 8.8573
Critical Path Slack: 9.8687
Critical Path Clk Period: 20.0000
Total Negative Slack: 0.0000
No. of Violating Paths: 0.0000
Worst Hold Violation: 0.0000
Total Hold Violation: 0.0000
No. of Hold Violations: 0.0000

Cell Count

Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 258
Buf/Inv Cell Count: 2
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 194
Sequential Cell Count: 64
Macro Count: 0

How to measure area/power:
report-power > power.tpt
report-area > area.tpt.
in CompileAnalyze.tcl

```

1 module accumulator_ha( PHI, RST, CIN, SOUT, COUT);
2
3 input PHI;
4 input RST;
5 input CIN;
6 output reg[63:0] SOUT;
7 output COUT;
8
9 wire [63:0] B;
10 wire [64:0] S;
11
12 assign B = SOUT;
13 assign COUT=S[64];
14 assign S = B+CIN;
15
16 always @(posedge PHI)
17 begin
18   if(RST)
19     SOUT <= 64'h0;
20   else
21     SOUT <= S[63:0];
22 end
23
24 endmodule
25

```

Step C2.

```

① module test( PHI, RST, SOUT);
  input RST;
  input PHI;
  output reg SOUT;

  wire S;
  wire B;

  assign B = SOUT;
  assign S = ~B;

  always @(posedge PHI)
  begin
    if(RST)
      SOUT <= 1'b1;
    else
      SOUT <= ~S;
  end
endmodule

```

How I change Constraints.tcl:

```

set CLK-PER 3.0
set FANOUT 50

```

② Load Area Timing violation? Cells used

Load	Area	Timing violation?	Cells used
50	5.3	no	DFF-X1, NAND2-X1
100	5.9	no	DFF-X2, NAND2-X1
150	6.6	no	DFF-X1, INV-X1, NAND2-X1
200	6.6	no	DFF-X1, NAND2-X1, INV-X4
225	7.7	no	DFF-X1, NAND2-X1, INV-X8
250	13.3	no	DFF-X1, NAND2-X1, INV-X1, INV-X2, BUF-X16

③ obviously, the Design Compiler should correctly apply the ideas of effort-based sizing, because with the increase of load, the number of cell increase and accordingly the size of cell become bigger in order to have a multi-stage driver with progress size to reduce the size.

