

### Step 1:

the coordinate is (x,Y) format  
 (0,0) to (2,2).  
 $(0,0) \rightarrow (1,0) \rightarrow (2,0) \rightarrow (2,1) \rightarrow (2,2)$   
 $(2,2) \rightarrow (1,2) \rightarrow (1,1)$

### Step 2:

```
# Loading work,crossbar(fast)
VSIM 6> run -all
#
# finished initializing tile memories at time 0
#
# finished initializing tile memories at time 5160
# Router (0,0) received packet [1,2,f1] from PROC @ 5240
# Router (0,1) received packet [1,2,f1] from west @ 5280
# Router (0,2) received packet [1,2,f1] from west @ 5320
# Router (1,2) received packet [1,2,f1] from north @ 5360
# Router (0,0) received packet [2,2,f2] from PROC @ 5390
# Router (0,1) received packet [2,2,f2] from west @ 5430
# Router (0,2) received packet [2,2,f2] from west @ 5470
# Router (1,2) received packet [2,2,f2] from north @ 5510
# Router (2,2) received packet [2,2,f2] from north @ 5550
# Break in Module Testbench at /home/ece658_2021/junfeiwang/lab5/Testbench.v line 64
```

when I need find testbench file, I can not understand what is the difference between project panel and library panel.

And I solve it by understanding what is library panel.

### Step 3:

For setup.tcl : set modname Tile  
 purpose: change the top level module name and synthesize a tile.

For read.tcl :

```
read_verilog $RTL_DIR/Tile.v
read_verilog $RTL_DIR/ALU32.v
read_verilog $RTL_DIR/Controller.v
read_verilog $RTL_DIR/crossbar.v
read_verilog $RTL_DIR/InstructionDecoder.v
read_verilog $RTL_DIR/matrix5arb.v
read_verilog $RTL_DIR/Memory.v
read_verilog $RTL_DIR/Processor.v
read_verilog $RTL_DIR/ram_dp_ar_aw.v
read_verilog $RTL_DIR/RegisterFile.v
read_verilog $RTL_DIR/route_table.v
read_verilog $RTL_DIR/router.v
read_verilog $RTL_DIR/syn_fifo.v
read_verilog $RTL_DIR/NangateOpenCellLibrary.v
read_verilog $RTL_DIR/system.v
```

purpose : read Tile.v and map onto a generic library.

For Constraints.tcl : set CLK\_PERIOD 10.0

purpose : a loose clock period can make for an easier synthesis job for design compiler

For CompleteAnalyze.tcl : ungroup -all -flatten

purpose : ensure that the post-synthesis tile is a single flattened module with no hierarchy.

Approximately 30689 cells instances are in the synthesized design.  
 the total cell area of the tile is 59602.09  
 how to obtain the answer : see the area.rpt  
 report-area > area.rpt

$$\text{maximum clock frequency}, \frac{1}{15\text{ns}} = 66.7 \text{MHz}$$

critical path length : 14.7613  
 level of logic : 54.0

how to found the answer : see the qor.rpt  
 report-qor > qor.rpt.

### Step 4 :

modification for system.v: Tile-final tile5 (. ...)

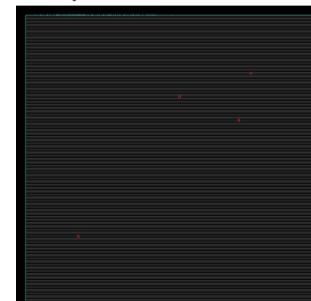
just instantiate the tile-final not Tile.

```
VSIM 3> run -all
#
# finished initializing tile memories at time 0
#
# finished initializing tile memories at time 5160
# Router (0,0) received packet [1,2,f1] from PROC @ 5240
# Router (0,1) received packet [1,2,f1] from west @ 5280
# Router (0,2) received packet [1,2,f1] from west @ 5320
# Router (1,2) received packet [1,2,f1] from north @ 5360
# Router (0,0) received packet [2,2,f2] from PROC @ 5390
# Router (0,1) received packet [2,2,f2] from west @ 5430
# Router (0,2) received packet [2,2,f2] from west @ 5470
# Router (1,2) received packet [2,2,f2] from north @ 5510
# Router (2,2) received packet [2,2,f2] from north @ 5550
# Break in Module Testbench at /home/ece658_2021/junfeiwang/lab5/Testbench.v line 64
```

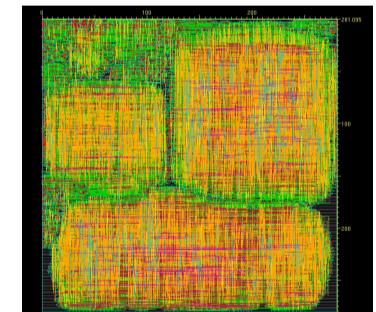
which matches the pre-synthesis simulation. it indicates that the synthesized design work correctly.

### Step 5:

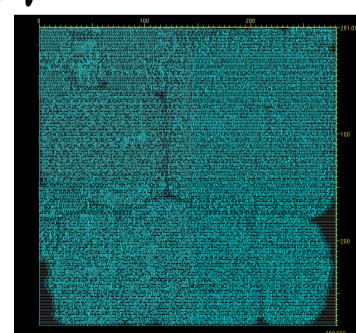
floorplan:



physical view with wire and bias:



physical view without wire and bias



the design dimensions is about 281um x 281um.

$$281\text{ }\mu\text{m} \times 281\text{ }\mu\text{m} = 78961\text{ }\mu\text{m}^2$$

in cell\_report\_final.rpt:

DFF\_X1 inlaygateopenCellLibrary

4.5220 n

valid\_data\_reg DFF\_X1 NangateOpenCellLibrary  
4.5220 n

Total 30689 cells 59088.1754

1

in encounter.log:

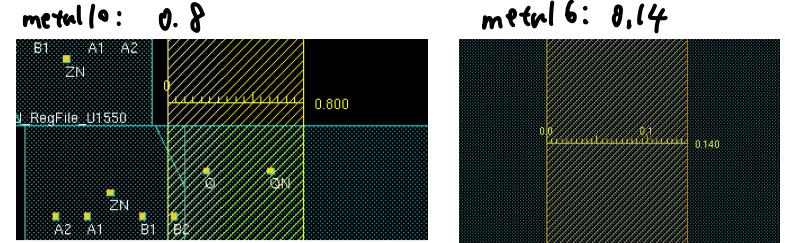
```
354 #std cell=30689 #block=0 (0 floating + 0 preplaced) #ioInst=0 #net=33//1 #term
355 stdCell: 30689 single + 0 double + 0 multi
356 Total standard cell length = 42.2058 (mm), area = 0.0591 (mm^2)
357 Average module density = 0.750.
358 Density for the design = 0.750.
359     = stdcell_area 222136 (59088 um^2) / alloc_area 296000 (78736 um^2).
360 Pin Density = 0.553.
361     = total # of pins 122766 / total Instance area 222136.
362 Checking spec file integrity...
```

$$78961\text{ }\mu\text{m}^2 \approx 78736\text{ }\mu\text{m}^2$$

$$59088.1754\text{ }\mu\text{m}^2 \approx 59088\text{ }\mu\text{m}^2$$

the dimensions do not consistent with the area reported by Design Compiler, but consistent with the alloc-area in

encounter.log. Because there is some black space in the layout, the dimension just show the alloc-areas, but the area report show the stdcell-area.

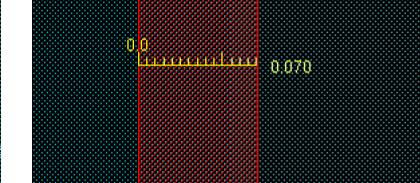
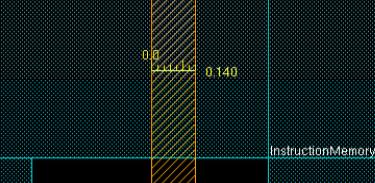


metal10: 0.8

metal6: 0.14

metal4: 0.14

metal2: 0.07



In the module 7-interconnecte.pdf, the picture show this:

1 μm Intel 45 nm metal stack



Layer	<i>t</i> (nm)	<i>w</i> (nm)	<i>s</i> (nm)	pitch (nm)
M9	7 μm	17.5 μm	13 μm	30.5 μm
M8	720	400	410	810
M7	504	280	280	560
M6	324	180	180	360
M5	252	140	140	280
M4	216	120	120	240
M3	144	80	80	160
M2	144	80	80	160
M1	144	80	80	160

Transistors

upper metal will be wider, which match the description in lecture.

$$1\text{ mm} \times 1\text{ mm} = 1000\text{ nm} \times 1000\text{ nm}$$

$$\text{number of tiles} = (1000\text{ nm} \times 1000\text{ nm}) / 78736\text{ }\mu\text{m}^2 \\ \approx 12$$

∴ 12 tiles I can fit

table:

name	dimension (mm)
------	----------------

Via 1 0.07 x 0.07

Via 2 0.07 x 0.07

Via 3 0.07 x 0.07

Via 4 0.14 x 0.14

Via 5 0.14 x 0.14

Via 6 0.14 x 0.14

Via 7 0.4 x 0.4

Via 8 0.4 x 0.4

Via 9 0.8 x 0.8

## step 6:

```
1178 #Complete Detail Routing.
1179 #Total wire length = 711197 um.
1180 #Total half perimeter of net bounding box = 493162 um.
1181 #Total wire length on LAYER metal1 = 8675 um.
1182 #Total wire length on LAYER metal2 = 128859 um.
1183 #Total wire length on LAYER metal3 = 223694 um.
1184 #Total wire length on LAYER metal4 = 111636 um.
1185 #Total wire length on LAYER metal5 = 97521 um.
1186 #Total wire length on LAYER metal6 = 84422 um.
1187 #Total wire length on LAYER metal7 = 25009 um.
1188 #Total wire length on LAYER metal8 = 17236 um.
1189 #Total wire length on LAYER metal9 = 10115 um.
1190 #Total wire length on LAYER metal10 = 4031 um.
1191 #Total number of vias = 301838
1192 #Up-Via Summary (total 301838):
1193 #
1194 #-----#
1195 # Metal 1 123709
1196 # Metal 2 116231
1197 # Metal 3 33755
1198 # Metal 4 13233
1199 # Metal 5 9284
1200 # Metal 6 2999
1201 # Metal 7 1616
1202 # Metal 8 755
1203 # Metal 9 256
1204 #
1205 # 301838
1206 #
```

the number of metal layer is 10, and metal3 have the most routing. I think it is reasonable.

image the uppermost metal is used.

