# ECE668 Final Project Summary_Team2

In this project, our team need design a MIPS processor architecture including Tomasulo algorithm. For the Tomasulo demo, the solution is divide into three parts: Register Status and Value, Reservation Station and Instruction Sets. We complete the printf of register status, register content and time table. But unfortunately, for printing reservation station, the word field need too much new variables to deal with the logic, and the workload will increase too much, so we give up the idea of printing word field of reservation station. And on the other hand, we also do not consider the branch instruction, simply because, the C++ is in order execution, if we add the branch instruction in the program, we need write the new funciton to deal with the new order. We try it and failed.

For the improving part, i think our team could renew the Tomasulo algorithm by adding hardware speculation, which means we can create a reorder buffer and remove the storing buffer. Furtherly, wider CDB is also allowed in order to make the processor support multiple-issue.

In couclusion, our team really ddi not do well because we just complete the basic goal for the Topic but in fact we can go further. Hardware speculation and multi-issue should be considered in the Tomasulo Algorithm but we didn’t do that because the team members were not well coordinated, which wasted too much time. As the coordinator, I should take the main responsibility.