Modification of the Two-Graph Method for Symbolic Analysis of Circuits with Non-Admittance Elements

B.S. Rodanski

University of Technology, Sydney (UTS), Faculty of Engineering
P.O. Box 123, Broadway NSW 2007, Australia
benr@eng.uts.edu.au

ABSTRACT

In its original form, the two-graph method allows only circuit components that are described by a *v-i* relationship of the admittance type (G, C, g_m). In particular, it excludes resistors (expressed as resistance R rather ten conductance G), inductors and current-controlled current sources. Practising circuit designers often prefer to have symbolic analysis results expressed in terms of resistances, current or voltage gains, or other symbols that cannot be represented by admittances. This paper describes a simple modification of the two-graph method that allow symbolic analysis of circuits containing components other than admittances. The two-graph method is extended by introducing new element stamps for all non-admittance components.

Keywords: symbolic circuit analysis, two-graph method, element stamp.

1 INTRODUCTION

Recent advances of symbolic analysis of electronic circuits allow for obtaining (approximate) transfer function formulae even for the large-scale analogue circuits [1, 2]. The method, which is currently considered the most efficient, is the two-graph method of Mayeda and Seshu [3]. In this approach, for a lumped, linear, time-invariant circuit, two graphs are constructed: the voltage graph, G_V, and the current graph, G_I. Both graphs have the same number of vertices and edges, but (for active circuits) have different topology. Each edge is labelled with an admittance term, corresponding to a circuit element. Assuming that the circuit is described by the node admittance matrix (NAM), the determinant of this matrix can be calculated as the sum of signed admittance products of all common spanning trees of G_V and G_I. (A common spanning tree is a set of edges that form spanning trees in both G_V and G_I.) If circuit augmentation is used, important transfer functions can be obtained by appropriate sorting of the terms of NAM's determinant [4]. Of course, the number of spanning trees of a graph associated with a typical industrial-sized analogue circuit (tens of nodes and hundreds of

elements) is astronomical. Thus, the exact symbolic expressions can be obtained (and are meaningful) only for relatively small circuits.

The major advantages of the two-graph method are: there are no term cancellations and efficient techniques exist to generate common spanning trees in decreasing order of magnitude. This is extremely important in approximate symbolic analysis of large analogue electronic circuits, where only a relatively small number of common spanning trees with significant contribution to the solution need to be generated.

However, existing graph-based symbolic techniques are not optimal from the point of view of formula interpretability. As the underlying tree enumeration concept is inherently tied to nodal analysis, these approaches are restricted to circuits with elements represented by admittances. In particular this excludes resistors (expressed as resistance R rather ten conductance G), inductors and current-controlled current sources [5]. Although integrated circuits can be modelled using only capacitors, conductances and voltage-controlled current sources, practising circuit designers often prefer to have symbolic analysis results expressed in terms of symbols that they are more familiar with (like resistance) or symbols that cannot be represented by admittances (like current gain of a BJT, for example). If symbolic circuit analysis is to find wider acceptance in teaching and in the industry, the problem of allowing all element representations in a symbolic formula must be positively addressed in future symbolic simulators[1].

A method well suited to address the above stated problem has been known for decades and is used in almost every numerical circuit simulator. It is the Modified Node Admittance Method (MNAM) [6]. For a certain price - increase of the size of the system matrix - it allows all types of circuit components. Moreover, there is a one-to-one relationship between the MNAM and the two-graph method. The two-graph modified nodal representation, as proposed in [6], is not suitable for symbolic analysis because it may lead to graphs G_V and G_I not having the same number of vertices and edges.

In this paper a MNAM-based two-graph circuit representation is proposed which admits all types of circuit components and is suitable for generating symbolic transfer functions in either exact or approximate forms. There are several ways in which the non-admittance type components can be introduced into the nodal equations. For the purpose of this paper, the well known gyrator transformation will be used.

2 MODIFICATION OF THE TWO-GRAPH FORMULATION

It is well known that every circuit component that does not have an admittance representation (or we do not wish it to appear as an admittance in the formula) can be modelled by a circuit that contains only admittances and voltage-controlled current sources. Consider, for example, an inductor. Its admittance is expressed as $1/sL$, but in most symbolic formulation techniques

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[1]Two known symbolic simulators already have this ability: Analog INSYDES (http://www.itwm.uni-kl.de/as/products/ai/regeval2.html) and SAPWin 3 (http://www.cirlab.unifi.it/Sapwin/index.htm). Analog INSYDES uses matrix-based formulation [5], while the method used in SAPWWin 3 has not been published to date.

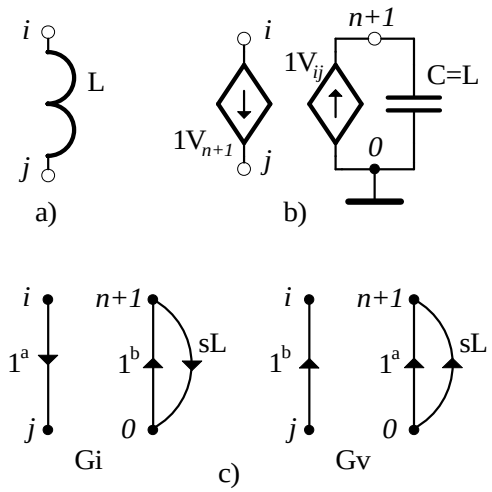


Figure 1: Inductor (a), its model (b) and corresponding two-graph representation (c).

neither terms $1/s$, nor impedances are permitted. To overcome this problem, we can model an inductor with a circuit shown in Fig. 1b, where capacitance C has the same numerical value as the modelled inductance L. Formally replacing the capacitor label '*C*' with the inductor label '*L*' does the trick and in subsequent manipulations we can use symbol sL that in fact represents the admittance of a capacitor. This technique can be generalised to model any impedance Z by an equivalent admittance Y. Furthermore, with the use of coupled unity VCCS's (which represent a circuit component called the unity gyrator), all other circuit elements, including controlled sources, transformers, etc.) can be modelled. Note, that the price we pay for this convenience is the increased circuit complexity.

One problem remains: how to treat the unity transconductances symbolically? Being equal to one, they do not contribute (numerically) to a product of spanning tree admittances, so they can be removed from each product term as soon as a common tree is generated that contain edges corresponding to those transconductances. The only exception is a common spanning tree that consists solely of such unity transconductances. In these cases the tree admittance is represented by the symbol '1'.

In computer implementation of the above technique it is not necessary to label the unity VCCS's in any special way, other than flag them for subsequent removal. For clarity of presentation, however, in this paper the labels '1^aX', '1^bX' will be used, where 'X' is replaced by the label of the modelled component.

Using similar approach, all circuit elements can be modelled and, since admittances and VCCS have the two-graph representations suitable for symbolic analysis, their two-graph element stamps can be obtained. Some of these stamps are presented in Table 1.

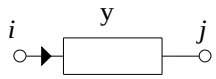
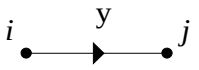
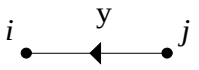
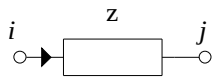
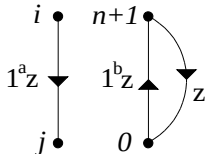
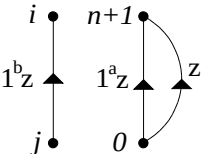
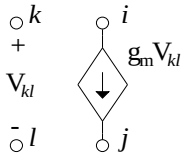
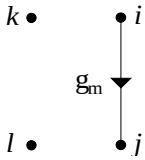
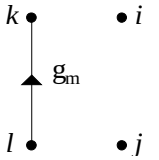
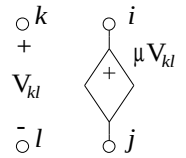
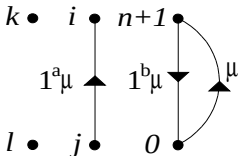
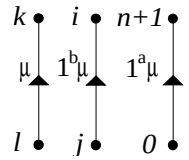
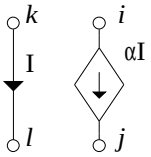
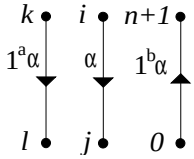
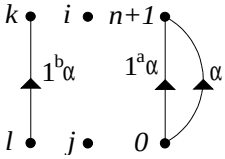
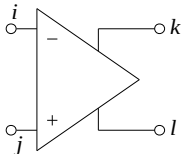
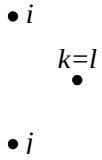
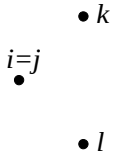
Element	Symbol	Current Graph	Voltage Graph
Admittance *G, sC, Y*			
Impedance *R, sL, Z*			
VCCS			
VCVS			
CCCS			
Nullor (ideal op amp)			

Table 1: Two-graph element stamps for some circuit elements.

3 AN ILLUSTRATIVE EXAMPLE

To illustrate usefulness of the above method to symbolic circuit analysis, consider the following simple example. Fig. 2a shows a small-signal, low-frequency equivalent circuit of a BJT common-emitter amplifier. It is required to find the symbolic expression for the voltage

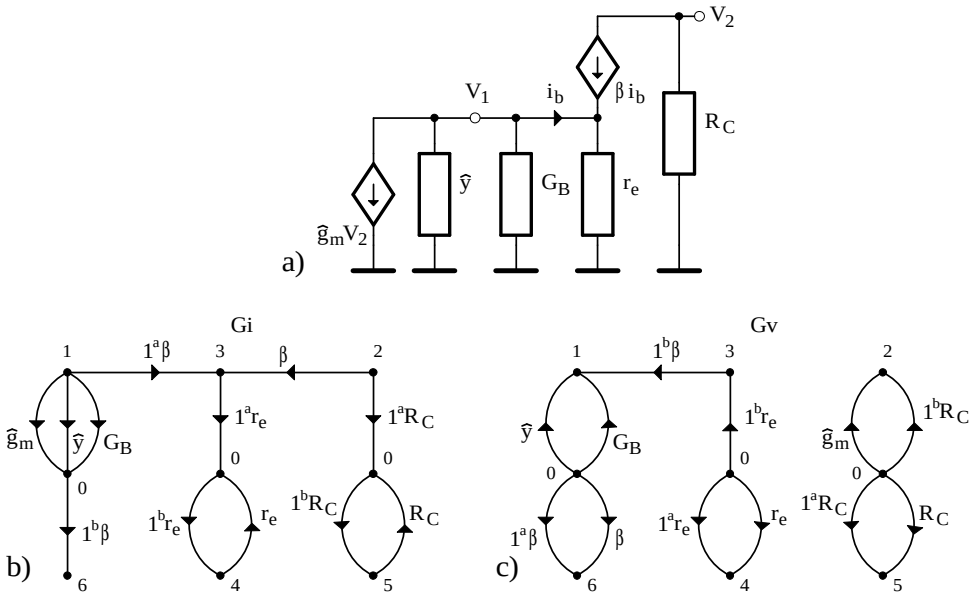


Figure 2: Circuit with resistors and CCCS (a) and its modified current (b) and voltage (c) graphs.

transfer function, $T_v \doteq V_2/V_1$, of this circuit. Of course, for such an elementary circuit the required transfer function can be calculated by hand as $T_v = -\dfrac{\beta}{\beta+1}\dfrac{R_C}{r_e}$. Note that three circuit components: R_C, r_e and the CCCS βi_b, could not be handled by the standard two-graph approach.

Analysis is performed on a circuit augmented with an admittance $\hat{y}$ and a VCCS $\hat{g}_m V_2$. This augmentation allows simultaneous calculation of the determinant of the MNAM of the original circuit as well as two of its cofactors, required for the transfer functions [4].

Using the element stamps from Table 1, the current and voltage graphs are constructed, as shown in Fig. 2b and 2c, respectively. These graphs have only six common trees, which are listed below with appropriate signs:

+, $1^a\beta$, 1^aR_C, 1^ar_e, $1^b\beta$, 1^bR_C, 1^br_e
+, $1^a\beta$, 1^aR_C, $1^b\beta$, 1^bR_C, r_e, $\hat{y}$
+, $1^a\beta$, 1^aR_C, $1^b\beta$, 1^bR_C, r_e, G_B
+, 1^aR_C, $1^b\beta$, 1^bR_C, β, r_e, $\hat{y}$
+, 1^aR_C, $1^b\beta$, 1^bR_C, β, r_e, G_B
-, 1^ar_e, $1^b\beta$, 1^br_e, β, $\hat{g}_m$, R_C

Removing terms 1^aX and 1^bX from the common trees and sorting the product terms with respect to symbols $\hat{y}$ and $\hat{g}_m$, we can write the determinant of the MNAM of the augmented circuit as $\Delta' = \Delta + \hat{y}\Delta_{11} + \hat{g}_m\Delta_{12} = 1 + G_B r_e + \beta G_B r_e + \hat{y}(r_e + \beta r_e) - \hat{g}_m \beta R_C$. Now, the required

transfer function can be obtained as a ratio of two cofactors: $T_v = \frac{\Delta_{12}}{\Delta_{11}} = \frac{-\beta R_C}{r_e + \beta r_e}$ $= -\frac{\beta}{\beta + 1}\frac{R_C}{r_e}$.

It can be easily confirmed that other transfer functions, namely: $Z_{in} = \frac{\Delta_{11}}{\Delta}$ and $R_T = \frac{\Delta_{12}}{\Delta}$, are also calculated correctly using the proposed modification of the two-graph method.

4 CONCLUSION

Existing graph-based symbolic circuit analysis techniques are not optimal from the point of view of formula interpretability. The two-graph method of Mayeda and Seshu is currently considered the most efficient, especially for generating approximate symbolic formulae. The original method is restricted to circuits containing components that can be described by admittance relationships (G, C, g_m). Users often require symbolic solutions in terms of familiar circuit variables (like resistances) and other non-admittance parameters (voltage and current gains, for instance). This paper suggests a simple modification to the standard two-graph method that solves this problem by introducing new two-graph representations (element stamps) for non-admittance components. The new element stamps are based on using a unity gyrator to model those components. Because the unity transconductances are removed from the terms as soon as they are generated, the final expression contains only symbols from the original circuit. In addition, since the unity transconductance does not contribute numerically to the tree admittance product, the modified method is suitable for generating approximate symbolic expressions.

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