Chapter 1

Class F Amplifier ADS Simulations, Comparisons to Specs

The initial goal of the class F amplifier design was to try and control up the fifth harmonic which would ideally allow 90.5% drain efficiency and to have a center frequency of 5 GHz. After looking through the past amplifier competitions and looking at various RF transistor manufacturers, the Wolfspeed CGHV1F006S GaN HEMT transistor was chosen. This model was chosen over others to the relatively new release of the transistor, the high operating frequency of the transistor (18 GHz), and the fact that the transistor came in a QFP package versus a semiconductor die. The majority of past winners of the amplifier competition used Cree (now Wolfspeed) transistors and Wolfspeed provides a transistor level models for the amplifier for accurate simulations to design amplifiers. The design goals are in Table 1.1, the initial goals were relatively aggressive in trying to push the PAE and center frequency for the highest figure of merit. After simulating, fabricating, and testing multiple versions the design goals were set to a more conservative value. This chapter discusses the simulations results of the final version of the amplifier.

The initial design was pushing the limits of the specification by attempting to achieve the minimum output power with the highest allowed input power. This was risky because designing for the minimum gain allows for little margin for non-ideal

Table 1.1: Design Goals of Amplifier

Parameter	Initial Goal	Final Goal
Center Frequency, GHz	5	3
PAE, %	80	70
Gain, dB	15	22

factors that couldn't be taken into account of the simulation. The first amplifier that I fabricated had a simulated gain of X with a PAE of Y at an input power of Z dBm. The amplifier initially had a short from the drain and explain more. Once the amplifier was working the measured gain was only A so even at the maximum allowed input power of 24 dBm, it would not be able to deliver 36 dBm of power. For the final version of the amplifier, the design margins were increased substantially so stuff could happen better.

1.1 DC Bias Point

The simulation of the various parts of the class F amplifier was done using Keysight ADS 2016. The first step in the simulation process was determining the optimal DC bias. Using the provided transistor model from Wolfspeed, various drain and gate voltages were simulated to see what the drain current and transducer gain CHECK THIS STATEMENT the transistor would have using the circuit seen in Figure 1.1. The bias for the class F amplifier should be in the "deep" AB region so the drain current resembles a half sinusoid shape but still allows for the negative third harmonic to be present. The drain current should be minimized in order to maximize the PAE of the amplifier. The competition rule states the amplifier should have a minimum of 36 dBm output power at a maximum of 24 dBm input power resulting in a minimum gain of 12 dBm. For the final amplifier, the target gain was 22 dB so there would be a margin for various effects that wouldn't be able to be taken into account in the simulation like the fabrication process. The transistor maximum operating ratings can be seen in Table 1.2.

Table 1.2: Maximum Operating Parameters of CGHV1F006S Transistor

Parameter	Rating
Maximum Drain-Source Voltage, V	100
Maximum Drain-Source Current, A	0.95
Maximum Gate-Source Voltage, V	-10,+2
Maximum Gate-Source Current, mA	1.2

A starting point to select the gate voltage is to choose a value so the drain current is 10% of the maximum current so the conduction cycle is close to π. The final version of the amplifier had a gate source voltage of -2.4 V which in Figure (Ids vs Vds) figure is in the "deep AB" region of the device as shown in Figure 1.2 and draws only 80 mA of quiescent current. The drain-source voltage was chosen to be 40 V because it's the recommended operating voltage from the datasheet for the transistor. After the gate voltage was selected, the stability factor (k) and the stability measurement (Δ) were then simulated to see what the stability of the amplifier is near the center frequency seen in Figures 1.3 and 1.4 respectively. For an amplifier to be unconditionally stable, k must be greater than one and Δ be positive CITE NEEDED, and because k is less than one the amplifier has potentially unstable regions. The stability regions of the load and source plane were then simulated to determine a starting point for the load and source pulls. The results of the load and source stability regions can be seen in Figures 1.5 and 1.6. The region of stability for both stability circles is outside the circle.

1.2 Talk about fundamental load and source pull

After determining the DC bias of the amplifier, fundamental load and source pulls are done to determine the optimal load and source impedances for the transistor. Load pulls are done keeping the source impedance fixed and sweeping the load over a uniformly sampled space on the Smith Chart to then measuring the transducer gain. Various drain efficiency and gain contours can be produced by doing load pulls. The

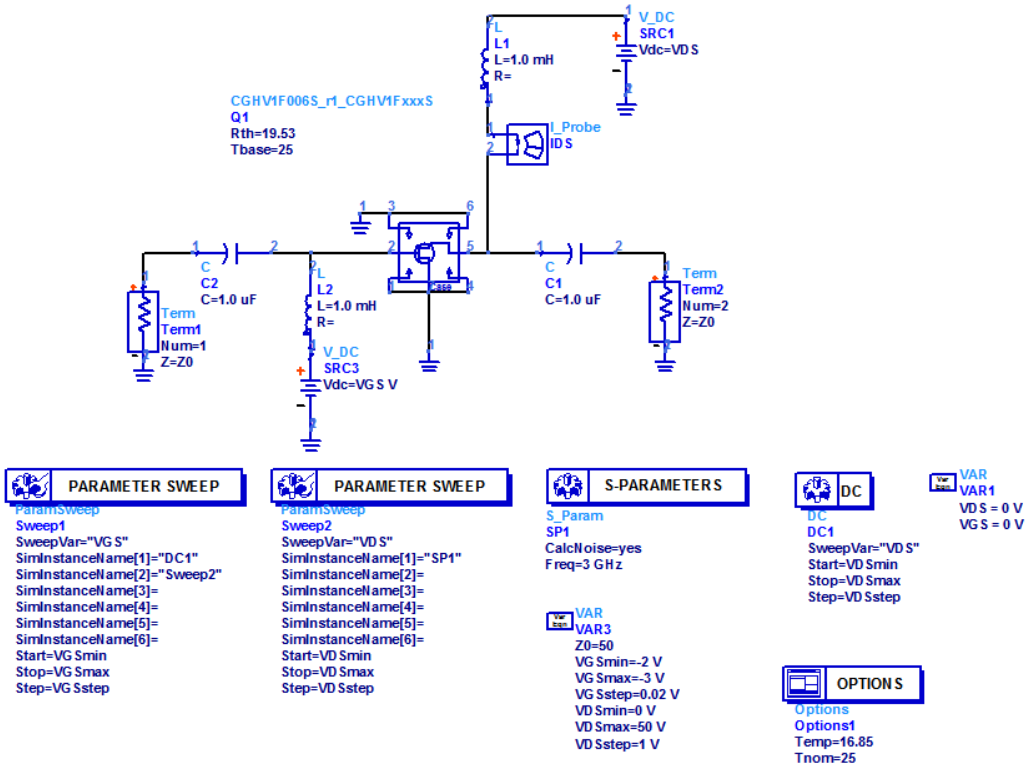

Figure 1.1: Bias Circuit Setup

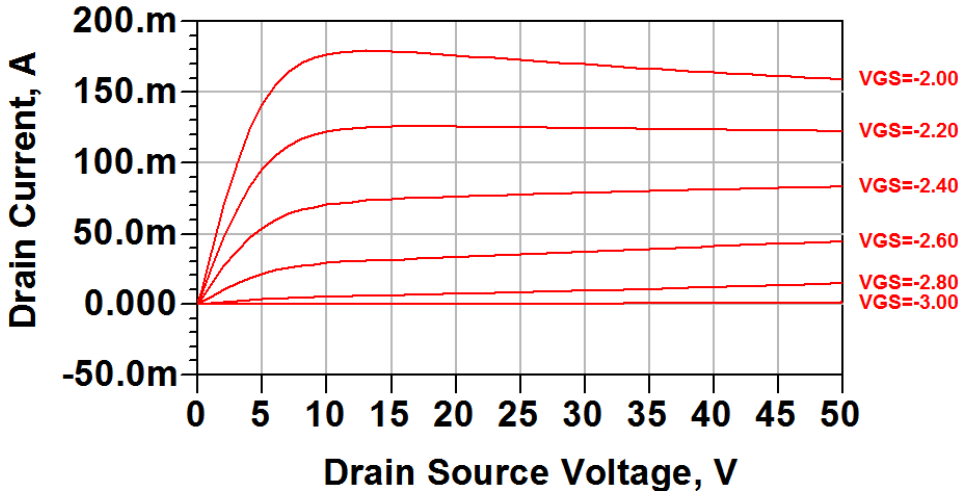

Figure 1.2: Drain Current versus Drain Voltage for Various Gate Voltages

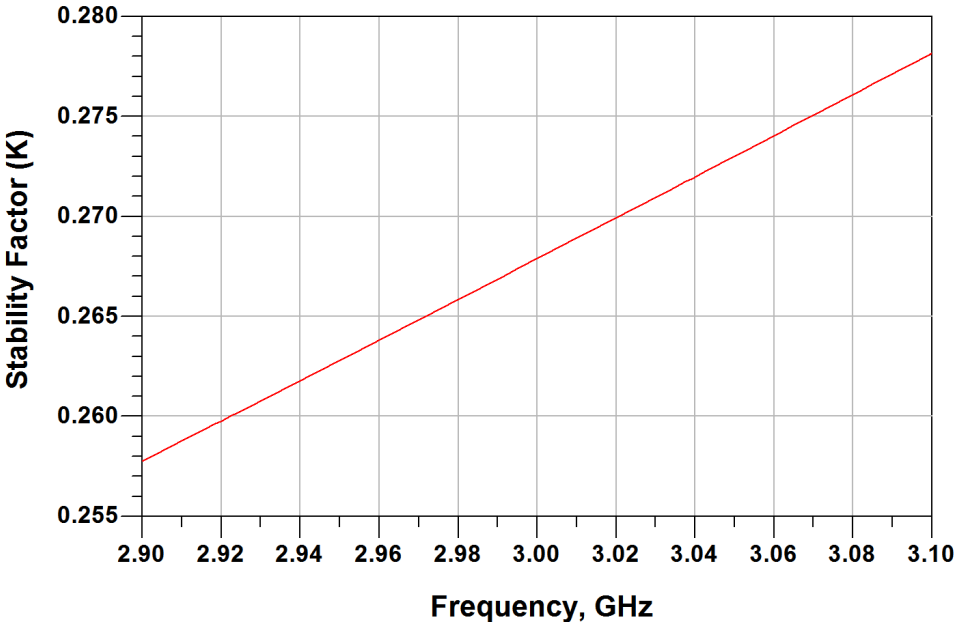

Figure 1.3: Stability Factor (k) versus Frequency

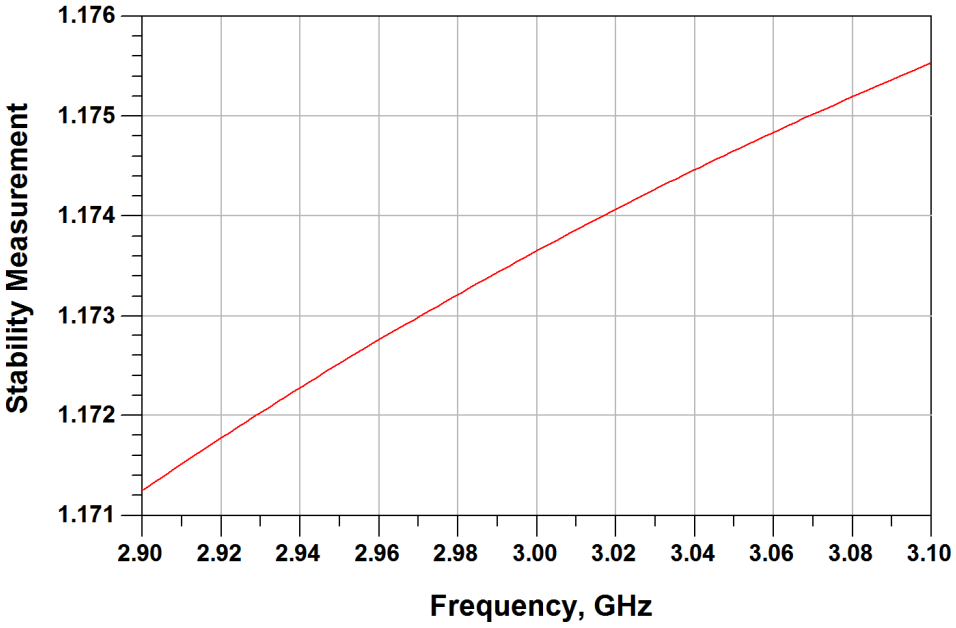

Figure 1.4: Stability Measure (Δ) versus Frequency

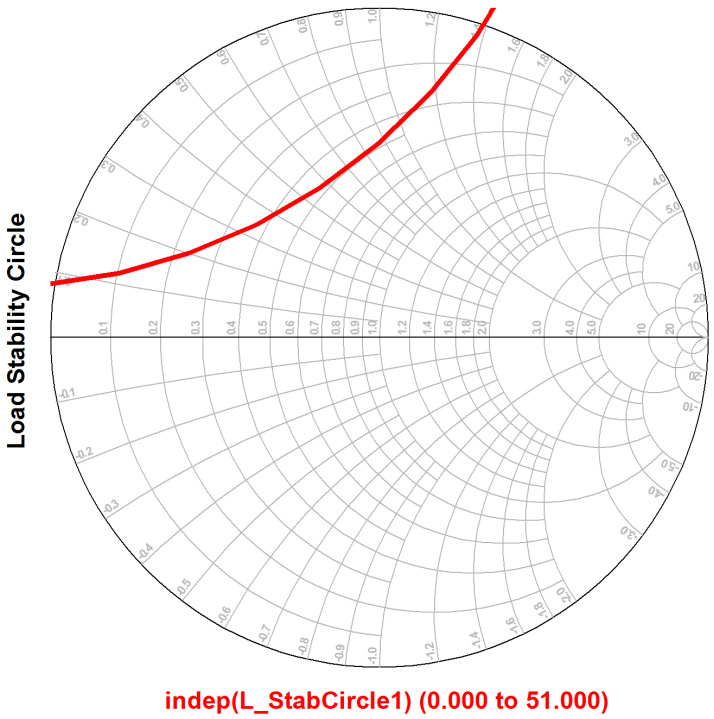

Figure 1.5: Load Stability Circle of Transistor. Stable Region Outside of Circle

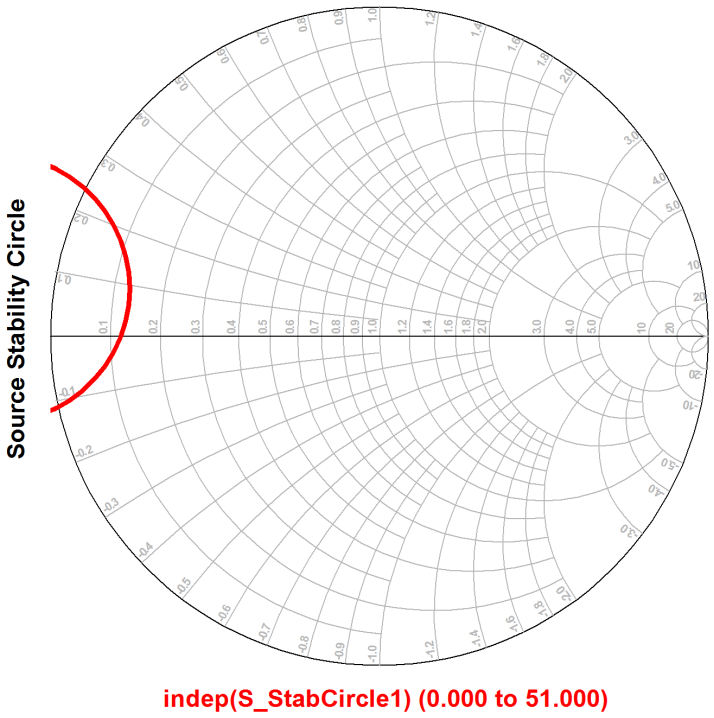

Figure 1.6: Source Stability Circle of Transistor. Stable Region Outside of Circle

typical process starts with sampling the entire Smith Chart then load pulling again around the region with the highest efficiency contour. As a starting point the source impedance was set to a low impedance of 10Ω but still outside of the source stability circle. Source pulling is done after load pulling and follows a similar process by keeping the load impedance fixed then sweeping the source impedance for the highest efficiency while still having the target gain. The load and source pulls are done at the fundamental frequency at an input power of 15 dBm to provide an additional margin in the design. In practice the amplifier the amplifier will require a higher input power to achieve the simulation results due to losses that could not be simulated in ADS FLESH OUT. Also the source and load impedances for the higher harmonics are shorted.

For the sake of brevity only the final load and source pull results are shown but the process will be described. The initial load pull results showing PAE and power delivered contours can be seen in Figure 1.7 and 1.8. The highest power delivered is only 35.45 dBm at a drain efficiency of 35% while the highest PAE 40% results in a power delivered of 35.2 dBm. The PAE should be less than 50% because an amplifier with only the fundamental present is a class A amplifier with a maximum efficiency of 50%. As more harmonics are properly added the power delivered and PAE should increase. The final fundamental load impedance selected from the simulation results was 14.3+j54 Ω.

The next step is the source pull done with the load set to the impedance discussed earlier. The results of the source pull can be seen in Figures 1.9 and 1.10. The maximum PAE and power delivered has dropped but this isn't unexpected. The pulling process is iterative and if another load pull was done using a new source impedance, one would see the PAE and power delivered increase from the first load pull. Multiple iterations are required to fine tune the parameters because they are dependent on one another. A fundamental source impedance of 3+j3 Ω was chosen for the final amplifier configuration as a compromise between high PAE while still delivering over 36 dBm of power.

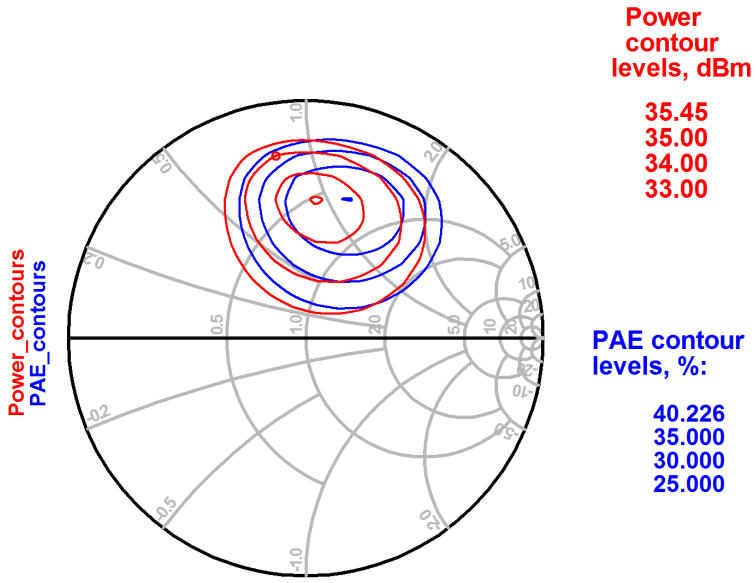

Figure 1.7: Smith Chart Load Pull Simulation Results at 3 GHz with PAE and Power Delivered Contours

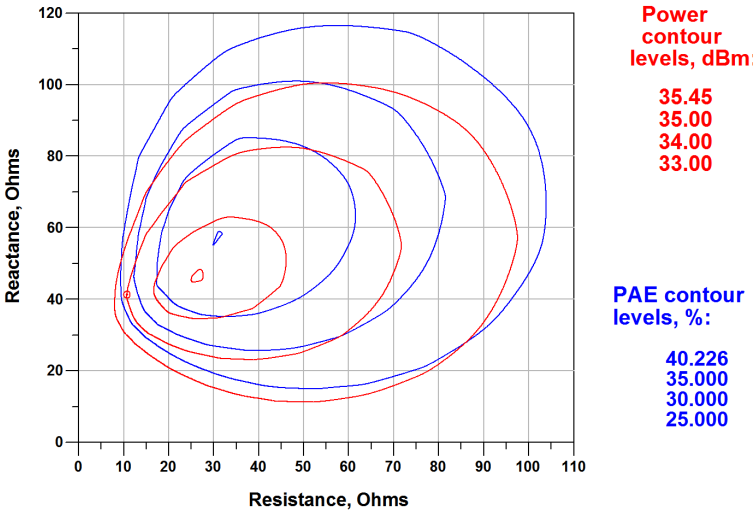

Figure 1.8: Don't know how to title this

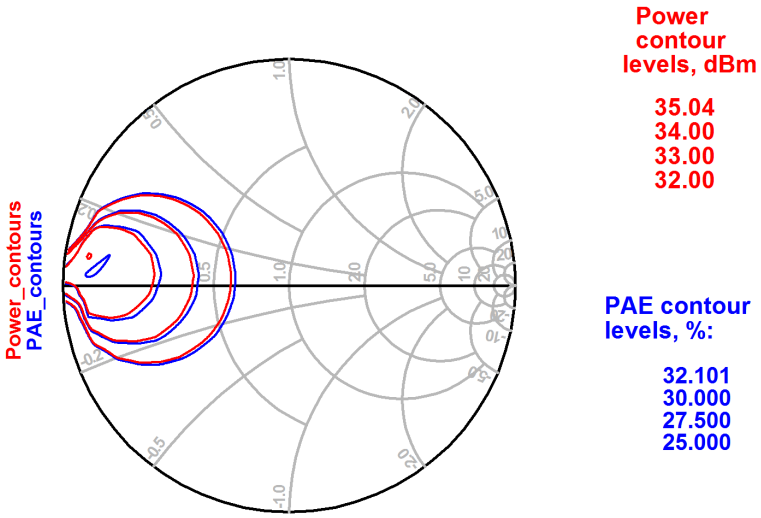

Figure 1.9: Smith Chart Source Pull Simulation Results at 3 GHz with PAE and Power Delivered Contours

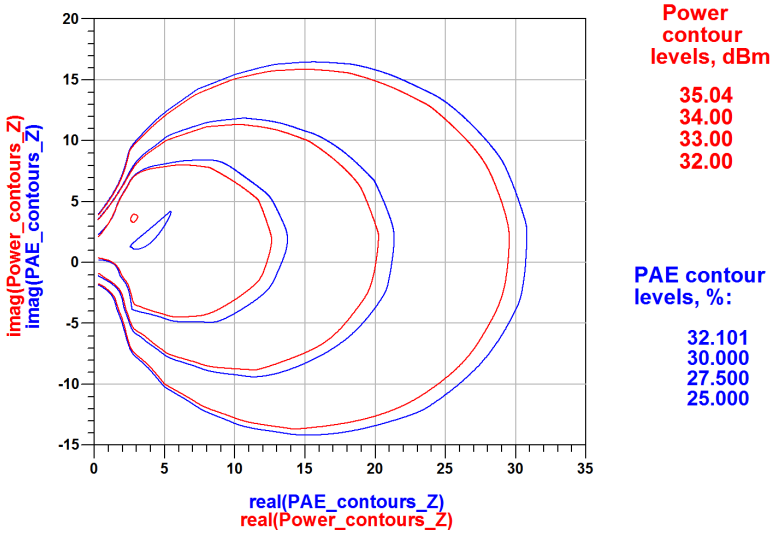

Figure 1.10: Don't know how to title this

Table 1.3: Final Harmonic Impedances for Amplifier

Frequency, GHz	Load Impedance, Ω	Source Impedance, Ω
3	14.3+j54.0	3+j3
6	1.4+j37.0	3-j55
9	0.3+j13.4	0.5-j2.6

1.3 Harmonic Pulls

The load and source pulls are done at the fundamental frequency while the harmonic pulls are done at the higher harmonics. The process starts with the second harmonic load pull with the fundamental load and source impedances set to the values determined in the previous section. The source impedance at the second harmonic and all the higher harmonic impedances are set to 0 Ω. After determining the optimal load for maximum PAE while still delivering enough output power, a source pull is done at the second harmonic with the optimal load. This process is then repeated for at the third harmonic. After all of the load and source pulls, one last load pull is done at the fundamental to confirm an the increase of PAE and power delivered. The final fundamental load pull can be seen in Figure 1.11 and 1.12. At the highest power delivered of 38.9 dBm the PAE is 69% while at the highest PAE of 79% the output delivered is 36.9 dBm.

A table of the load and source impedances used for the final amplifier configuration can be seen in Table 1.3. The final amplifier had an output power of 37 dBm with 22 dB of gain and a PAE of 79.25% resulting in a figure of merit of 104. While the figure of merit is not the highest compared to the past winners, it is still competitive. The drain efficiency of the final amplifier is 79.2% which is close to the theoretical maximum of 81.7%. The source and load impedances are used to design matching networks, this sentence is terrible. The simulated harmonic pulls are used to determine the maximum theoretical performance that can be extracted from the transistor.

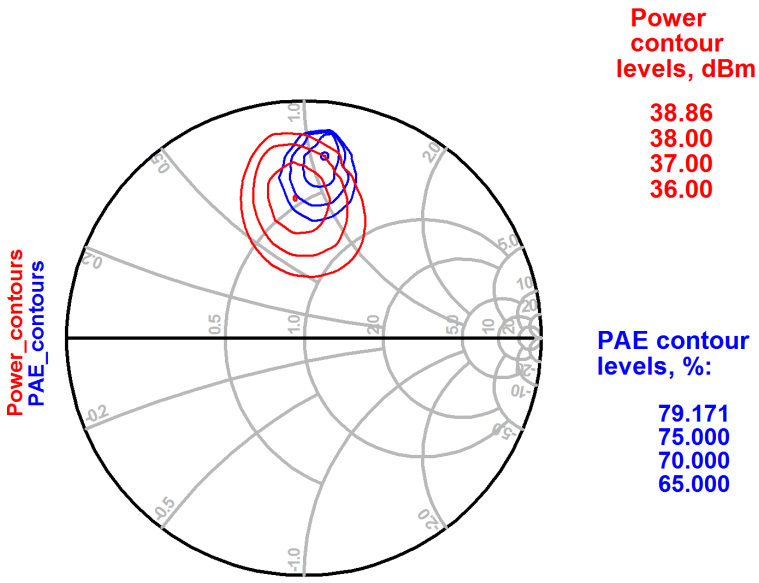

Figure 1.11: Final Fundamental Load Pull on Smith Chart

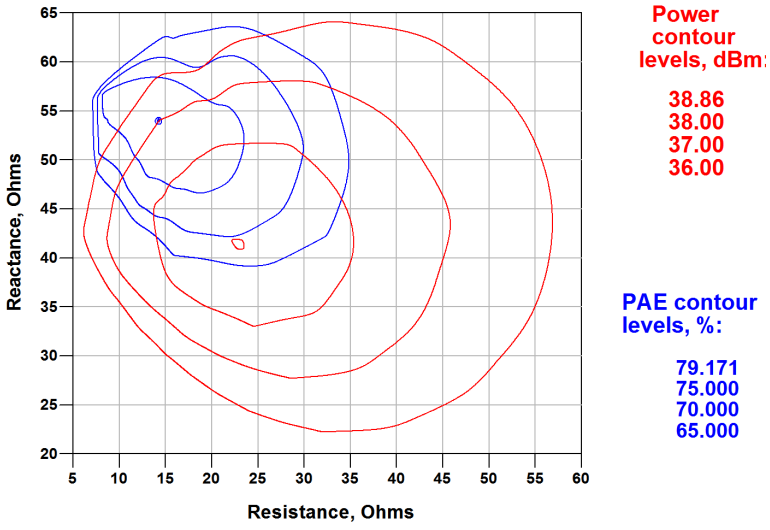

Figure 1.12: Final Fundamental Load Pull Fix This Label

1.4 Harmonic matching network

The harmonic matching network is the key in keeping the proper harmonics at the drain. It is composed of a matching network and a wave shaping network that is on the load and source side of the transistor. The wave shaping network consists of a series section that is a quarter wavelength long with an eight wavelength open shunt stub. An additional series element is added that is used for tuning that goes to a two more stubs that used for the second harmonic and bias circuitry seen in Figure 1.13. Most class F wave shaping network follow a similar pattern of various fractional wavelength sections so the drain is properly terminated. The downside of these networks is the relatively large electrical lengths due to the presence of a quarter wavelength sections in nearly all such networks. This design explores if coupling the open circuit shunt stubs in the wave shaping network can decrease the electrical size of the class F amplifier. Two versions of the amplifier were simulated, one that uses coupled microstrip lines and one without to compare the overall electrical size of the amplifier.

After the wave shaping network comes the matching network so the amplifier is matched as close as possible to 50Ω. This amplifier used a shunt stub and a series transmission line for the matching network on the load and source side.

Need to do two tone tests and stability tests for the amplifier! More content!

1.5 Talk about simulated amplifier

The transmission lines were simulated using Rogers INSERT NUMBER HERE. After comparing various low loss laminates like Duroid, the Rogers NUMBER HERE was selected. This was partially due to the larger sample size that could be ordered so more amplifier boards could be fabricated. Also it has the lowest tangent loss and relative permittivity that allowed the transmission lines going to the transistor gate and drain to be thin enough. Reword all of this later man. All of the amplifier dimensions were set as parameters with goals to maximize the PAE with a minimum set gain at a fixed RF input power and the optimizer was used to tune the amplifier

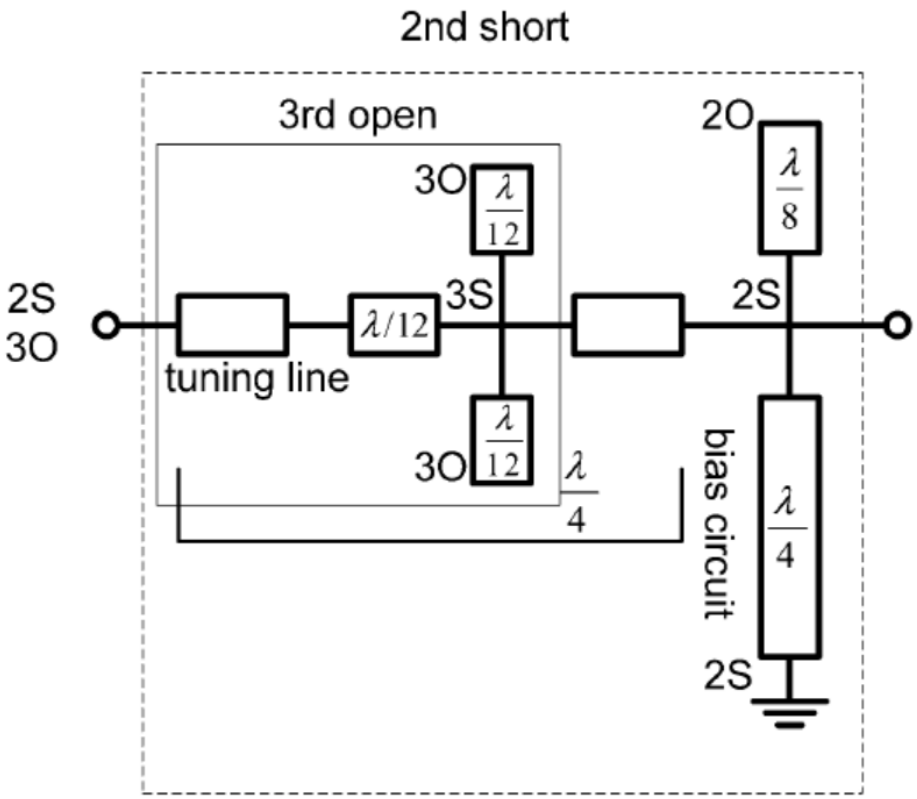

Figure 1.13: Matching Network for Amplifier

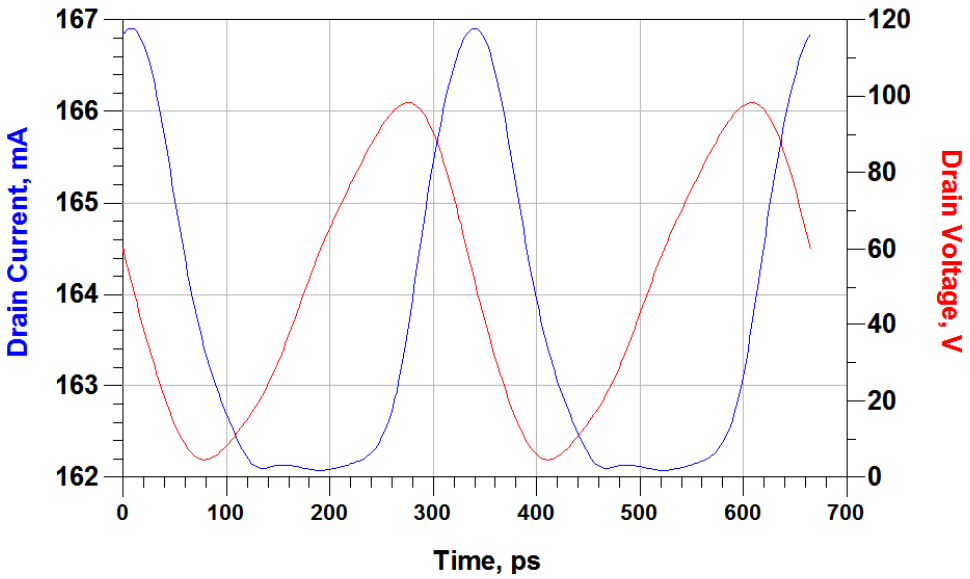

Figure 1.14: Simulated Drain Current and Voltage Versus Time

dimensions. The board discussed in this section is the third revision. The previous two amplifiers were malfunctioned with one acting as an oscillator and the other not working at all. This was most likely due to fabrication issues.

The simulated drain current and voltage waveforms can be seen in Figure 1.14 which show some partial overlap. Although the waveforms aren't ideal, the amplifier still has high PAE and meets the minimum output power. Even during the off cycle of the drain current, there is still quiescent current flowing which dissipates significant power due to the high drain voltage.

VSWR plots

Gain vs frequency and input power

PAE and Gain vs input power

power out vs power in

Table of simulated amplifier measurements

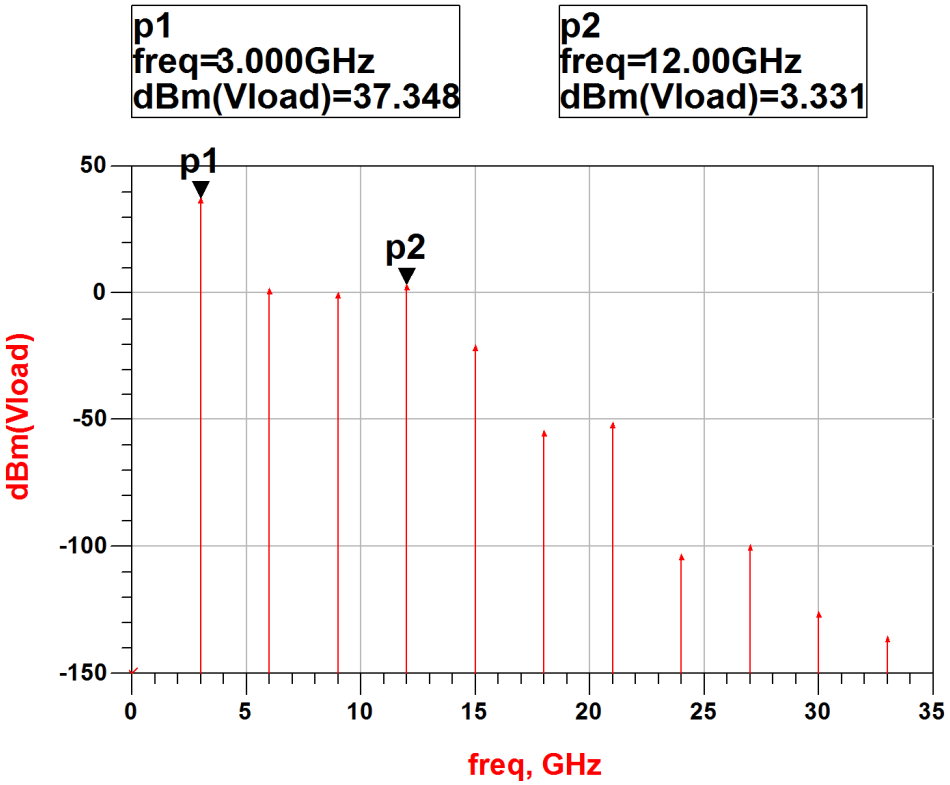

Figure 1.15: Simulated Single Tone IMD

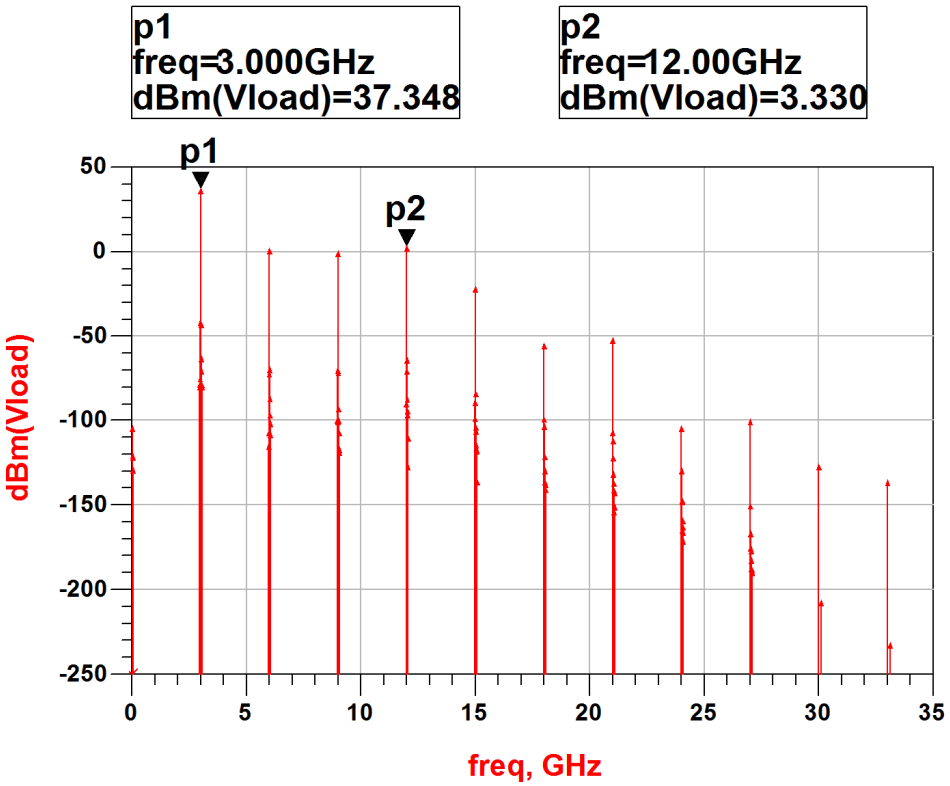

Figure 1.16: Simulated Two Tone IMD with 10 MHz Offset

Bibliography

[1] Y. Y. Woo, Y. Yang, and B. Kim. Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 54(5):1969–1973, 2006.