Chapter 1

Abstract and IEEE Design Competition Rules

This thesis talks about the design and implementation of a class F amplifier for the International Microwave Symposium (IMS) 2016 High Efficiency Power Amplifier Student Design competition. The competition focuses on maximizing the power added efficiency (PAE) and operating frequency of the amplifier over a wide range of input powers. Power added efficiency is defined as the difference of output RF power and RF input power over the DC bias power seen in Equation 1.1. PAE is an important metric for power amplifiers to show how efficient the amplifier is converting the DC power into RF power.

$$PAE, \% = \frac{RF\ Power_{out} - RFPower_{in}}{DC\ Power} \tag{1.1}$$

To qualify for the design competition the amplifier must output at least 36 dBm (4 Watts) with less than 24 dBm input power for a single carrier and less than 22 dBm per tone for two carriers spaced 5 MHz apart. Also the amplifier must have a carrier-to-intermodulation ratio (C/I), defined as the ratio in dB between the amplitude of either carrier and highest intermodulation product, greater than 30 dB at an input power of 0 dBm.

The rules for the amplifier require the amplifier have a center frequency between 1 GHz and 10 GHz. The RF ports should use SMA female connectors, and the bias connections should use banana plugs with a maximum of two DC supply voltages. The source and load impedance of your amplifier should be matched to 50 Ω. The amplifier can use any technology but must be the result of new design and fabrication methods. The amplifier PAE will be measured with at the first RF output power when the C/I ratio drops below 30 dB. The winning amplifier will have the highest figure of merit seen in Equation 1.2.

$$Figure of Merit = PAE * (Center Frequency, GHz)^{0.25} \tag{1.2}$$

A table of past competition winners can be seen in Table X. The highest scores in the competition have all been from class F amplifiers with a center frequency around 3 GHz CHECK THIS STATEMENT. The class F amplifier was chosen for the design due to highest PAE compared to other amplifier classes. This thesis explores coupling the harmonic matching networks to reduce the electrical size of the amplifier using a gallium nitride (GaN) high electron mobility (HEMT) transistor from Wolfspeed.

Class f because ideally highest efficiency over other operating classes. Challenge was keeping C/I ratio at 30 dB at high input powers

Insert past contest winners table and their score? It would be content and give context

Chapter 2

Amplifier Classes

The generic power amplifier consists of a transistor with a DC bias and AC coupled to the RF input and output ports. For the sake of simplicity this thesis will describe the operation of FET amplifiers. The major source of power consumption of an amplifier comes from the drain source current and voltage that occurs during operation. Power amplifiers come in a variety of classes, and the most commonly used ones are A, B, AB, C, D, E, and F. Classes A through C can be described by the conduction angle of the device and modeling the transistor as a current source. The conduction angle is the amount of current flowing through the transistor from drain to source during a single cycle of the AC signal being amplified ranging from 0 to 2π [4]. Classes D through F are defined as switching amplifiers and vary due to the output matching network which shape the waveforms of the current and voltage at the drain of the device [30]. This chapter will describe a high level overview of the various amplifier classes and discuss the limitations of each in practice.

2.1 Efficiency of Amplifiers

To reduce the power consumption of a power amplifiers, two major concepts are important: zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS). ZVS is when there is zero voltage when the amplifier is switched on and

conducting so while current flows through the output no power is consumed. ZVDS is when there is no overlap between the voltage and current waveforms so no power is consumed during switching. If an amplifier can achieve ZVS and ZVDS it would theoretically be 100% efficient. A measure of amplifier efficiency is the power added efficiency (PAE) defined in equation 2.1. PAE is a measure of how efficient an amplifier is able to convert the input DC power into RF power gain. Ideally all of the DC power used to power the amplifier would be used to increase the input RF power. The maximum limit for a lossless system is 100%, for example if a power amplifier consumed 1 Watt and was able to output 1.001 Watt of RF power from 1 mW of RF input power, the PAE would be 100.% because all of the DC power was used to increase the RF power.

$$PAE, \% = \frac{RF\ Power_{out} - RFPower_{in}}{DC\ Power} \tag{2.1}$$

Another measure of amplifier efficiency is the drain efficiency which is the proportion of the output power of the fundamental harmonic over the DC power consumed seen in Equation 2.2. The drain efficiency is typically used when talking about the theory behind the different amplifier classes. In practice, PAE is used as the metric to compare power amplifier efficiency because it takes in account RF input power which is relatively large compared to small signal amplifiers.

$$\eta, \% = \frac{P_{Fundamental}}{DC\ Power} \tag{2.2}$$

2.2 Current Source Amplifiers

2.2.1 Class A Amplifier

The class A amplifier uses a bias that results in a conduction angle of 2π, seen in Figure 2.1, and a theoretical quiescent current of 50% the maximum drain current. This results in power always being consumed due to the constant bias current and voltage present at the drain of the amplifier. The bias point is chosen so the transistor

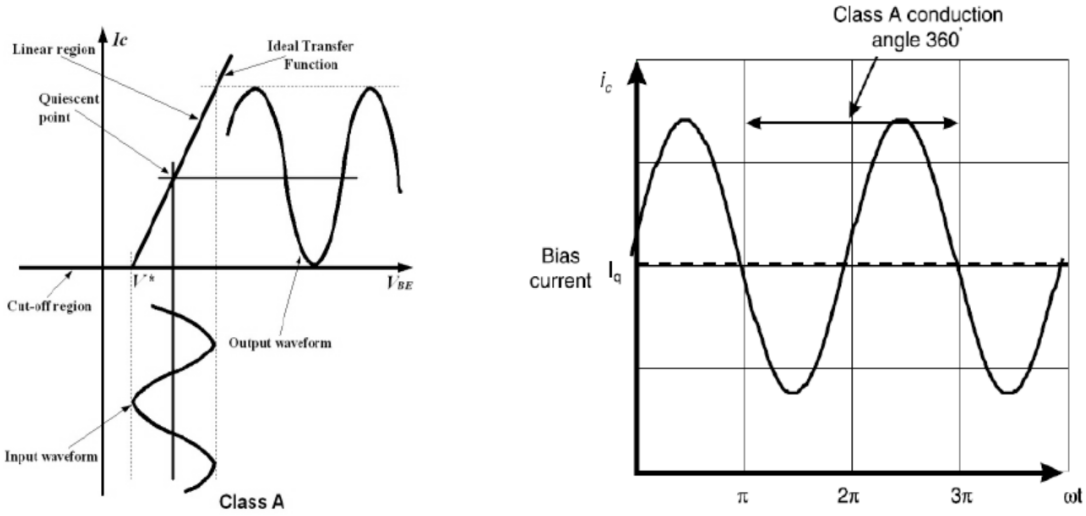

Figure 2.1: Class A Bias Point and Conduction Cycle [28]

operates in the active region which can be seen in Figure 2.1. The constant power consumption limits the maximum efficiency of the class A amplifier for a continuous wave (CW) signal to 50% [1].

The class A amplifier is the most linear of all classes due to the conduction angle that provides ideally no clipping of the current or voltage waveforms. The high linearity allows the class A amplifier to have the lowest intermodulation distortion (IMD) of all the amplifier classes. The downside of the linearity is that the input drive level is proportional to the IMD present at the output of the amplifier. Class A amplifiers are also able to operate closer to the highest operating frequency of a transistor due to lack of harmonics present in the amplifier [28].

2.2.2 Class B Amplifier

Class B uses a conduction angle of π resulting in a half sinusoid waveform for the drain current seen in Figure 2.2 with a theoretical quiescent current of 0 A. The maximum efficiency for a CW signal is 78.5%. The reduced conduction angle causes the required input power to achieve the maximum efficiency to be 6 dB higher compared to the class A amplifier [1]. The drain current is proportional to the input

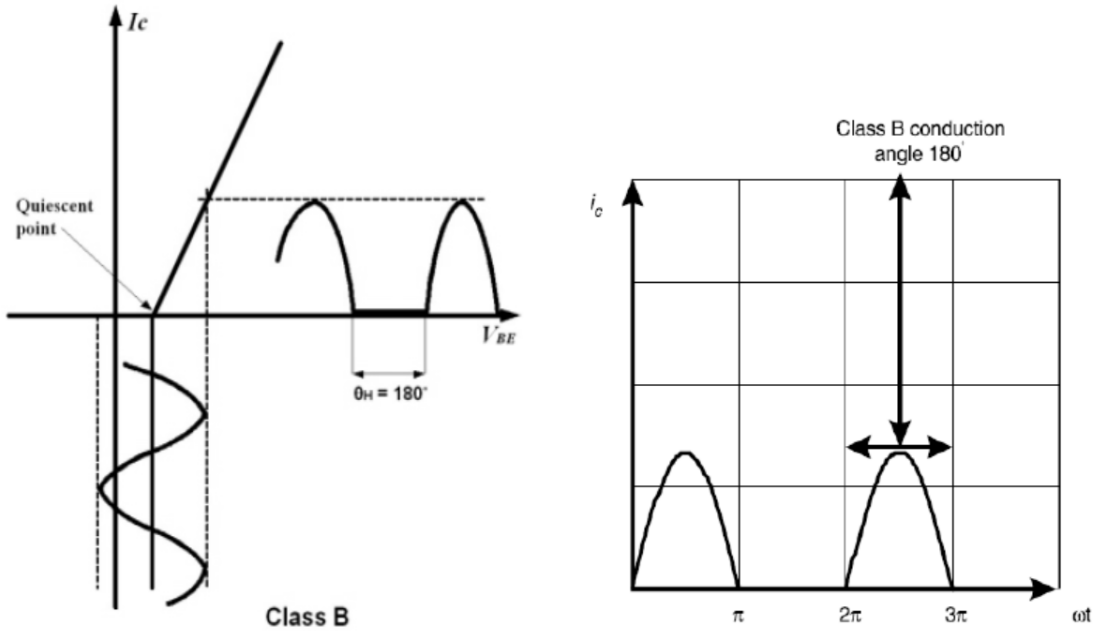

Figure 2.2: Class B Bias Point and Conduction Cycle [28]

signal so the Class B amplifier is considered a linear amplifier but will result in harmonic distortion due to the clipping of the drain current. The output is usually filtered to reduce the harmonic distortion[25]. In most applications, the class B amplifier is used in a push pull configuration to reduce distortion by providing a full sine wave output and maintain greater efficiency than a class A amplifier. Also instead of setting the quiescent current to 0, the drain current is typically set to 10% of the max drain current of the transistor to reduce the harmonic distortion. An interesting result of the push pull configuration is that even harmonics subtract one another out while odd harmonics add together [28]

2.2.3 Class AB Amplifier

The class AB amplifier uses a conduction angle ranging between π and 2π and is a compromise between class A and class B amplifiers. The drain efficiency lies between 50% and 78.5% with approximately the same output power as the class A amplifier [1]. The bias point and conduction cycle can be seen in Figure 2.3. The class AB amplifier offers a wider dynamic range than class A or class B because the conduction

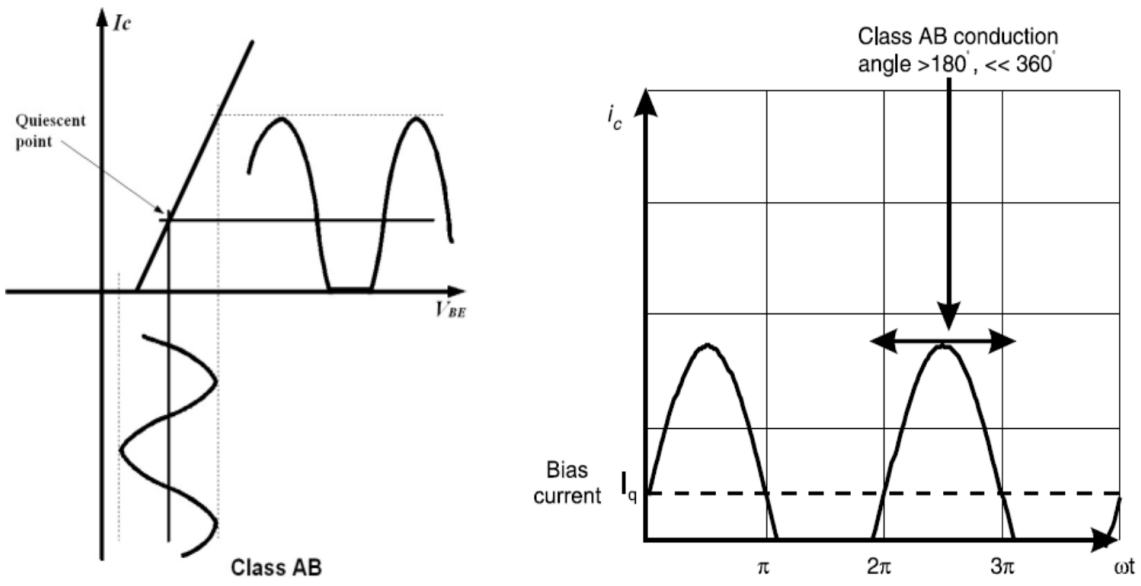

Figure 2.3: Class AB Bias Point and Conduction Cycle [28]

angle is proportional to the drain current which also results in the class AB amplifier being a non-linear amplifier [1].

2.2.4 Class C Amplifier

The class C amplifiers is biased such that the quiescent current is 0 A and the conduction angle is between 0 and π seen in Figure 2.4. The class C amplifier is non-linear with a higher efficiency than class B with a maximum drain efficiency of 100% at zero conduction angle but will have zero gain. In practice, the class C amplifier has a conduction angle slightly less than π for a maximum efficiency of 85% while still having a useful gain [25]. The class C has the highest harmonic distortion of all the current source amplifier classes which will be shown in the following section. The harmonic distortion requires significant filtering at the output of the amplifier. Class C amplifiers aren't typically used for microwave power amplifiers due to the large negative voltage present at the gate of the transistor which can cause reverse breakdown in the transistor [1]. In summary the class C amplifier offers a tradeoff of higher efficiency but with higher harmonic distortion and lower output power level compared to the other current source amplifier classes.

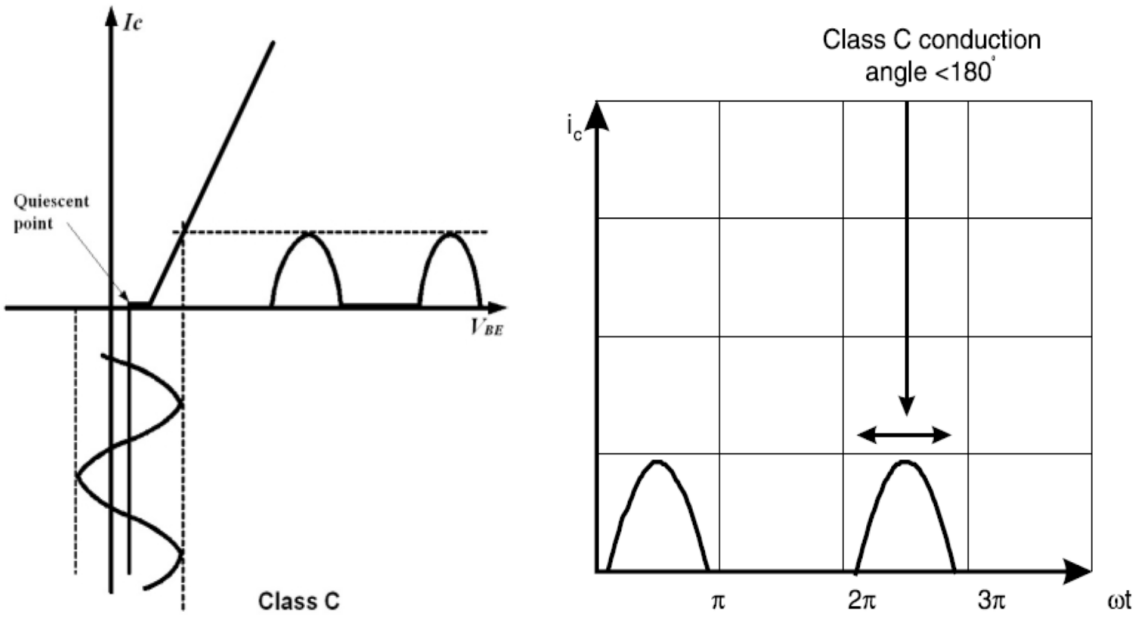

Figure 2.4: Class C Bias Point and Conduction Cycle [28]

2.2.5 Harmonic Distortion

The current source power amplifiers can be generalized to a power amplifier with various conduction angle and the drain efficiency, output power, and harmonic distortion can be described as a function of conduction angle seen in Equations 2.3, 2.4, and 2.5 [8]. Table 2.1 defines the various parameters to the various equations. Figure 2.5 shows the normalized output current harmonics versus conduction angle. At a conduction angle of 2π, the output has minimal harmonic distortion with only the fundamental and DC component present. The DC component is easily removed by coupling capacitor. As conduction angle increase, so does the harmonic amplitude which causes increased harmonic distortion and the DC power is reduced increasing the efficiency. At zero conduction angle, the transistor won't conduct any current and all of the harmonic amplitudes drop to 0. Figure 2.6 shows the RF power relative to class A and efficiency versus conduction angle assuming the harmonics are removed and the transistor is optimally loaded. A power amplifier is said to be properly loaded if the load resistance is equal to the DC drain voltage minus the knee voltage of the transistor divided by the fundamental drain current, see Equation 2.6 [8].

Table 2.1: Table of Current Source Waveform Parameters

Parameter	Definition	Units
I_m	Maximum drain current of transistor	A
I_n	Magnitude of current harmonic n	A
v_{dd}	DC drain voltage	V
v_{knee}	Knee voltage of transistor	V
v_{sat}	Saturation voltage of transistor	V
θ	Conduction angle	Radians

By generalizing the classes A through C it becomes clear that the current source amplifier is not able to ever achieve ZVS due to the constant drain voltage waveform present at the output, and can only achieve ZVDS at a conduction angle of 0 radians which results in 0 power delivered to the load. To achieve 100% efficiency and have a practical gain we look to the switching amplifier.

$$\eta_{Drain}, \% = \frac{v_{dd} - v_{sat}}{v_{dd}} \frac{\theta - sin\theta}{4(sin\frac{\theta}{2} - \frac{\theta}{2}cos\frac{\theta}{2})} \tag{2.3}$$

$$P_{out} = \frac{1}{2}(v_{dd} - v_{sat})\frac{I_m}{2\pi}(\theta - sin\theta) \tag{2.4}$$

$$I_n = \frac{1}{\pi}\int_{-\frac{\theta}{2}}^{\frac{\theta}{2}} \frac{I_m}{1 - cos(\frac{\theta}{2})}(cos\alpha - cos(\frac{\theta}{2}))cos(n\alpha)\ d\alpha \tag{2.5}$$

$$R_{opt} = \frac{v_{dd} - v_{knee}}{I_{Fundemetnal}} \tag{2.6}$$

2.3 Switching Amplifiers

Switching amplifiers model the transistor as a switch instead a dependent current source. Figure 2.7 shows the ideal operation of a switching amplifier. The transistor

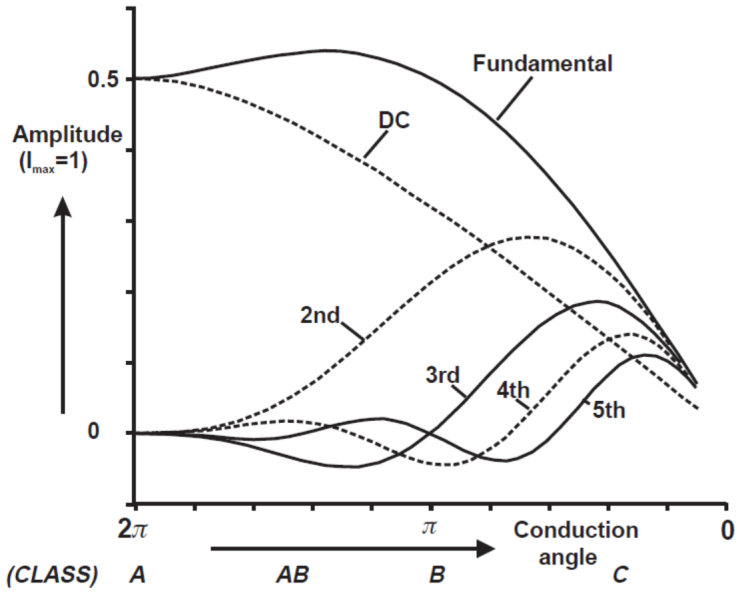

Figure 2.5: Normalized Current Harmonic Amplitude versus Conduction Angle [1]

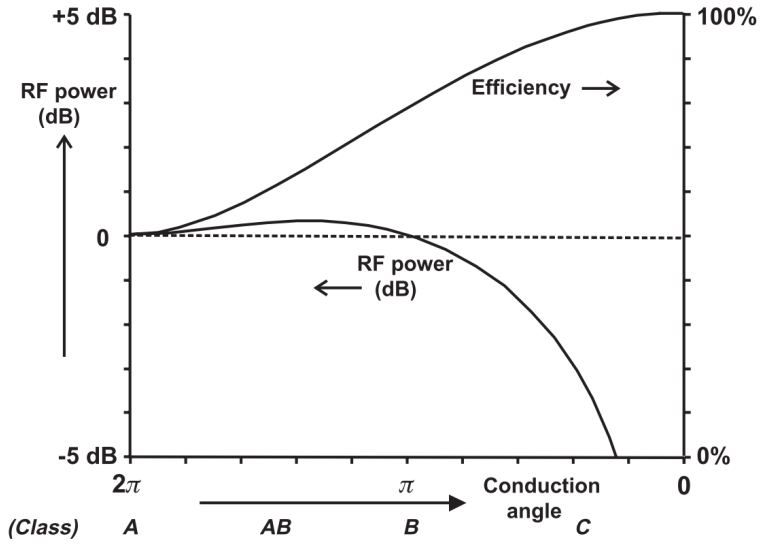

Figure 2.6: RF Power (relative to Class A) and Efficiency versus Conduction Angle [1]

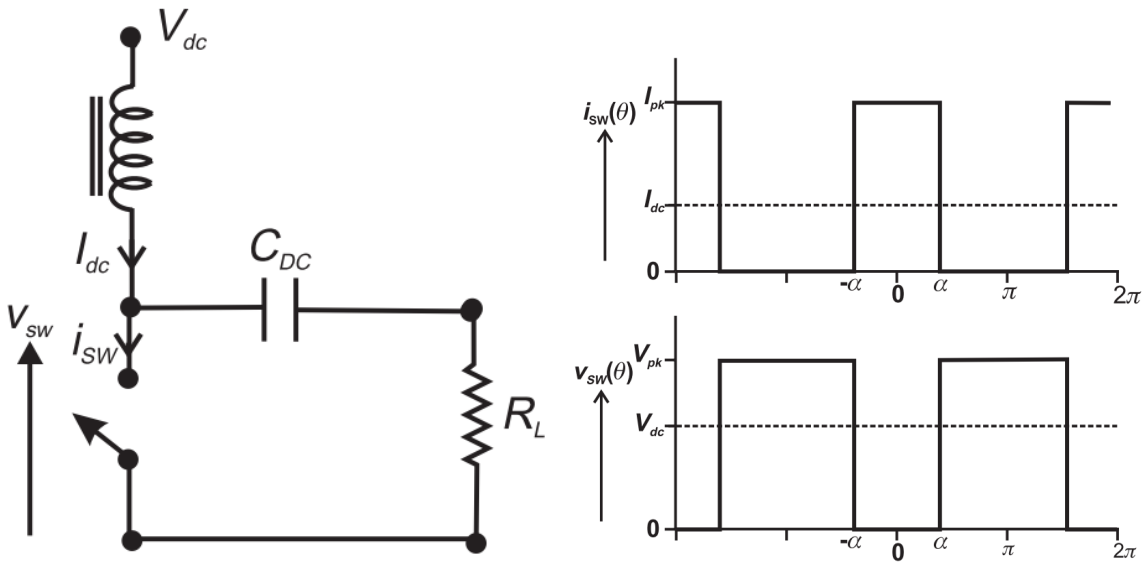

Figure 2.7: Basic Switching Amplifier Circuit and Waveforms[1]

is modeled as a switch that can only be "on" or "off" depending on the gate voltage. The switching operation allows for current to flow while the switch is on with 0 drain voltage, and for 0 current while the switch is off with a non-zero drain voltage. Ideally this would allow for ZVS and for ZVDS which could result in 100% efficiency. The switching amplifier classes (D, E, and F) build upon this ideal model and are able to achieve higher efficiencies in practice than current source amplifiers.

2.3.1 Class D Amplifier

The class D amplifier can be thought of as push pull version of a switching amplifier. The amplifier consists of two transistors to operate as switches to conduct during the positive half and negative half cycle of the input seen in Figure 2.8 [1]. This allows for a full wave drain current to flow through the output load that is filtered through a high Q LC network while the drain voltage is a square wave with 0 overlap between the transistor that is on that allows for ZVS and ZVDS [28]. The LC network is tuned to the fundamental frequency of the input. Class D looks effective

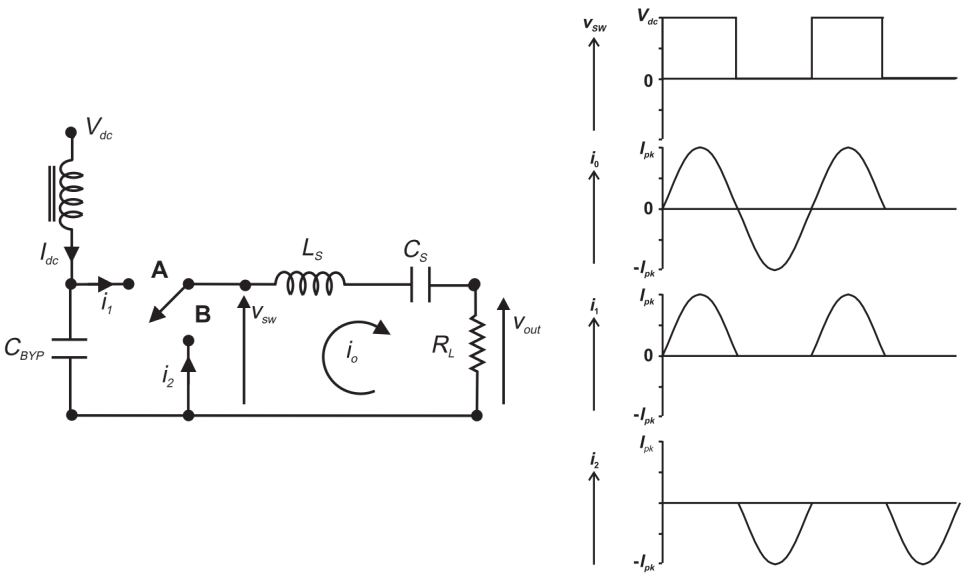

Figure 2.8: Class D Amplifier Circuit and Waveforms[1]

in theory but suffers due to switching resistances and drain capacitances which limit the maximum frequency of operation to VHF in practice [25].

2.3.2 Class E Amplifier

The class E amplifier builds up on the ideal switch amplifier takes in account for the shunt output drain capacitance and amplification is the result of DC and RF currents that charge the drain shunt capacitance [25]. As seen in Figure 2.9, the switch is turned on from time $-\alpha_1$ to α_2 allowing current to flow solely from the power supply and the load through the switch and the voltage across the drain capacitance is shorted. Then as the switch is turned off from time α_2 to α_1 the current from the power supply and load will flow through the drain capacitor [1]. To achieve high efficiency, the switching current waveforms are adjusted so that the capacitor current and charge is 0 when the switch is turned on which allows for ZVS and ZVDS conditions allowing for theoretically 100% efficiency. [12].

The class E amplifier produces significant harmonic distortion due to the switching action and the output must be filtered to suppress harmonics [30]. Another concern with using the class E amplifier in practice is the large peak voltages at the drain

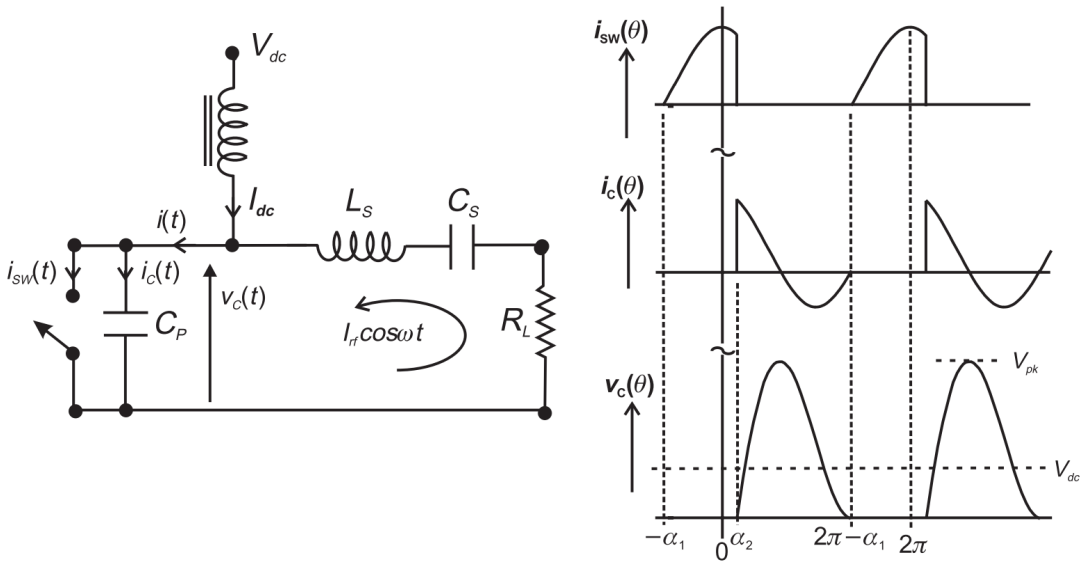

Figure 2.9: Class E Amplifier Circuit and Waveforms[1]

of the transistor which are around three times the drain supply voltage when the switch turns off [8]. In addition the output drain capacitance limits the frequency of operation that is required to create the proper drain waveforms [28].

2.3.3 Class F Amplifier

The class F amplifier has a theoretical efficiency of 100% through the use of multi harmonic terminations. The theory behind the class F amplifier relies on the generation of odd voltage harmonics and shorting of even voltage harmonics at the drain of the device to increase the efficiency of the amplifier. By keeping only the odd harmonics of the signal at the output, ideally a square wave would appear and by biasing the amplifier at a conduction angle of pi the amplifier has zero overlap between the current and voltage waveforms and no power consumed when the amplifier is switched on. The harmonics are generated due to the knee voltage of the transistor. When the AC signal causes the transistor to reach saturation the abrupt change in current flow generates voltage harmonics. In practice it becomes challenging to design matching networks as the number of harmonics to control increases. Also the output capacitance of the transistor will eventually short out higher order harmonics so 100% efficiency is not realizable in practice. By controlling up to the 5th harmonic, 90.5%

efficiency can be achieved. A more in depth analysis of the class F amplifier follows in the next chapter.

Chapter 3

Class F Detailed Description

The class F amplifier is able to achieve high efficiency through the use of harmonic trapping to ideally create a square waveform for the drain current and a half sinusoid waveform the for the drain voltage that don't overlap so power is consumed. It's theoretically capable of 100% drain efficiency but in practice only a finite amount of harmonics can be matched, so the efficiency in the real world is around 80% to 90%. Through Fourier series analysis it can be shown that by loading the drain so that odd harmonics see an open circuit and even harmonics see a short circuit, the ideal current and voltage waveforms conditions will arise [5]. The class F amplifier also has a counterpart, the class F^{-1} in which the current and voltage waveforms are opposite so that ideally the voltage waveform is a square wave and the current is a half sinusoid which will be discussed later in this chapter [17].

3.1 Fourier Analysis

To begin the analysis of the class F amplifier and how it uses harmonics at the drain to increase efficiency, it would be useful to talk about how the harmonics are generated in the first place. With large signal power amplifiers, the assumption that the drain current and voltage waveforms are purely sinusoidal is no longer true and the presence of harmonics must be taken into account. The source of the harmonics

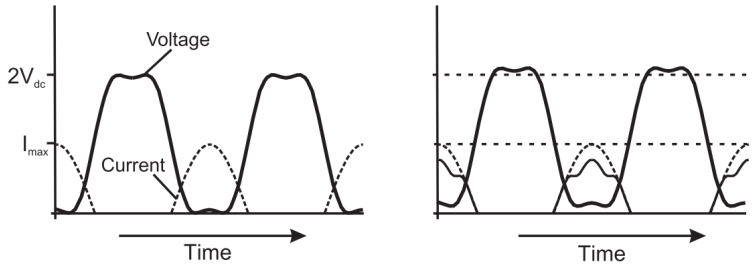

Figure 3.1: Transient Waveforms of Class B Amplifier With and Without Knee Voltage [1]

in power amplifiers attributed to the knee voltage of the device that essentially clips the peak of the drain current and due to the relatively large discontinuity harmonics are generated [4]. The current source amplifier theory doesn't predict the effect of the knee voltage in analysis but as seen in Figure 3.1 even in the class B amplifier the knee voltage will cause a discontinuity. No rigorous analysis that shows the relation of the knee voltage to the harmonic generation has been done but measurements have verified the presence of harmonics.

To begin the analysis it is assumed the DC bias of the amplifier is set so the conduction angle is π, like the other switching amplifiers, so the drain current waveform can be modeled as a half sinusoid. It will be shown later that in practice the conduction angle should be close to π but not exactly π. The drain current and voltage waveforms can be modeled as a Fourier series with odd components for the voltage and even for the current as seen in Equations 3.1 and 3.2 [23]. In the equations I_{mf0} and V_{mf0}, m represents the harmonics of the fundamental frequency $f0$.

$$i_d(t) = I_{DD} - I_{f0}sin(\omega t) - I_{2f0}sin(2\omega t) - I_{4f0}sin(4\omega t) + \ldots \tag{3.1}$$

$$v_d(t) = V_{DD} + V_{f0}sin(\omega t) + V_{3f0}sin(3\omega t) + V_{5f0}sin(5\omega t) + \ldots \tag{3.2}$$

From Equations 3.1 and 3.2, four new parameters: $\gamma_v, \gamma_i, \delta_v$ *and* δ_i relate the fundamental and peak amplitude to the DC component for the drain and voltage. These parameters can be used to define the ideal load at the fundamental frequency Equation 3.7 , the RF output power Equation 3.8, DC input power Equation 3.9, and the drain efficiency Equation 3.10 from [29]. The key take away from the all of this

is that the drain efficiency is a function of γ_v and γ_i.

$$V_{f0} = \gamma_v V_{DD} \tag{3.3}$$

$$I_{f0} = \gamma_i I_{DD} \tag{3.4}$$

$$v_{max} = \delta_v V_{DD} \tag{3.5}$$

$$i_{max} = \delta_i I_{DD} \tag{3.6}$$

$$V_{f0} = I_{f0} Z \tag{3.7}$$

$$P_{o,f0} = \frac{V_{f0}^2}{2Z} = \frac{\gamma_v^2 V_{DD}^2}{2Z} \tag{3.8}$$

$$P_i = V_{DD} I_{DD} = \frac{\gamma_v V_{DD}^2}{\gamma_i Z} \tag{3.9}$$

$$\eta = \frac{P_{o,f0}}{P_i} = \frac{\gamma_v \gamma_i}{2} \tag{3.10}$$

The γ and δ parameters can be extended for all the harmonics and is used to describe what is called maximally flat waveforms. The term maximally flat refers to the ideal scenario were all the odd harmonics see an open circuit and all the even harmonics see a short circuit at the drain which results in the square wave for the drain voltage which has a flat top that doesn't overlap with the half sinusoid drain current seen in Figure .

Fourier series can be used to determine the amplitudes of each harmonics in Equation 3.6 and 3.5 for a maximally flat waveform. In the ideal case were infinite number of odd voltage harmonics can be properly terminated, the amplitude of the each harmonic is that of a square wave seen in Equation 3.12. For the ideal case for terminating all the even current harmonics, the amplitude of each harmonic is equal to

that of a half sinusoid in Equation . For the ideal case, $\gamma_v = \frac{4}{\pi}$ and $\gamma_i = \frac{\pi}{2}$ and from Equation 3.10, $\eta = \frac{\gamma_v \gamma_i}{2} = \frac{\frac{4}{\pi}\frac{\pi}{2}}{2} = 100\%$. The efficiency is dependent on the input power because of required harmonic level to produce the maximally flat waveforms. As input power is backed off, the harmonic levels and efficiency drops as well and the class F amplifier becomes more like a class A amplifier. The class F amplifier has a counterpart, the class F^{-1} amplifier which swaps the voltage and current waveforms so the ideally the drain current is a square wave and the voltage is a half sinusoid.

Theoretically it has the same properties as the class F amplifier and experimentally it has been show to do things. Flesh this out.

In practice, a matching network to terminate infinitely many harmonics is impossible and the output drain capacitance of the transistor will short out higher harmonics. Typically as a compromise between feasability and efficiency, up to the third harmonic is terminated which is called third harmonic peaking. This is more common in class F amplifiers that operate in the couple of gigahertz which can take advantage of the high transition frequency of new technologies like high electron mobility (HEMT) transistors. In the high frequency (HF) and very high frequency (VHF) domain, higher harmonics are present and are typically more efficient than their gigahertz counterparts.

To solve for the harmonic amplitude of each component when only a finite number of harmonics are terminated, the derivatives of Equation 3.2 and 3.1 are solved with the condition at $\omega t = \frac{3\pi}{2}$, $v_d = 0$ and all higher harmonic amplitudes are set to 0. For example for terminating up to the third harmonic, the second derivative for the voltage, seen in Equation 3.11, with the conditions applied is $0 = V_{f0} - 9V_{3f0}$, therefore $V_{3f0} = \frac{1}{9}V_{f0}$. Then using Equation 3.2 with the same conditions, $V_{f0} = \frac{9}{8}V_{DD}$ and $V_{3f0} = \frac{1}{8}V_{DD}$. The same process applied to the current waveform results in $I_{f0} = \frac{4}{3}I_{DD}$ and $I_{2f0} = \frac{1}{3}I_{DD}$. The drain efficiency for terminating up to the third harmonic can now be calculated, $\eta = \frac{\gamma_v \gamma_i}{2} = \frac{\frac{9}{8}\frac{4}{3}}{2} = 75\%$. A table of how efficient the class F amplifier for a finite number of harmonic terminations can be seen in Table 3.1. Going back to the current source amplifiers, the class A amplifier only controls the first harmonic of the current and voltage and from Table 3.1 it's only 50%. The class B amplifier controls only the first voltage harmonic and ideally all of the current harmonics and is ideally 78.5% efficient.

Table 3.1: Maximum Efficiency of Class F Amplifier

Harmonics	$n = 1$	$n = 3$	$n = 5$	$n = \infty$
$m = 1$	50.0%	57.7%	60.3%	63.7%
$m = 2$	70.7%	81.7%	85.3%	90.0%
$m = 4$	75.0%	86.6%	90.5%	95.5%
$m = \infty$	78.5%	90.7%	94.8%	100%

m,n are the maximum order of drain current and voltage harmonics

$$\frac{d^2 v_d}{d\theta^2} = -V_{f0} sin(\omega t) - 9V_{3f0} sin(3\omega t) - 25V_{5f0} sin(5\omega t) + \dots \tag{3.11}$$

$$V_{mf0} = \frac{4}{m\pi} \begin{cases} 0, & \text{if } m = even \\ 1, & \text{if } m = odd \end{cases} \tag{3.12}$$

A key factor that is missing from the Fourier analysis of the waveforms is the phase relation between the harmonics, if all of the harmonics are in phase the amplifier will have a much lower efficiency due to destructive interference. This can especially be seen in third harmonic peaking amplifiers seen in Figure 3.2. The right part of the figure shows the drain voltage if the third harmonic is in phase. This results in triangle wave instead of a square wave which would overlap with the half sinusoidal current. The left part of the figure shows the drain voltage with an out of phase third harmonic which results in the proper square wave shape. Going back to Figure 2.5, in order for the third harmonic to be out of phase the class F amplifier must be biased between so the conduction angle is between π and 2π. Within these conduction angles, the third harmonic is negative relative to the fundamental so it is out of phase. For conduction angles less than π, the third harmonic will be in phase and will result in a loss of efficiency. In practice, the class F amplifier is biased in the so called "deep AB" region so that it slightly greater than a conduction angle of π so the drain current will still resemble a half sinusoid shape and the voltage waveform will be maximally flat.

The design of a class F amplifier starts with finding a suitable "deep" AB bias with sufficient gain for the application. Then applying a load pull at the fundamental

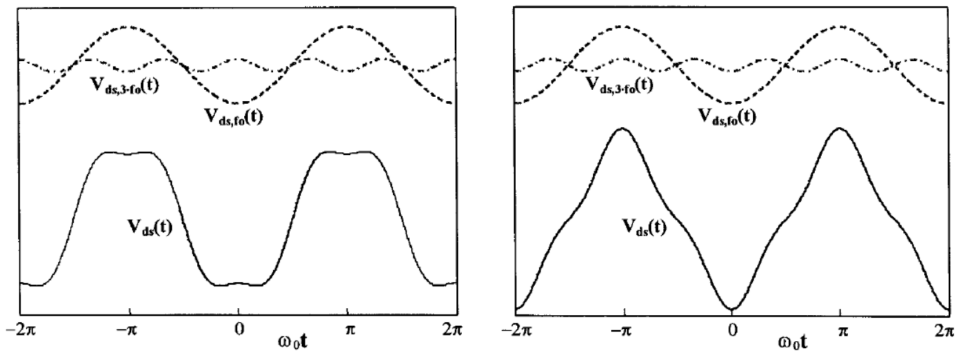

Figure 3.2: Drain Voltage Waveform with In Phase and Out of Phase Third Harmonic [4]

frequency to determine the optimal load impedance, and then a source pull at the fundamental frequency for the optimal source impedance. Load pulling and source pulling are measurements that take the s-parameters of a device while applying it to a uniformly sampled smith chart on the load and source side. Simulated load pulls require accurate device models to be of any use and to take real world load pull measurements are time intensive without automated test equipment. After determining the optimal load and source impedances, a harmonic phase load pull is done which is similar to a load pull, but applied to a harmonic frequency and the smith chart is sampled uniformly in phase at a constant gamma value. For the class F amplifier to keep the drain current and voltage harmonics at the drain, the odd harmonics have to see a open and the even harmonics a short.The harmonic phase load pulls are done at a reflection coefficient value of 1 and swept to measure the transistor efficiency if the harmonics are terminated properly. This process is usually iterated until a proper bias is found that allows for sufficient gain and the load pulling results in the desired efficiency.

The matching network for a class F amplifier can be down with discrete components, some closed form methods use the output drain capacitance and impedance as parameters to come up with matching networks but this has only been shown to work in sub 1 GHz band [6]. Multiple papers show that the output capacitance is non-linear at higher frequencies and some work has explored methods to make compensate for the non-linearity using varactors [15]. The most common methods rely on resonant transmission line matching networks which are intuitive to a certain

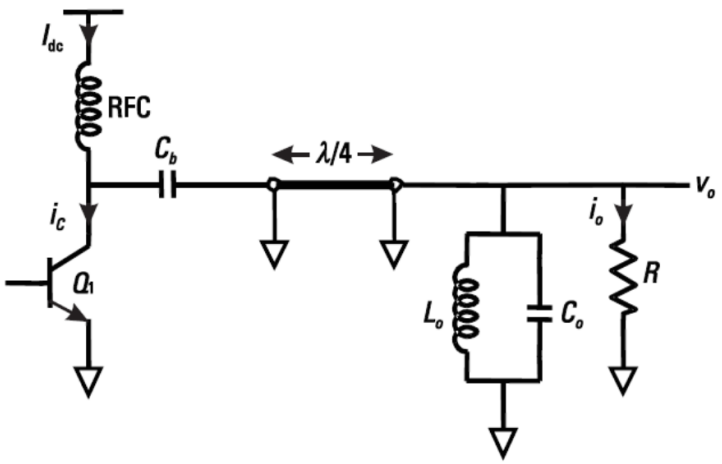

Figure 3.3: Quarter Wavelength Matching Network for Class F Amplifiers

degree. The simplest transmission line matching network for the class F amplifier uses a quarter wavelength line at the drain to a tuned load as seen in Figure 3.3. The tuned load is such that at odd harmonics it appears as a short and even harmonics an open, so when reflected back at the drain the odd harmonics see an open and even harmonics a short [5]. In practice with this type of matching network, the impedances of the various sections are parameterized and are left to be found by an optimizer using simulation software. It's also been experimentally determined that a harmonic matching network at the input of the transistor increases the efficiency over just having a matching network at the output.

Chapter 4

Class F Amplifier ADS Simulations, Comparisons to Specs

The initial goal of the class F amplifier design was to try and control up the fifth harmonic which would ideally allow 90.5% drain efficiency. After looking through the past amplifier competitions and looking at various RF transistor manufacturers, the Wolfspeed CGHV1F006S GaN HEMT transistor was chosen. This model was chosen over others to the relatively new release of the transistor, the high operating frequency of the transistor (18 GHz), and the fact that the transistor came in a QFP package versus a semiconductor die. The majority of past winners of the amplifier competition used Cree (now Wolfspeed) transistors and Wolfspeed provides a transistor level models for the amplifier for accurate simulations to design amplifiers.

Talk about DC bias The simulation of the various parts of the class F amplifier was done using Keysight ADS 2016. The first step in the simulation process was determining the optimal DC bias. Using the provided transistor model from Wolfspeed, various drain and gate voltages were simulated to see what the drain current and transducer gain CHECK THIS STATEMENT the transistor would have. The bias for the class F amplifier should be in the "deep" AB region so the drain current resembles a half sinusoid shape but still allows for the negative third harmonic to be present. The drain current should be minimized in order to maximize the PAE of

the amplifier. The competition rule states the amplifier should have a minimum of 36 dBm output power at a maximum of 24 dBm input power resulting in a minimum gain of 12 dBm. For the final amplifier, the target gain was 16 dB CHECK THIS STATEMENT so there would be a margin for various effects that wouldn't be able to be taken into account in the simulation like the fabrication process.

Talk about fundamental load and source pull After determining the DC bias of the amplifier, fundamental load and source pulls are done to determine the optimal load and source impedances for the transistor. Load pulls are done keeping the source impedance fixed and sweeping the load over a uniformly sampled space on the Smith Chart to then measuring the transducer gain. Various drain efficiency and gain contours can be produced by doing load pulls. The typical process starts with sampling the entire Smith Chart then load pulling again around the region with the highest efficiency contour. As a starting point the source impedance was set to a low value of 10Ω. Source pulling is done after load pulling and follows a similar process by keeping the load impedance fixed then sweeping the source impedance for the highest efficiency while still having the target gain. The load and source pulls are done at the fundamental frequency at an input power of 15 dBm to provide an additional margin.

Talk about RF input power used and why its low as a margin. For maximum PAE, the RF input power should be at the highest and produce the minimum output power. But for the C/I

Harmonic phase pull The load and source pulls are done at the fundamental frequency while the harmonic phase pulls are done at the higher harmonics. A phase pull is analogous to a load and source pull, but instead of sampling an area of the Smith Chart the phase pull samples a constant gamma value over a range of phase angles. For the class F amplifier the gamma value should be close one because the odd and even harmonics should see a open and short at the drain respectively CHECK THIS STATEMENT. The harmonic phase pull is done at the lowest harmonic from load to source then to the highest harmonic. The harmonic phase pull is done at the input and output because it's been shown experimentally that harmonic matching networks at the input can also increase the drain efficiency INSERT REFERENCE HERE. The harmonic phase pull can measure gain and efficiency contours just like the load and source pulls. The end result of all the various pull simulations is the ideal

gain and efficiency of the amplifier in class F operation if the harmonics are ideally terminated. The process of determining a DC bias, fundamental load and source pull, and harmonic phase pulls is repeated until the requirements are met. Table X shows the iteration steps and amplifier performance. Initially the goal was to control up to the fifth harmonic to hopefully increase the efficiency near the theoretical value of 90.5% CHECK THIS VALUE. But this the transistor used there weren't any sufficient gains from controlling up to the third harmonic versus controlling up to the fifth harmonic so it was decided only up to the third harmonic will be controlled.

Harmonic matching network The harmonic matching network is the key in keeping the proper harmonics at the drain. It is composed of a matching network and a wave shaping network that is on the load and source side of the transistor. The wave shaping network consists of a series section that is a quarter wavelength long with an eight wavelength open shunt stub. Most class F wave shaping network follow a similar pattern of various fractional wavelength sections so the drain is properly terminated. The downside of these networks is the relatively large electrical lengths due to the presence of a quarter wavelength sections in nearly all such networks. This is especially cumbersome below X band and fix this statement. This design explores if coupling the open circuit shunt stubs in the wave shaping network can decrease the electrical size of the class F amplifier.

After the wave shaping network comes the matching network so the amplifier is matched as close as possible to 50Ω. This amplifier used a shunt stub and a series transmission line for the matching

Need to do two tone tests and stability tests for the amplifier! More content!

Talk about simulated amplifier The transmission lines were simulated using Rogers INSERT NUMBER HERE. After comparing various low loss laminates like Duroid, the Rogers NUMBER HERE was selected. This was partially due to the larger sample size that could be ordered so more amplifier boards could be fabricated. Also it has the lowest tangent loss and relative permittivity that allowed the transmission lines going to the transistor gate and drain to be thin enough. Reword all of this later man. All of the amplifier dimensions were set as parameters with goals to maximize the PAE with a minimum set gain at a fixed RF input power and the optimizer was

used to tune the amplifier dimensions. The board discussed in this section is the third revision. The previous two amplifiers were malfunctioned with one acting as an oscillator and the other not working at all. This was most likely due to fabrication issues.

Drain current and voltage waveforms

Two tone test

VSWR plots

Gain vs frequency and input power

PAE and Gain vs input power

power out vs power in

Table of simulated amplifier measurements

Chapter 5

Class F Amplifier Test Results, Comparisons to Specs

Talk about build process?

The final version of the amplifier was milled using INSERT MILLING MACHINE PART NUMBER. Vias were added underneath the transistor to improve the heat conduction after the board layout was done in ADS. In addition a fan was mounted on the board with a heatsink on the transistor for additional cooling. The fan draws 30 mA at 40 volts and was tied to the drain voltage of the amplifier. Two previous versions were built but due to the challenge of soldering the leadless package of the transistor they were damaged most likely due to shorts and insufficient cooling. The bias inductors, coupling capacitors, and transistor was mounted on the board using solder paste and a heatgun. A bill of materials and the board layout can be found in the Appendix. The final build of the amplifier is show in Figure X. The amplifier was measured with an Anritsu PART NUMBER HERE and the drain powered with an Agilent Power Supply PART NUMBER with the drain current being measured by an Agilent Multimeter PART NUMBER. The gate voltage was powered by an Agilent Power Supply PART NUMBER. The VNA was calibrated from x GHz to Y GHz and set to average ten samples. A 20 dB attenuator was put at the output of the amplifier so the VNA would not be damaged by the high RF power. The 20 dB attenuator

was measured so the attenuation could be removed and the amplifier gain could be properly measured.

The amplifier s-parameters and drain current was measured over a wide range of input powers from -10 dBm to 20 dBm.

Need a test black box diagram for and equipment part numbers

Unable to measure high power two tone due to lack of equipment. Only able to measure IMD at low input powers.

Need photo of amplifier lol

VSWR plots

Gain vs frequency and input power

PAE and Gain vs input power

power out vs power in

Chapter 6

Conclusion, Future Projects

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