Chapter 1

Abstract and IEEE Design Competition Rules

Telecommunications is the basis of our modern world. There is infrastructure from microwave links, fiber-optic links, and satellite links that connect people all over the world together. Each year more and more data is transferred through these networks. The Cellular Telephone Industries Association reported less than 100 MB of average monthly traffic per smartphone in the United States in 2009 and in 2014 this has jumped up to over 1800 MB of average monthly traffic. To transfer more data, higher order modulation schemes must be used like QAM which require linear amplifiers so amplitude and phase is not distorted during amplification. In portable devices were battery life is one of the key parameters, high efficiency power amplifiers are important due to the large power consumption of the RF amplifiers.

The International Microwave Symposium (IMS) 2016 High Efficiency Power Amplifier Student Design competition focuses on maximizing the power added efficiency (PAE) and operating frequency of the amplifier over a wide range of input powers. Power added efficiency is defined as the difference of output RF power and RF input power over the DC bias power seen in Equation 1.1. PAE is an important metric for

power amplifiers to show how efficient the amplifier is converting the DC power into RF power, ideally converting 100%.

$$PAE, \% = \frac{RF\ Power_{out} - RFPower_{in}}{DC\ Power} \tag{1.1}$$

To qualify for the design competition the amplifier must output at least 36 dBm (4 Watts) with less than 24 dBm input power for a single carrier and less than 22 dBm per tone for two carriers spaced 5 MHz apart. Also the amplifier must have a carrier-to-intermodulation ratio (C/I), defined as the ratio in dB between the amplitude of either carrier and the highest intermodulation product, greater than 30 dB at an input power of 0 dBm.

The rules for the amplifier require the amplifier have a center frequency between 1 GHz and 10 GHz. The RF ports should use SMA female connectors, and the bias connections should use banana plugs with a maximum of two DC supply voltages. The source and load impedance of your amplifier should be matched to 50 Ω. The amplifier can use any technology but must be the result of new design and fabrication methods. The amplifier PAE will be measured with at the first RF output power when the C/I ratio drops below 30 dB. The winning amplifier will have the highest figure of merit seen in Equation 1.2.

$$FigureofMerit = PAE * (CenterFrequency, GHz)^{0.25} \tag{1.2}$$

A table of past competition winners can be seen in Table 1. The highest scores in the competition have all been from class F amplifiers with a center frequency around 3.5 GHz with the best amplifier in the competitions past scoring 109.2 at a center frequency of 3.475 GHz and a PAE of 80.1% in 2011. Since 2011 the winning figure of merit has dropped by more than 20 points. The author thinks that in 2011 and earlier the amplifiers were scored at their highest PAE. And from 2012 on, the amplifiers were scored at the input power when the C/I ratio drops below 30 dB. The class F amplifier was chosen for the design due to highest PAE compared to other amplifier classes and because the design could be accomplished solo within an academic year. Most of the submissions were a group effort, especially the Doherty amplifiers which use a combination of two discrete amplifiers in the design. As per the rules, the

Table 1.1: Table of Past Competition Winners and Amplifier Parameters

Year	Device	Class	Frequency, GHz	PAE, %	Figure of Merit
2006	Si LDMOS	F^{-1}	1	75.9	75.9
2007	GaN HEMT	F	1.21	82.9	87.0
2008	GaN HEMT	F^{-1}	3.2	71.9	96.1
2009	GaN HEMT	F^{-1}	3.27	71.1	95.6
2010	GaN HEMT	J	3.5	74.7	102.1
2011	GaN HEMT	F	3.475	80.1	109.2
2012	GaN HEMT	Doherty	3.5	59.0	80.7
2013	GaN HEMT	Doherty	3.5	62.5	85.5
2014	GaN HEMT	Doherty	5	57.8	86.4

amplifier has to be a result of a new effort and this work explores coupling the stubs of the harmonic matching networks to reduce the electrical size of the amplifier using a gallium nitride (GaN) high electron mobility (HEMT) transistor.

Chapter 2

Amplifier Classes

The generic power amplifier consists of a transistor with a DC bias and AC coupled to the RF input and output ports. For the sake of simplicity this work will only describe the operation of field effect transistor amplifiers. The major source of power consumption of an amplifier comes from the drain source current and voltage that occurs during operation. Power amplifiers come in a variety of classes, and the most commonly used ones are A, B, AB, C, D, E, and F. Classes A through C can be described by the conduction angle of the device and modeling the transistor as a current source. The conduction angle is the amount of current flowing through the transistor from drain to source during a single cycle of the AC signal being amplified and ranges from 0 to 2π [4]. Classes D through F are defined as switching amplifiers and vary due to the matching networks which shape the waveforms of the current and voltage at the drain and gate of the device [29]. This chapter will describe a high level overview of the various amplifier classes and discuss the limitations of each in practice.

2.1 Efficiency of Amplifiers

To reduce the power consumption of a power amplifiers, two major concepts are important: zero voltage switching (ZVS) and zero voltage derivative switching

(ZVDS). ZVS is when there is zero voltage when the amplifier is switched on and conducting so while current flows through the output no power is consumed. ZVDS is when there is no overlap between the voltage and current waveforms so no power is consumed during the switching. An amplifier can be 100% if it achieves ZVS and ZVDS because no power would be consumed at any point in the amplification process. A measure of amplifier efficiency is the power added efficiency (PAE) defined in Equation 2.1. PAE is a measure of how efficient an amplifier is able to convert the input DC power into RF power gain. Ideally all of the DC power used to power the amplifier would be used to increase the input RF power. The maximum limit for a lossless system is 100%, for example if a power amplifier consumed 1 Watt and was able to output 1.001 Watt of RF power from 1 mW of RF input power, the PAE would be 100.% because all of the DC power was used to increase the RF power.

$$PAE, \% = \frac{RF\ Power_{out} - RFPower_{in}}{DC\ Power} \tag{2.1}$$

Another measure of amplifier efficiency is the drain efficiency which is the proportion of the output power of the fundamental harmonic over the DC power consumed seen in Equation 2.2. The drain efficiency is typically used when talking about the theory behind the different amplifier classes. In practice, PAE is used as the metric to compare power amplifier efficiency because it takes in account RF input power which is relatively large compared to small signal amplifiers. Small signal amplifiers operate at a bias point that can be assumed to be linear for small input powers. Power amplifiers are large signal devices that operate in the non-linear regions of transistor.

$$\eta, \% = \frac{P_{Fundamental}}{DC\ Power} \tag{2.2}$$

Figure 2.1: Class A Bias Point and Conduction Cycle [27]

2.2 Current Source Amplifiers

2.2.1 Class A Amplifier

The class A amplifier uses a bias that results in a conduction angle of 2π, seen in Figure 2.1, and a theoretical quiescent current of 50% the maximum drain current. This results in power always being consumed due to the constant bias current and voltage present at the drain of the amplifier. The bias point is chosen so the transistor operates in the active region which can be seen in Figure 2.1. The constant power consumption limits the maximum efficiency of the class A amplifier for a continuous wave (CW) signal to 50% [1].

The class A amplifier is the most linear of all classes due to the conduction angle that provides ideally no clipping of the current or voltage waveforms. The high linearity allows the class A amplifier to have the lowest intermodulation distortion (IMD) of all the amplifier classes. The downside of the linearity is that the input drive level is proportional to the IMD present at the output of the amplifier. Class A amplifiers are also able to operate closer to the highest operating frequency of a transistor because it does't use the harmonics present in the amplifier for it's amplification [27].

Figure 2.2: Class B Bias Point and Conduction Cycle [27]

2.2.2 Class B Amplifier

Class B uses a conduction angle of π resulting in a half sinusoid waveform for the drain current seen in Figure 2.2 with a theoretical quiescent current of 0 A. The maximum efficiency for a CW signal is 78.5%. The reduced conduction angle causes the required input power to achieve the maximum efficiency to be 6 dB higher compared to the class A amplifier [1]. The drain current is proportional to the input signal so the Class B amplifier is considered a linear amplifier but will result in harmonic distortion due to the clipping of the drain current. The output is usually filtered to reduce the harmonic distortion[24]. In most applications, the class B amplifier is used in a push pull configuration to reduce distortion by providing a full sine wave output and maintain greater efficiency than a class A amplifier. Also instead of setting the quiescent current to 0, the drain current is typically set to 10% of the max drain current of the transistor to reduce the harmonic distortion. An interesting result of the push pull configuration is that even harmonics subtract one another out while odd harmonics add together [27].

Figure 2.3: Class AB Bias Point and Conduction Cycle [27]

2.2.3 Class AB Amplifier

The class AB amplifier uses a conduction angle ranging between π and 2π and is a compromise between class A and class B amplifiers. The drain efficiency lies between 50% and 78.5% with approximately the same output power as the class A amplifier [1]. The bias point and conduction cycle can be seen in Figure 2.3. The class AB amplifier offers a wider dynamic range than class A or class B because the conduction angle is proportional to the drain current which also results in the class AB amplifier being a non-linear amplifier [1].

2.2.4 Class C Amplifier

The class C amplifiers is biased such that the quiescent current is 0 A and the conduction angle is between 0 and π seen in Figure 2.4. The class C amplifier is non-linear with a higher efficiency than class B with a maximum drain efficiency of 100% at zero conduction angle but will have zero gain. In practice, the class C amplifier has a conduction angle slightly less than π for a maximum efficiency of 85% while still having a useful gain [24]. The class C has the highest harmonic distortion of all the current source amplifier classes which will be shown in the following section.

Figure 2.4: Class C Bias Point and Conduction Cycle [27]

The harmonic distortion requires significant filtering at the output of the amplifier. Class C amplifiers aren't typically used for microwave power amplifiers due to the large negative voltage present at the gate of the transistor which can cause reverse breakdown in the transistor [1]. The class C amplifier offers a tradeoff of higher efficiency but with higher harmonic distortion and lower output power level compared to the other current source amplifier classes.

2.2.5 Harmonic Distortion

The current source power amplifiers can be generalized to a power amplifier with various conduction angles and the drain efficiencies. The output power and harmonic distortion can be described as a function of conduction angle seen in Equations 2.3, 2.4, and 2.5 [8]. Table 2.1 defines the various parameters to the various equations. Figure 2.5 shows the normalized output current harmonics versus conduction angle. At a conduction angle of 2π, the output has minimal harmonic distortion with only the fundamental and DC component present. The DC component is easily removed by coupling capacitor. As conduction angle increase, the other harmonic amplitudes increase which causes increased harmonic distortion and the DC power is reduced

Table 2.1: Table of Current Source Waveform Parameters

Parameter	Definition	Units
I_m	Maximum drain current of transistor	A
I_n	Magnitude of current harmonic n	A
v_{dd}	DC drain voltage	V
v_{knee}	Knee voltage of transistor	V
v_{sat}	Saturation voltage of transistor	V
θ	Conduction angle	Radians

increasing the efficiency. At zero conduction angle, the transistor won't conduct any current and all of the harmonic amplitudes drop to 0. Figure 2.6 shows the RF power relative to class A and efficiency versus conduction angle assuming the harmonics are removed and the transistor is optimally loaded. A power amplifier is said to be properly loaded if the load resistance is equal to the DC drain voltage minus the knee voltage of the transistor divided by the fundamental drain current, see Equation 2.6 [8].

The generalized form of the current source amplifiers are not able to ever achieve ZVS due to the constant drain voltage waveform present at the output which is required to bias the amplifier. And current source amplifiers can only achieve ZVDS at a conduction angle of 0 radians which results in 0 power delivered to the load. To achieve 100% efficiency and have a practical gain we look to the switching amplifier.

$$\eta_{Drain}, \% = \frac{v_{dd} - v_{sat}}{v_{dd}} \frac{\theta - sin\theta}{4(sin\frac{\theta}{2} - \frac{\theta}{2}cos\frac{\theta}{2})} \tag{2.3}$$

$$P_{out} = \frac{1}{2}(v_{dd} - v_{sat})\frac{I_m}{2\pi}(\theta - sin\theta) \tag{2.4}$$

$$I_n = \frac{1}{\pi}\int_{-\frac{\theta}{2}}^{\frac{\theta}{2}} \frac{I_m}{1 - cos(\frac{\theta}{2})}(cos\alpha - cos(\frac{\theta}{2}))cos(n\alpha)\ d\alpha \tag{2.5}$$

Figure 2.5: Normalized Current Harmonic Amplitude versus Conduction Angle [1]

$$R_{opt} = \frac{v_{dd} - v_{knee}}{I_{Fundemetnal}} \tag{2.6}$$

2.3 Switching Amplifiers

Switching amplifiers model the transistor as a switch instead a dependent current source. Figure 2.7 shows the ideal operation of a switching amplifier. The transistor is modeled as a switch that can only be "on" or "off" depending on the gate voltage. The switching operation allows for current to flow while the switch is on with 0 drain voltage, and for 0 current while the switch is off with a non-zero drain voltage. Ideally this would allow for ZVS and for ZVDS which could result in 100% efficiency. The switching amplifier classes (D, E, and F) build upon this ideal model and are able to achieve higher efficiencies in practice than current source amplifiers by using matching networks to shape the waveforms at the drain and gate.

Figure 2.6: RF Power (relative to Class A) and Efficiency versus Conduction Angle [1]

Figure 2.7: Basic Switching Amplifier Circuit and Waveforms[1]

Figure 2.8: Class D Amplifier Circuit and Waveforms[1]

2.3.1 Class D Amplifier

The class D amplifier can be thought of as push pull version of a switching amplifier. The amplifier consists of two transistors to operate as switches to conduct during the positive half and negative half cycle of the input seen in Figure 2.8 [1]. This allows for a full wave drain current to flow through the output load that is filtered through a high Q LC network while the drain voltage is a square wave with 0 overlap between the transistor that is on that allows for ZVS and ZVDS [27]. This allows the class D amplifier to theoretically have 100% drain efficiency. The LC network is tuned to the fundamental frequency of the input. Class D looks effective in theory but suffers due to switching resistances and drain capacitances which limit the maximum frequency of operation to VHF in practice [24].

2.3.2 Class E Amplifier

The class E amplifier builds up on the ideal switch amplifier takes in account for the shunt output drain capacitance and amplification is the result of DC and RF currents that charge the drain shunt capacitance [24]. As seen in Figure 2.9, the switch is turned on from time $-\alpha_1$ to α_2 allowing current to flow solely from

Figure 2.9: Class E Amplifier Circuit and Waveforms[1]

the power supply and the load through the switch and the voltage across the drain capacitance is shorted. Then as the switch is turned off from time α_2 to α_1 the current from the power supply and load will flow through the drain capacitor [1]. To achieve high efficiency, the switching current waveforms are adjusted so that the capacitor current and charge is 0 when the switch is turned on which allows for ZVS and ZVDS conditions allowing for theoretically 100% efficiency. [11].

The class E amplifier produces significant harmonic distortion due to the switching action and the output must be filtered to suppress harmonics [29]. Another concern with using the class E amplifier in practice is the large peak voltages at the drain of the transistor which are around three times the drain supply voltage when the switch turns off [8]. In addition the output drain capacitance limits the frequency of operation that is required to create the proper drain waveforms [27].

2.3.3 Class F Amplifier

The class F amplifier has a theoretical efficiency of 100% through the use of multi harmonic terminations. The theory behind the class F amplifier relies on the generation of odd voltage harmonics and shorting of even voltage harmonics at the drain of

the device to increase the efficiency of the amplifier. By keeping only the odd voltage harmonics of the signal at the output, ideally a square wave would appear and by biasing the amplifier at a conduction angle of pi the amplifier has zero overlap between the current and voltage waveforms and no power consumed when the amplifier is switched on. The harmonics are generated due to the knee voltage of the transistor. When the AC signal causes the transistor to reach saturation the abrupt change in current flow generates voltage harmonics. In practice it becomes challenging to design matching networks as the number of harmonics to control increases. Also the output capacitance of the transistor will eventually short out higher order harmonics so 100% efficiency is not realizable in practice. By controlling up to the 5th harmonic, 90.5% efficiency can be achieved. A more in depth analysis of the class F amplifier follows in the next chapter.

Chapter 3

Class F Detailed Description

The class F amplifier is able to achieve high efficiency by using the harmonics generated during amplification to ideally produce a square wave for the drain voltage and a half sinusoid for the drain current that don't overlap. This allows for ZVS and ZVDS conditions to occur so ideally no power is consumed during amplification. The class F amplifier theoretically capable of 100% drain efficiency but in practice only a finite amount of harmonics can be matched and the drain capacitance will eventually short the harmonics, the actual typical efficiency is around 80% to 90%. Through Fourier series analysis it can be shown that by loading the drain so that odd voltage harmonics see an open circuit and even current harmonics see a short circuit, the ideal current and voltage waveforms conditions will arise [5]. The class F amplifier also has a counterpart, the class F^{-1} in which the current and voltage waveforms are opposite so that ideally the voltage waveform is a square wave and the current is a half sinusoid which will be discussed later in this chapter [16].

3.1 Fourier Analysis

Power amplifiers typically operate in the large signal mode which includes the non-linear region of a transistor. This results in harmonic and intermodulation distortion but can also be used to increase the efficiency of the amplifier. The source of the

Figure 3.1: Transient Waveforms of Class B Amplifier With and Without Knee Voltage [1]

harmonics in power amplifiers is attributed to the knee voltage of the device. The knee voltage essentially clips the peak of the drain current and due to the relatively large discontinuity harmonics are generated [4]. The current source amplifier theory doesn't predict the effect of the knee voltage in analysis but as seen in Figure 3.1 even in the class B amplifier the knee voltage will cause a discontinuity. No rigorous analysis that shows the relation of the knee voltage to the harmonic generation has been done but measurements have verified the presence of harmonics.

For simplified a discussion it is assumed the DC bias of the amplifier is set so the conduction angle is π, like the other switching amplifiers, so the drain current waveform can be modeled as a half sinusoid. It will be shown later that in practice the conduction angle should be close to π but not exactly π but to explain the ideal case the conduction angle should be π. The drain current and voltage waveforms can be modeled as a Fourier series with odd components for the voltage and even for the current as seen in Equations 3.1 and 3.2 [22].

$$i_d(t) = I_{DD} - I_{f0}sin(\omega t) - I_{2f0}sin(2\omega t) - I_{4f0}sin(4\omega t) + \ldots \tag{3.1}$$

$$v_d(t) = V_{DD} + V_{f0}sin(\omega t) + V_{3f0}sin(3\omega t) + V_{5f0}sin(5\omega t) + \ldots \tag{3.2}$$

From Equations 3.1 and 3.2, four new parameters: $\gamma_v, \gamma_i, \delta_v$ *and* δ_i relate the fundamental and peak amplitude to the DC component for the drain and voltage.

Table 3.1: Various Parameters of Maximally Flat Waveforms for Class F Amplifier

Equation	Description
$\gamma_v = \frac{V_{f0}}{V_{DD}}$	Voltage Ratio of Fundamental Amplitude to DC Amplitude
$\gamma_i = \frac{I_{f0}}{I_{DD}}$	Current Ratio of Fundamental Amplitude to DC Amplitude
$\delta_v = \frac{v_{max}}{V_{DD}}$	Ratio of Maximum Drain Voltage to DC Amplitude
$\delta_i = \frac{i_{max}}{I_{DD}}$	Ratio of Maximum Drain Current to DC Amplitude
$Z = \frac{V_{f0}}{I_{f0}}$	Optimal Impedance at Fundamental for Max Power Transfer
$P_{o,f0} = \frac{V_{f0}^2}{2Z} = \frac{\gamma_v^2 V_{DD}^2}{2Z}$	Output Power at Fundamental
$P_i = V_{DD} I_{DD} = \frac{\gamma_v V_{DD}^2}{\gamma_i Z}$	DC Input Power
$\eta = \frac{P_{o,f0}}{P_i} = \frac{\gamma_v \gamma_i}{2}$	Drain Efficiency

These parameters can be used to define the ideal load at the fundamental frequency, RF output power at the fundamental frequency, DC input power, and the drain efficiency seen in Table 3.1 from [22]. The key take away from the all equations this is that the drain efficiency can be described as a function of γ_v and γ_i, which are the voltage and current ratios at the fundamental frequency to the DC amplitude.

The γ and δ parameters can be extended for all the harmonics and is used to describe what is called maximally flat waveforms. The term maximally flat refers to the ideal scenario were all the odd harmonics of the drain voltage see an open circuit and the even harmonics of the voltage are shorted. And all the even harmonics of the drain current see a short circuit and the odd harmonics are shorted at the drain which results in the square wave for the drain voltage which has a flat top that doesn't overlap with the half sinusoid drain current seen in Figure 3.2. The ideal waveforms allow for the ZVS and for ZVDS condition to occur so zero power would be consumed in the switching operation and all of the DC input power would be used to increase the input power so the PAE would also be 100%.

Fourier series analysis can be used to determine the amplitudes of each harmonics in Equation 3.1 and 3.2 for a maximally flat waveform. In the ideal case were infinite number of odd voltage harmonics can be properly terminated, the amplitude of the

Figure 3.2: Ideal Class F Waveforms [28]

each harmonic is that of a square wave seen in Equation 3.4. For the ideal case for terminating all the even current harmonics, the amplitude of each harmonic is equal to that of a half sinusoid in Equation . For the ideal case, $\gamma_v = \frac{4}{\pi}$ and $\gamma_i = \frac{\pi}{2}$ and from Table 3.1, $\eta = \frac{\gamma_v \gamma_i}{2} = \frac{\frac{4}{\pi}\frac{\pi}{2}}{2} = 100\%$. The efficiency is dependent on the input power because of required harmonic level to produce the maximally flat waveforms. As input power is backed off, the harmonic levels and efficiency drops as well and the class F amplifier becomes more like a class A amplifier. The class F amplifier has a counterpart, the class F^{-1} amplifier which swaps the voltage and current waveforms so the ideally the drain current is a square wave and the voltage is a half sinusoid.

In practice, a matching network to terminate infinitely many harmonics is impossible and the output drain capacitance of the transistor will short out higher harmonics. Typically as a compromise between feasability and efficiency, up to the third harmonic is terminated which is called third harmonic peaking. This is more common in class F amplifiers that operate in the couple of gigahertz which can take advantage of the high transition frequency of new technologies like high electron

Table 3.2: Maximum Efficiency of Class F Amplifier

Harmonics	$n = 1$	$n = 3$	$n = 5$	$n = \infty$
$m = 1$	50.0%	57.7%	60.3%	63.7%
$m = 2$	70.7%	81.7%	85.3%	90.0%
$m = 4$	75.0%	86.6%	90.5%	95.5%
$m = \infty$	78.5%	90.7%	94.8%	100%

m,n are the maximum order of drain current and voltage harmonics

mobility (HEMT) transistors. In the high frequency (HF) and very high frequency (VHF) domain, higher harmonics are present and are typically more efficient than their gigahertz counterparts.

To solve for the harmonic amplitude of each component when only a finite number of harmonics are terminated, the derivatives of Equation 3.2 and 3.1 are solved with the condition at $\omega t = \frac{3\pi}{2}$, $v_d = 0$ and all higher harmonic amplitudes are set to 0. For example for terminating up to the third harmonic, the second derivative for the voltage, seen in Equation 3.3, with the conditions applied is $0 = V_{f0} - 9V_{3f0}$, therefore $V_{3f0} = \frac{1}{9}V_{f0}$. Then using Equation 3.2 with the same conditions, $V_{f0} = \frac{9}{8}V_{DD}$ and $V_{3f0} = \frac{1}{8}V_{DD}$. The same process applied to the current waveform results in $I_{f0} = \frac{4}{3}I_{DD}$ and $I_{2f0} = \frac{1}{3}I_{DD}$. The drain efficiency for terminating up to the third harmonic can now be calculated, $\eta = \frac{\gamma_v \gamma_i}{2} = \frac{\frac{9}{8}\frac{4}{3}}{2} = 75\%$. A table of how efficient the class F amplifier for a finite number of harmonic terminations can be seen in Table 3.2. Going back to the current source amplifiers, the class A amplifier only controls the first harmonic of the current and voltage and from Table 3.2 it's only 50%. The class B amplifier controls only the first voltage harmonic and ideally all of the current harmonics and is ideally 78.5% efficient.

$$\frac{d^2 v_d}{d\theta^2} = -V_{f0} sin(\omega t) - 9V_{3f0} sin(3\omega t) - 25V_{5f0} sin(5\omega t) + \dots \tag{3.3}$$

$$V_{mf0} = \frac{4}{m\pi} \begin{cases} 0, & \text{if } m = even \\ 1, & \text{if } m = odd \end{cases} \tag{3.4}$$

Figure 3.3: Drain Voltage Waveform with In Phase and Out of Phase Third Harmonic [4]

3.2 Practical Implementation

A key factor that is missing from the Fourier analysis of the waveforms is the phase relation between the harmonics, if all of the harmonics are in phase the amplifier will have a much lower efficiency due to destructive interference. This can especially be seen in third harmonic peaking amplifiers seen in Figure 3.3. The right part of the figure shows the drain voltage if the third harmonic is in phase. This results in triangle wave instead of a square wave which would overlap with the half sinusoidal current. The left part of the figure shows the drain voltage with an out of phase third harmonic which results in the proper square wave shape. Going back to Figure 2.5, in order for the third harmonic to be out of phase the class F amplifier must be biased between so the conduction angle is between π and 2π. Within these conduction angles, the third harmonic is negative relative to the fundamental so it is out of phase. For conduction angles less than π, the third harmonic will be in phase and will result in a loss of efficiency. In practice, the class F amplifier is biased in the so called "deep AB" region so that it slightly greater than a conduction angle of π so the drain current will still resemble a half sinusoid shape and the voltage waveform will be maximally flat.

The design of a class F amplifier starts with finding a suitable "deep" AB bias with sufficient gain for the application. Then applying a load pull at the fundamental frequency to determine the optimal load impedance, and then a source pull at the fundamental frequency for the optimal source impedance. Load pulling and source pulling are measurements that measure the s-parameters of a device while applying it

to a uniformly sampled smith chart on the load and source side while the source and load impedance respectively is held constant. Simulated load pulls require accurate device models to be of any use and to take real world load pull measurements are time intensive without automated test equipment. After determining the optimal load and source impedances, a harmonic phase load pull is done which is similar to a load pull, but applied to a harmonic frequency and the smith chart is sampled uniformly in phase at a constant gamma value. For the class F amplifier to keep the drain current and voltage harmonics at the drain, the odd harmonics have to see a open and the even harmonics a short.The harmonic phase load pulls are done at a reflection coefficient value of 1 and swept to measure the transistor efficiency if the harmonics are terminated properly. This process is usually iterated until a proper bias is found that allows for sufficient gain and the load pulling results in the desired efficiency.

3.3 Matching Networks

The matching network for a class F amplifier can be down with passive components, some closed form methods use the output drain capacitance and impedance as parameters to come up with matching networks but this has only been shown to work in sub 1 GHz band [6]. Multiple papers show that the output capacitance is non-linear at higher frequencies and some work has explored methods to make compensate for the non-linearity using varactors [14]. The most common methods rely on resonant transmission line matching networks which are intuitive to a certain degree. The simplest transmission line matching network for the class F amplifier uses a quarter wavelength line at the drain to a tuned load as seen in Figure 3.4. The tuned load is such that at odd harmonics it appears as a short and even harmonics an open, so when reflected back at the drain the odd harmonics see an open and even harmonics a short [5]. In practice with this type of matching network, the impedances of the various sections are parameterized and are left to be found by an optimizer using simulation software. It's also been experimentally determined that a harmonic matching network at the input of the transistor increases the efficiency over just having a matching network at the output [2].

Figure 3.4: Quarter Wavelength Matching Network for Class F Amplifiers

Chapter 4

Class F Amplifier ADS Simulations, Comparisons to Specs

The initial goal of the class F amplifier design was to try and control up the fifth harmonic which would ideally allow 90.5% drain efficiency and to have a center frequency of 5 GHz. After looking through the past amplifier competitions and looking at various RF transistor manufacturers, the Wolfspeed CGHV1F006S GaN HEMT transistor was chosen. This model was chosen over others to the relatively new release of the transistor, the high operating frequency of the transistor (18 GHz), and the fact that the transistor came in a QFP package versus a semiconductor die. The majority of past winners of the amplifier competition used Cree (now Wolfspeed) transistors and Wolfspeed provides a transistor level models for simulations to help design amplifiers. The design goals are in Table 4.1, the initial goals were relatively aggressive in trying to push the PAE and center frequency for the highest figure of merit. After simulating, fabricating, and testing multiple versions the design goals were set to a more conservative value. This chapter discusses the simulations results of the final version of the amplifier. The initial design would have had a figure of merit of 120 which would be 10 points higher than the previous highest score in the competition. The final amplifier on the other hand would have a figure of merit of 92 which is still competitive with the past years submissions.

Table 4.1: Design Goals of Amplifier

Parameter	Initial Goal	Final Goal
Center Frequency, GHz	5	3
PAE at Input Power, %	80	70
Output Power, dBm	>36	>36
Input Power, dBm	24	15
Input and Output VSWR	<2	<2

The initial design was pushing the limits of the specification by attempting to achieve the minimum output power with the highest allowed input power. This was risky because designing for the minimum gain allows for little margin for non-ideal factors that couldn't be taken into account of the simulation. The first amplifier that was fabricated had a simulated gain of 12 with a PAE of 80.1% at an input power of 24 dBm. The amplifier initially had a short from the drain and had to be reheated with the a heatgun multiple times to fix the short. Once the amplifier was working the measured gain was only 10 dB so even at the maximum allowed input power of 24 dBm, it would not be able to deliver 36 dBm of power. For the final version of the amplifier, the design margins were increased substantially to compensate for fabrication issues and to ensure a working amplifier would be built even if the score was lower.

4.1 DC Bias Point

The simulation of the various parts of the class F amplifier was done using Keysight ADS 2016. The first step in the simulation process was determining the optimal DC bias. Using the provided transistor model from Wolfspeed, various drain and gate voltages were simulated to predict the drain current and transducer gain of the transistor using the circuit seen in Figure 4.1. The bias for the class F amplifier should be in the "deep" AB region so the drain current resembles a half sinusoid shape but still allows for the negative third harmonic to be present. The drain current should

Table 4.2: Maximum Operating Parameters of CGHV1F006S Transistor

Parameter	Rating
Maximum Drain-Source Voltage, V	100
Maximum Drain-Source Current, A	0.95
Maximum Gate-Source Voltage, V	-10,+2
Maximum Gate-Source Current, mA	1.2

be minimized in order to maximize the PAE of the amplifier. The competition rule states the amplifier should have a minimum of 36 dBm output power at a maximum of 24 dBm input power resulting in a minimum gain of 12 dBm. For the final amplifier, the target gain was 21 dB at input power of 15 dBm so there would be a margin for various effects that wouldn't be able to be taken into account in the simulation like the fabrication process. So even if the gain was lower than 21 dB, at higher input power the amplifier would still be able to output at least the 36 dBm required.

The transistor maximum operating ratings can be seen in Table 4.2. A starting point to select the gate voltage is to choose a value so the drain current is 10% of the maximum current so the conduction cycle is close to π. The final version of the amplifier had a gate source voltage of -2.4 V which in Figure 4.2 is in the "deep AB" region of the device and draws only 80 mA of quiescent current compared to the maximum drain current of 0.95 A. The drain-source voltage was chosen to be 40 V because it's the recommended operating voltage from the datasheet for the transistor. After the gate voltage was selected, the stability factor (k) and the stability measurement (Δ) were then simulated to see what the stability of the amplifier is near the center frequency seen in Figures 4.3 and 4.4 respectively. For an amplifier to be unconditionally stable, k must be greater than one and Δ be positive, and because k is less than one the amplifier has potentially unstable regions. The stability regions of the load and source plane were then simulated to determine a starting point for the load and source pulls. The results of the load and source stability regions can be seen in Figures 4.5 and 4.6. The region of stability for both stability circles is outside the circle.

Figure 4.1: Bias Circuit Setup

Figure 4.2: Drain Current versus Drain Voltage for Various Gate Voltages

Figure 4.3: Stability Factor (k) versus Frequency

Figure 4.4: Stability Measure (Δ) versus Frequency

Figure 4.5: Load Stability Circle of Transistor. Stable Region Outside of Circle

Figure 4.6: Source Stability Circle of Transistor. Stable Region Outside of Circle

4.2 Fundamental Load and Source Pull

After determining the DC bias of the amplifier, fundamental load and source pulls are done to determine the optimal load and source impedances for the transistor. Load pulls are done keeping the source impedance fixed and sweeping the load over a uniformly sampled space on the Smith Chart and measuring the transducer gain and PAE. Various gain and PAE contours can be produced by doing load pulls. The process starts with sampling the entire Smith Chart then load pulling again around the region with the highest efficiency contour to find the optimal load impedance. As a starting point the source impedance was set to a low impedance of 10Ω that was within the stable region on the source side. Source pulling is done after load pulling and follows a similar process by keeping the load impedance fixed then sweeping the source impedance for the highest efficiency while still having the target gain. The load and source pulls are done at the fundamental frequency at an input power of 15 dBm to provide an additional margin in the design. In practice the amplifier the amplifier will require a higher input power to achieve the simulation results due to losses that could not be simulated in ADS. Also for the fundamental load and source pull, the source and load impedances for the higher harmonics are shorted.

For the sake of brevity only the final load and source pull results are shown but the general process will be described. The initial load pull results showing PAE and power delivered contours can be seen in Figure 4.7 and 4.8. The highest power delivered is only 35.45 dBm at a drain efficiency of 35% while the highest PAE 40% results in a power delivered of 35.2 dBm. The PAE should be less than 50% because an amplifier with only the fundamental present is a class A amplifier with a maximum efficiency of 50%. As more harmonics are properly added the power delivered and PAE should increase. The final fundamental load impedance selected from the simulation results was 14.3+j54 Ω.

The next step is the source pull done with the load set to the impedance found in the load pull. The results of the initial source pull can be seen in Figures 4.9 and 4.10. The maximum PAE and power delivered has dropped but this isn't unexpected. The pulling process is iterative and if another load pull was done using a new source impedance, the PAE and power delivered increase from the first load pull. Multiple

Figure 4.7: Initial Smith Chart Load Pull Simulation Results at 3 GHz

Figure 4.8: Initial Reactance vs Resistance Load Pull Simulation Results at 3 GHz

iterations are required to fine tune the parameters because they are dependent on one another. A fundamental source impedance of 3+j3 Ω was chosen for the final amplifier configuration as a compromise between high PAE while still delivering over 36 dBm of power.

4.3 Harmonic Load and Source Pulls

The load and source pulls are done at the fundamental frequency while the harmonic pulls are done at the higher harmonics. The process starts with the second harmonic load pull with the fundamental load and source impedances set to the values determined in the previous section. The source impedance at the second harmonic and all the higher harmonic impedances are set to 0 Ω. After determining the optimal load for maximum PAE while still delivering enough output power, a source pull is done at the second harmonic with the optimal load. This process is then repeated for at the third harmonic. After all of the load and source pulls, one last load pull is done at the fundamental to confirm an the increase of PAE and power delivered at the fundamental frequency. The final fundamental load pull can be seen in Figure 4.11 and 4.12. At the highest power delivered of 38.9 dBm the PAE is 69% while at the highest PAE of 79% the output delivered is 36.9 dBm.

A table of the load and source impedances used for the final amplifier configuration can be seen in Table 4.3. The final amplifier had an output power of 37 dBm with 22 dB of gain and a PAE of 79.25% resulting in a figure of merit of 104. While the figure of merit is not the highest compared to the past winners, it is still competitive. The drain efficiency of the final amplifier is 79.2% which is close to the theoretical maximum of 81.7%. The simulated harmonic pulls are used to determine the maximum theoretical performance that can be extracted from the transistor. The PAE and output power of the amplifier with physical transmission lines will be less than the ideal case.

Figure 4.9: Initial Smith Chart Source Pull Simulation Results at 3 GHz

Figure 4.10: Initial Reactance vs Resistance Source Pull Simulation Results at 3 GHz

Table 4.3: Final Harmonic Impedances for Amplifier

Frequency, GHz	Load Impedance, Ω	Source Impedance, Ω
3	14.3+j54.0	3+j3
6	1.4+j37.0	3-j55
9	0.3+j13.4	0.5-j2.6

Figure 4.11: Final Fundamental Load Pull on Smith Chart

Figure 4.12: Final Fundamental Load Pull Fix This Label

4.4 Harmonic Matching Network

The harmonic matching network is the key in keeping the proper harmonics at the drain. It is composed of a matching network and a wave shaping network that is on the load and source side of the transistor. The wave shaping network consists of a series section that is a quarter wavelength long with an eight wavelength open shunt stub. An additional series element is added that is used for tuning that goes to a two more stubs that used for the second harmonic and bias circuitry seen in Figure 4.13. Most class F wave shaping network follow a similar pattern of various fractional wavelength sections so the harmonics at the drain are properly terminated. The downside of these networks is the relatively large electrical lengths due to the presence of a quarter wavelength sections in nearly all such networks. This design explores if coupling the open circuit shunt stubs in the wave shaping network can decrease the electrical size of the class F amplifier. Two versions of the amplifier were simulated, one that uses coupled microstrip lines and one without to compare the overall electrical size of the amplifier. After the wave shaping network comes the matching network so the amplifier is matched as close as possible to 50Ω. This amplifier used a shunt stub and a series transmission line for the matching network on the load and source side. The matching networks were designed to match to 50 Ω.

4.5 Simulated Amplifier

After simulating the maximum theoretical performance of the class F amplifier, the amplifier was simulated using the harmonic matching network discussed previously. Microstrip was chosen as the transmission line to be used for the harmonic matching network because the milling machine that was used to fabricate the boards could only remove the top layer of a copper clad board. Coplanar waveguide was also considered but not chosen because it would greatly reduce the bit life of the fine milling parts. The transmission lines were simulated using Rogers RO3035 with a dielectric constant of 3.5±0.05 with a thickness of 60 mil. R03035 was chosen after comparing various low loss laminates like Duroid from Rogers Corporation. This was partially due to the larger sample size that could be ordered so more amplifier boards

Figure 4.13: Matching Network for Amplifier

could be fabricated. Also it has the lowest tangent loss and dielectric constant that allowed the transmission lines going to the transistor gate and drain to be narrow enough make contact without shorting to the ground pins on the package. Duroid was used for the first version of the amplifier and complications arose due to the width of the microstrip line going in to the transistors drain and gate pins. Using high dielectric constant materials like RT/duroid 6010 with a dielectric constant of 10.2±0.25 resulted in dimensions to narrow to be fabricated on the milling machine. The board discussed in this section is the third revision. The previous two amplifiers malfunctioned with one acting as an oscillator and the other not working at all. This was most likely due to fabrication issues because of the leadless package of the transistor.

Two versions of the amplifier were simulated to compare the electrical length of the harmonic matching network with coupled stubs and without. The harmonic matching network in Figure 4.13 was used as the starting point in the design. The Linecalc tool in ADS used to calculate the quarter, eighth, and twelfth wavelength at the center frequency of 3 GHz on the R03035 laminate. One key element lacking from the fractional wavelength based harmonic matching network is any analysis of

the impedances for the sections of the transmission lines. A majority of papers seem to fix the transmission line length and then leave the impedances of each line to be determined by an optimizer. The load and source side of the matching networks were initially optimized independently of each other. To optimize the load matching network, the source impedance was set to the fundamental value of 3+j3 Ω then the width of the microstrip lines were optimized for maximum PAE and an output power greater than 36 dBm at an RF input power of 15 dBm. The same process was done with the source matching network by fixing the load impedance to 14.3+j54.0 Ω and repeating the optimization. The overall goal for this was to try and approach the global optimum for the load and source matching networks separately and also minimize the number of variables the optimizer in ADS would have to tune. After tuning the load and source sides of the harmonic matching networks independently of one another, both sides were then connected to the transistor. Further optimization was applied to fine tune the performance of the amplifier.

This process was repeated with coupled and not coupled microstrip lines for the shunt stub parts of the harmonic matching network. The total series length of the microstrip lines used in the designs was used to compare the electrical size of the two amplifiers. The total series length of the non-coupled amplifier was 6484 mils while the coupled amplifier was 3735 mils which is a 57.6% reduction in size. While this was only done at a single frequency, bias and matching network; coupling the stubs in the matching network is shown here to reduce the electrical size of the class F amplifier. The original plan for the thesis was to test if coupling the matching networks works for various types harmonic matching networks that use transmission lines. Unfortunately due to time constraints that arose trying to build a working amplifier only one matching network was tested.

The amplifier was simulated using the harmonic balance and large signal s-parameters tools of ADS. Harmonic balance allows for proper simulation of non-linear devices by taking in account harmonic distortion by assuming a Fourier series steady state solution exists for any given circuit. The harmonic balance simulation is done in the frequency domain and is done by exciting the circuit with multiple tones with a given power. Linear elements in a circuit can be solved in the frequency domain while non-linear elements are sampled in the time domain and then converted in the fre-

Table 4.4: Comparison of the Specification and Simulated Performance of Amplifier

Parameter	Specification	Simulation
Center Frequency, GHz	3	3
Input Power for Max PAE, dBm	15	19
Output Power for Max PAE, dBm	>36	37.5
Maximum PAE, %	70	78
Input and Output VSWR	<2	<2

quency domain. This allows for accurate simulation of large signal devices like power amplifiers were inter-modulation and harmonic distortion occurs. If the amplifier was simulated using small signal s-parameters the harmonic generation at the drain of the transistor would not be taken into account because s-parameters uses a small signal model which assumes a non-linear device can be assumed to have linear properties at a specific bias. The large-signal s-parameter simulation uses the harmonic balance simulation results to produce s parameter results of a device.

The simulated drain current and voltage waveforms can be seen in Figure 4.14 which show some partial overlap during switching. Although the waveforms aren't ideal, the amplifier still has high PAE and meets the minimum output power. Even during the off cycle of the drain current, there is still quiescent current flowing which dissipates significant power due to the high drain voltage. Figure 4.15 shows the amplifier performance at 3 GHz from an input power of -30 dBm to 30 dBm. The amplifier is able to achieve an output power of 36 dBm at input powers greater than 11 dBm. The amplifier is able to achieve a peak PAE of 78% at 19 dBm of input power resulting in a figure of merit score of 103. For the high PAE, the amplifier is operating beyond the 1 dB compression point which hints at the presence of intermodulation distortion. The simulated VSWR can be seen in Figure 4.17, and load and source stability circles in Figures 4.18 and 4.19 which show the amplifier is stable at 50Ω at the center frequency.

Figure 4.14: Simulated Drain Current and Voltage Versus Time

Figure 4.15: Gain, PAE, and Output Power versus Input Power

Figure 4.16: Simulated Single Tone IMD

Figure 4.17: Simulated Input (1) and Output (2) VSWR of Amplifier

Figure 4.18: Load Stability Circle of Amplifier. Stable Region Inside of Circle

Figure 4.19: Source Stability Circle of Amplifier. Stable Region Inside of Circle

Chapter 5

Class F Amplifier Fabrication and Test Results, Comparisons to Specs

The final version of the amplifier was milled using the LPFK S62 in the Cal Poly anechoic chamber. One aspect that wasn't taken into account in the ADS simulation was cooling the amplifier during operation. Even when the amplifier is operating at high PAE, it must still dissipate a heat equal to the power that wasn't used to amplify the input signal. The heat dissipation calculations were done assuming the cooling would have to dissipate all of the DC bias power at the highest input power which for the final amplifier was equal to the 170 mA times the bias voltage of 40 V which is equal to 6.8 Watts. The cooling was done with a fan and heatsink mounted on top of the transistor by using the thermal resistance supplied by the manufacturer of the transistor to determine the cooling required. The fan draws 30 mA at 40 volts and was tied to the drain voltage of the amplifier and was included in the PAE measurements of the amplifier. Also to increase the thermal conduction in the final amplifier vias were added underneath the transistor to improve the heat conduction after the board layout was done in ADS. A photo of a previous version of the amplifier that did not have vias can be seen in Figure 5.8. Holes were drilled adjacent to the amplifier and copper tape was soldered from the ground pin on the top layer to the bottom layer was used to conduct the heat. The vias proved far superior in conducting heat

because they were able to place directly underneath the transistor allowing the heat to be conducted to the ground plane with less thermal resistance.

The bias network for the final amplifier used grounded shunt caps on the quarter wavelength stubs to create RF shorts. The DC bias was then fed through the quarter wavelength stubs through a series wideband spiral inductor. Two previous versions of the amplifier were built but due to the challenge of soldering the leadless package of the transistor they were damaged most likely due to shorts and insufficient cooling. The bias inductors, coupling capacitors, and transistor was mounted on the board using solder paste and a heatgun. SMA connectors were soldered on the input and output traces and banana plugs were soldered to the DC bias pads to comply with the competition rules. The final build of the amplifier without the fan can be seen in Figure 5.1 and with the fan in Figure 5.2. The amplifier was measured with an Anritsu MS4622B and the drain powered with an Agilent Power Supply E3640A with the drain current being measured by an Agilent Multimeter Agilent U3606A. The gate voltage was powered by an Agilent Power Supply E3630A. After tuning the gate bias and measuring the amplifier performance, a final gate voltage of -2.66 V for the amplifier. A photo of the test setup can be seen in Figure 5.7.

For the RF measurements the VNA was calibrated from 2 GHz to 4 GHz and set to average ten samples. A 20 dB attenuator was put at the output of the amplifier so the VNA would not be damaged by the high RF output power. The 20 dB attenuator was measured so the attenuation could be removed and the amplifier gain could be properly measured. The measured center frequency of the final amplifier was 2.91 GHz and the various measured parameters of the amplifier can be seen in Figure 5.4. The VNA used to measure the amplifier was only able output a maximum of 20 dBm of power compared to the competition maximum of 24 dBm input power which limits the maximum PAE the amplifier can achieve.

The amplifier s-parameters and drain current was measured over a wide range of input powers from -30 dBm to 20 dBm. Only the input VSWR seen in Figure 5.3 could be measured properly. The 20 dB attenuator at the output resulted in erroneous output VSWR when de-embedded which is most likely due to the reflection from the attenuator being larger than the reflection from the output of the amplifier. The amplifier had the best input match at slightly below the center frequency at 2.89

Figure 5.1: Photo of Final Amplifier Without the Fan

Figure 5.2: Photo of Final Amplifier With the Fan

Figure 5.3: Measured Input VSWR of Final Amplifier

GHz with a VWSR of 1.11 and at the center frequency of 2.91 GHz the VSWR was measured to be 1.9.

The final amplifier was able to output a maximum of 37 dBm at an input power of 20 dBm and a PAE of 59.8% resulting in a figure of merit of 78. The amplifier is able to output 36 dBm at input powers 18 dBm or greater which is 3 dB more than the design goal. The amplifier most likely has a maximum PAE in the 70% range at the maximum allowed input power of 24 dBm from looking at the increase in input power from 15 dBm to 20 dBM, the PAE increases from 36% to 60%. The amplifier has 19 dB of gain from -30 dBm to 15 dBm of input power and shows gain compression beyond 15 dBm seen in Figure 5.4.

To qualify for the IMS competition the amplifier carrier-to-interference (C/I) ratio must be greater than 30 dB using two 5 MHz spaced tones at an input power of 0 dBm. The C/I was measured by taking an intermodulation distortion measurement of the amplifier from 2.8 GHz to 3 GHz seen in Figure 5.6. The IMD was well below the required 30 dB and was around -80 dB across the entire frequency band. The output third order intercept (OIP3) was calculated using the IMD measurement, and

Figure 5.4: Measured Parameters of Final Amplifier

can be shown in Figure 5.5. At the center frequency of 2.9 GHz the OIP3 is around 55 dBm.

A comparison of the amplifier measurements and the design specifications can be seen in Table 5.1. It should be reiterated that it was expected the fabricated amplifier would require a higher input power than the design specification to take in account non-idealities that could not be taken into account in the simulation. The amplifier has a lower center frequency than expected but at a fixed PAE it amounts to less than a one point difference in the figure of merit. Overall while the amplifier may not have met all of the design specifications, it is still a functional class F amplifier that can compete in the design competition.

A major challenge of the thesis was finding equipment to measure the amplifier. Only one of the signal generators in the microwave laboratory was able to output 24 dBm at 3 GHz. Some of the equipment that was rated to output the RF power needed to measure the amplifier was measured on signal analyzers to be much less. No equipment was able to do the two tone test at a high power and will have to be done at the conference. The two-tone intermodulation distortion measurement had to be done on the Antritsu MS4622B VNAs which had a maximum output power of

Table 5.1: Comparison of the Specification and Measured Performance of Amplifier

Parameter	Specification	Measured
Center Frequency, GHz	3	2.9
Input Power for Max PAE, dBm	15	20
Output Power for Max PAE, dBm	>36	37
Maximum PAE, %	70	59.8
Input and Output VSWR	<2	<2

Figure 5.5: Measured Output Third Order Intercept of Final Amplifier

Figure 5.6: Measured Intermodulation Distortion of Amplifier Using 2 Tones 5 MHz Apart

7 dBm. Fortunately to qualify for the competition, the carrier-to-interference (C/I) specification of greater than 30 dB at 0 dBm input power was able to be measured.

Figure 5.7: Photo of Test Setup

Figure 5.8: Photo of Previous Version of Amplifier

Chapter 6

Conclusion, Future Projects

The process of designing a power amplifier through the iterative process of simulation, fabrication, and measurement was a great learning experience. The final version of the amplifier was able to meet the specifications required from the competition. For students that are looking to compete in the future it is recommended that they explore the Doherty amplifier configuration. The Doherty amplifier was not discussed in this thesis but was explorered during the literature search. The Doherty amplifier is able to maintain high PAE and drain efficiency over a wide range of input powers and with lower inter-modulation distortion than a class F amplifier by using two amplifiers with different bias points. The author decided not to pursue to the Doherty amplifier configuration due to the complexity required and time constraints. The past competition winners that have used the Doherty amplifier have always been a group endeavour with a group member assigned to each amplifier then another to combining the amplifiers in the Doherty configuration. The class F amplifier seems to be better suited for applications with a fixed transmission power because then the high efficiency will always be maintained. Also the class F amplifier seems better for systems that use constant amplitude modulation schemes like CW, FM, or FSK due to high degree of non-linearity which make's it challenging to use for modulation schemes that use phase to transmit information.

Another aspect not discussed in this thesis is active gate biasing. Wolfspeed, the manufacturer of the transistor used, recommends changing the gate voltage 0.4 mV

per degree Celsius in order to maintain a constant drain current. The efficiency of the amplifier would most likely be increased if this was done but due to time constraints only a constant bias voltage was used during testing. Wolfspeed has an application note that has an example circuit for an active gate bias power supply. Digital predistortion could also be investigated to reduce the intermodulation distortion (IMD) of the class F amplifier. Digital predistortion is not allowed for the IMS design competition but would be an interesting avenue to investigate.

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