

Qatec  
2/2/93

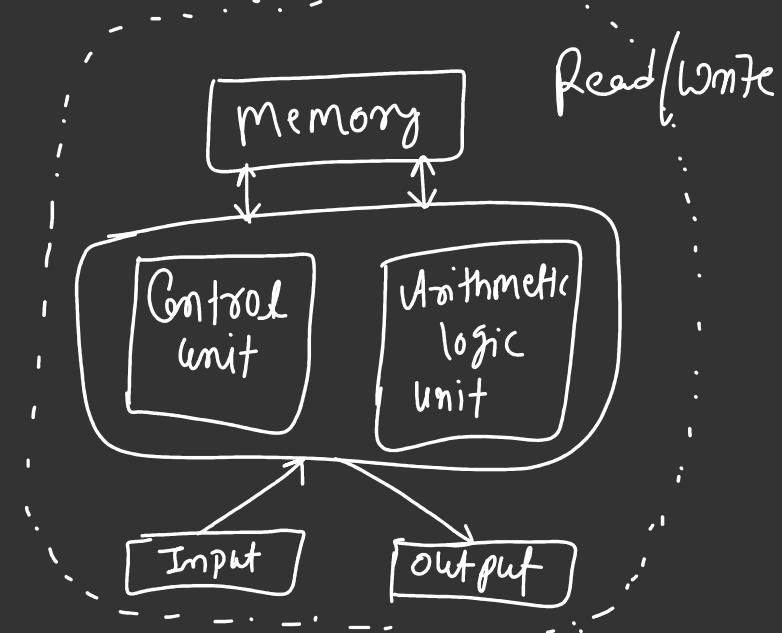
## { Parallel & Distributed Computing }

### { Von Neumann Architecture }

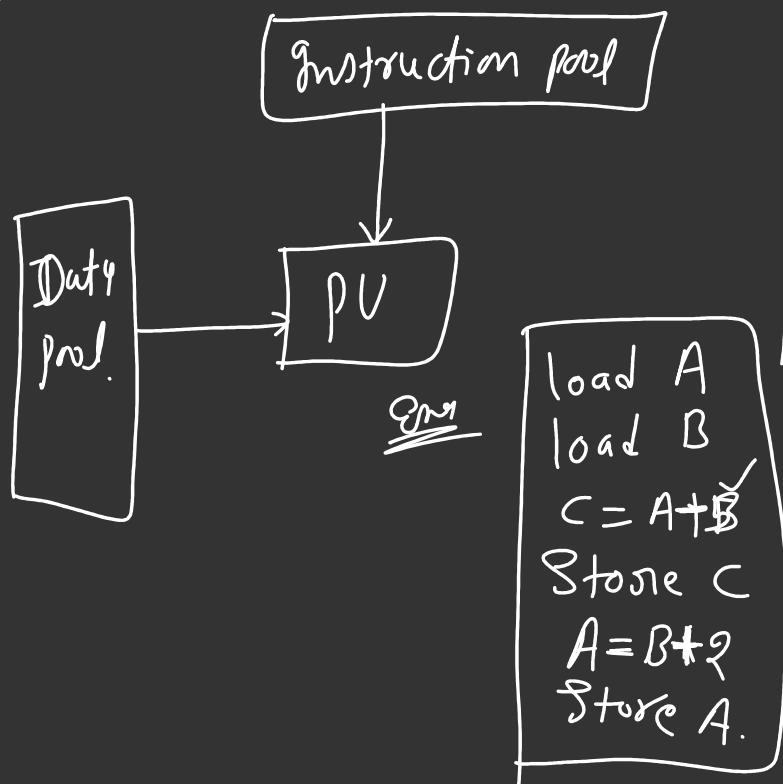
Flynn's Classical taxonomy ::

There are no. of different ways to classify Parallel Computers based on Instruction & Data Stream.

(Single | Multiple)



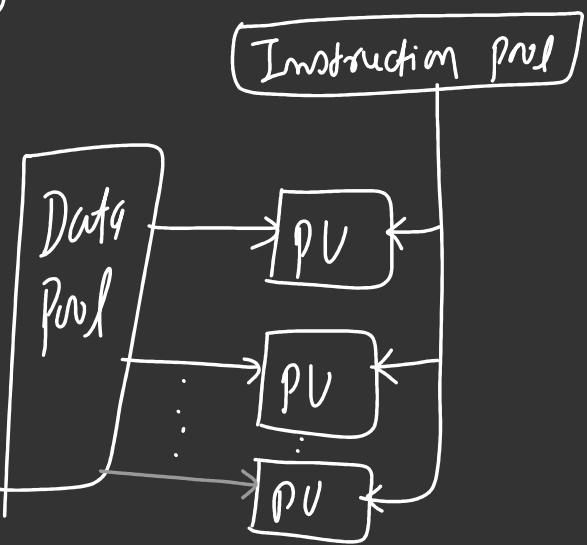
§ SISD ::



SISD Single Instruction Single data	SIMD Single Instruction Multiple Data
MISD multiple Instruction Single Data	MIMD multiple Instruction Multiple data Stream.

Serial Computer

SIMD:

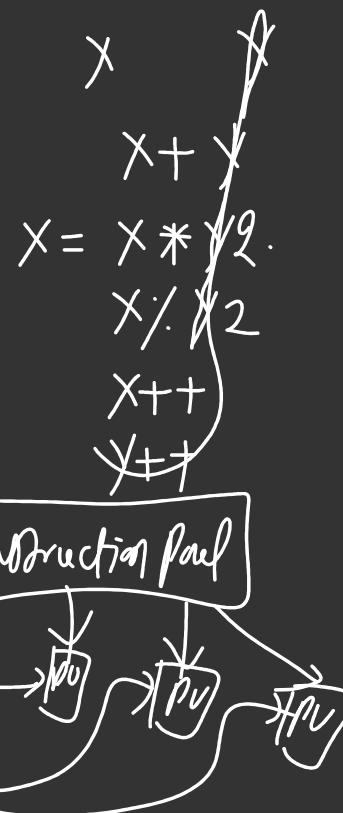
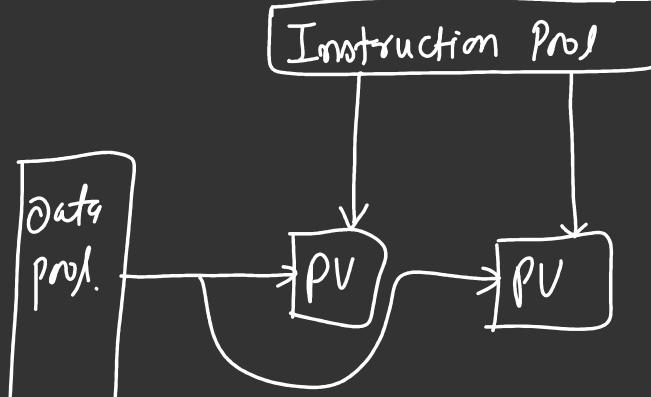


$$X[n] = [x_n \ | \ \dots \ | \ x_3 \ | \ x_2 \ | \ x_1]$$

$$Y[n] = [y_n \ | \ \dots \ | \ y_3 \ | \ y_2 \ | \ y_1] =$$

$$Z[n] = [x_n + y_n \ | \ \dots \ | \ x_3 + y_3 \ | \ x_2 + y_2 \ | \ x_1 + y_1]$$

MISD:



$x = x * y$

$x \% y$

$x++$

$y++$

Instruction pool

MIMD

$x + y$

$x * y$

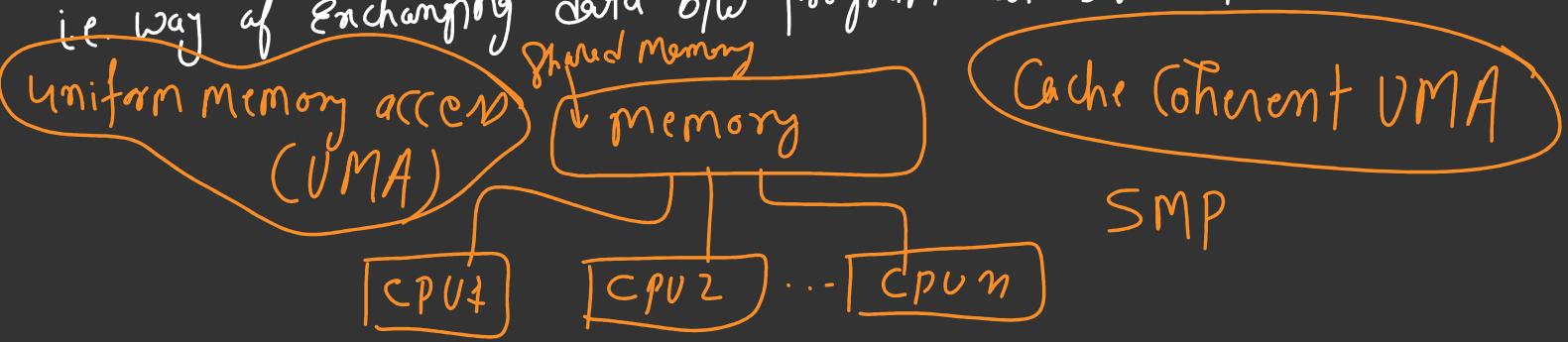
$x + a$

$a \% b$

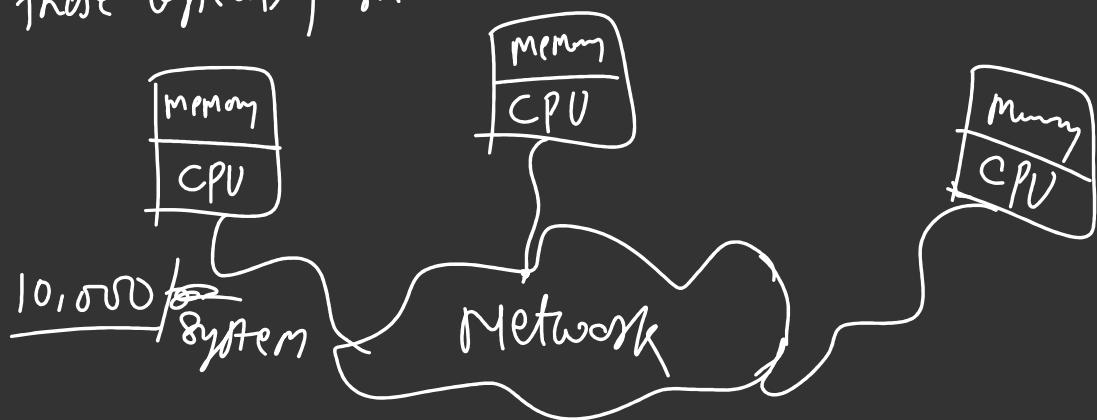
⋮

## § Shared memory v/s Distributed Memory :-

- Shared memory is memory that may be simultaneously accessed by multiple processors/programs with an intent to provide communication among them or avoid redundant copies.
- Shared memory is either a method of Interprocess Communication (IPC) i.e. way of exchanging data b/w program at same time.

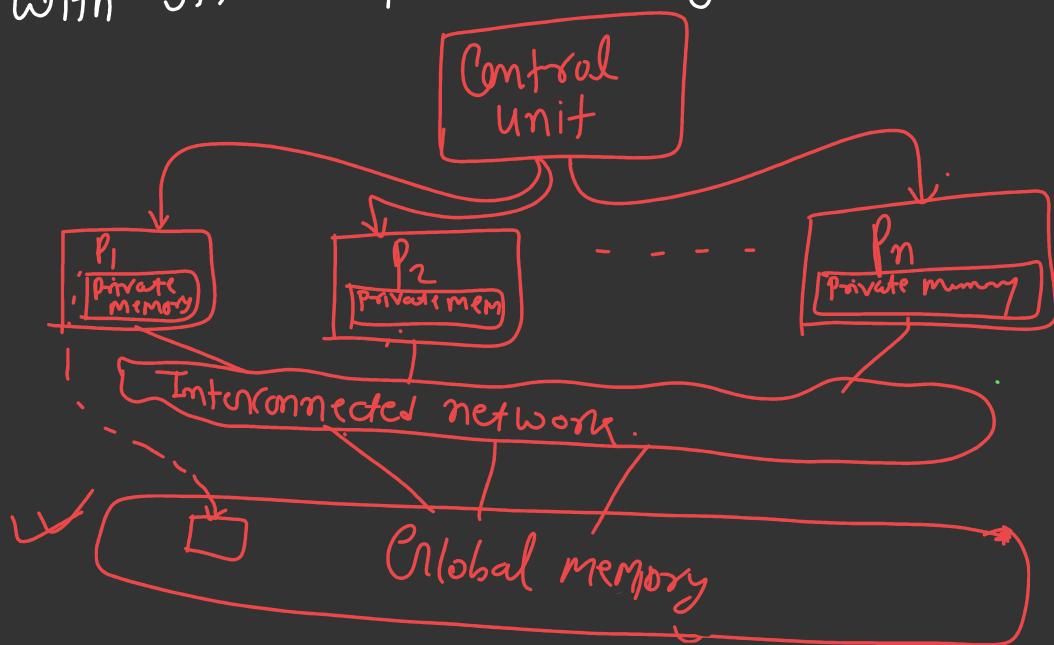


- Distributed Memory is a physical memories are logically shared over large address space via network.
- So the process going to access the physical memory through these logically shared address space.



IAAS ✓  
SAAS ✓  
PAAS

§ Parallel Random Access Machine (PRAM) :: A PRAM consists of a Control unit, global memory, and unbounded set of processors each with its own private memory.



Conflict :: Read/Write

EREW (Exclusive read Exclusive write) :: Read/Write Conflict not allowed.

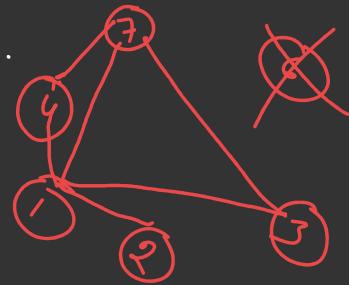
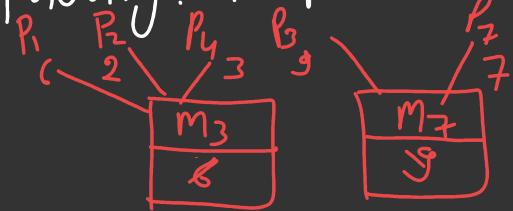
CREW (Concurrent read Exclusive write) :: multiple processor allows to read but write not allowed.

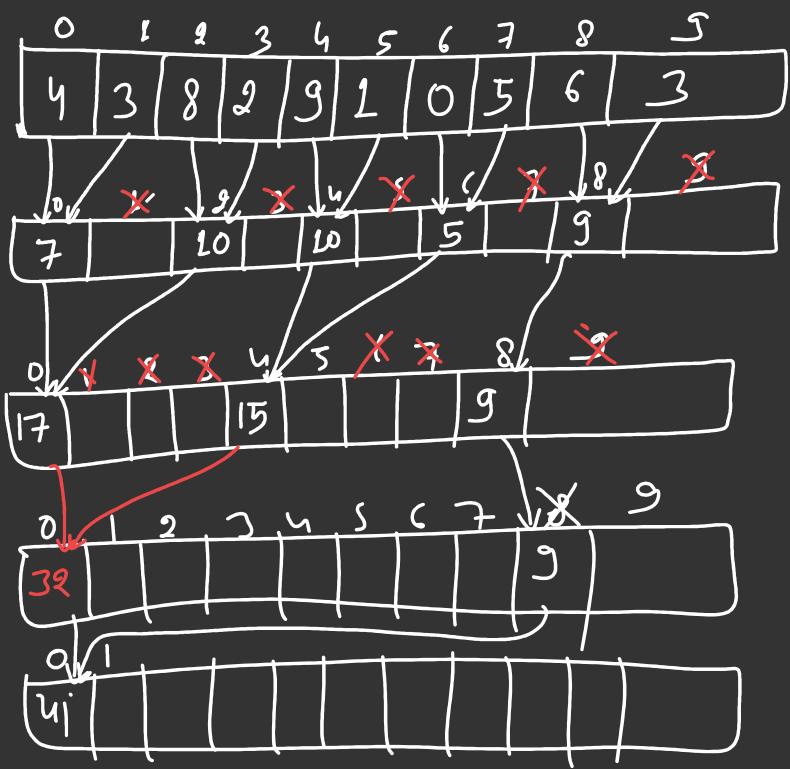
CRCW (Concurrent read Concurrent write) :: Resolve Concurrent writing

- Common :: Write Same Values.

- Arbitrary :: Election Comes in picture & winner will write.

- Priority :: The processor with lower index will write.



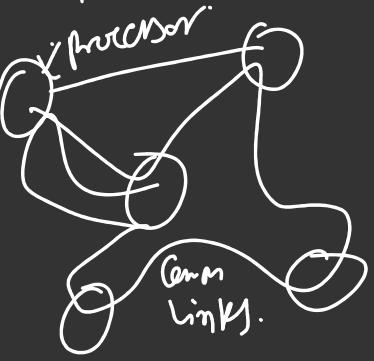


Handwritten notes to the right of the arrays:

- Top row: 4, 3, 8, 2, 9, 1, 0, 5, 6, 3
- Second row: 7, 10, 10, 5, 9
- Third row: 17, 15, 15, 9
- Fourth row: 32, 1, 2, 4, 5, 6, 7, 9
- Fifth row: ui
- Bottom row: 41, 15, 32, 17

Basic Architectures: A processor organization can be represented by a graph in which the nodes represent processors & edges represent communication links.

- Diameter of graph: Largest distance b/w two nodes.
- Bisection width: Bisection width of a network is minimum no. of edges that must be removed in order to divide the network into two halves.



1) Mesh Network :: 2D Mesh.

$$q = 2$$

$$\text{no. of processors} = k^q.$$

$$\text{Diameter of network} = 6$$

$$q(k-1)$$

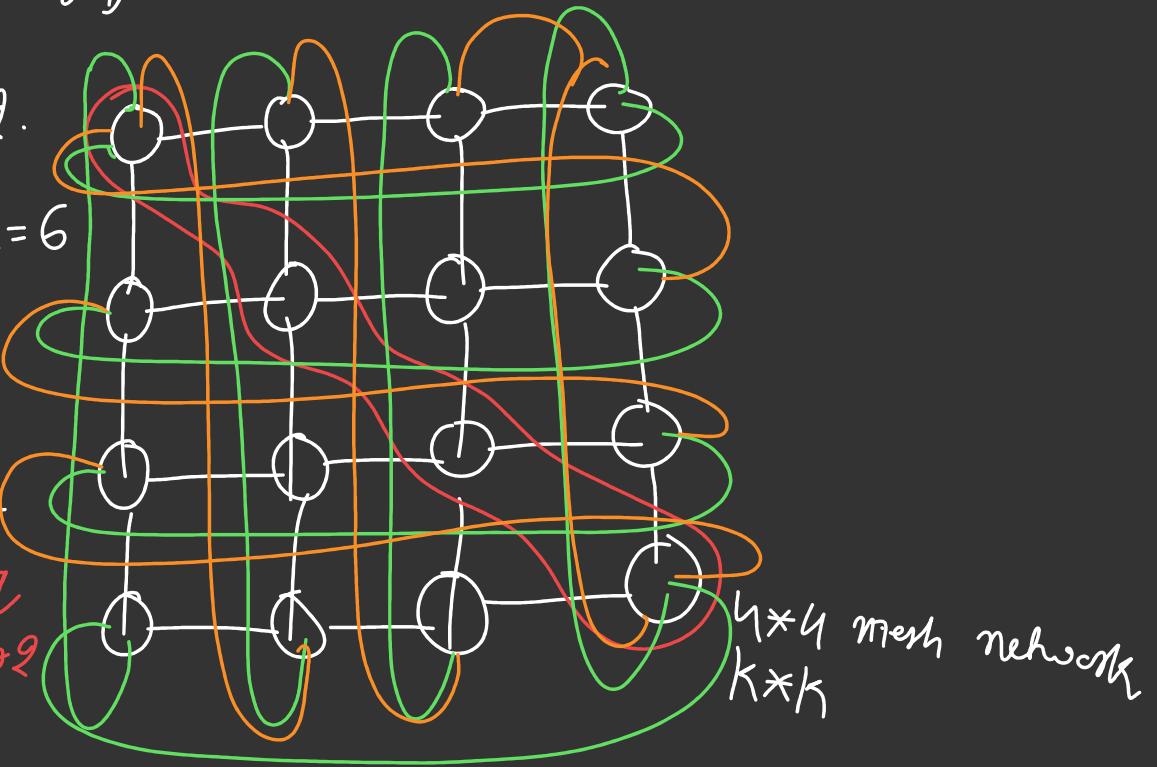
$$2(u-1)$$

$$2 \times 3 = 6$$

$$\text{Bisection width} = 2^q$$

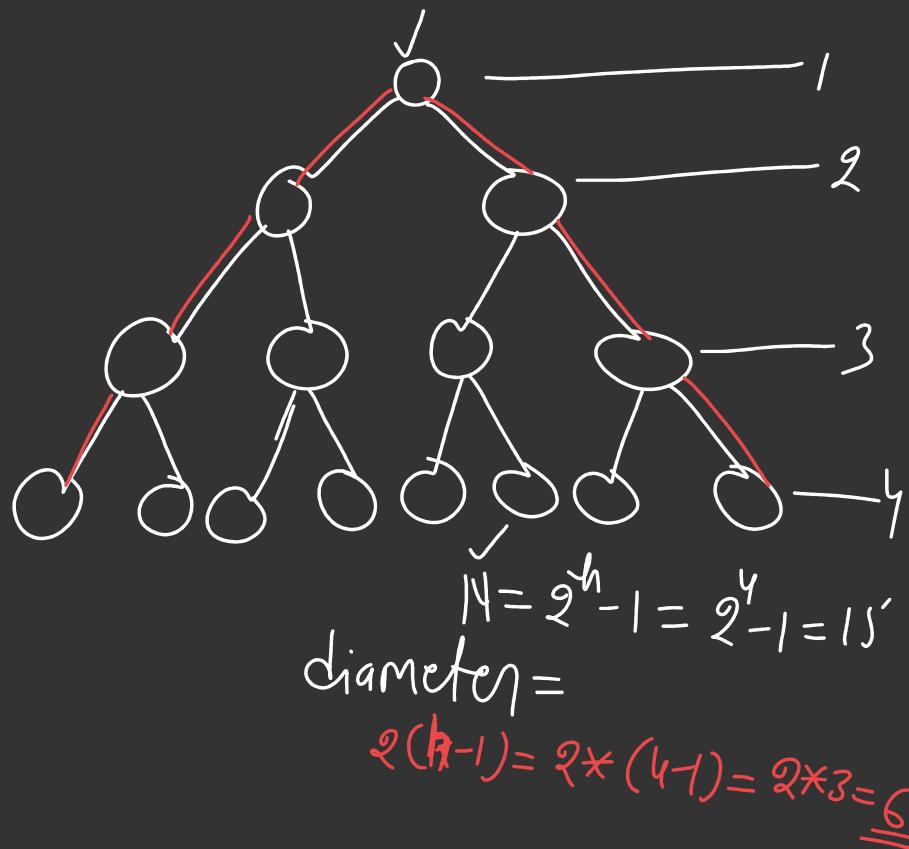
$$= 2 \times 2$$

$$= 4$$



Binary tree network:-

Diameter = minimum M

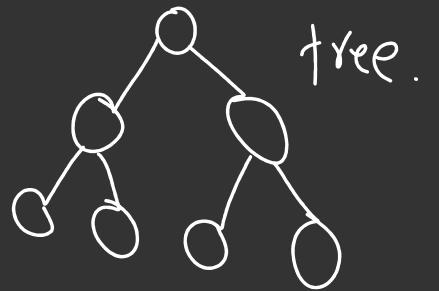
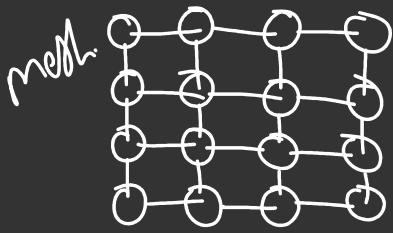


$$N = 2^h - 1 = 2^4 - 1 = 15$$

diameter =

$$2(h-1) = 2 \times (4-1) = 2 \times 3 = \underline{\underline{6}}$$

Pyramid Network..



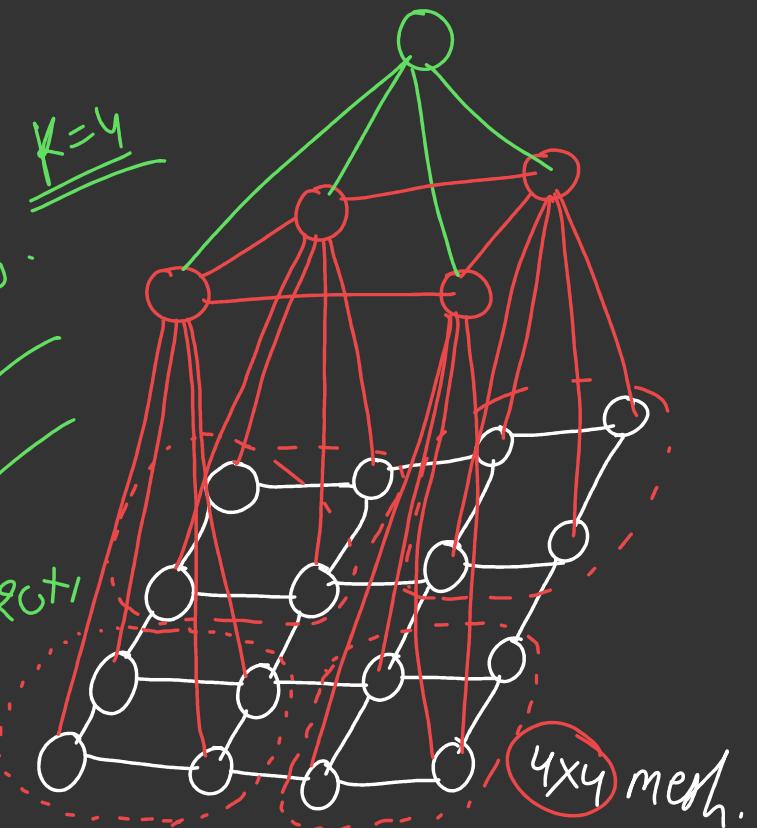
No. of processors

$$= \frac{4}{3}(K^2 - 1) + 1$$

$$= \frac{4}{3}[16 - 1] + 1$$

$$= \frac{4}{3}[15] = \frac{60}{3} = 20 + 1$$

$$\boxed{\text{Nodes} = 21}$$

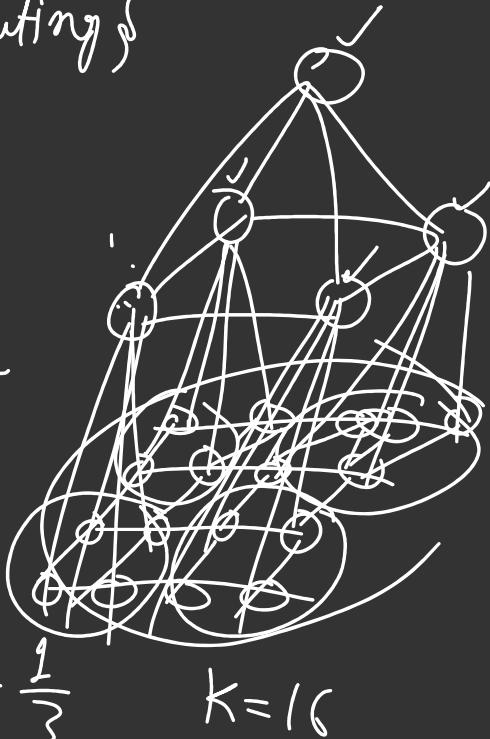


Date) 03/02/23  
Pyrat

# § Parallel & Distributed Computing §

Pyramid Network:

$$\frac{4*16}{3} - \frac{1}{3} = \frac{64-1}{3} = \frac{63}{3} = \underline{21}$$



$$\frac{4}{3}\pi r^3 = \frac{1}{3}$$

{ Hypercube Interconnection Network:

$n=1$

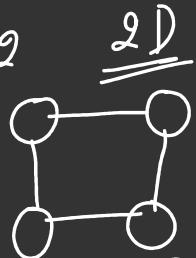


$$\text{No. of nodes} = 2^K = 2^1$$

$$\text{Diameter} = K = 3$$

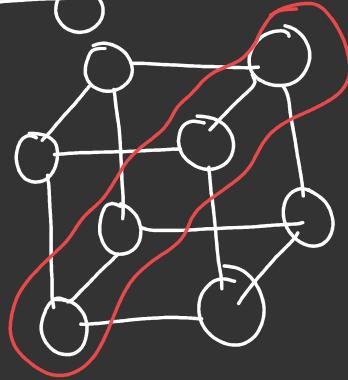
$$\text{Dimension} = 2^{K-1} = 2^2 = 4$$

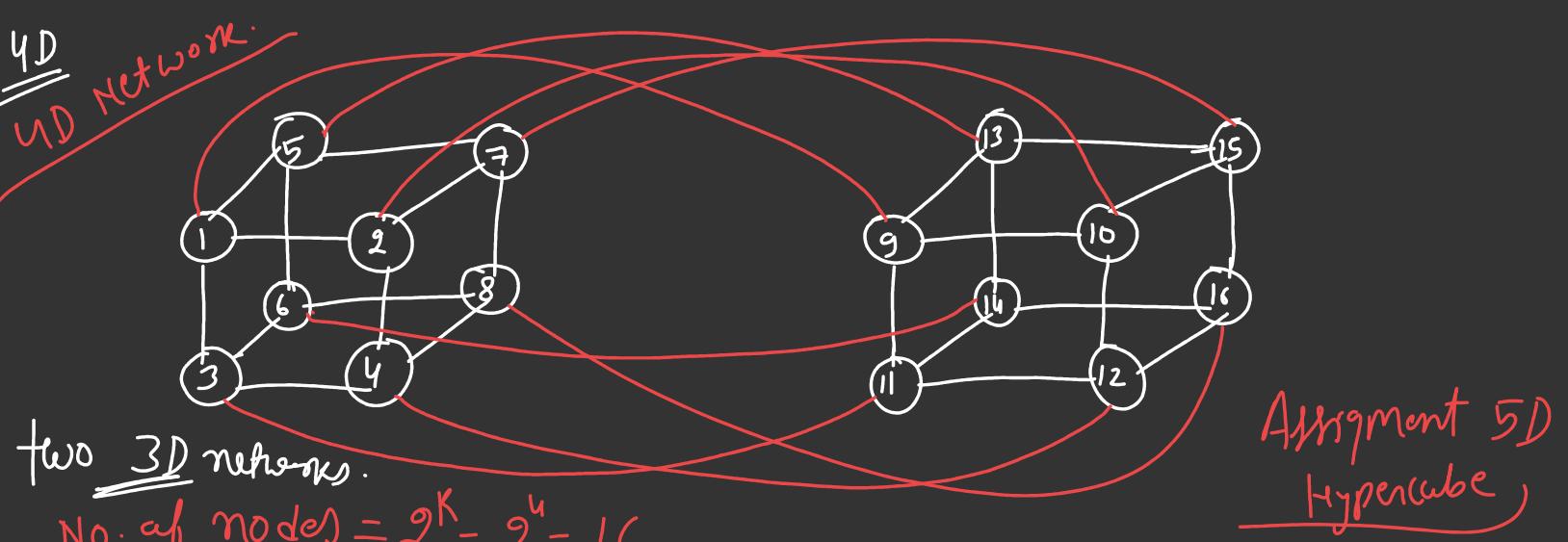
$n=2$



$\underline{2D}$

$\frac{3D}{2^3} = 8$





$$\text{No. of nodes} = 2^k = 2^4 = 16$$

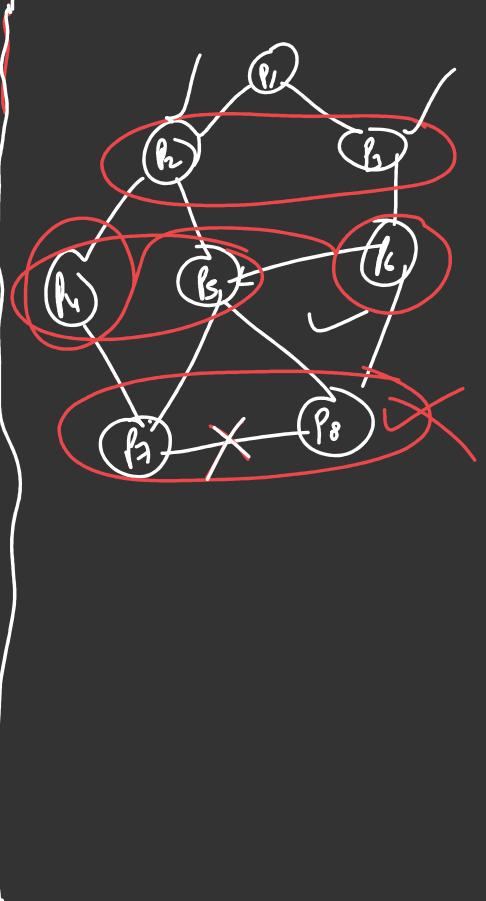
$$\text{diameter} = k = 4$$

$$\text{Bisection} = 2^{k-1} = 2^3 = 8$$

Assignment 5D  
Hypercube)

Bernstein's Conditions: Conditions applied on two statements  $s_1$  &  $s_2$  that are to be executed in the processor. It states that three conditions are explained must be satisfied for two successive statements  $s_1$  &  $s_2$  to be concurrently and still produce the same result.

- Intersection b/w read-write set, write-read set write-write set must be NULL.



Exm Consider a simple Case. given processes  $P_1$  to  $P_5$

Statement	$I_i$	$O_i$
$P_1$	$\{D, E\}$	$\{C\}$
$P_2$	$\{U, C\}$	$\{M\}$
$P_3$	$\{B, C\}$	$\{A\}$
$P_4$	$\{L, M\}$	$\{C\}$
$P_5$	$\{U, E\}$	$\{F\}$

$$\begin{array}{l}
 P_1 \parallel P_2 ? \\
 \{D, E\} \cap \{M\} \neq \emptyset \\
 \{U, C\} \cap \{C\} \neq \emptyset
 \end{array}$$
  

$$\begin{array}{l}
 P_1 \not\sim P_2 \\
 P_1 \parallel P_3 ?
 \end{array}$$

$$\begin{array}{l}
 \{D, E\} \cap \{A\} = \emptyset \\
 \{B, C\} \cap \{C\} \neq \emptyset
 \end{array}$$

two processes  $P_1$  &  $P_2$  with input set  $I_1$  &  $I_2$ , and output set  $O_1$  and  $O_2$

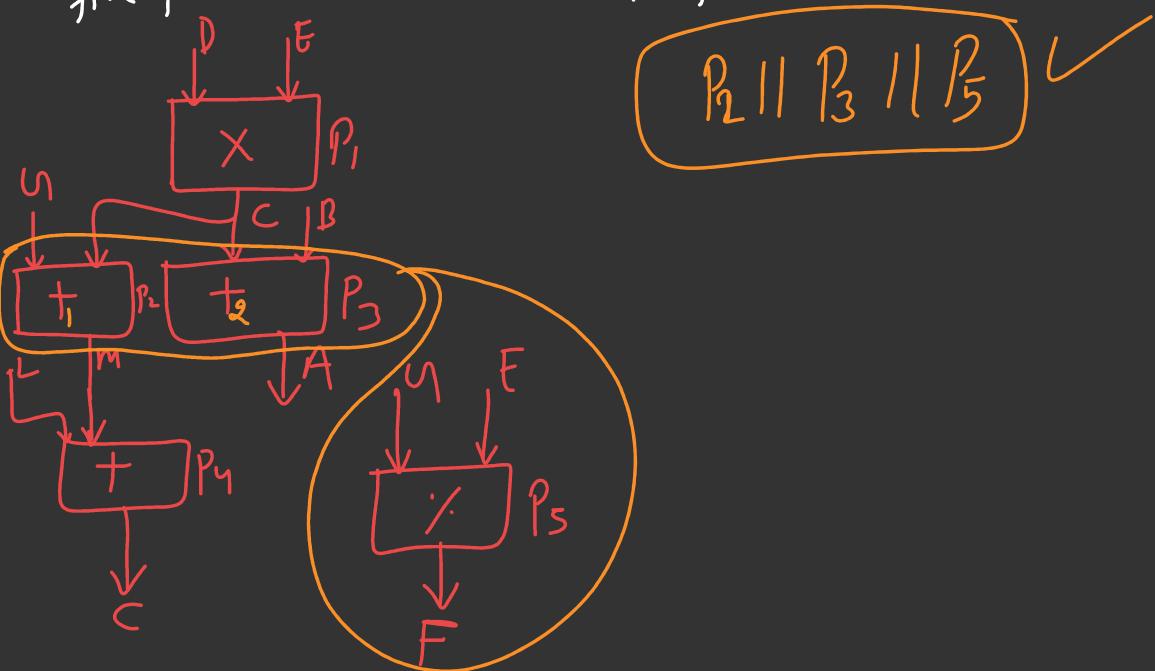
$$\begin{array}{l}
 I_1 \cap O_2 = \emptyset \\
 I_2 \cap O_1 = \emptyset \\
 O_1 \cap O_2 = \emptyset
 \end{array}$$

5  
2

$$\begin{array}{l}
 P_1 : C = D \times E \\
 P_2 : M = U + C \\
 P_3 : A = B + C \\
 P_4 : C = L + M \\
 P_5 : F = U \% E
 \end{array}$$

$P_1 \parallel P_5$ ,  $P_2 \parallel P_5$ ,  $P_2 \parallel P_3$ ,  $P_3 \parallel P_5$ ,  $P_4 \parallel P_5$

five pairs can be execute in parallel.



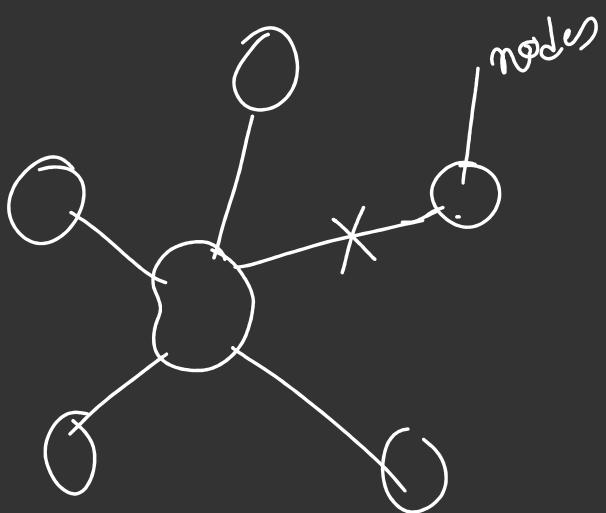
Date  
06/02/23

## Unit-2 Distributed Systems.

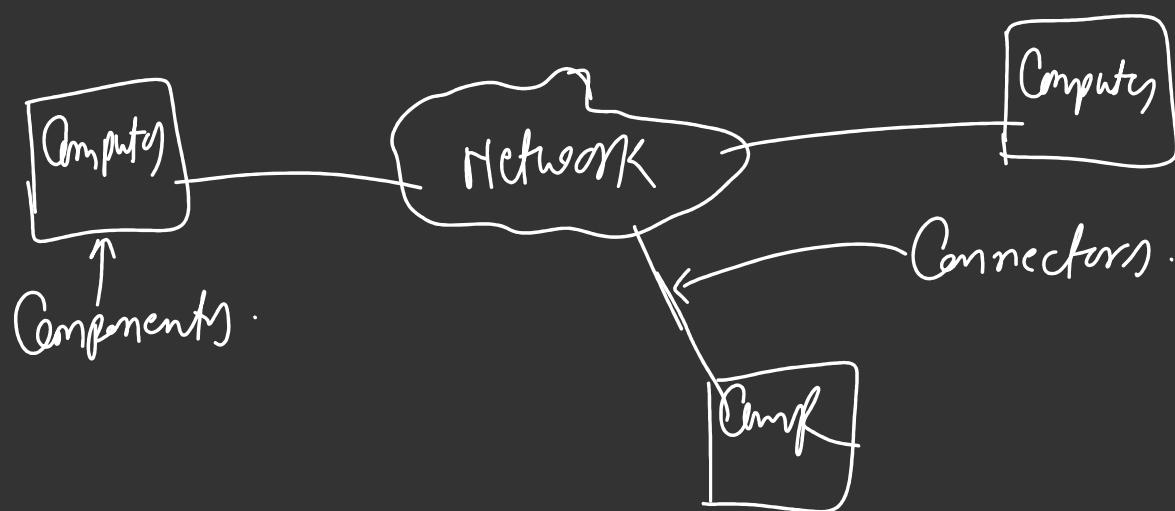
§ Goal of distributed System:-

- 1) Resource Sharing:- whether it's the hardware, software or data that can be shared.
- 2) Openness:- How open is the software designed to be developed and shared with each other.
- 3) Concurrency:- multiple machines can process the data at same time.
- 4) Fault tolerance:- How easy and quickly failure in parts of the system can be detected.

Transparency: How much access does one node have to locate and communicate with each other.



{ Distributed System Architecture :: Distributed system architectures are bundled with Components and Connectors.

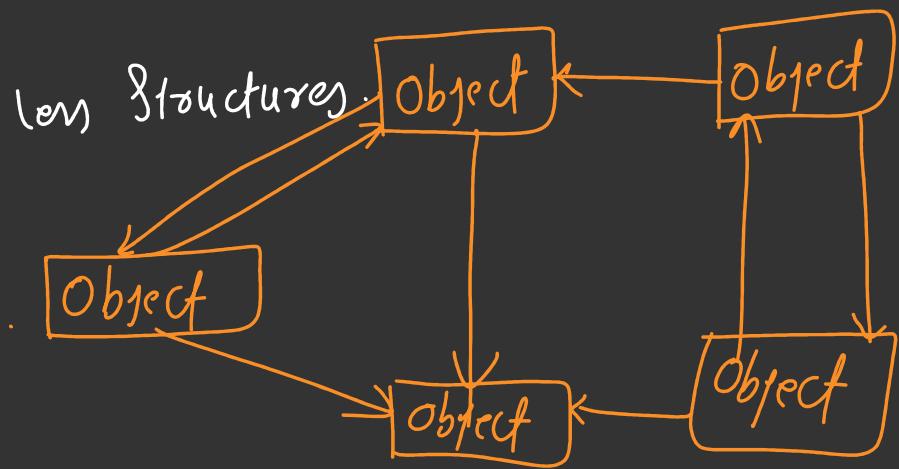


§ Architectural Styles: There are three different Architectural styles plus one hybrid architectural style. The basic idea is to organize logically different components and distributed those computers over the various machines.

- 1) Layered Architecture
- 2) Object Based Architecture
- 3) Event based Architecture
- 4) Hybrid Architecture.

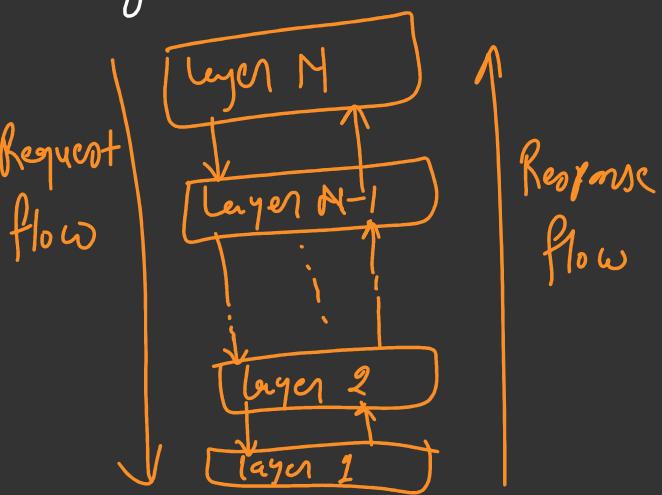
## {Object based Architecture}:

- In object based architecture, it is based on loosely coupled arrangements of objects.
- Each object corresponds to what we have defined as a component, these components are connected through remote procedure call (RPC).
- This architectural style is less structures.



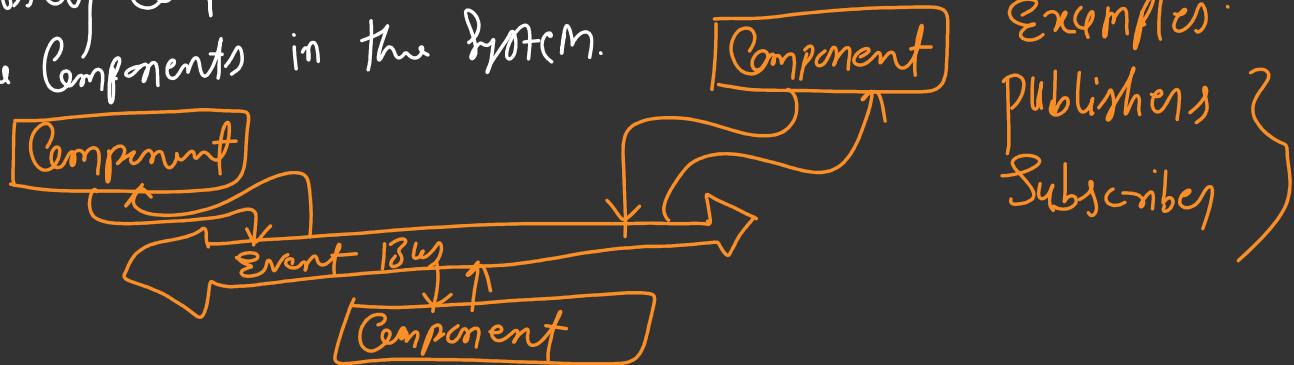
## 1) Layered Architecture:

- The basic idea for the layered style architecture is very simple, Components are organized in linear fashion.
- It is a modular approach layer to layer.
- Layer on the bottom provide a service to upper layer.



Date  
09/02/23  
3) Event based Architecture: This kind of Architecture is based on Events.

- Processes essentially communicate through the events, which also carry the data.
- Advantages of this architecture is that the Components are loosely coupled so can be add, remove and modify the components in the system.



{ Hybrid Architecture: This kind of Architecture based on Edge Computing System.

- These Systems are deployed on the Internet where Servers are placed "at the edge" of network.
- The Edge Servers main purpose to Serve Content possibly after applying the filtering.
- The basic model is that for specific organization, one Edge Server act as an origin Server from which all Content originates. This Server can use another Edge Server for replacing the web pages.



§ Architectural Model: Deals with the organization of Components across the network of Computer and their relationship.

Client/Server Model  
Distributed System.

Peer to Peer Model

