TABLE OF CONTENTS

List of Figures

1 Abstract

This document presents the layout design of a 2-input NAND gate in Cadence Virtuoso, utilizing the 90nm architecture. Building upon the results of a prior experiment, which involved the schematic design of the NAND gate using NMOS and PMOS transistors, this research aims to translate the schematic design into an optimized layout. Leveraging the advanced features of the 90nm technology node, the layout was meticulously crafted to optimize area, power consumption, and propagation delay while ensuring robustness against process variations. Rigorous simulations were conducted to validate the functionality and performance of the layout, demonstrating its efficacy in modern integrated circuit design.

2 Keywords

2-input NAND gate, Layout design, Cadence Virtuoso, 90nm architecture, Integrated circuit design, NMOS and PMOS transistors.

3 Objectives

1. To create a layout view of the basic two input NAND circuit from scratch.
2. To perform the design rule check (DRC) of the NAND gate layout.
3. To perform the layout vs. schematic (LVS) check for the NAND gate layout.
4. To perform parasitic extraction on the NAND gate layout.

4 Introduction

By performing this experiment, we will learn about the usage of CADENCE VIRTUOSO. We will also learn about layout design process. We will also learn about the design rule check (DRC), layout vs. schematic (LVS) check and parasitic extraction. We will also observe the extracted layout design.

5 Theory

NAND gate is a fundamental digital logic gate used extensively in digital circuits due to its versatility and functional completeness. A NAND gate performs the logical NAND operation, where the output is true (or high) unless both inputs are true (or high). This gate is a building block for various digital systems, including arithmetic logic units, memory storage, and more complex logic circuits. Designing a 2-input NAND gate in Cadence Virtuoso, an advanced electronic design automation (EDA) tool, involves a series of methodical steps, from schematic capture to simulation. Cadence Virtuoso offers a comprehensive environment for the design and verification of custom ICs, providing tools for schematic entry, layout editing, and extensive simulation capabilities. The process begins with creating a transistor-level schematic of the NAND gate using PMOS and NMOS transistors. This is followed by generating a symbol for the NAND gate, enabling its use in hierarchical design contexts. The next step is the simulation. This step is followed by the layout design process. This process contains the actual designing process as well as different types of checking and verification process.

6 Truth Table

A (input)	B (input)	Pull Down Network	Pull Up Network	O (output)
0	0	Off	On	1
0	1	Off	On	1
1	0	Off	On	1
1	1	On	Off	0

7 Layout Design

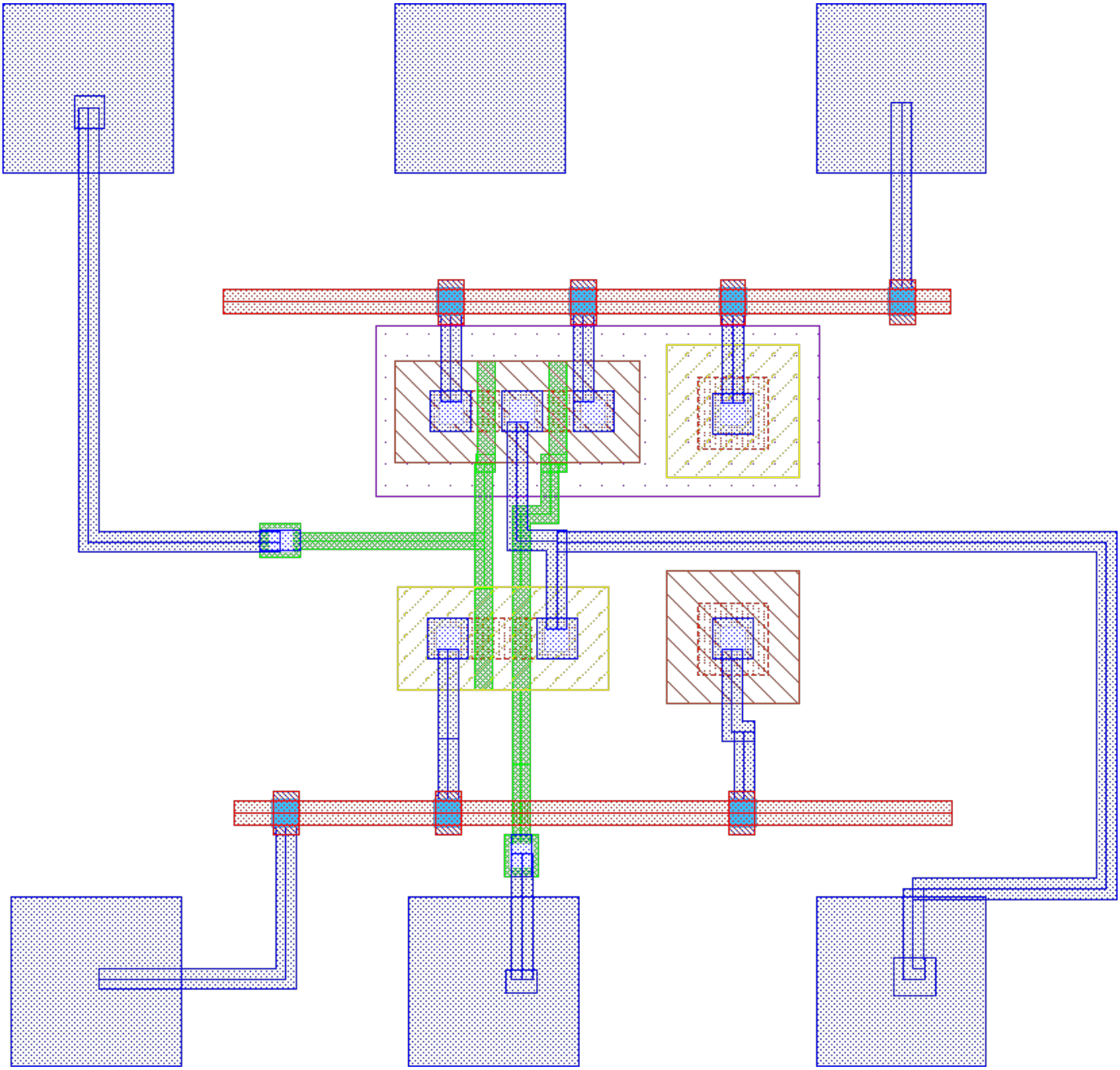
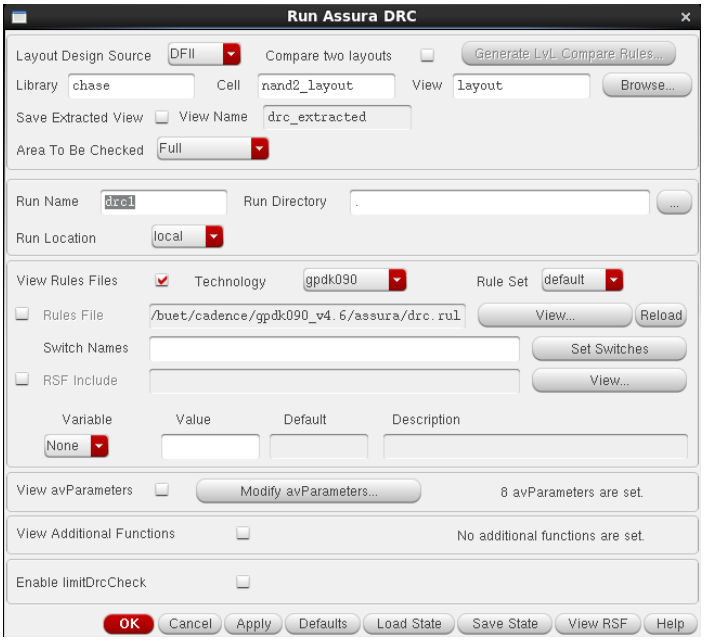


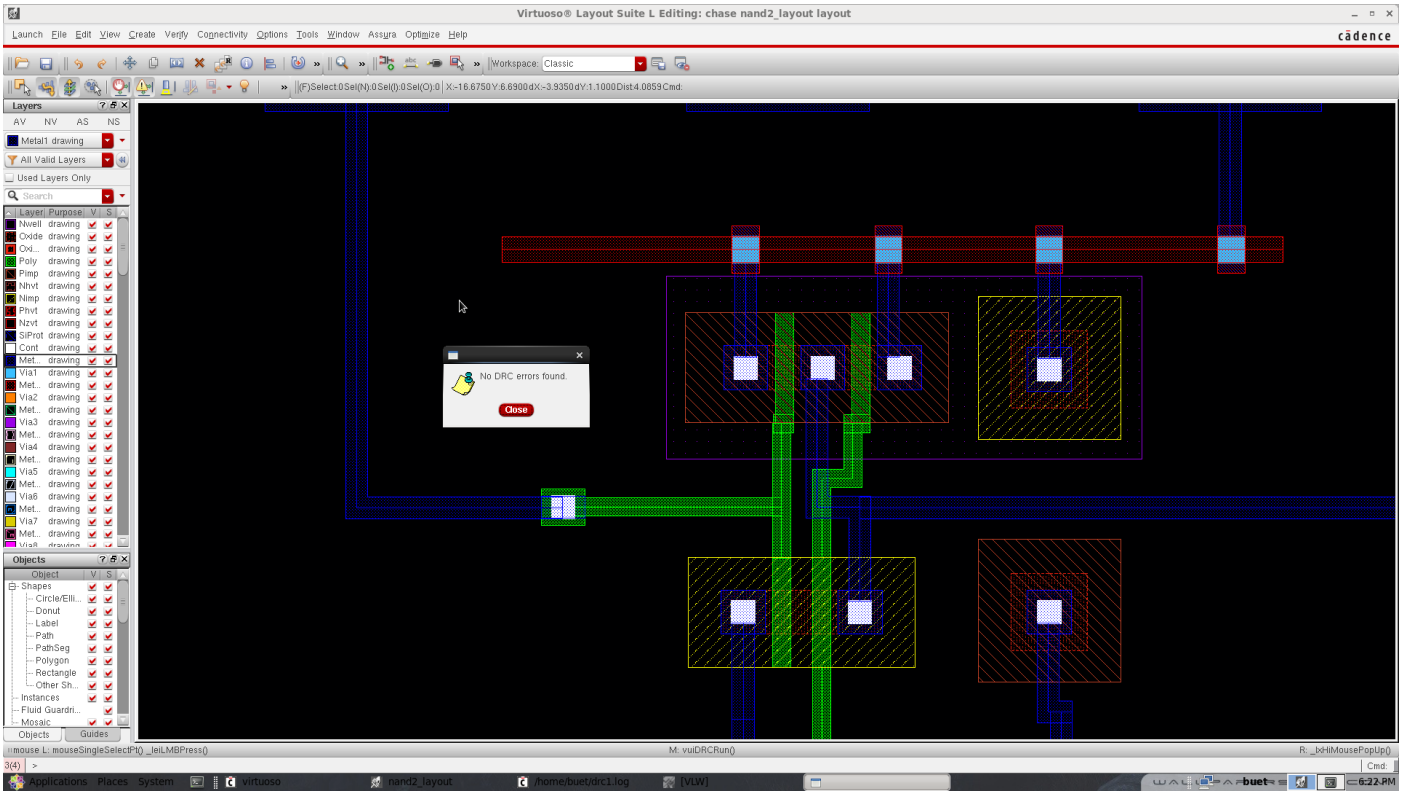
Figure 1: Layout of 2-input NANAD gate.

8 Layout Design Check

8.1 Design Requirement Check



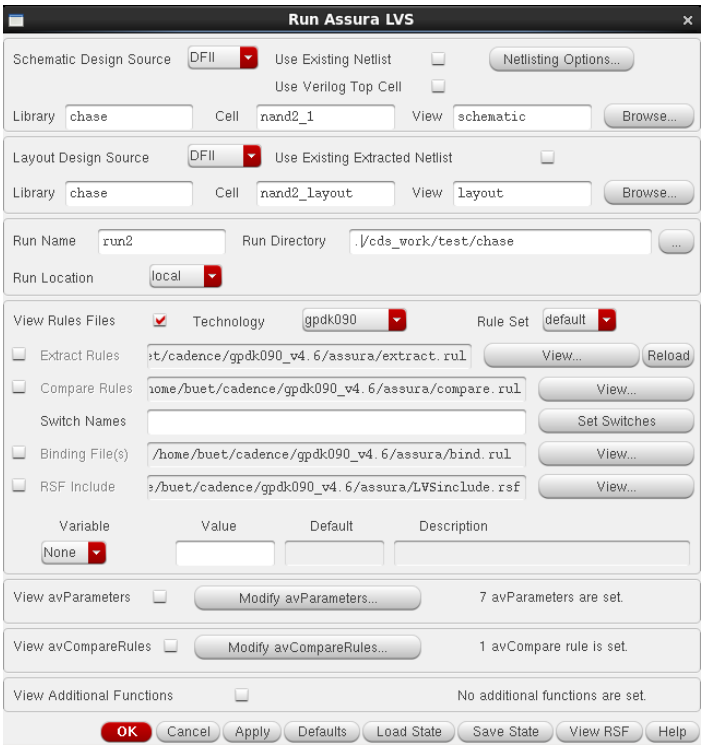
(a) Assura DRC setup.



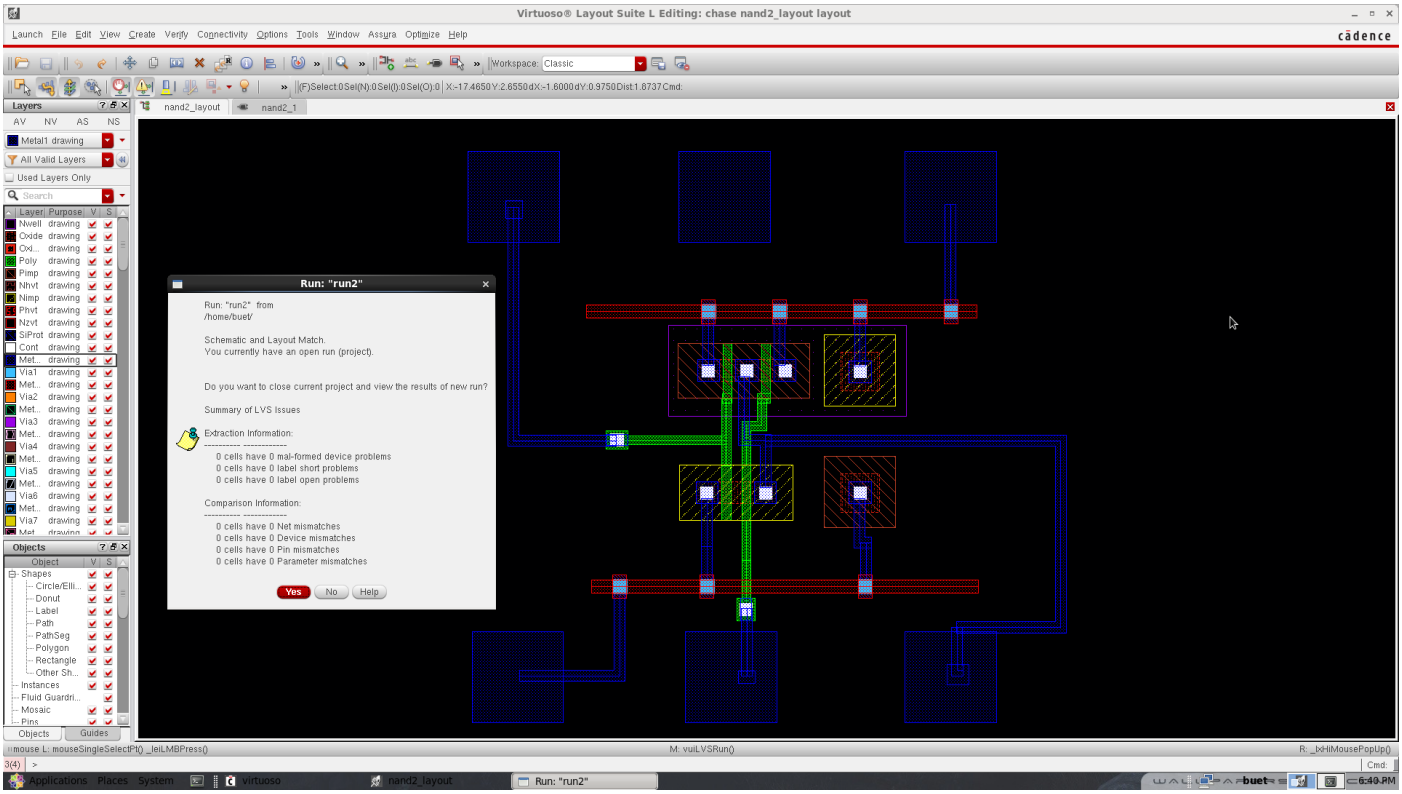
(b) Assura DRC check result.

Figure 2: Assura Design Requirement Check (DRC) setup and result.

8.2 Layout Vs. Simulation check



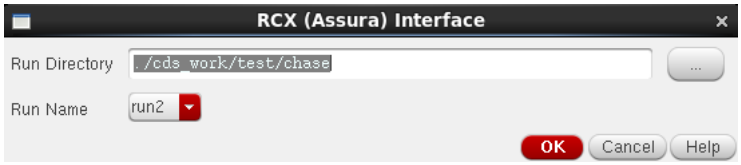
(a) Assura LVS setup.



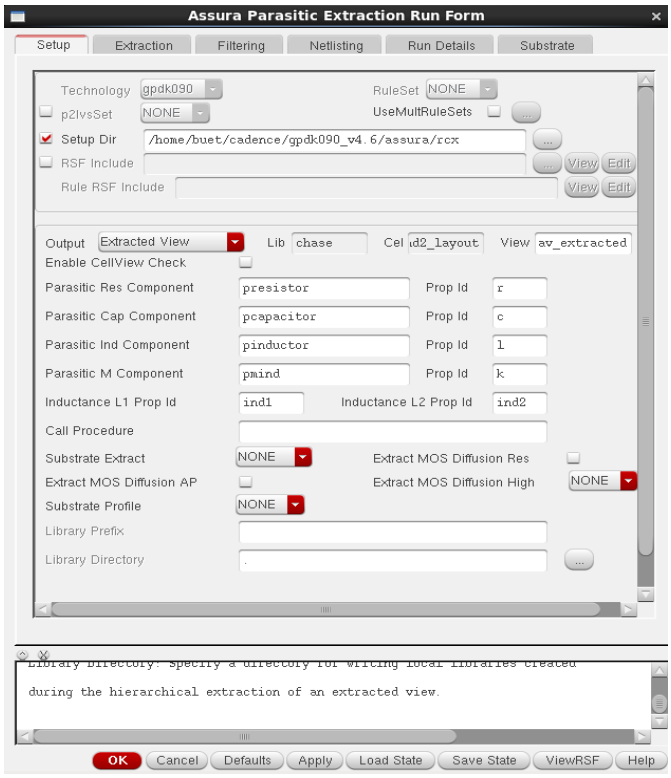
(b) Assura LVS check result.

Figure 3: Assura Layout Vs. Schematic (LVS) check setup and result.

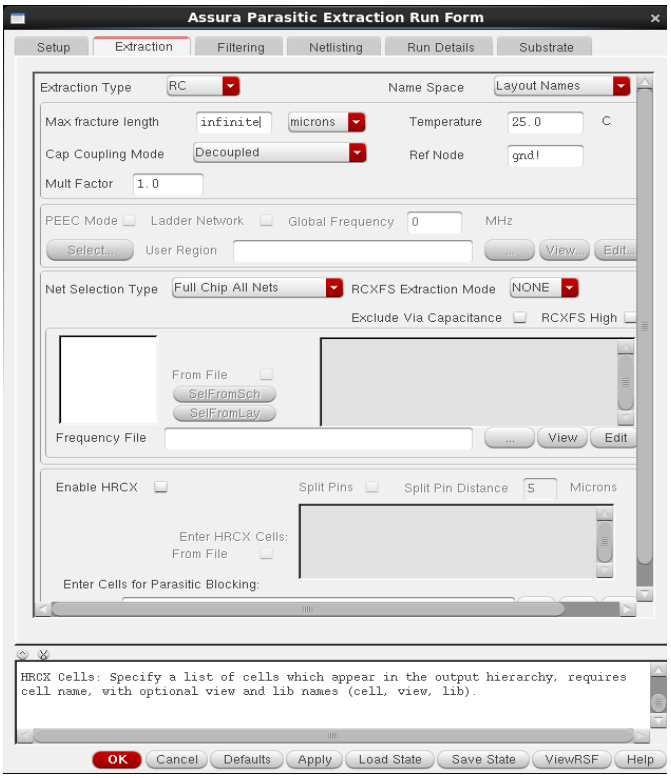
8.3 RCX Run and Parasitic Extraction



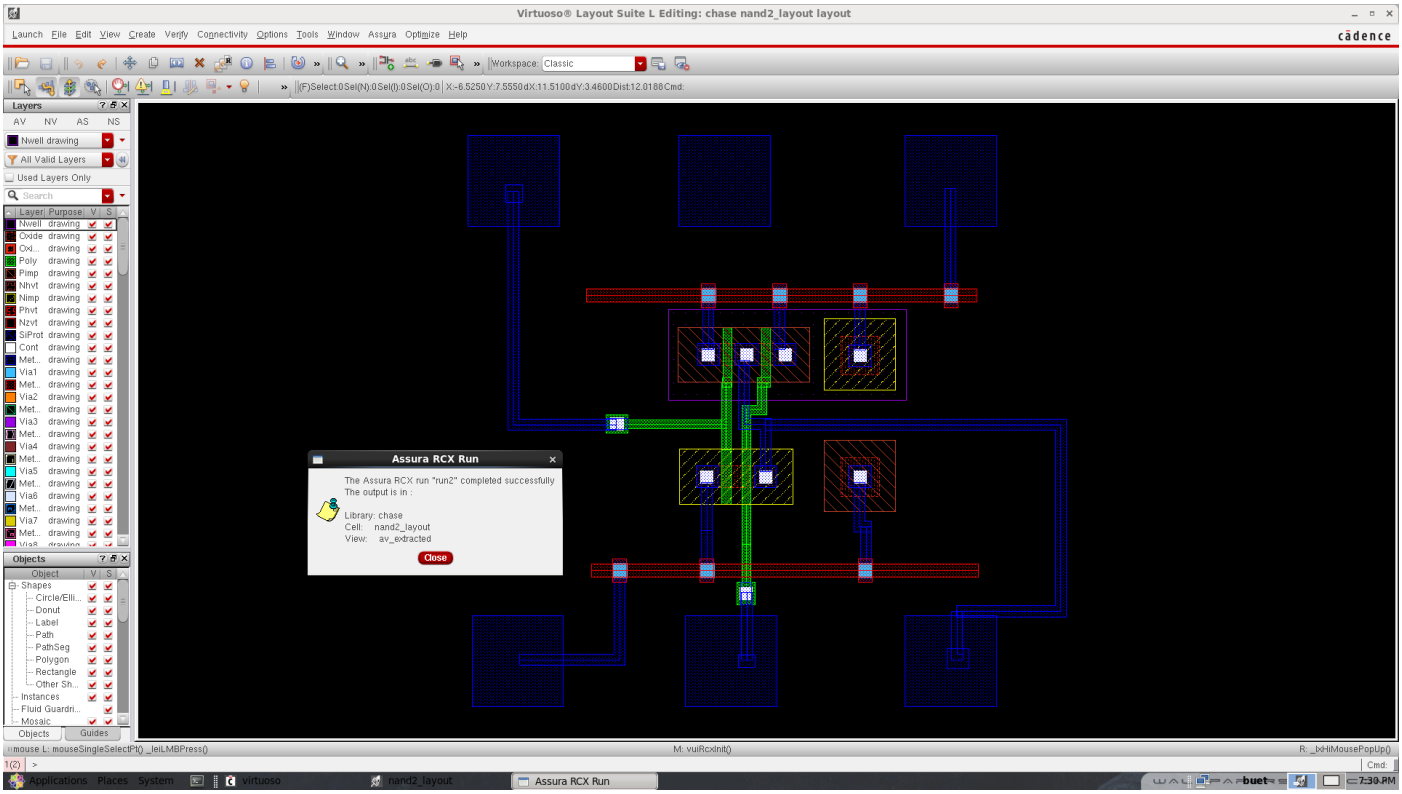
(a) RCX interface.



(b) Assura Parasitic Extraction Run Form – Setup tab.



(c) Assura Parasitic Extraction Run Form – Extraction tab.



(d) Assura RCX Run result.

Figure 4: Assura RCX and Parasitic Extraction setup and result.

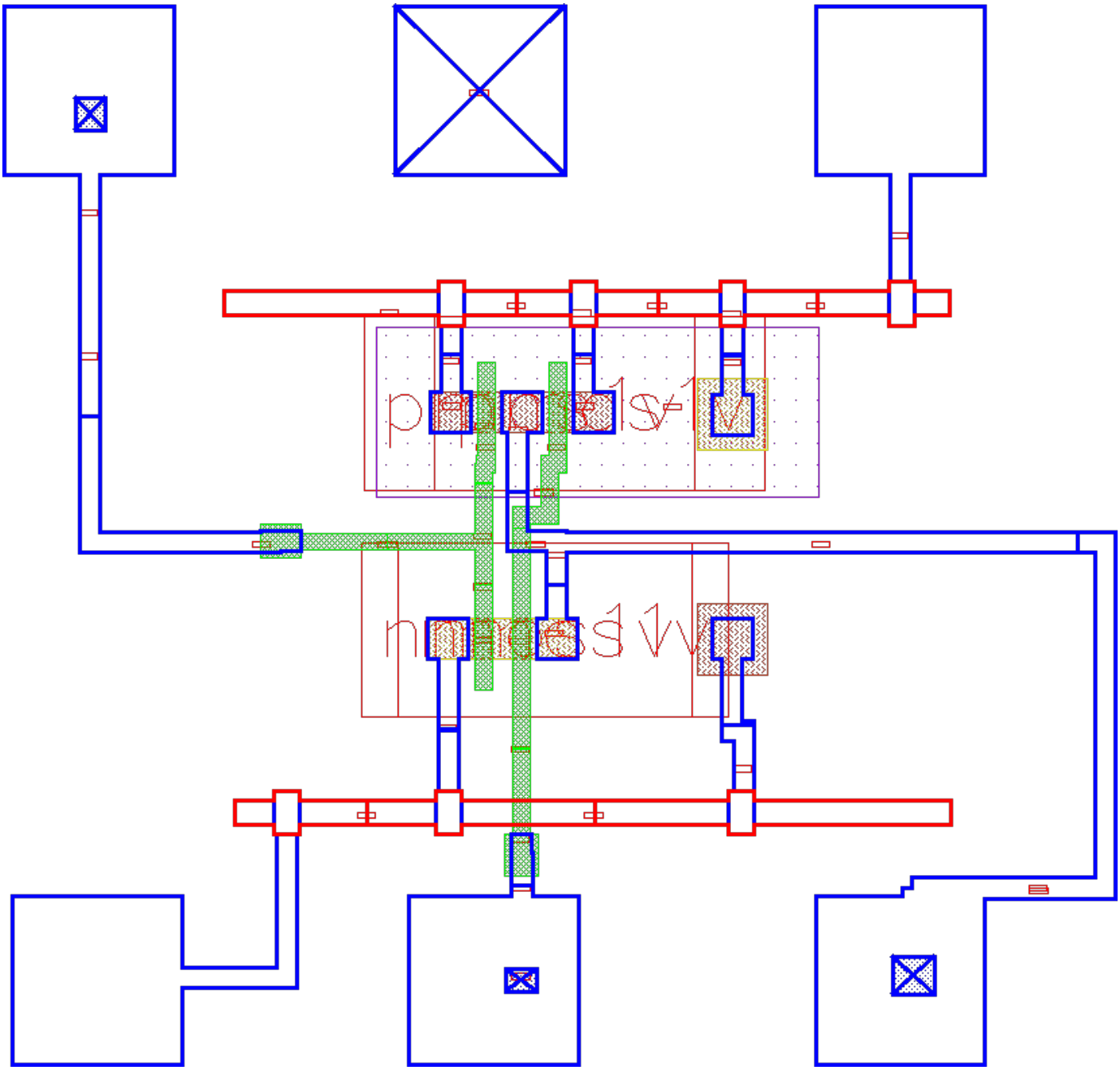


Figure 5: AV Extracted Layout.

9 Conclusion

In this experiment, we became acquainted with Cadence Software . We created the layout for a 2-input NAND gate and identified the required designed parameters and requirements. We also performed DRC, LVS, RCX, and parasitic extraction.

10 References

1. Lab Manual.

2. Cadence Virtuoso Tutorial - University of Southern California.