# Chittagong University of Engineering and Technology

## Department of Electrical and Electrical Engineering

# EEE 476: VLSI Technology Sessional

**Experiment Number – 1**
**Experiment Name: Draw the Schematic of a 2 - input NAND Gate, Create a Symbol, Perform Simulation and Plot the Output Wave Forms**

*Prepared by*

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Group No. : $X_1$
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