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1 Abstract

This report presents the design and analysis of a two-stage CMOS operational amplifier (Op-Amp) using Cadence Virtuoso. The objective was to examine both large-signal DC and small-signal AC characteristics while adhering to specific design requirements. Simulations focused on the DC transfer characteristics, frequency response, and Common Mode Rejection Ratio (CMRR) to evaluate key performance metrics such as gain, phase margin, and bandwidth. The results of these simulations were compared with the design specifications to assess the Op-Amp's performance under typical operating conditions.

2 Keywords

Two-stage CMOS Operational Amplifier, Cadence Virtuoso, DC Transfer Characteristics, Frequency Response, Common-Mode Rejection Ratio (CMRR), Gain-Bandwidth Product (GB), Slew Rate, Phase Margin, Analog Circuit Design, CMOS Technology.

3 Objectives

1. To design an un-buffered two stage CMOS Operational Amplifier with an n-channel input pair.
2. To study the large signal dc characteristics of the Op-Amp.
3. To study the small signal characteristics of the Op-Amp.

4 Introduction

Operational amplifiers are key components in analog circuits, essential for applications such as signal amplification, filtering, and various mathematical operations. This report focuses on the design and analysis of a two-stage CMOS Op-Amp, with an n-channel input differential pair, designed using Cadence Virtuoso. The goal of the experiment was to analyze the Op-Amp's performance under typical operating conditions while meeting a set of predefined specifications, including voltage gain, output voltage swing, and slew rate. The design procedure was based on the methodology described in CMOS Analog Circuit Design by Allen and Holberg, with simulations conducted to study both the DC and AC characteristics. The main aspects explored included the transfer characteristics of the Op-Amp, its frequency response, and its Common Mode Rejection Ratio (CMRR). Power Supply Rejection Ratio (PSRR) analysis and corner simulations were not part of this experiment.

5 Theory

The two-stage CMOS Op-Amp designed in this experiment consists of two main stages: the differential input stage and the common-source output stage. The differential pair forms the first stage and provides the necessary differential gain, while the second stage amplifies the output. The compensation capacitor (Cc) plays a crucial role in stabilizing the amplifier by controlling its frequency response and ensuring sufficient phase margin.

Key performance parameters :

1. **Gain:** The voltage gain, $A_v = \frac{V_{out}}{V_{in}}$ is crucial for amplification, with a target gain greater than 5000 V/V.
2. **Gain-Bandwidth Product:** The product of the amplifier's gain and bandwidth, with a target of 5 MHz.
3. **Phase Margin:** A stability measure that helps prevent oscillations, determined by the phase shift at the gain crossover frequency.
4. **Gain Margin:** A stability measure that helps prevent oscillations, determined by the gain at the phase crossover frequency.

6 Simulation Setup

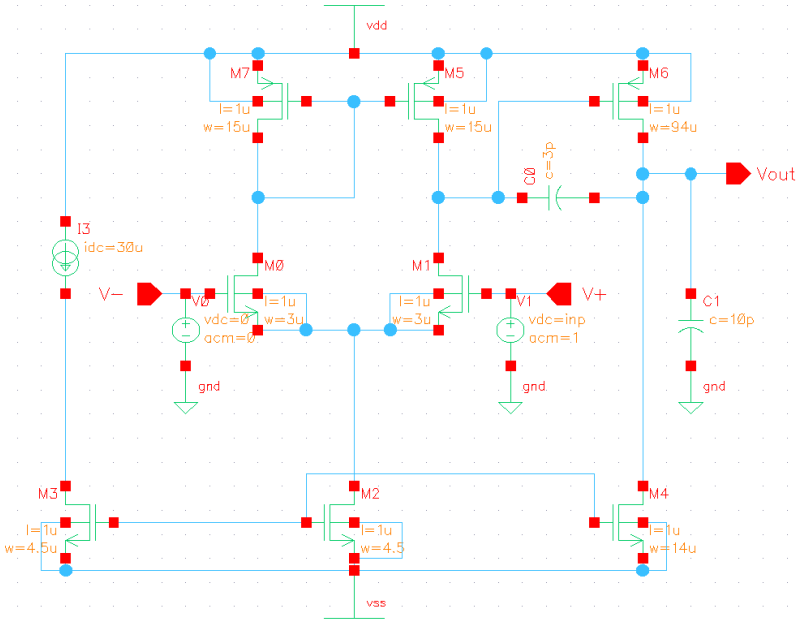

Figure 1: Schematic diagram of two stage Op-Amp for Transfer Characteristics and Frequency Response.

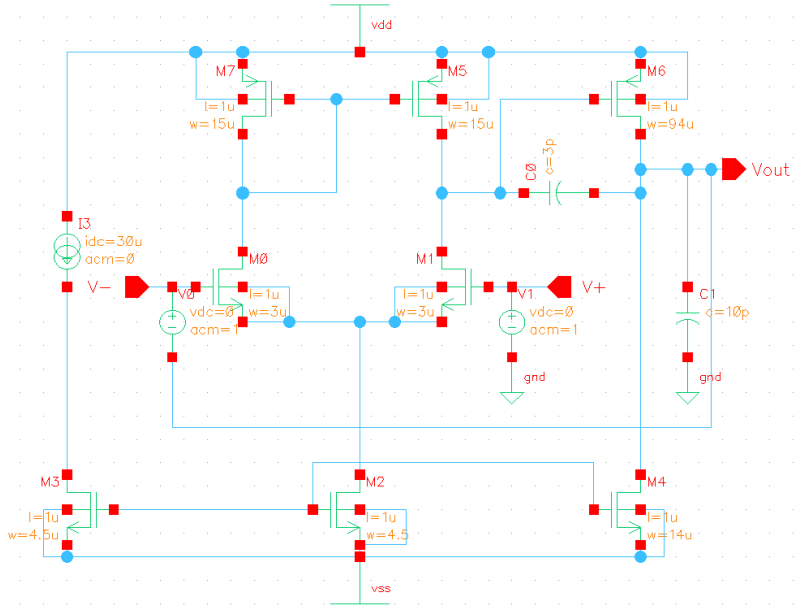

Figure 2: Schematic diagram of two stage Op-Amp for CMRR Response.

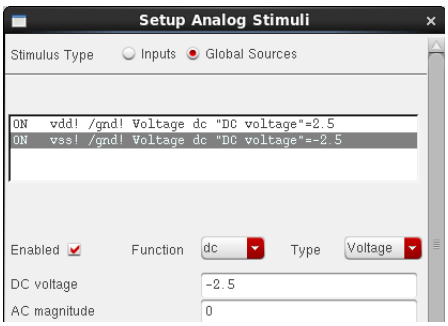

Figure 3: Global source parameters.

7 Simulation Result

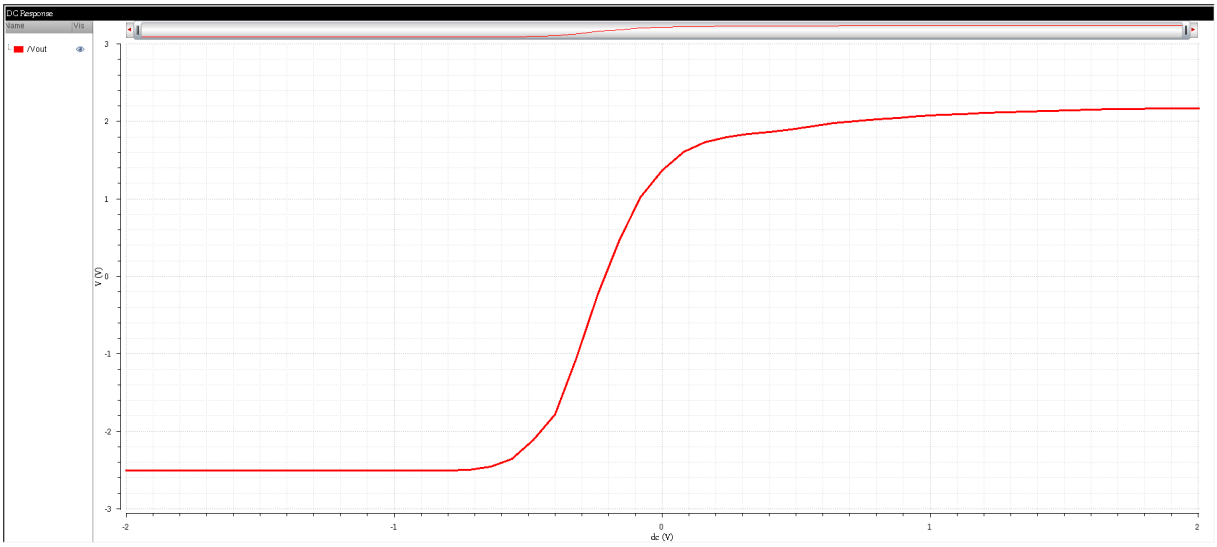

Figure 4: Transfer Characteristics of the Op-Amp.

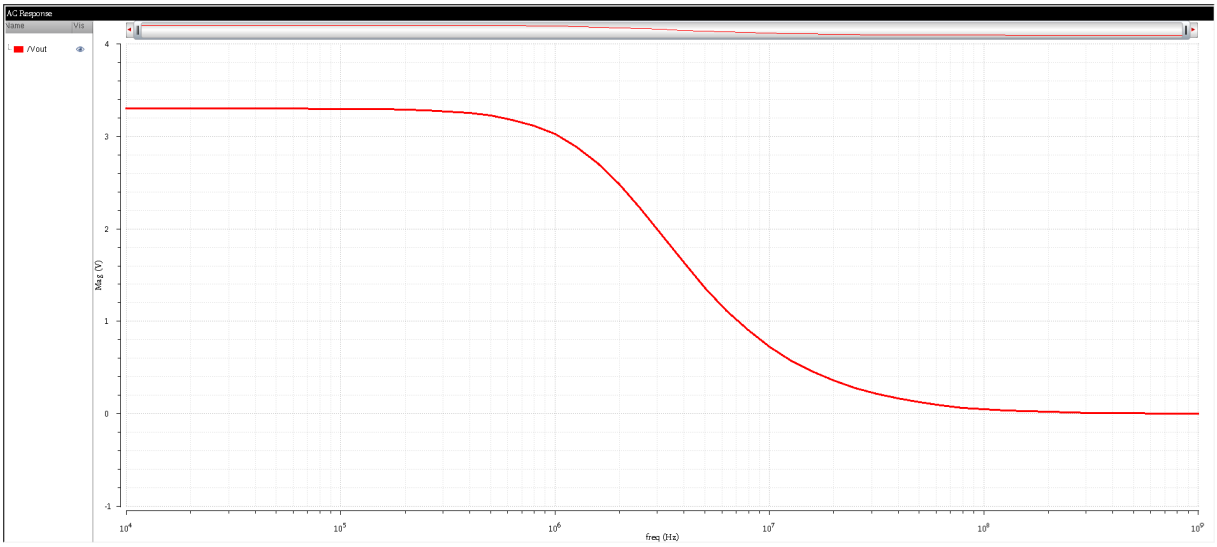

Figure 5: Frequency Response of the Op-Amp.

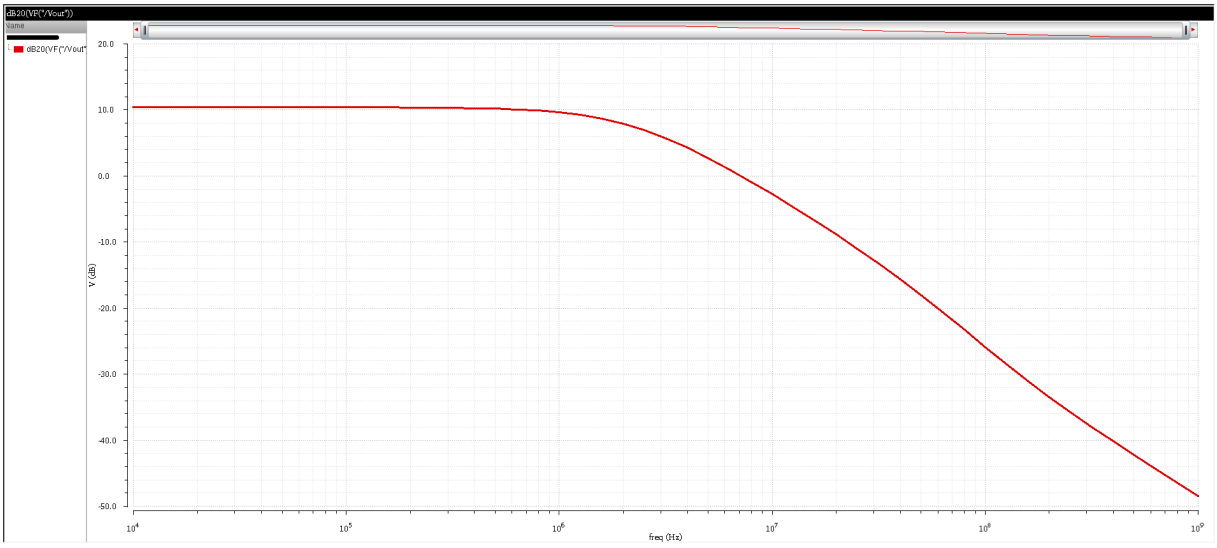

Figure 6: Frequency Response of the Op-Amp in Decibel(dB) scale.

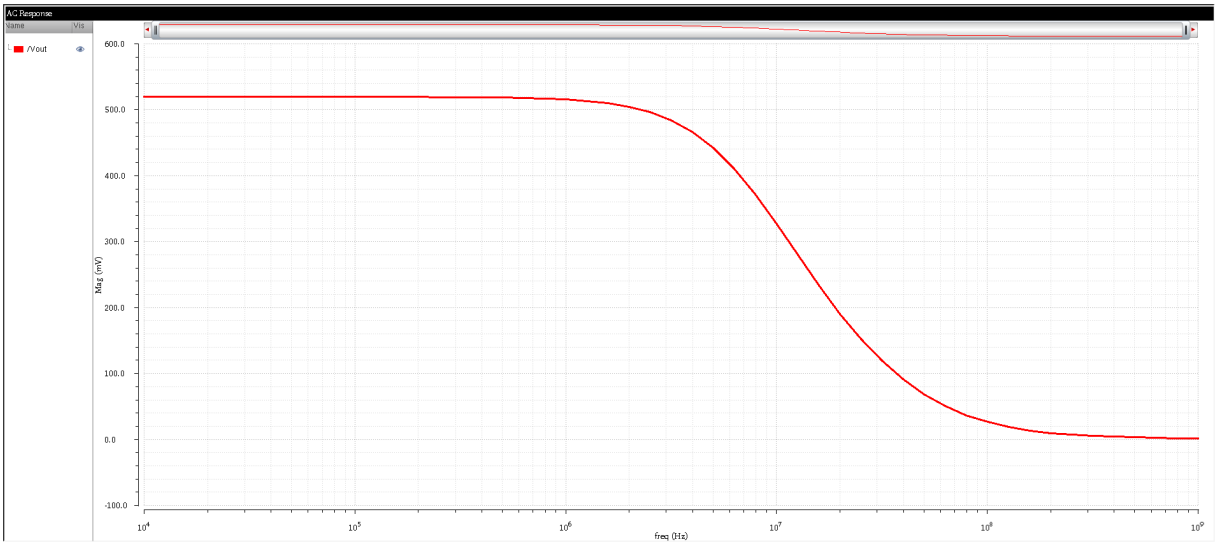

Figure 7: Frequency Response of CMRR of the Op-Amp.

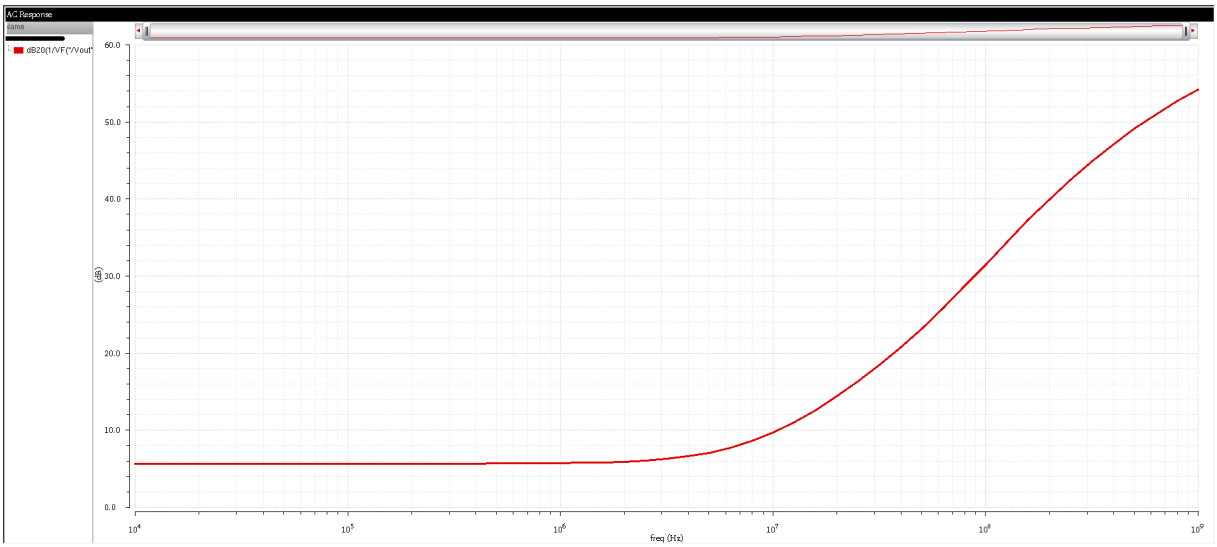

Figure 8: Frequency Response of (1/CMRR) of the Op-Amp in Decibel(dB) scale.

Gain Bandwidth Product (gainBWProd)	7.541×10^6 Hz
Phase Margin	$97.86°$
Gain Margin	-24.34 dB

Table 1: Gain Bandwidth Product, Phase Margin and Gain Margin of the Op-Amp

8 Conclusion

The two-stage CMOS Op-Amp was successfully designed and analyzed using Cadence Virtuoso. The simulations demonstrated compliance with the design specifications in terms of voltage gain, bandwidth, and phase margin. The DC transfer characteristics and frequency response were studied, and the amplifier's Common Mode Rejection Ratio (CMRR) was evaluated. Although corner analysis and Power Supply Rejection Ratio (PSRR) simulations were not performed, the overall results indicate that the Op-Amp meets the required specifications and functions reliably under typical conditions.

9 References

1. Lab Manual.
2. Cadence Virtuoso Tutorial - University of Southern California.