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1 Abstract

In this lab, we explored the design and simulation of a CMOS circuit representing the Boolean equation $Y = A \cdot (B + C) \cdot (D + E)$ using Cadence Virtuoso. The objective was to construct a functional schematic that accurately reflects the equation's logic. Through simulation, we analyzed the performance characteristics of the circuit, including logic levels and propagation delay. The results validated the design approach and demonstrated the effectiveness of CMOS technology in implementing complex Boolean functions.

2 Keywords

CMOS, VLSI, Boolean algebra, digital logic design, Cadence Virtuoso, circuit simulation, NMOS, PMOS, logic gates, schematic design, circuit implementation, digital circuits.

3 Objectives

1. To design a CMOS circuit from the given Boolean equation.
2. To observe the transient response of the designed CMOS circuit.

4 Introduction

The integration of digital circuits in modern electronics necessitates efficient design methodologies that leverage complementary metal-oxide-semiconductor (CMOS) technology. CMOS circuits are favored for their low power consumption and high noise immunity. This lab focused on designing a CMOS schematic to implement the specific Boolean function $Y = A \cdot (B + C) \cdot (D + E)$. By utilizing Cadence Virtuoso for simulation, we aimed to visualize the circuit's behavior, validate its functionality, and understand the interplay of logic gates in realizing the intended output. This hands-on experience provided a practical understanding of how Boolean algebra translates into physical circuit designs.

5 Theory

The Boolean equation $Y = A \cdot (B + C) \cdot (D + E)$ consists of both AND and OR operations. In this equation:

- A is an AND input that controls the output based on its logic level.
- $(B + C)$ and $(D + E)$ re OR inputs that contribute to the overall output when combined with A.

The corresponding CMOS implementation involves using PMOS and NMOS transistors to create the desired logic levels. PMOS transistors are used to pull the output high (logic 1) when the input conditions are met, while NMOS transistors pull the output low (logic 0). The circuit employs a combination of parallel and series connections to reflect the OR and AND operations respectively, allowing for a dynamic response to varying input conditions. Cadence Virtuoso facilitates detailed circuit analysis, providing insights into the electrical characteristics and timing behavior of the designed schematic.

6 Truth table

A	B	C	D	E	$Y = A \cdot (B + C) \cdot (D + E)$
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

Table 1: Theoretical Truth table of the Boolean expression $Y = A \cdot (B + C) \cdot (D + E)$.

7 Simulation Setup

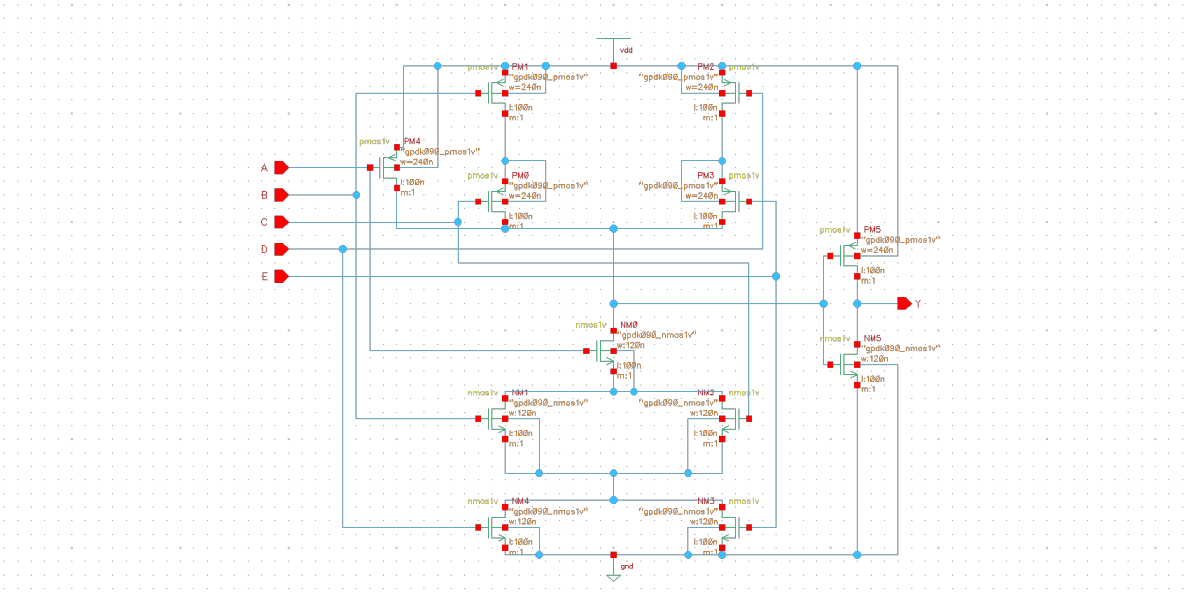
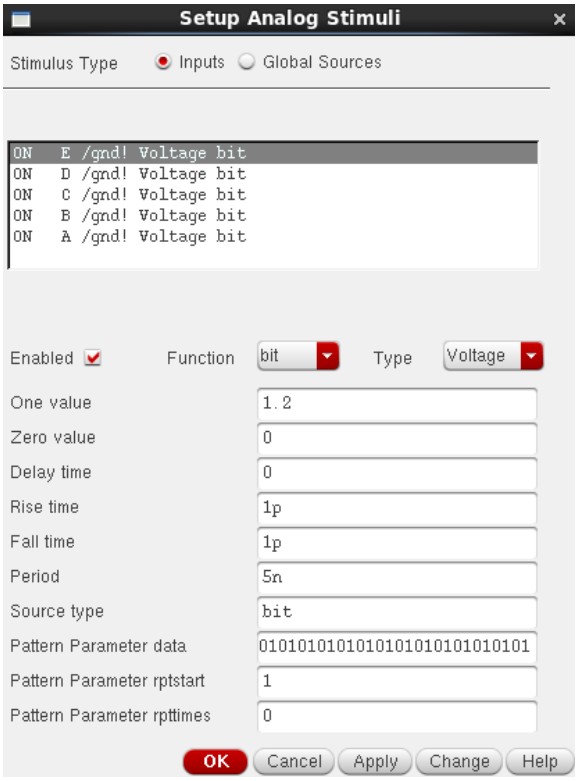
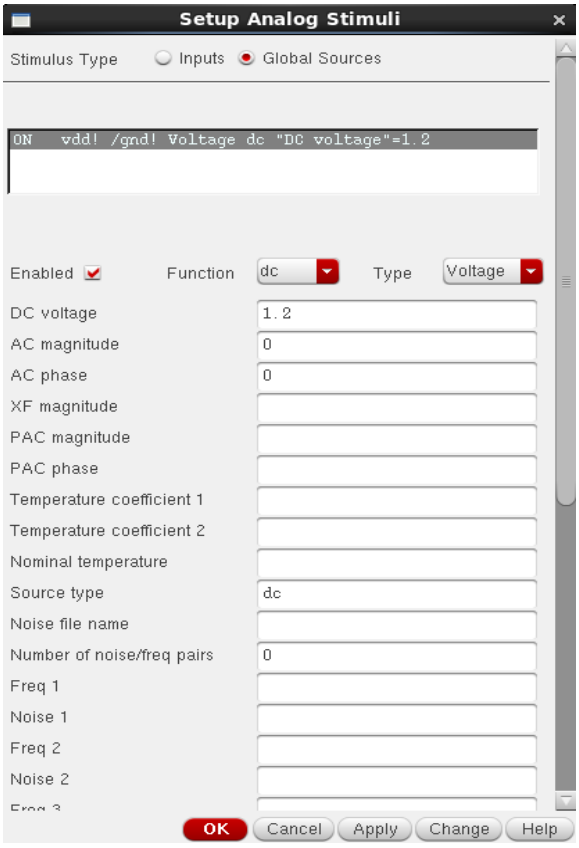


Figure 1: CMOS schematic diagram of the Boolean expression $Y = A \cdot (B + C) \cdot (D + E)$.



(a) Input Setup.



(b) Global source Setup.

Figure 2: Input and Global source Setup.

8 Simulation Result

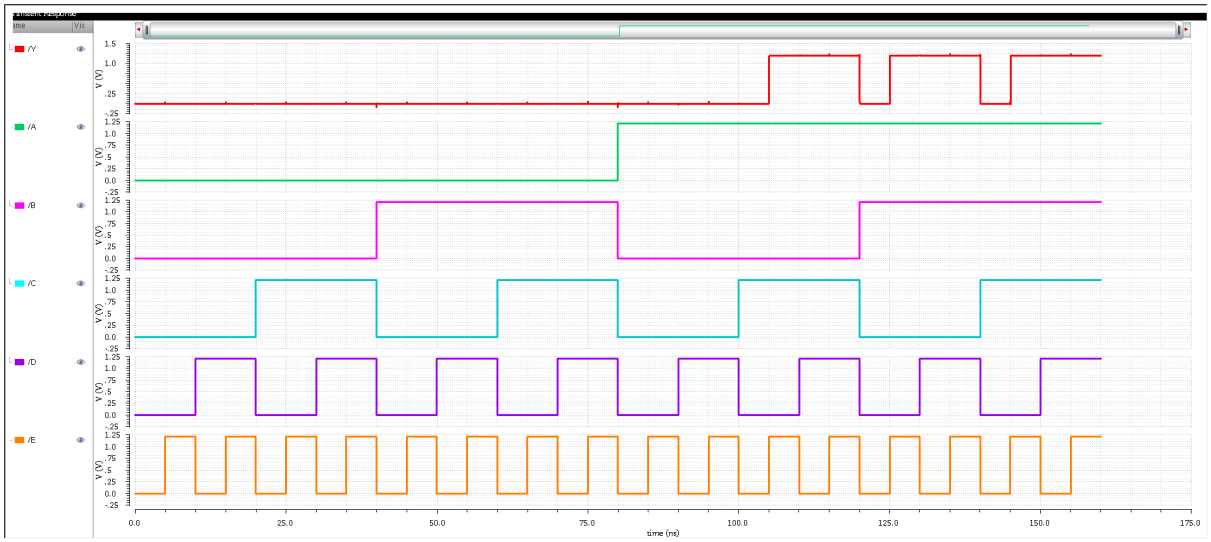


Figure 3: Waveforms of inputs A (Green), B (Pink), C (Indigo), D (Purple), E (Orange) and output Y (Red).

A	B	C	D	E	$Y = A \cdot (B + C) \cdot (D + E)$
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	1

1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

Table 2: Truth table based on the Simulation Result.

9 Conclusion

The simulation of the CMOS schematic for the Boolean function $Y = A \cdot (B + C) \cdot (D + E)$ using Cadence Virtuoso successfully demonstrated the practicality of CMOS technology in digital logic design. The resulting circuit accurately represented the logical operations outlined in the Boolean equation, confirming the reliability of our design methodology. Through this lab, we gained valuable insights into the behavior of CMOS circuits, particularly in their response to different input combinations. The successful implementation underscored the importance of understanding both Boolean algebra and circuit design principles in the field of VLSI engineering.

10 References

1. Lab Manual.

2. Cadence Virtuoso Tutorial - University of Southern California.