Chittagong University of Engineering and Technology

Department of Electrical and Electrical Engineering

EEE 476: VLSI Technology Sessional

Experiment Number – 1
Experiment Name: Draw the Schematic of a 2 - input NAND Gate, Create a Symbol, Perform Simulation and Plot the Output Wave Forms

Prepared by

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1 Abstract

This document outlines the design and simulation of a 2-input NAND gate using Cadence Virtuoso. The design process involves creating a schematic, symbol, and performing the necessary simulations to verify the functionality of the NAND gate. Initially, the transistor-level schematic is designed using PMOS and NMOS transistors configured in a complementary arrangement. Following the schematic creation, a symbol view is generated for hierarchical design use. The layout design involves placing and routing the transistors, ensuring proper connectivity and adherence to design rules. Check and save process is conducted to ensure correctness. Finally, simulations, including DC, transient, and parametric analyses, are performed to verify the gate's logical functionality and performance metrics.

2 Keywords

2-input NAND Gate, Rise time, Fall time, Propagation delay

3 Objectives

1. To login in to the Cadence Server shell and start the Cadence virtuoso software
2. To create a working library
3. To draw the schematic of a 2-input NAND gate in Cadence Virtuoso Schematic Editor
4. To create a symbol view of the NAND gate from the schematic
5. To simulate the NAND gate using MMSIM Spectre
6. To determine the rise time and fall time of the output waveforms.

4 Introduction

By performing this experiment, we will learn about the usage of CADENCE VIRTUOSO. We will also learn about the addition process of the libraries (basic, analogLib, gpdk090). We will also learn about the making process about the schematic, symbol and simulate, outputting the signals. We will also learn about the propagation delay, rise time, fall time.

5 Theory

NAND gate is a fundamental digital logic gate used extensively in digital circuits due to its versatility and functional completeness. A NAND gate performs the logical NAND operation, where the output is true (or high) unless both inputs are true (or high). This gate is a building block for various digital systems, including arithmetic logic units, memory storage, and more complex logic circuits. Designing a 2-input NAND gate in Cadence Virtuoso, an advanced electronic design automation (EDA) tool, involves a series of methodical steps, from schematic capture to simulation. Cadence Virtuoso offers a comprehensive environment for the design and verification of custom ICs, providing tools for schematic entry, layout editing, and extensive simulation capabilities. The process begins with creating a transistor-level schematic of the NAND gate using PMOS and NMOS transistors. This is followed by generating a symbol for the NAND gate, enabling its use in hierarchical design contexts. The next step is the simulation.

6 Truth Table

A	B	Pull Down Network	Pull Up Network	Output (O)
0	0	Off	On	1
0	1	Off	On	1
1	0	Off	On	1
1	1	On	Off	0

7 Propagation Delay

7.1 $\mathbf{P}_{mos} = 240\ nm$, $\mathbf{N}_{mos} = 240\ nm$

(0 indicates Falling; 1 indicates Rising)

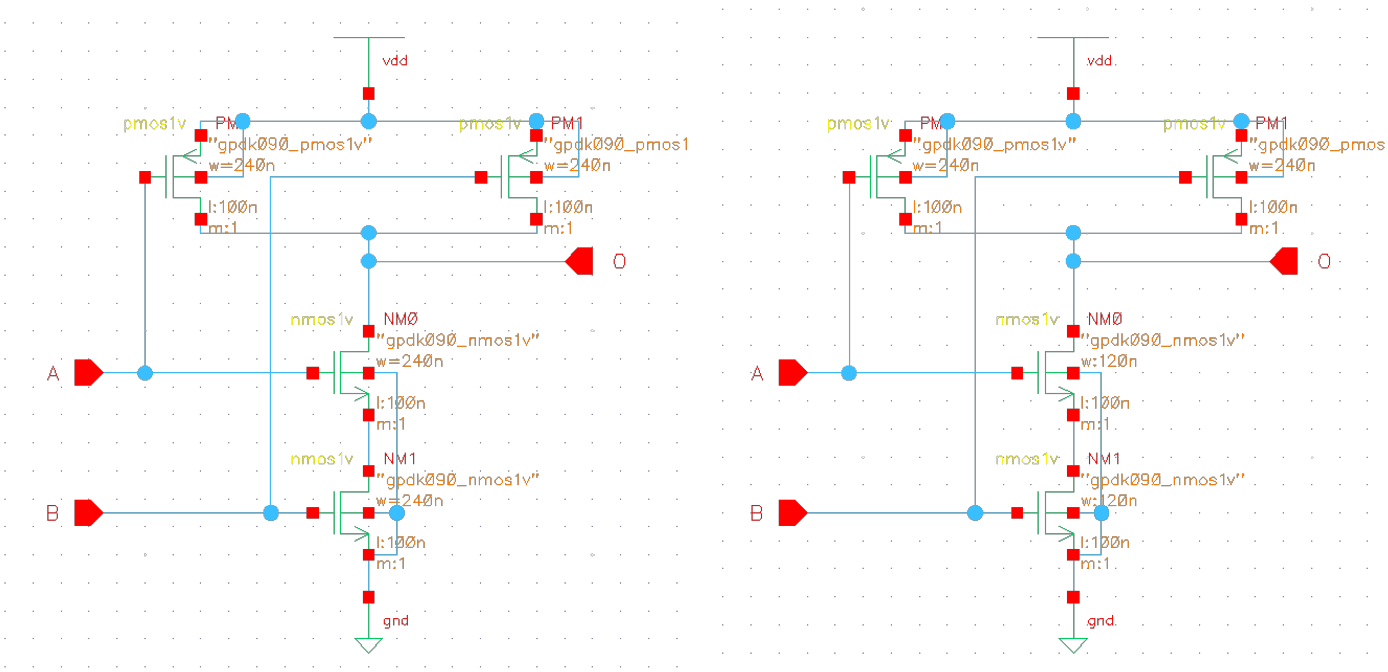
A	B	Propagation Delay (s)
0	0	5.006×10^{-9}
0	1	8.201×10^{-12}
1	0	6.254×10^{-12}
1	1	4.992×10^{-12}

7.2 $\mathbf{P}_{mos} = 240\ nm$, $\mathbf{N}_{mos} = 120\ nm$

(0 indicates Falling; 1 indicates Rising)

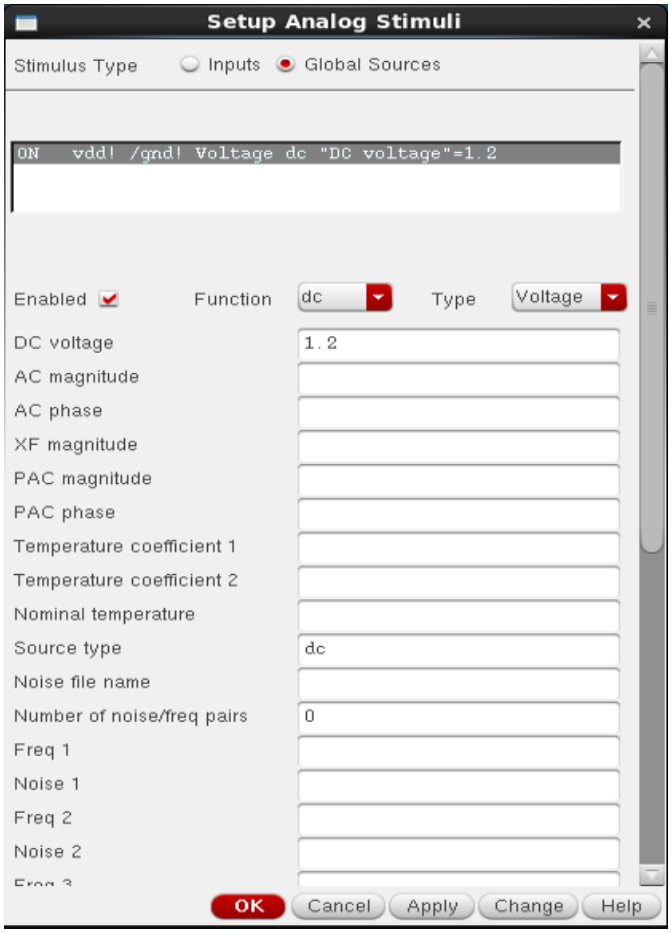
A	B	Propagation Delay (s)
0	0	5.01×10^{-9}
0	1	7.228×10^{-12}
1	0	9.79×10^{-12}
1	1	4.993×10^{-12}

8 Simulation Setup

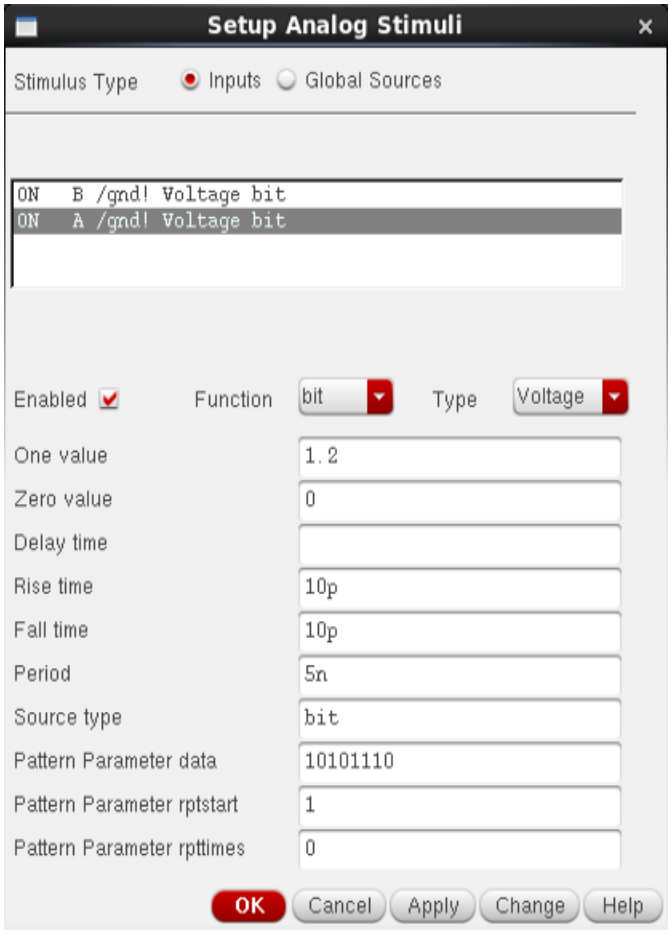


(a) Schematic where $\mathrm{P}_{mos} = 240\ nm$, $\mathrm{N}_{mos} = 240\ nm$ (b) Schematic where $\mathrm{P}_{mos} = 240\ nm$, $\mathrm{N}_{mos} = 120\ nm$

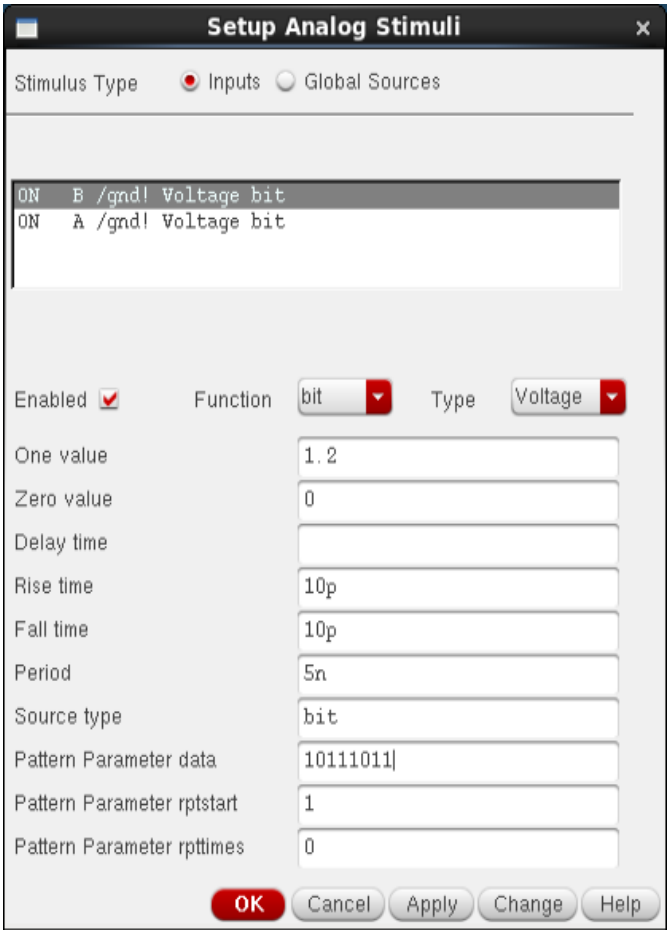
Figure 1: Internal circuitry of NAND gates



(a) Parameter selection for global source



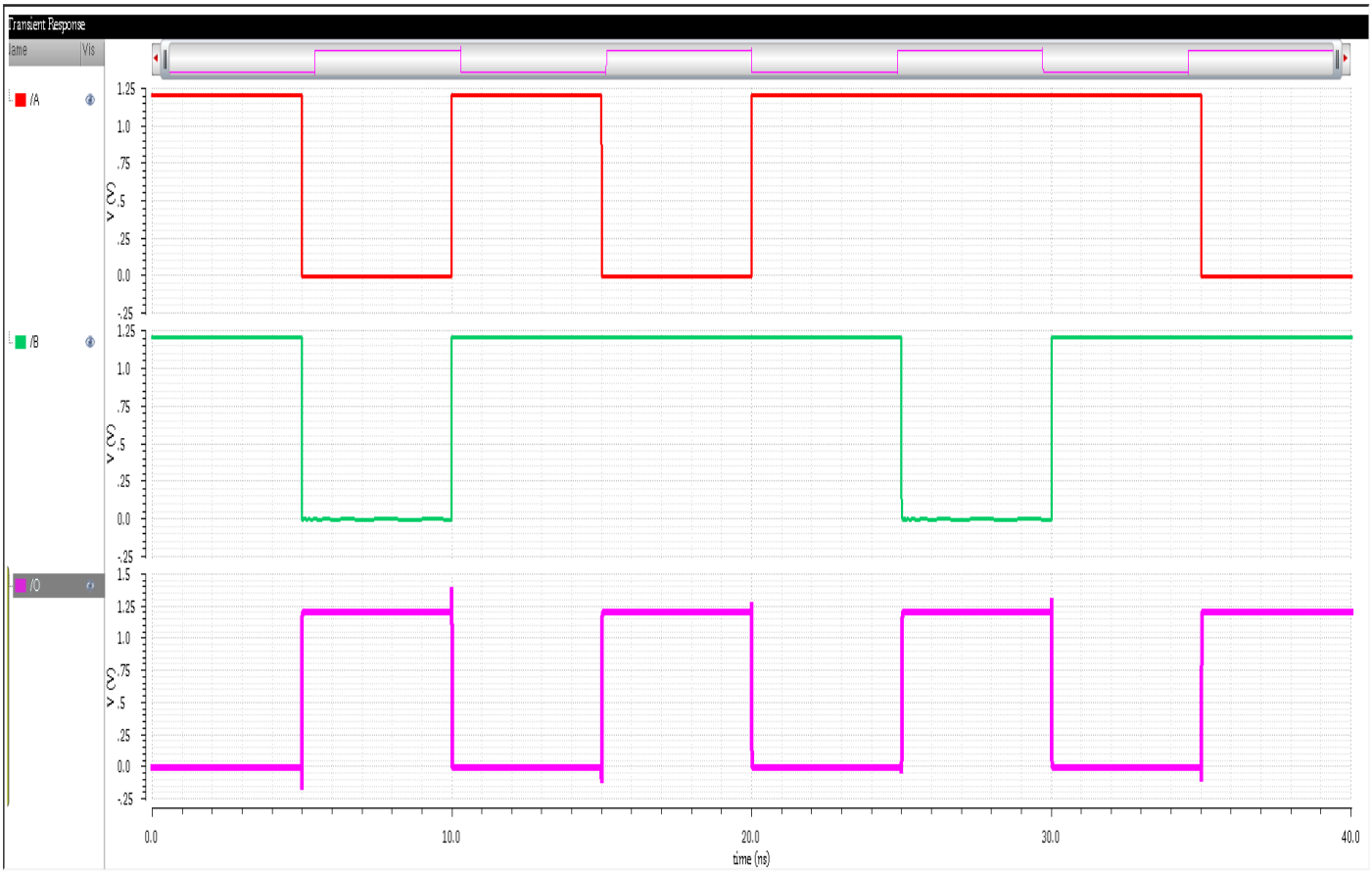
(b) Parameter selection for input A



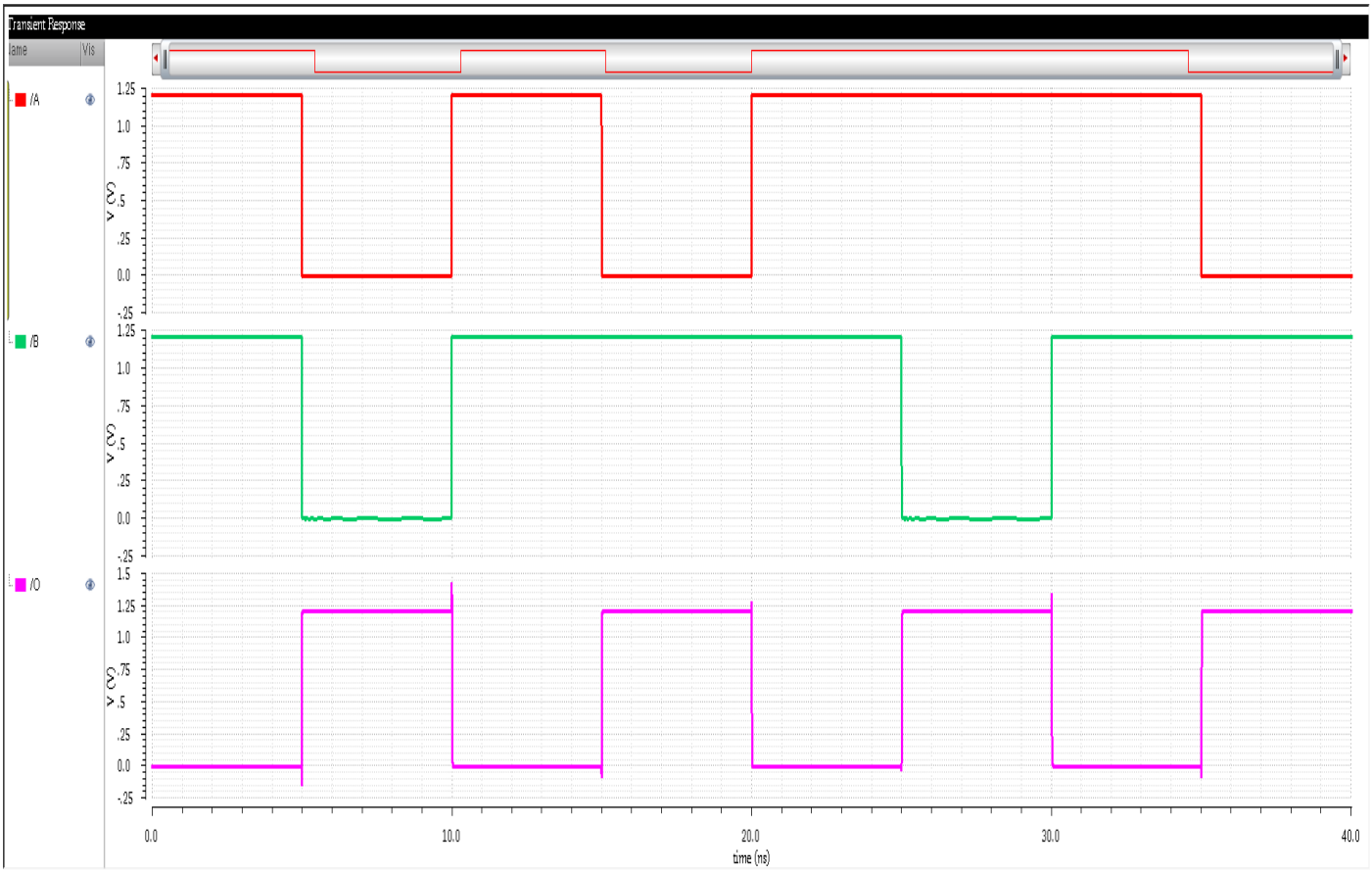
(c) Parameter selection for input B

Figure 2: Definition of Input Parameters

9 Simulation Result

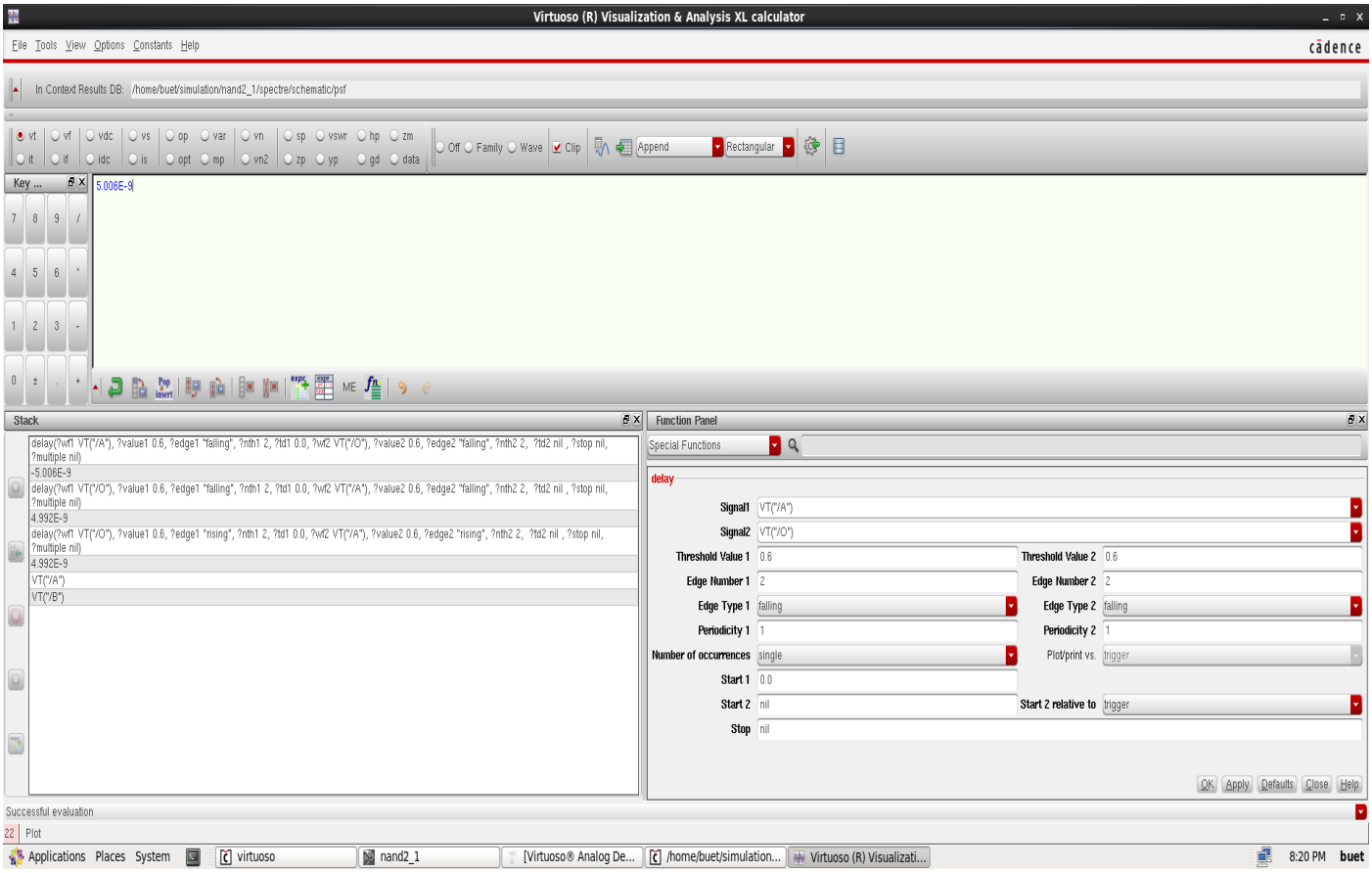


(a) Output wave forms for $P_{mos} = 240\ nm$, $N_{mos} = 240\ nm$

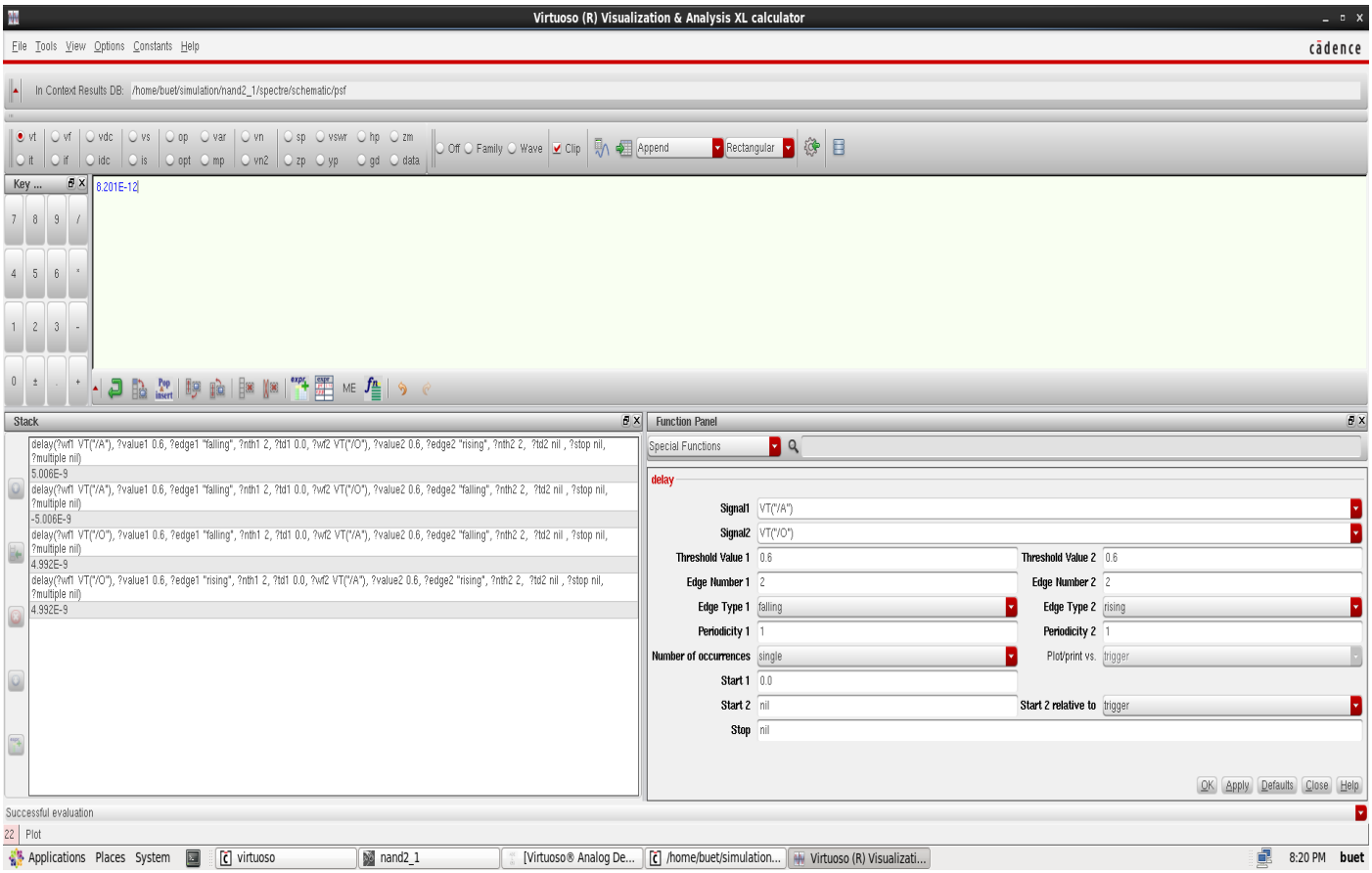


(b) Output wave forms for $P_{mos} = 240\ nm$, $N_{mos} = 120\ nm$

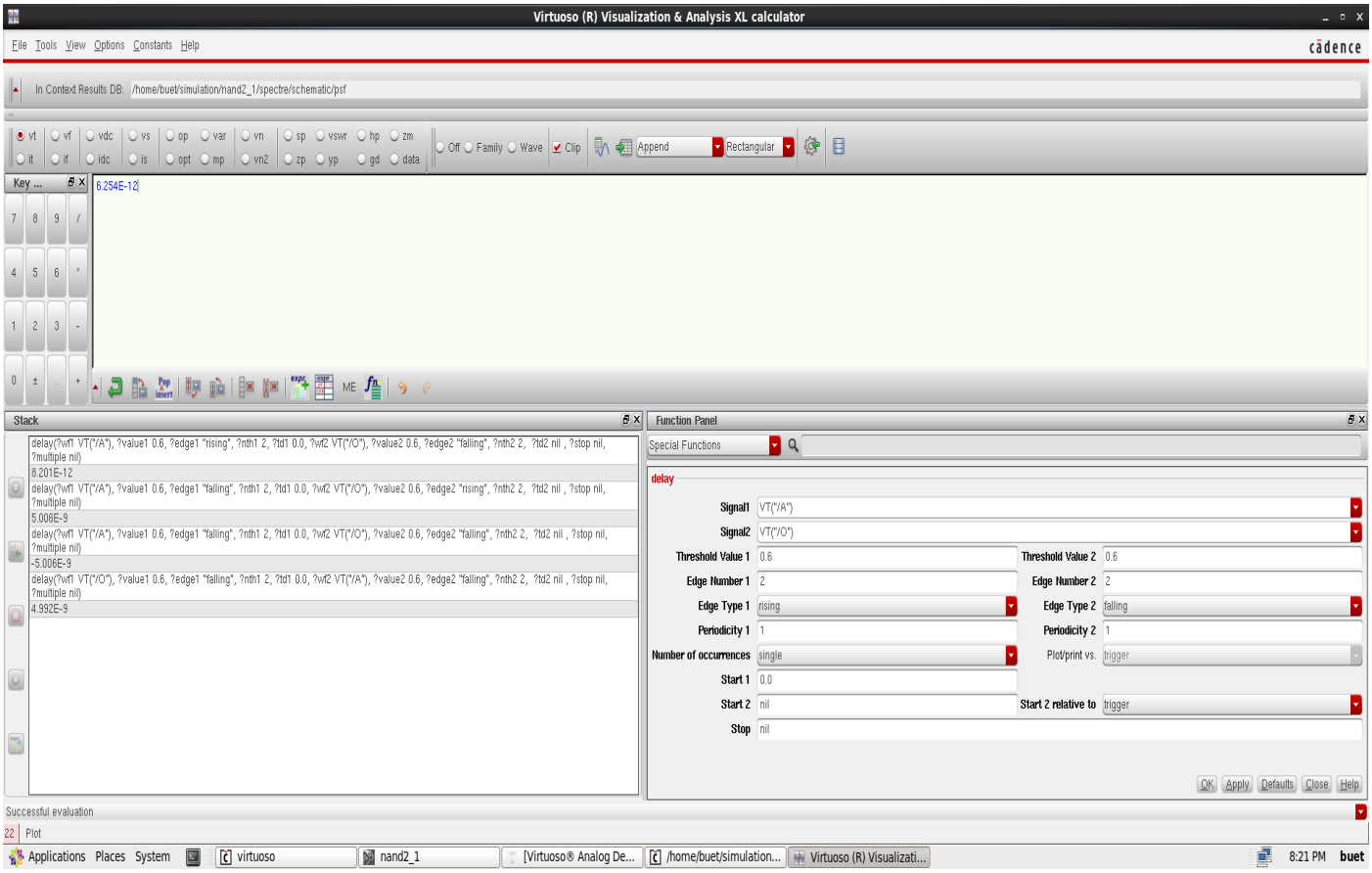
Figure 3: Input and Output waveforms of NAND Gates



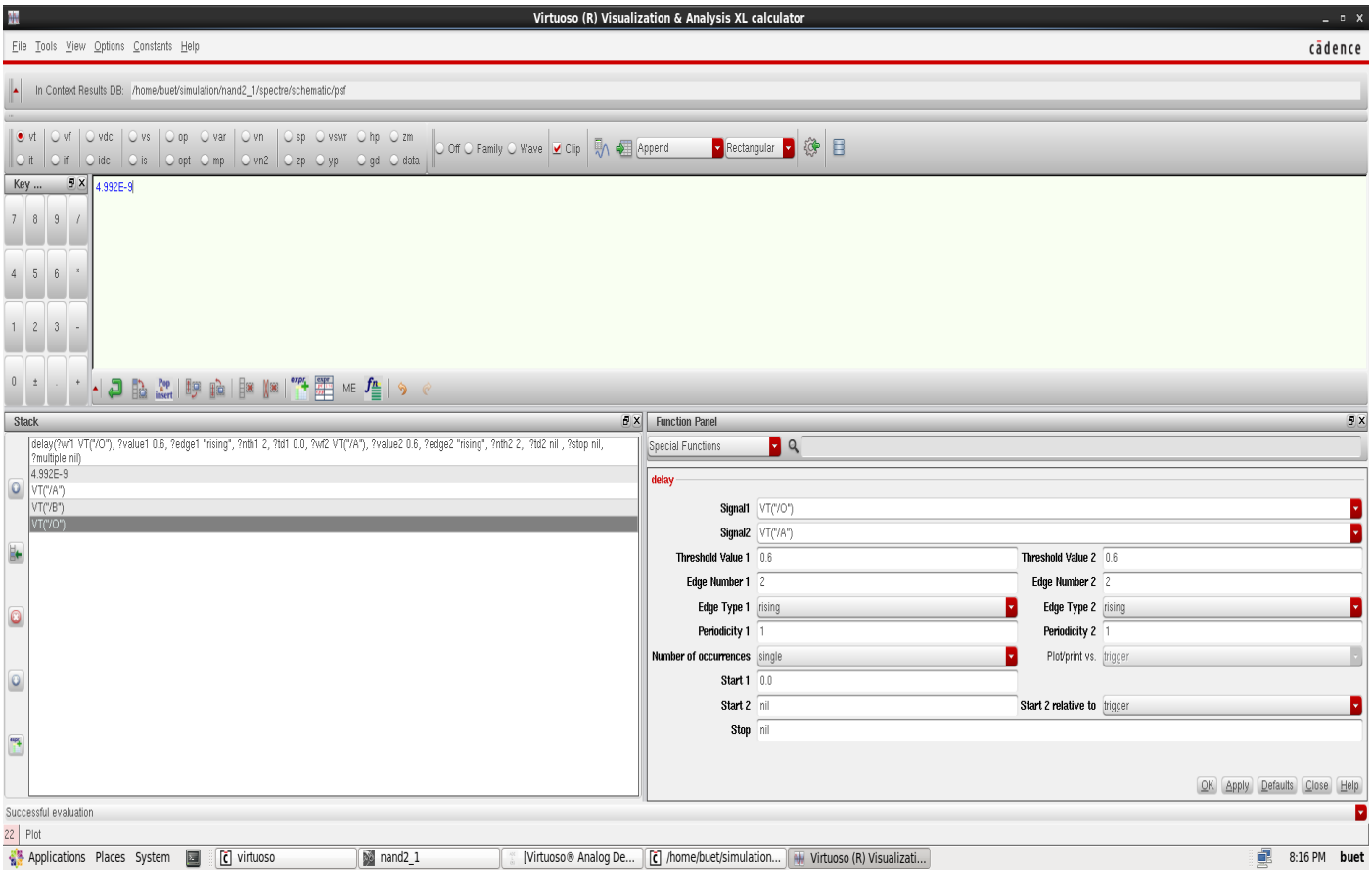
(a) When both edges are falling



(b) When edge 1 is falling but edge 2 is rising

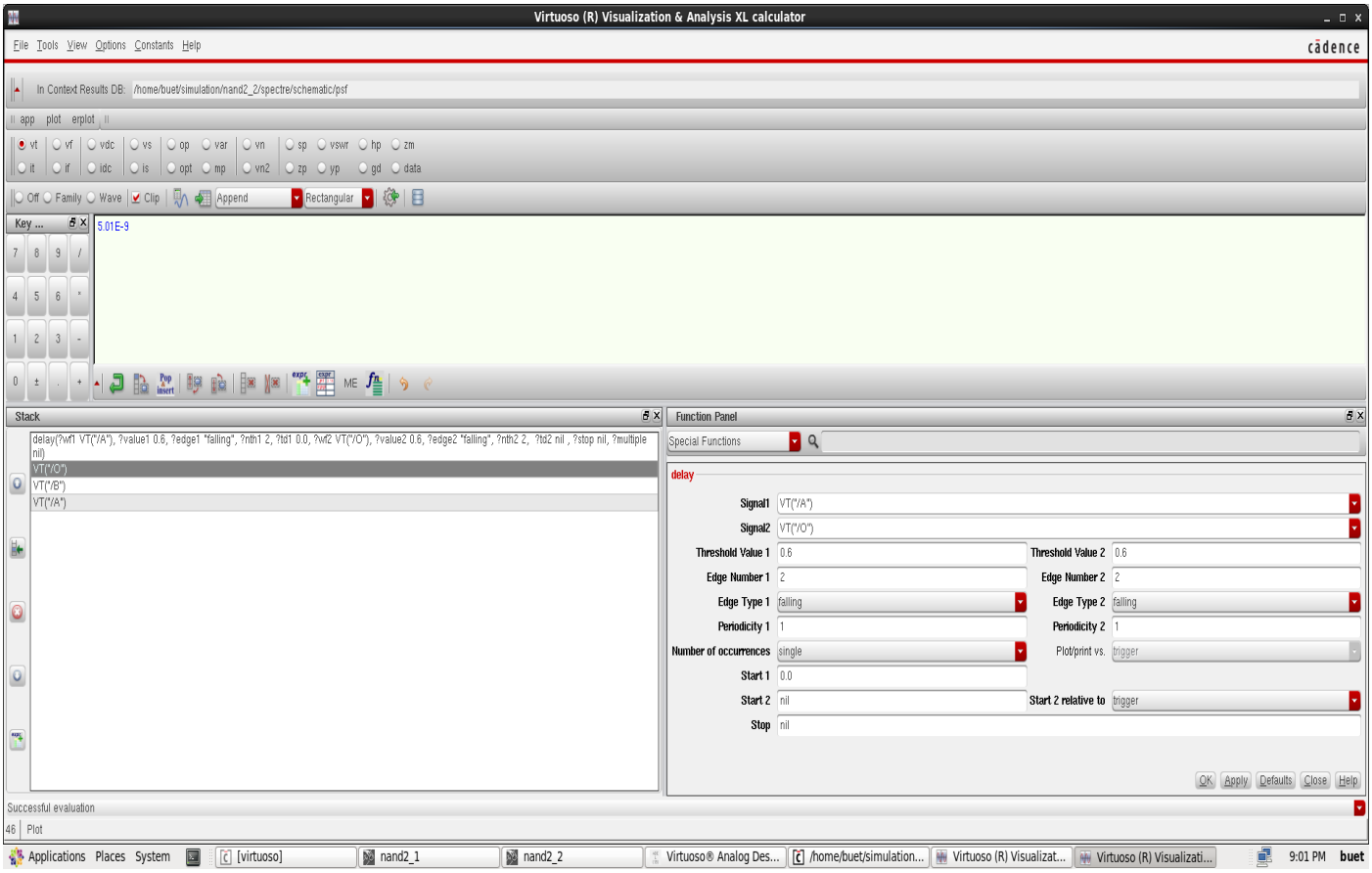


(c) When edge 1 is rising but edge 2 is falling

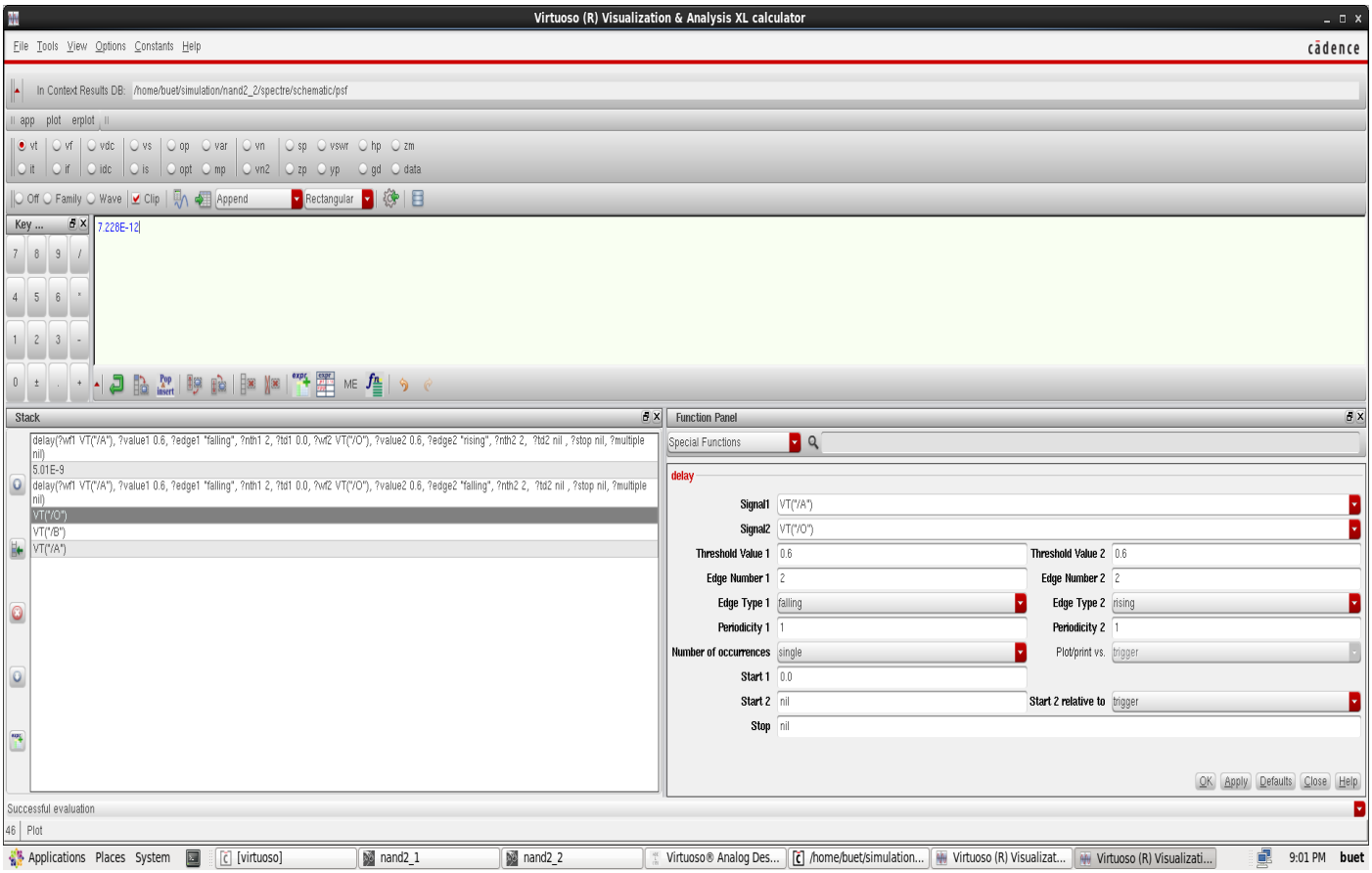


(d) When both edges are rising

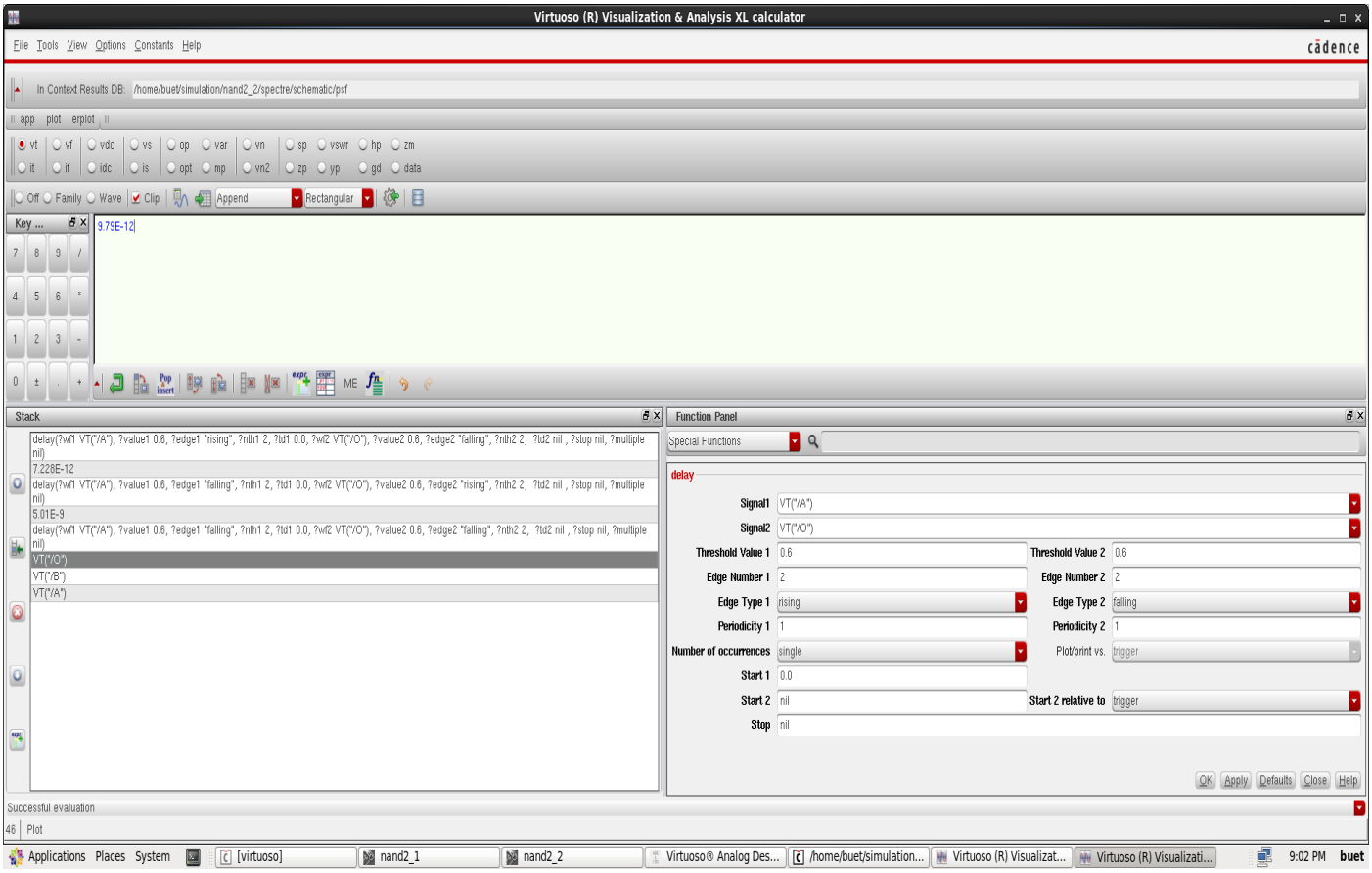
Figure 4: Propagation delay for 240 nm N_{mos} architecture



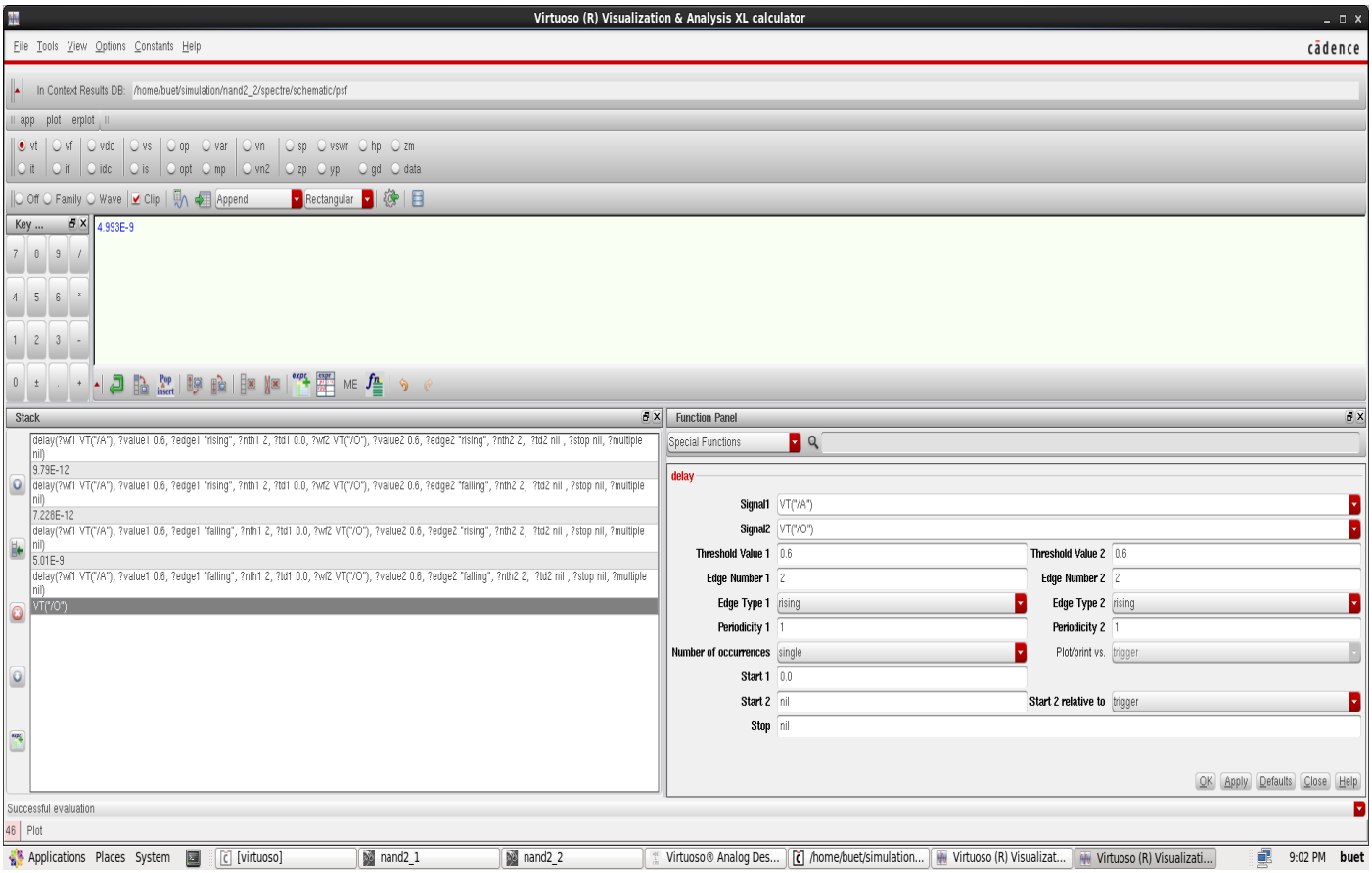
(a) When both edges are falling



(b) When edge 1 is falling but edge 2 is rising



(c) When edge 1 is rising but edge 2 is falling



(d) When both edges are rising

Figure 5: Propagation delay for 120 nm N_{mos} architecture

10 Tools Used

1. Cadence Virtuoso.
2. VMware Hypervisor.

11 Conclusion

In this experiment, we became acquainted with Cadence Software. We created the schematic for a 2-input NAND gate and identified the required parameters and waveforms. We also prepared a truth table and compared it with the simulation results.

12 References

1. Lab Manual.
2. Cadence Virtuoso Tutorial - University of Southern California.