Chittagong University of Engineering and Technology

Department of Electrical and Electrical Engineering

EEE 476: VLSI Technology Sessional

Experiment Number – 2
Experiment Name: Create the Layout of a 2 - input NAND Gate, perform Design Rule Check (DRC), Layout Vs. Schematic (LVS) test, run RCX and perform Parasitic extraction.

Prepared by

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Group No. : X_1
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