Department of Electrical & Electronic Engineering
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EEE 476 VLSI Sessional
Experiment No.: 04
Design a Two Stage CMOS Operational Amplifier and Study of its DC and AC Characteristics Using Cadence Virtuoso

Objectives:

- To design an un-buffered two stage CMOS Operational Amplifier with an n-channel input pair
- To study the large signal dc characteristics of the Op-Amp
- To study the small signal characteristics of the Op-Amp

Lab 8-1. To write the specification of a two stage CMOS Op-Amp and to fix the transistor sizes and bias currents from the level 2 model parameters of the NMOS and PMOS transistors.

The design procedures of the Two-stage CMOS Op-Amp are described in great details in the book : *CMOS Analog Circuit Design, Second Edition by Philips E. Allen and Douglas R. Holberg, OXFORD University Press*. You are required to study *section 6.3 Design procedure for the Two-stage CMOS Op-Amps (Page 269-280)* carefully and design the op-amp using typical NMOS and typical PMOS transistors of the Analog library provided by Cadence.

Specification of the Op-Amp :
The specification of the of the Op-Amp is given below

Av> 5000 V/V	VDD : 2.5 V	VSS : -2.5 V
GB : 5 MHz	C_L: 10 pF	SR > 10 V/us
V_{out} range : ± 2V	ICMR : -1 to 2 V	$P_{diss} \leq 2$ mW

The model files of the typical NMOS and PMOS transistors are in the following location:
/home/eda/Cadence/IC615/tools.lnx86/dfII/samples/artist/models/spectre/cornerMos_mod.scs
We will use the typical NMOS and typical PMOS section of the model (Section TNTP)

simulator lang=spice
* VTI-derived Level=2 nominal model
.model nmos4 nmos level=2 vto = 0.775 gamma=0.4 tox = 400e-10 nsub = 8e+15 xj = 0.15U ld = 0.20U u0 = 650 ucrit = 0.62e+5 uexp = 0.125 vmax = 5.1e+4 neff = 4.0 delta = 1.4 rsh = 36 cgso = 1.95e-10 cgdo = 1.95e-10 cj = 195U cjsw = 500P mj = 0.76 mjsw = 0.30 pb = 0.8

.model pmos4 pmos level=2 vto = -0.75 gamma=0.57 tox = 400e-10 nsub = 6e+15 xj = 0.05U ld = 0.20U u0 = 255 ucrit = 0.86e+5 uexp = 0.29 vmax = 3.0e+4 neff = 2.65 delta = 1.0 rsh = 101 cgso = 1.90e-10 cgdo = 1.90e-10 cj = 250U cjsw = 350P mj = 0.535 mjsw = 0.34 pb = 0.8

PRE_LAB : From the model parameters and with reference to *Figure 6.3-2* of the Book *CMOS Analog Circuit Design by Philips E Allen*, *and Douglas R. Holberg* design the various components of the Op-Amp and fill up the table below. Please fill up the form before coming to the Lab for this experiment. You will not be allowed to proceed further without completing the PRE-LAB.

Parameters	Equation/Criteria used to fix value	Design value
Compensation capacitor Cc		
Steering current I_5 Current Mirror Transistor size $(W/L)_3$ and $(W/L)_4$		
gm_1		
Input Pair Transistor size $(W/L)_1$ and $(W/L)_2$		
VDS_5		
Current source transistor size $(W/L)_5$, $(W/L)_8$		
gm_6		
Output stage load transistor size $(W/L)_6$		
Output stage drive transistor size $(W/L)_7$		

Lab 8-2. Design of the Two Stage CMOS Operational Amplifier

The following figure show the Schematic diagram of the two stage Op amp. Take nmos4, pmos4 etc. from analog lib. Please note that the transistor dimension of your circuit may be different from that shown in the figure below.

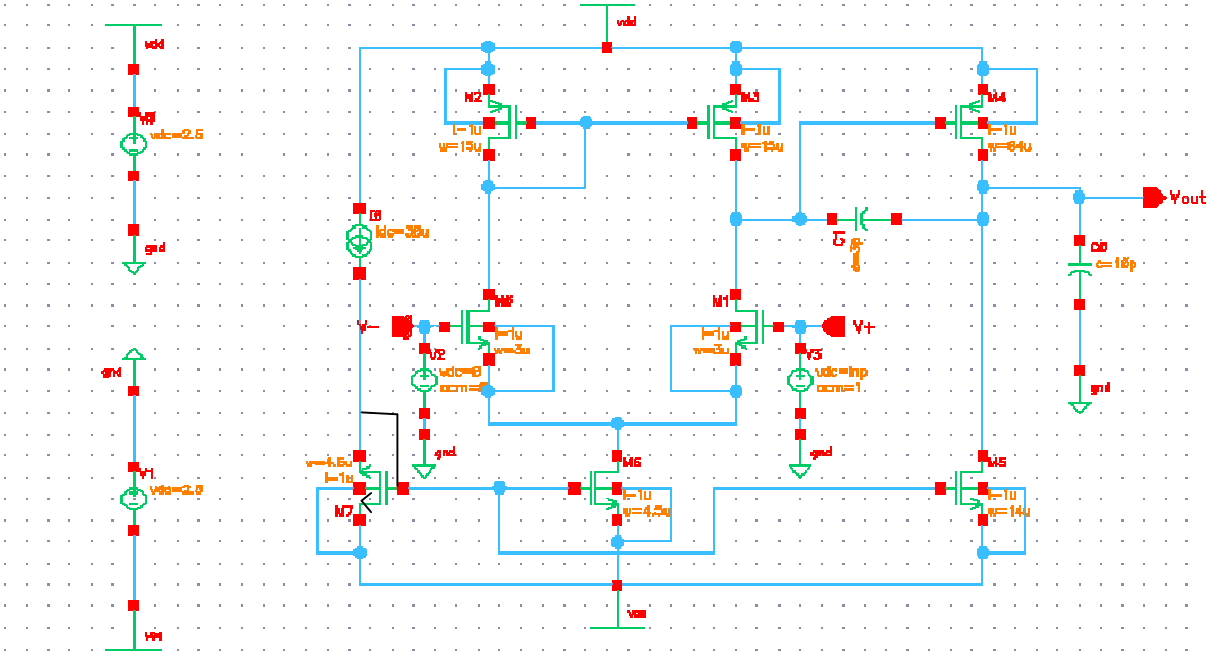


Fig. Schematic of the two stage Op-Amp (Change the figure)

1. **Simulate the transfer characteristics of the Op-Amp.**

   Find the transfer characteristics of the Op-amp and determine the output offset voltage of the amplifier. For this purpose set the voltage of the *V*+ terminal as a variable and then make a coarse sweep of this variable form -2 Volts to +2 Volts and run a dc analysis to find the values of *Vin* where the output makes the transition from VDD to VSS. Once the transition range is found, *Vin* is swept over values that only include the transition region. Use the following voltage specification for the *V*+ and the *V*- terminal.

V+	DC voltage : inp, AC magniture : 1 V
V-	DC voltage: 0 , AC magintude: 0 V

   From the transfer characteristics curve determine the output off-set voltage as well as the input off-set voltage.

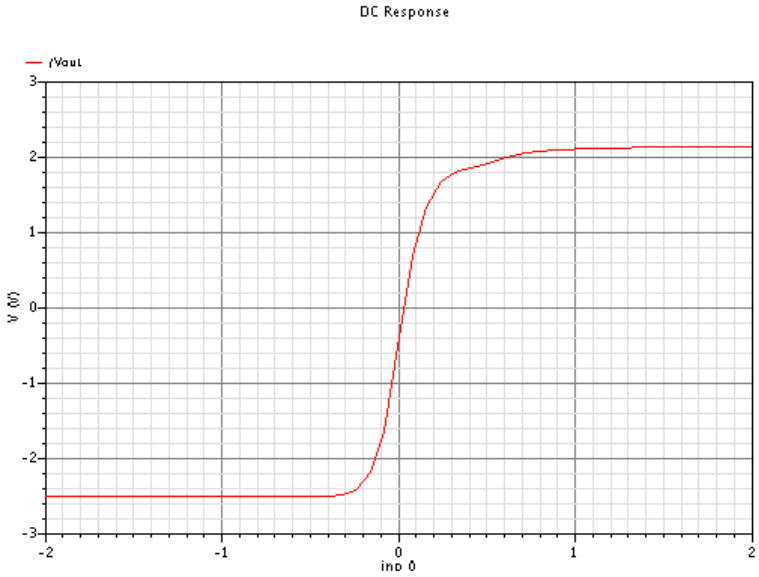
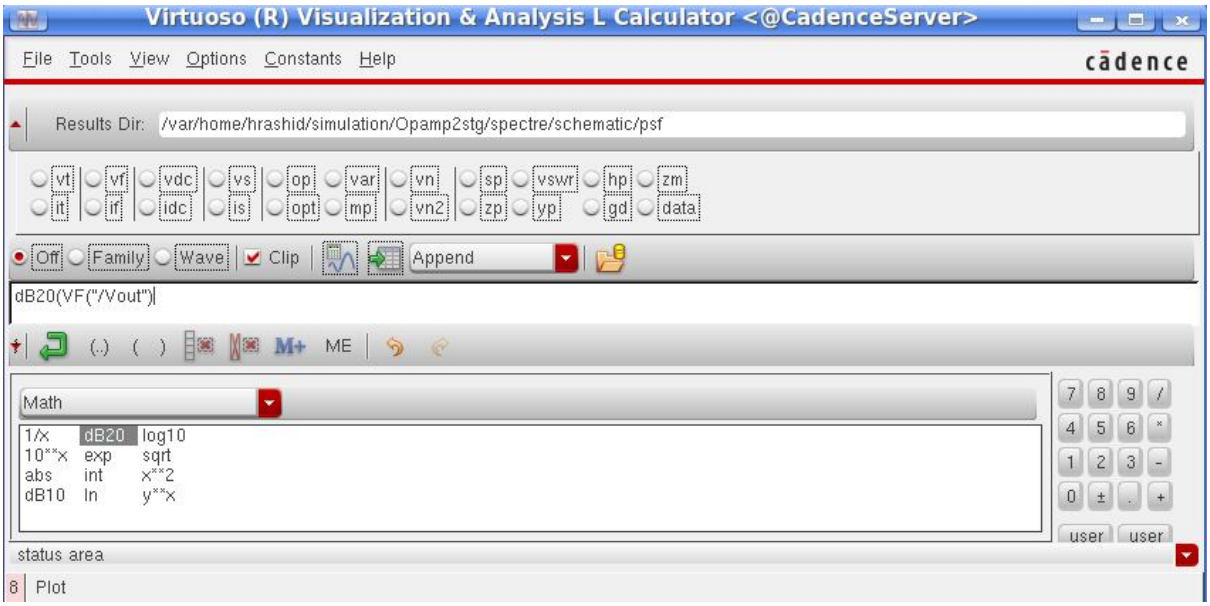


Fig. Transfer characteristics of the Op-Amp

2. Frequency response of the Op-AMP

For this purpose we will perform the ac analysis in spectre. In the ac sweep use *frequency* as a *sweep variable*, and vary the frequency from 10 kHz to 1 GHz. Set *sweep type* as *automatic*. Now a plot of output voltage magnitude in V versus frequency in Hz will be plotted out. However, we want to plot the output voltage in dB. For this purpose in the graph window execute *Tools* → *Calculator*. The Virtuoso Visualization and Analysis Calculator window will appear as follows. In the calculator window execute *Options* → *Algebric*. Now double click the dB20 function and it will appear in the evaluation window.



Click the *vf* variable to select the ac voltage expression. The cursor will automatically move to the virtuoso schematic window. Now select the voltage *Vout* in the schematic window and it will be automatically loaded to the expression. You need to close the bracket of the expression manually. Now the expression is ready to be plotted. In the calculator window execute ***Tools → plot***. The output voltage *Vout* in dB versus frequency curve will be plotted.

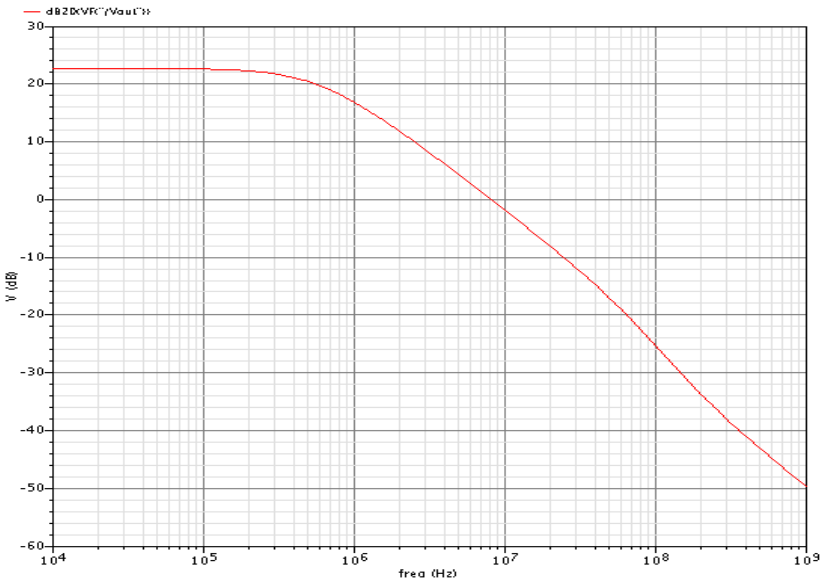


Fig. Frequency response of Output Voltage

From the graph determine the location of the dominant pole and the gain band width (GB) of the amplifier. Also determine the phase margin and the gain margin of the amplifier from the calculator. You can find the *gainBWProd*, *PhaseMargin* and the *GainMargin* in the special function of the calculator.

3. simulation of Common Mode Rejection Ratio

The objective of this simulation is to get an output that is equal to CMRR or can be related to CMRR. The following figure shows a method that can accomplish this objective. Two identical voltage sources designated as *Vcm* are placed in series with both op amp inputs where the op amp is connected in the unity gain configuration. To accomplish this first create a symbol of the Op-Amp and then connect it as shown below. For this circuit it can be shown that $\frac{V_{out}}{V_{cm}} = \frac{1}{CMRR}$

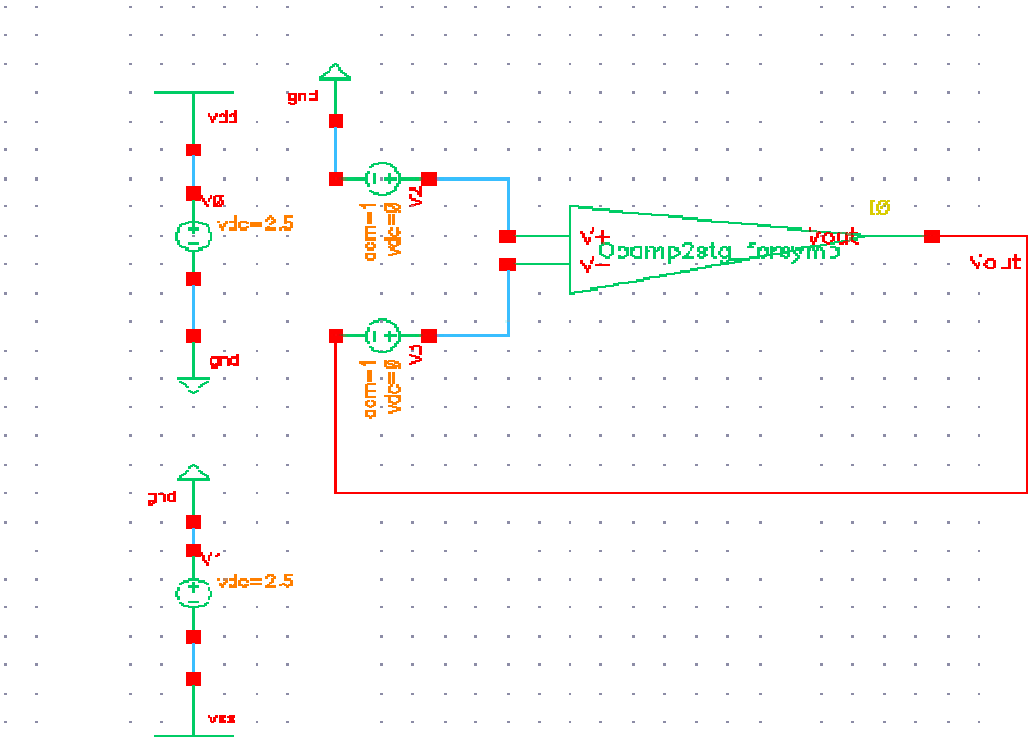


Fig. Set-up for the simulation of the CMRR

The frequency response of 1/CMRR is given in figure below.

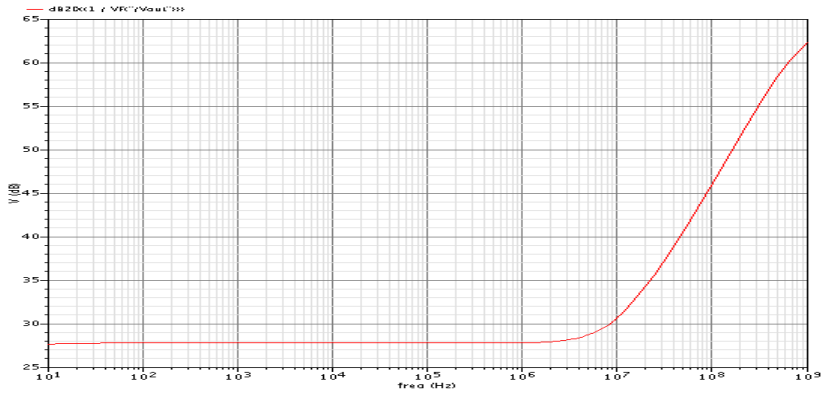


Fig. Frequency response of (1/CMRR)

4. Simulation of PSRR$^+$ and PSRR$^-$

Use similar circuits to measure the PSRR$^+$ ($\nabla V_{DD}/\nabla V_{out}$) and PSRR$^-$ ($\nabla V_{SS}/\nabla V_{out}$)

Report :

1. Provide the circuit diagram and performance curves of the circuits
2. Compare in a table the design specifications with the simulated specifications.
3. Discuss about the discrepancy between the design specifications and the simulated specifications.
4. Simulate the design at fast fast and slow slow corner and compare the specification again.