Hardware Test Sheet

MSc in Digital Systems Engineering
Department of Electronics
University of York

Group Project

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1 Test #1

2 Tester name: Simone Ledda

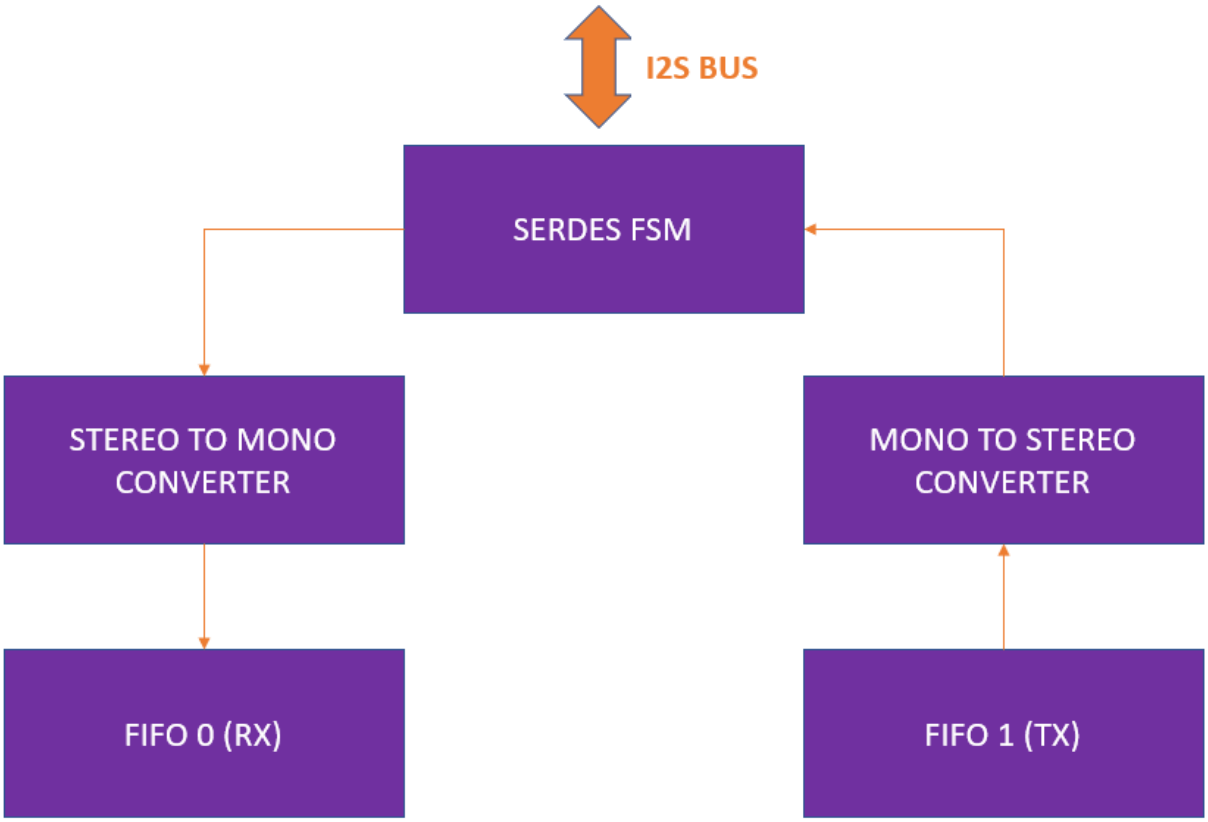
3 Test date start: 02-07

4 Test date finish: 04-07

5 UUT typology (VHDL entity ~~/ custom IP / subsystem~~)

6 UUT name: Mono to stereo converter

7 Hardware block design screenshot



8 Objective of test

1. Ensure the entity gets reset done correctly
2. Ensure entity calls for data only on left channels
3. Ensure entity duplicates the fetched sample and feeds it to the SERDES FSM on both channels

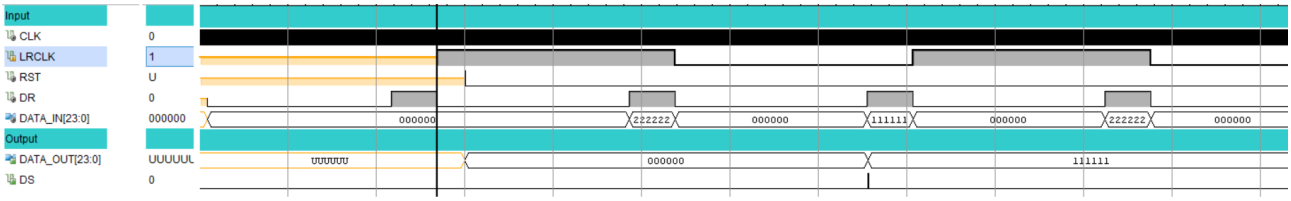
The following test is ran in compliance with the V-model testing strategy

9 Testbench description / test strategy overview:

The testbench uses several processes to emulate LRCLK behaviour from the I2S bus. Input lines are loaded with two different set of values to ensure only left channel values are sampled and reach the SERDES FSM.
LRCLK has a frequency of 48kHz.
DR is driven by a serdes-like process to emulate the behaviour of the FSM

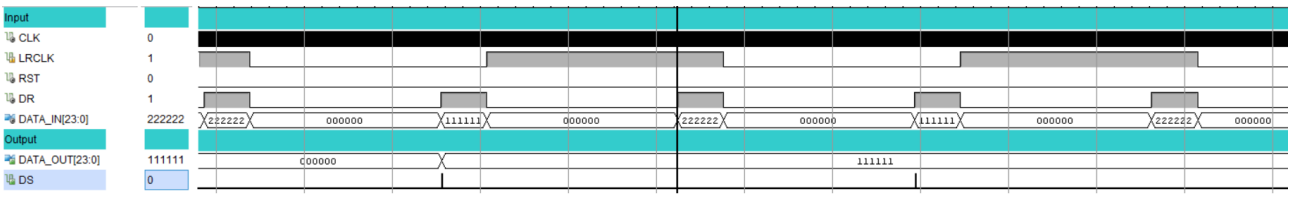
Left channel sample: 0x111111
Right channel sample: 0x222222

10 Test results:



Entity reset

It's possible to observe that the entity is reset correctly.



Operation

It's possible to observe that the entity pulls the data strobing signal high just for 10ns only when the left channel needs to be read.
From the picture above it's visible that the only samples reaching the SERDES are left channel samples as it was expected.

11 Observations:

Strobing signal (DS) and bus are loaded simultaneously and the bus is not loaded with 0s when not used, instead it was chosen to leave the previous sample on it so that when the FSM tries to read for the right channel it reads the same sample read on the left one.

12 Grade (pass/fail):

PASS

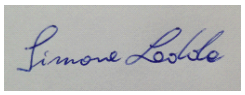
13 Approval signatures

Recoverable Signature

X M. Reynolds

Matt Reynolds
Hardware Manager
Signed by: 645892a3-94a8-42ef-8ccc-0fe12b98ad6a

Recoverable Signature

X 

Simone Ledda
Test Manager
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