Software Test Sheet

MSc in Digital Systems Engineering
Department of Electronics
University of York

Group Project

Contents

1 Test #1

2 Tester name: Simone Ledda

3 Test date start: 18-05

4 Test date finish: 5-06

5 UUT typology (~~VHDL entity / custom IP~~ / subsystem)

6 UUT name: ADAU 1761 audio codec

7 Software/driver functionality description

The drivers, written in C, have to read and write the codec registers. It should also be possible to burst write and burst read registers (respectively reading and writing multiple adjacent registers). The communication between the PL and the audio codec is handed over to the I2C protocol. The driver should initialize the codec's PLL, then configure ADCs, DACs, Mixers involved in the input and output path, configure the headphones, gains, serial port, protocol, sampling frequency, bit-clock samples, and power settings.

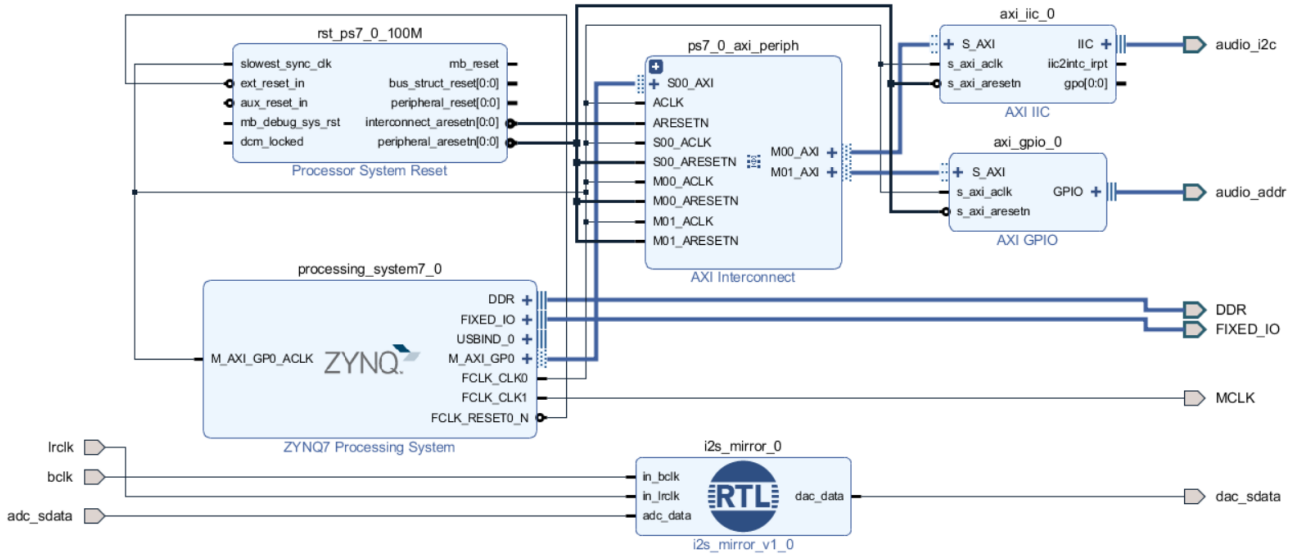
8 Objective of test

1. Ensure reading and writing functionality over I2C protocol
2. Configure the PLL register and check lock bit assert
3. Buffer the input to the output headphones
4. Tune gains and noise filtering for better audio quality

The black-box testing strategy is used for this test.

9 Test results

The audio codec has to be interfaced using two protocols, I2C for the control registers and I2S for audio streaming data. Before being able to hear anything from the streaming data, it's crucial to have solid I2C functions set to successfully customize the 62 registers of the ADAU1761.



Block diagram of the architecture under test

To test the system it was necessary to create the block design above so that the PL features an audio buffer (i2S_mirror) and sends back to the codec over the dac_sdata line whatever it wrote on the adc_sdata line.

Two important hardware blocks, located on the PL, are the AXI-GPIO and the AXI-IIC. The AXI-IIC handles the communication through the SDA and SCL lines, the AXI-GPIO is instead used to set two codec's pin down to 0. These pins represent two programmable bits in the codec's chip address, in case on the bus there were multiple devices and some may have close addresses.

For the correct codec setup, it was chosen to feed it an 8MHz clock from the PL named MCLK in the above block design.

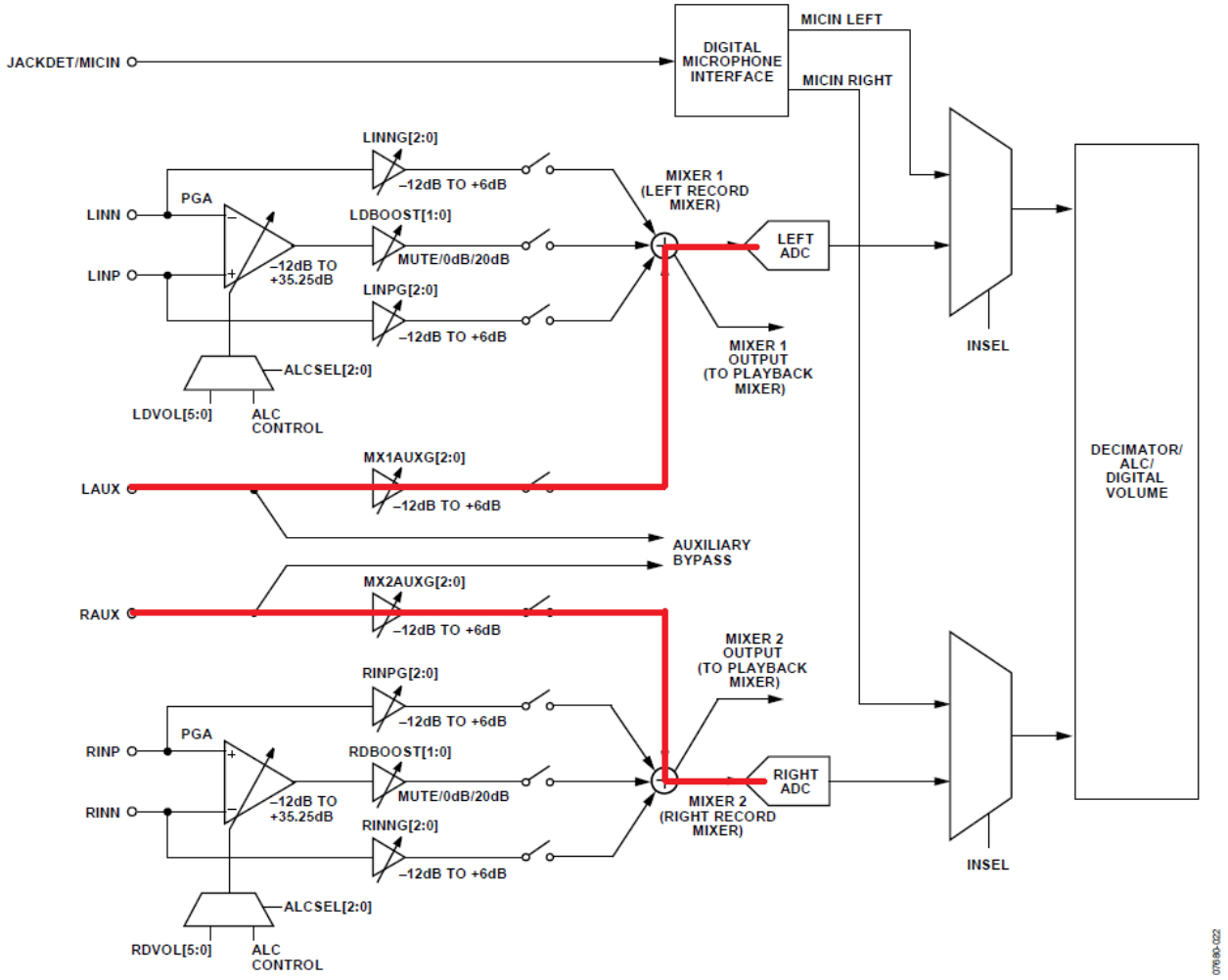
A huge amount of time was spent understanding the functioning of the AXI-IIC IP block and the Xilinx's function set, but finally, the interface is up and running and it's possible to read and write even in burst mode.

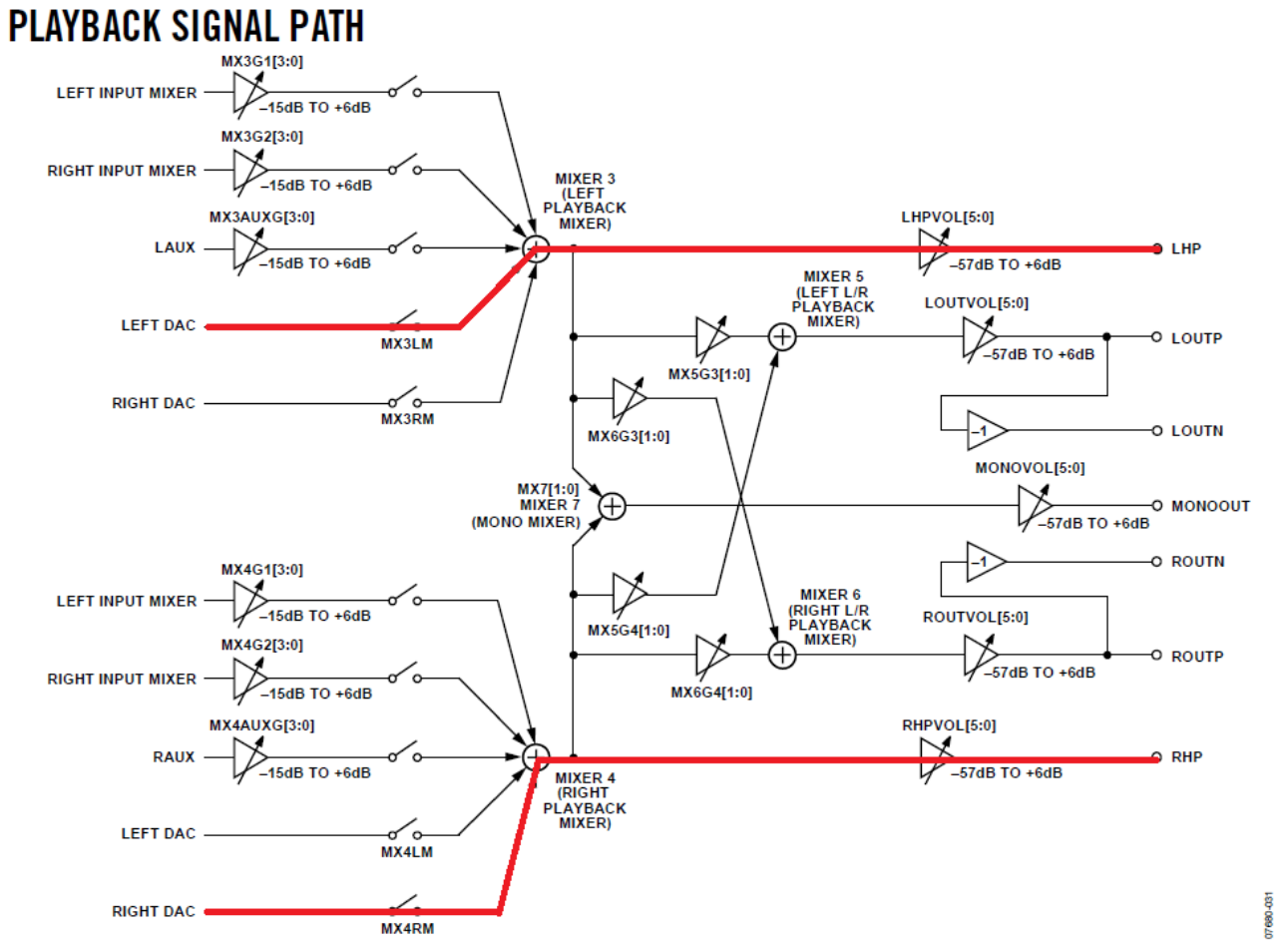
Burst mode is necessary to set the PLL register that is 6 bytes long.
PLL lock bit was also polled and was asserted by the codec.

Due to the board layout, it was chosen to use LINE IN as input and HP+MIC as the output jack, hence register settings follow this setup.

Mixer registers were set accordingly to the following diagrams

RECORD SIGNAL PATH

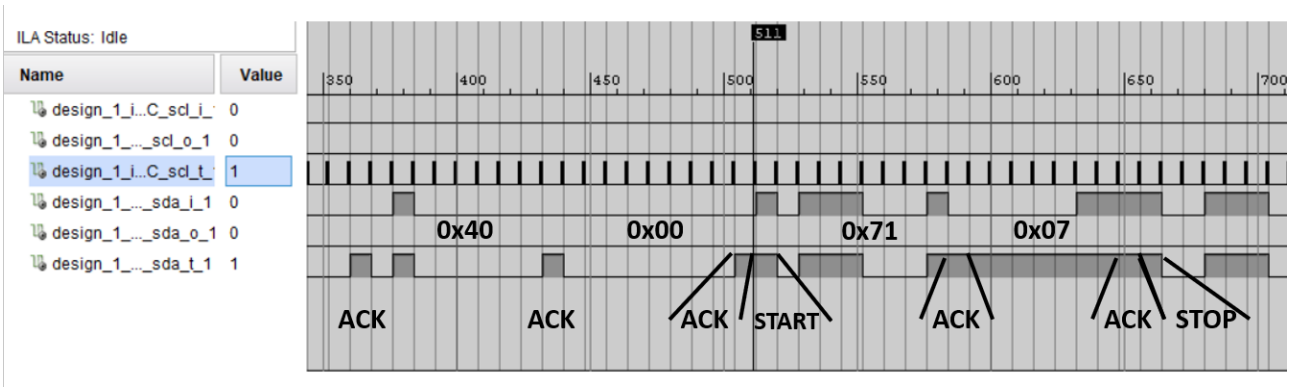




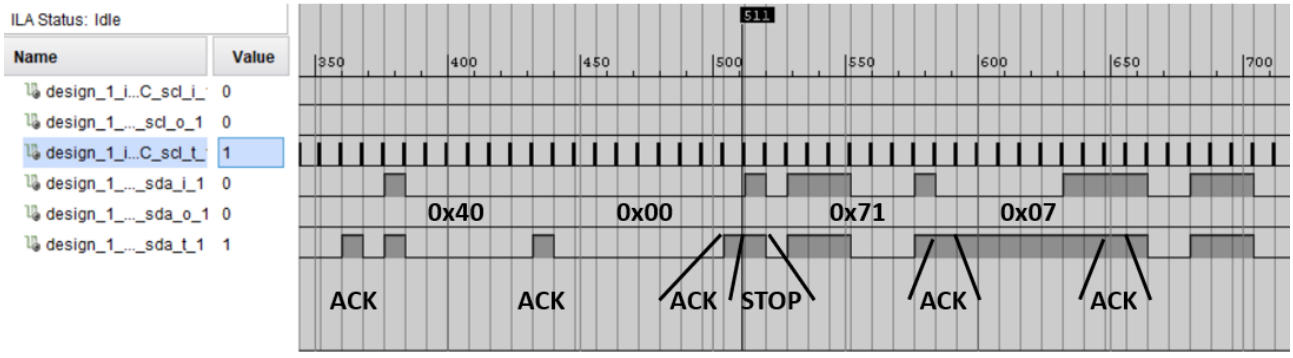
It was chosen to use 48kHz sampling frequency, after the project specs, for every internal device in the codec (from the serial port to ADCs and DACs).

All gains were pushed to the maximum value available to avoid phenomenons like no output can be heard, when the actual output is there, it's just a low volume source.

Registers were also read back to double-check their values, to exclude that the registers may be corrupted or the I2C protocol didn't behave coherently.



Writing function I2C writing register 0x4000 of chip address 0x71 with data 0x07



Reading function I2C retrieving previously written data

Unfortunately, it wasn't possible to hear the input source through the output headphones, only a very loud buzzing and popping noise could be heard.

10 Observations

The absence of hardware acceleration and the certainty of reliability of IP blocks such as AXI-IIC and AXI-GPIO narrowed down the error to a wrong codec registers setting. A further test will follow to sort out the audio output.

11 Grade (pass/fail):

I2C drivers for reading and writing operations – PASS

ADAU 1761 codec settings – FAIL

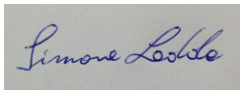
12 Software manager approval signature

Recoverable Signature

X Gavin Johnston

Gavin Johnston
Software Manager
Signed by: 1007ad75-1394-4c98-a3c5-949a4bae4391

Recoverable Signature

X 

Simone Ledda
Test Manager
Signed by: afcb6896-9ce1-4821-8979-577ea3a903e5