Hardware Test Sheet

MSc in Digital Systems Engineering
Department of Electronics
University of York

Group Project

Contents

1 Test #1

2 Tester name: Simone Ledda

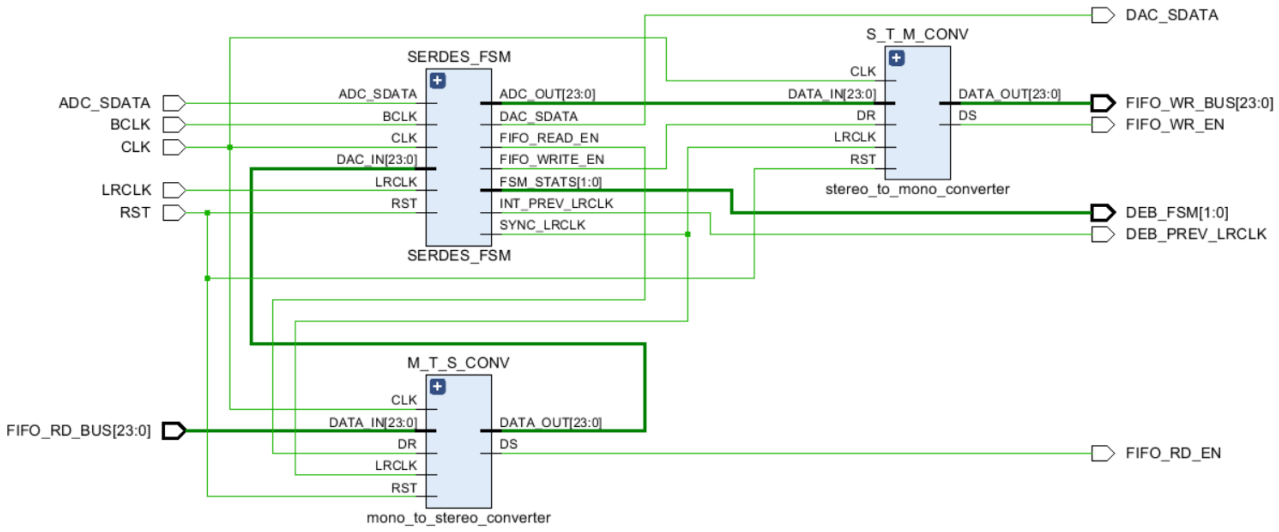
3 Test date start: 06-07

4 Test date finish: 07-07

5 UUT typology (~~VHDL entity~~ / custom IP / ~~subsystem~~)

6 UUT name: SERDES_INTERFACE

7 Hardware block design screenshot



8 Objective of test

1. Testbench the architecture and verify reset occurs correctly
2. Testbench inputs and outputs data is as expected
3. Testbench timing of the control signals

The following test is ran in compliance with the V-model testing strategy

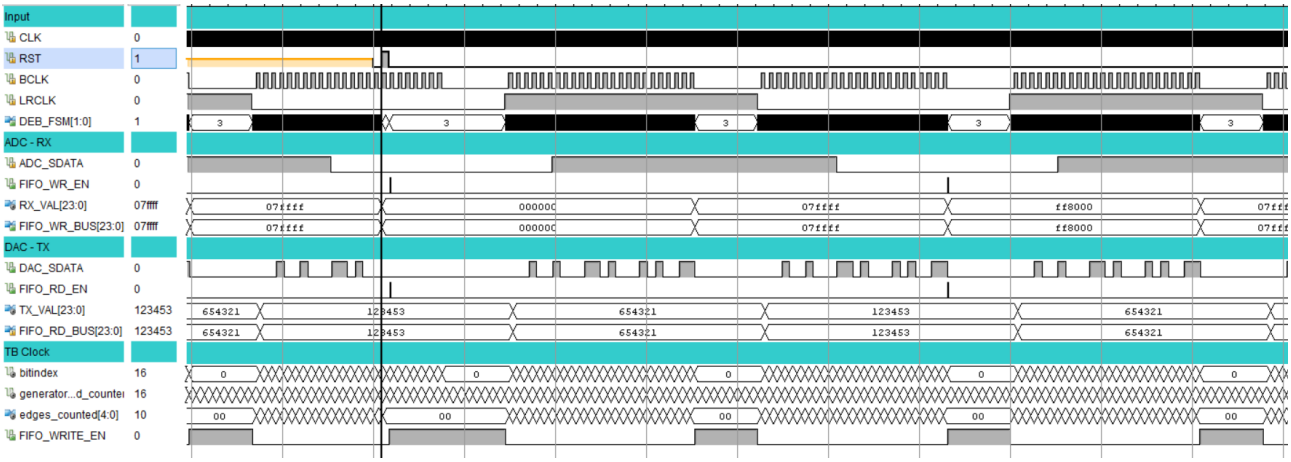
9 Testbench description / test strategy overview:

The testbench aims to reset correctly the IP, but also to correctly parallelize ADC_SDATA audio frames as well as serializing FIFO_RD_BUS samples.
To achieve this and ensure only left channel samples are involved, it was chosen to operate as follows

ADC_SDATA line was loaded with a BCLK and LRCLK-dependent process so that when the left channel is being received the sample being carried is 0xFF8000, instead when the right channel is being received it carries the sample 0x07FFFF, hence samples being written in the output FIFO_WR_BUS are expected to be 0xFF8000 only. This tests the correct behaviour of stereo to mono converter.

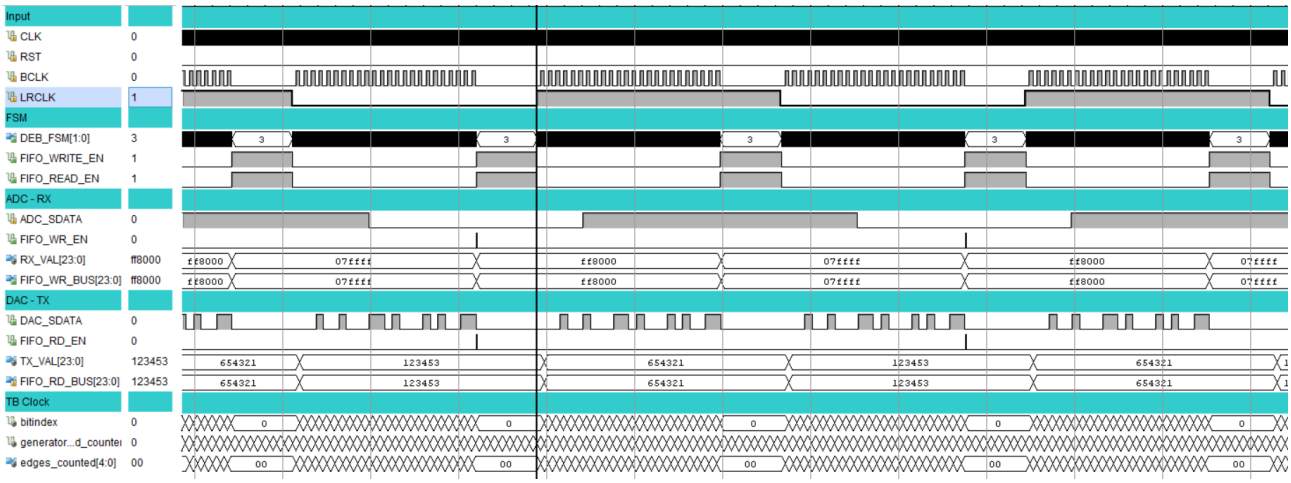
Samples being fetched on FIFO_READ_BUS carry two different samples as well to test the correct operation of mono to stereo converter entity. When the left channel is being sent the bus lines are loaded with 0x123456, instead on right channel there's 0x654321. The IP will have to send only 0x123456 on both channels. In reality this is an even augmented test environment since FIFO's samples will not change on right channels because the FIFO will not be reached by the read enable signal, but this test shows furthermore that the FSM is not seeing the wrong sample either because it's fed an internally stored sample (0x123456) stored in the mono to stereo entity register.

10 Test results:



SERDES INTERFACE RESET

The previous picture shows the correct behaviour of the IP under reset. The IP will only face a reset at the beginning of the program when the processing system reset blocks are enabled, after that it's a free-running IP as the audio codec keeps on sending samples even when there's no file in reproduction.



Behaviour of the IP

The previous picture shows how the IP behaves during the test. It's possible to observe that the audio frames are processed as expected as read and write commands to fifos are fired only on left channels and the DAC_SDATA line is loaded always with the same sample (0x123456)

11 Observations:

The IP fires instructions simultaneously as expected, it also needs to be tested on hardware as the starting point of our application's datapath. The first next test will be a buffering test.

12 Grade (pass/fail):

PASS

13 Approval signatures

Recoverable Signature

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Hardware Manager
Signed by: 645892a3-94a8-42ef-8ccc-0fe12b98ad6a

Recoverable Signature

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