Hardware Test Sheet

MSc in Digital Systems Engineering
Department of Electronics
University of York

Group Project

Contents

1 Test #1

2 Tester name: Simone Ledda

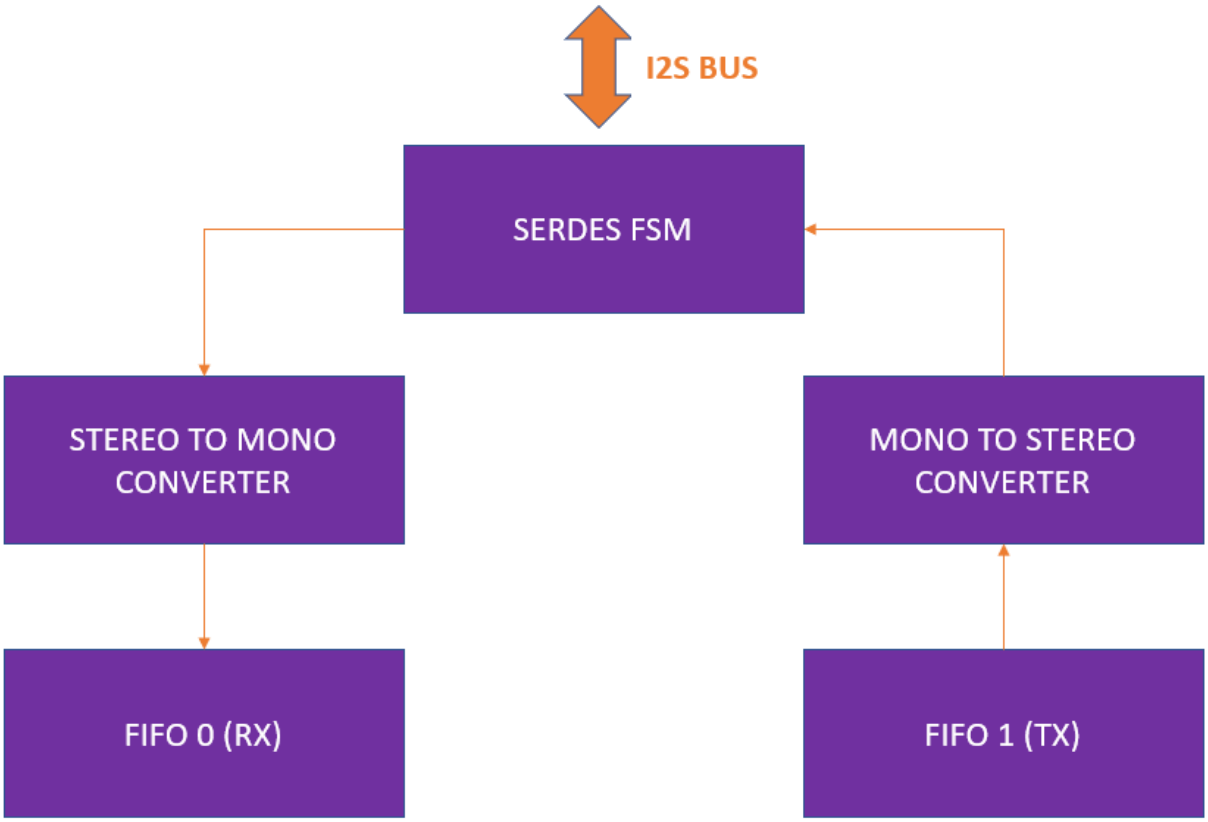
3 Test date start: 29-06

4 Test date finish: 01-07

5 UUT typology (VHDL entity ~~/ custom IP / subsystem~~)

6 UUT name: Stereo to mono converter

7 Hardware block design screenshot



8 Objective of test

1. Ensure entity gets reset correctly
2. Ensure the converter only allows left channel samples to reach the FIFO
3. Ensure the data strobing signal to the FIFO lasts for 1 clock period @100MHz

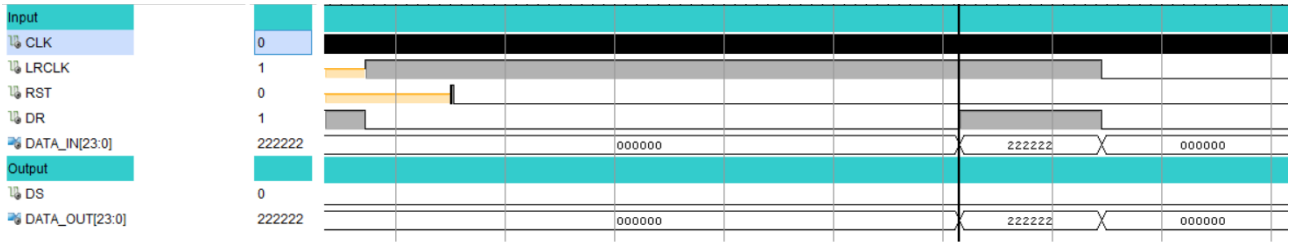
The following test is ran in compliance with the V-model testing strategy

9 Testbench description / test strategy overview:

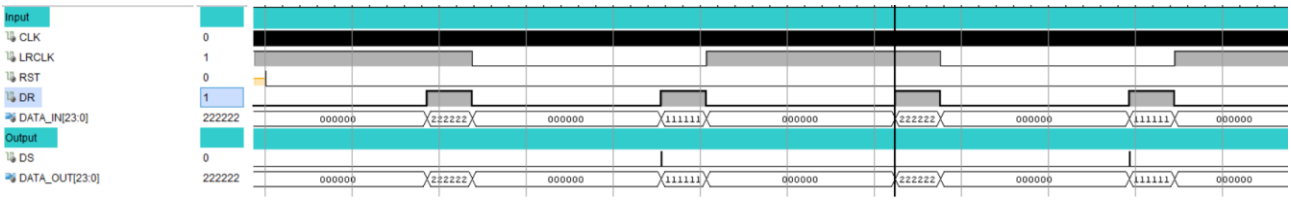
The following entity's testbench uses several processes to emulate I2S bus behaviour, in addition to this there's an initial reset followed by two different sets of data loaded one on the left channel and one on the right channel, so that it's clearly visible which one reaches the output.

Left channel data : 0x111111
Right channel data: 0x222222

10 Test results:



Initial reset



Global behaviour of the entity

From the images above it can be seen that the reset occurs correctly and the output of the entity is only 0x111111 which is all data belonging to left channels (LRCLK = '0'). Also the data strobing signal (DS) that drives the FIFO only stays high for 10 ns when a left channel data is present.

11 Observations:

DS and the bus are loaded simultaneously and in dead times between one sample and the other the bus is loaded with all 0s. It's also possible to find right channel data on the bus though no fifo write (DS) signal is present hence that data is lost as expected.

12 Grade (pass/fail):

PASS

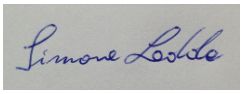
13 Approval signatures

Recoverable Signature

X M. Reynolds

Matt Reynolds
Hardware Manager
Signed by: 645892a3-94a8-42ef-8ccc-0fe12b98ad6a

Recoverable Signature

X 

Simone Ledda
Test Manager
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