Hardware Test Sheet

MSc in Digital Systems Engineering
Department of Electronics
University of York

Group Project

Contents

1 Test #1

2 Tester name: Simone Ledda

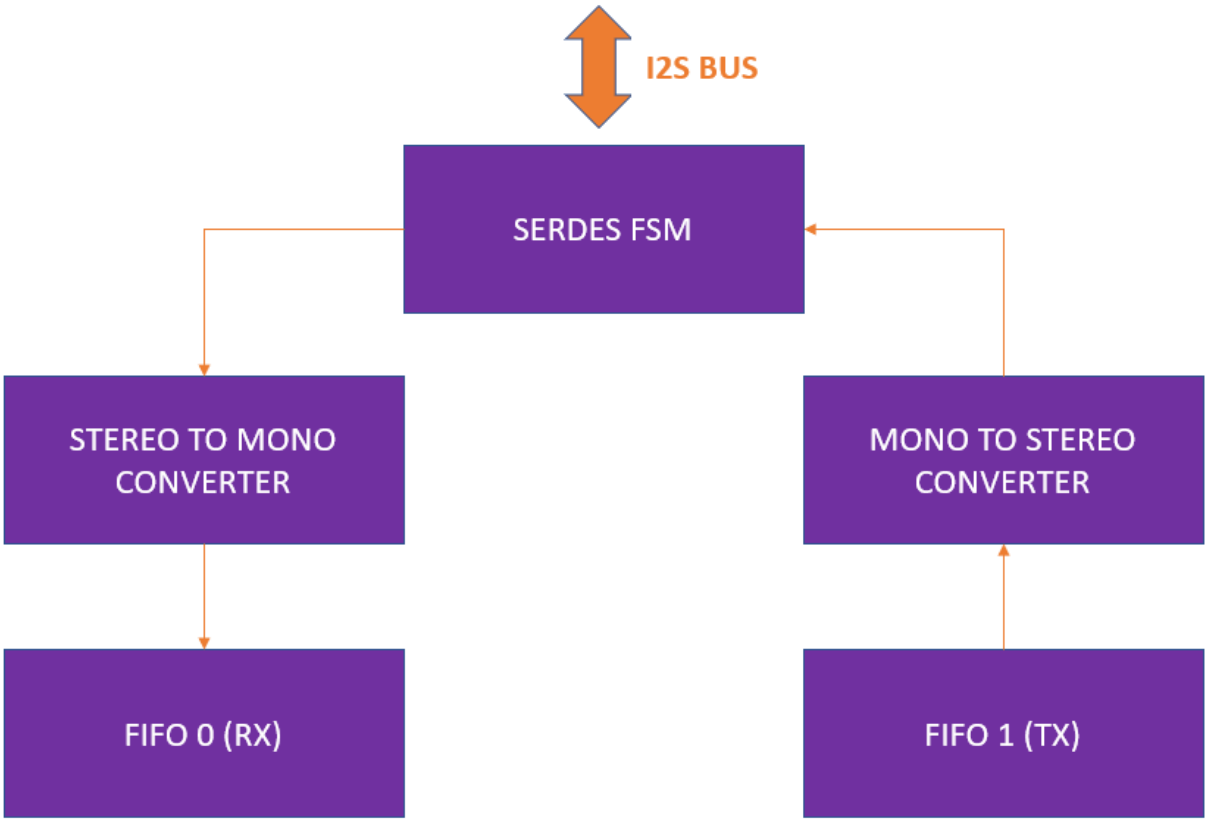
3 Test date start: 22-06

4 Test date finish: 28-06

5 UUT typology (VHDL entity ~~/ custom IP / subsystem~~)

6 UUT name: SERDES FSM

7 Hardware block design screenshot



8 Objective of test

1. Coherent behaviour of the FSM
2. Parallel output reflects ADC_SDATA
3. DAC_SDATA reflects parallel input
4. FIFO RD and WR signals are toggled correctly

The following test is ran in compliance with the V-model testing strategy

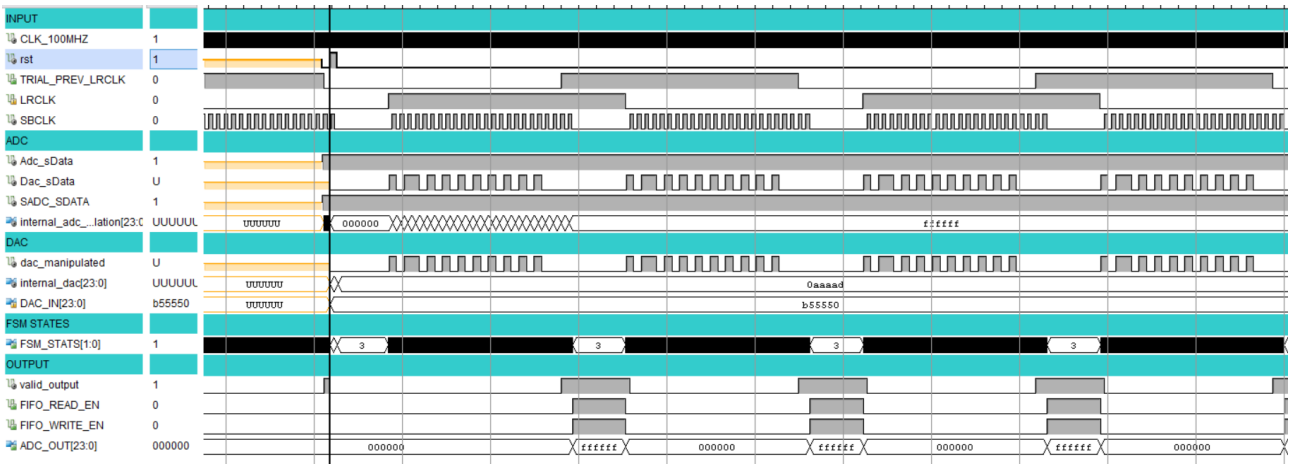
9 Testbench description / test strategy overview:

Before building the testbench, the ILA was used to scan the I2S bus line, map the timing of the bus according to the driver configuration. The present testbench features several processes to emulate the timing of the I2S bus so that the test can be as accurate as a real-case scenario.

The testbench drives the ADC_SDATA line high after reset, hence any value coming out of the FSM should be 0xFFFFFF, the input dac_in line is loaded with 0xB55550, asymmetric value to verify that internal DAC data manipulation occur flawlessly as expected.

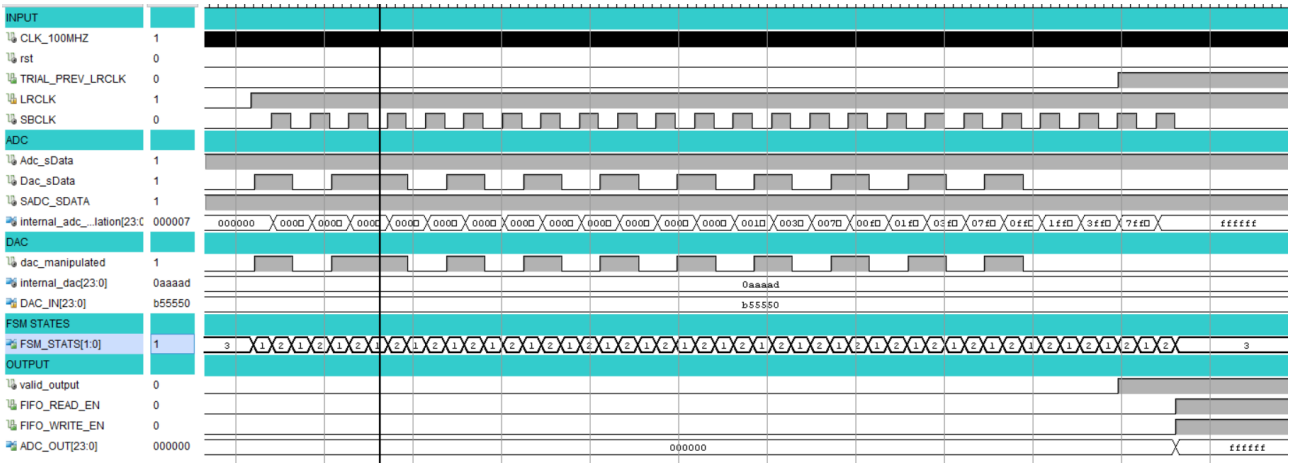
The FSM is based upon the I2S protocol, it loads dac_sdata on falling edges of BCLK and reads ADC_SDATA on rising edges of BCLK, once received the 24th bit the FSM enters CHANNEL_DETECT state (mapped as 3 in the state transitions map) and awaits a change in LRCLK line.

10 Test results:



Initial reset and following samples

The previous picture shows the correct position in time for FIFO read and write signal as well as the correct behaviour of DAC_SDATA line, repeating the same configuration.
It's also possible to observe that the output parallel data is 0xFFFFFF as expected.



Particular showing the state transitions

The previous picture shows the correct sequence of FSM states happening live, it's also possible to observe how the internal_adc_manipulation line changes its internal values as new adc bits are read upon rising BCLK edges.

11 Observations:

The FSM is operating in FULL-DUPLEX mode as expected, it's also outputting data in stereo mode (both channels left and right). It's also possible to see how every sensible data is fed to the next block on the datapath, by rising at the same time FIFO strobing signals as well as loading the output bus. To avoid inconvenients it was chosen to load all 0s on the bus in dead timings when the FSM is computing the next sample.

12 Grade (pass/fail):

PASS

13 Approval signatures

Recoverable Signature

X

Matt Reynolds
Hardware Manager
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Recoverable Signature

X

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