Stephanie Labasan

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Objective

Seeking a **full-time** research and development position in the area of **high-performance computing, power-constrained computing, and performance analysis**. Available beginning **June 2018**.

Education

Ph.D. in Computer Science University of Oregon, Eugene, OR, Advisor: Hank Childs *Expected Jun 2018*
Lawrence Scholar Graduate Fellow, *"Optimal Power Scheduling for Visualization on Supercomputers"*

M.S. in Computer Science University of Oregon, Eugene, OR *Dec 2016*

B.S. in Computer Engineering University of the Pacific, Stockton, CA *May 2013*
Minors in Engineering Management and Applied Mathematics, **Computer Engineering Department Outstanding Graduate**

Publications

Stephanie Labasan, Matthew Larsen, Hank Childs, and Barry Rountree. *PaViz: A Power-Adaptive Framework for Optimizing Visualization Performance.* In Proceedings of Eurographics Symposium on Parallel Graphics and Visualization (EGPGV), Barcelona, Spain, Jun 2017.

Stephanie Labasan, Matthew Larsen, and Hank Childs. *Exploring Tradeoffs Between Power and Performance for a Scientific Visualization Algorithm.* In Proceedings of IEEE Symposium on Large Data Analysis and Visualization (LDAV), Chicago, IL, Oct 2015.

M. Larsen, **S. Labasan**, P. Navrátil, J.S. Meredith, and H. Childs. *Volume Rendering Via Data-Parallel Primitives.* In Eurographics Symposium on Parallel Graphics and Visualization (EGPGV), Cagliari, Sardinia, Italy, May 2015.

Skills

Programming: C/C++, R, Bash, Python, HTML
Software: Intel RAPL Technology, Intel VTune, TAU
Operating Systems: Mac OS X, Linux/Unix, Windows

Work Experience

Lawrence Graduate Scholar, *Lawrence Livermore National Laboratory, Livermore CA* *Jun 2016–Present*
Contributing additional features to a C-based open-source library (libmsr) enabling tunability of hardware controls from user space. (Mentor: Barry Rountree).

HPC Power Management Researcher, *Intel Corporation, Hillsboro, OR* *Jul 2015-Jun 2016*
Prototyped a potential feature of future processors that will improve application performance by leveraging fine-grained power management capabilities within a node (Mentors: Fede Ardanaz, Jonathan Eastep).

Energy and Power Analysis Software Tools Intern, *Intel Corporation, Hillsboro, OR* *Jun 2014-Sept 2014*
Used C++ and XML to produce a detailed report of energy and power usage in mobile device components (Mentors: Grace Metri, Karla Callaghan).

Computation Student Intern, *Lawrence Livermore National Laboratory, Livermore, CA* *May 2013-Aug 2013*
Developed a noise simulator in R to predict load imbalance patterns of future exascale systems (Mentor: Barry Rountree).

Computation Student Intern, *Lawrence Livermore National Laboratory, Livermore, CA* *May 2012-Nov 2012*
Investigated the feasibility and portability of Cray's Chapel language for future HPC architectures (Mentor: Evi Dube).

Awards

Computation Department Best Poster Award, Lawrence Livermore National Laboratory *Aug 2016*
Lawrence Graduate Scholar Fellowship, Lawrence Livermore National Laboratory *Jun 2016*
SC13 Travel Grant Recipient, ACM SIGHPC *Nov 2013*
Grace Hopper 2013 Scholarship Recipient, Beyond Broader Engagement *Oct 2013*
Computer Engineering Department Outstanding Graduate, University of the Pacific *Apr 2013*
Computation Department Best Poster Award, Lawrence Livermore National Laboratory *Aug 2012*
Dochterman Outstanding Junior Scholarship Recipient, University of the Pacific *May 2012*