Stephanie Brink

Computer Scientist at Lawrence Livermore National Laboratory
High Performance Computing, Parallel Performance Tools

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Personal

Name	Stephanie Brink, née Labasan
Current Affiliation	Computer Scientist at Lawrence Livermore National Laboratory, CA
Research Interests	Energy- and power-constrained computing, performance analysis, high performance computing (HPC)
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Education

2019 **Ph.D. in Computer Science**, *University of Oregon*, Eugene, OR.
Thesis: "Optimal Power Scheduling for Visualization on Supercomputers"
Research Interests: High performance computing (HPC), parallel computing, distributed computing, power-constrained supercomputing, performance analysis
Advisor: Hank Childs

2016 **M.S. in Computer Science**, *University of Oregon*, Eugene, OR.

2013 **B.S. in Computer Engineering**, *University of the Pacific*, Stockton, CA, Minors in Engineering Management and Applied Mathematics.
Computer Engineering Department Outstanding Graduate

Awards

2019 LLNL award for championing a new mentoring opportunity for Livermore high school students to be exposed to computing.

2018 LLNL award for successfully managing the deployment of a patch for msr-safe.

2016 *Best Poster*, Computation Directorate, Annual Summer Intern Poster Symposium, Lawrence Livermore National Laboratory

2016 *Livermore Graduate Scholar Fellowship*, Lawrence Livermore National Laboratory. Full support for up to 4 years of Ph.D. research.

2013 *SC13 Travel Grant Recipient*, ACM SIGHPC. Award rate of 4% (3/70).

2013 *Grace Hopper 2013 Scholarship Recipient*, Beyond Broader Engagement

2013 *Computer Engineering Outstanding Graduate*, University of the Pacific

2012 *Best Poster*, Computation Directorate Annual Summer Intern Poster Symposium Lawrence Livermore National Laboratory

2012 *Dochterman Outstanding Junior Scholarship Recipient*, University of the Pacific

Skills

General C/C++, PYTHON, BASH, LaTeX, R, HTML, Git, SVN, CMake, Vim, Linux/UNIX

Parallel Computing — Parallel development in OpenMP and MPI. Parallel power-aware runtime system development. Performance tool development in C/C++. Performance analysis of large-scale simulation and visualization applications.

Power Management — Hardware component power monitoring and power capping interfaces. Performance analysis of power-constrained scientific visualization applications.

Research and Work Experience

04/2019–Present **Computer Scientist**, *Lawrence Livermore National Laboratory, Livermore, CA*.

06/2016–03/2019 **Livermore Graduate Scholar**, *Lawrence Livermore National Laboratory, Livermore, CA* | Technical Mentor: Barry Rountree.

- Developed a job-level runtime system in C++ to improve the distribution of power for scientific visualization algorithms by 33% by leveraging performance prediction.
- Maintaining and contributing additional features to libmsr, a C-based open-source library developed at LLNL that provides easier access to performance counters (*e.g.*, MSRs) on Intel platforms.
- Designing a more extensible C++-based library targeting performance counters across a variety of hardware architectures.

07/2015–06/2016 **HPC Power Management Researcher**, *Intel Corporation, Hillsboro, OR* | Technical Mentors: Fede Ardanaz, Jonathan Eastep.

- Prototyped in C/C++ a potential feature of future Intel processors that will improve application performance by leveraging fine-grained power management capabilities within a node.

06/2014-09/2014 **Software Tools Development Intern for Energy and Power Analysis**, *Intel Corporation, Hillsboro, OR* | Technical Mentors: Grace Metri, Karla Callaghan.

- Developed a tool in C++ and XML to generate a report detailing energy and power usage of the various components in mobile devices.

05/2013-08/2013 **Computation Student Intern**, *Lawrence Livermore National Laboratory, Livermore, CA* | Technical Mentor: Barry Rountree.

- Created a noise simulator in R to predict load imbalance patterns expected of future HPC systems, specifically exascale architectures.

05/2012–11/2012 **Computation Student Intern**, *Lawrence Livermore National Laboratory, Livermore, CA* | Technical Mentor: Evi Dube.

- Investigated the feasibility and portability of Cray's Chapel PGAS language on future LLNL clusters.

Publications

2019 **Hatchet: Pruning the Overgrowth in Parallel Profiles**, *Abhinav Bhatele,* Stephanie Brink*, and Todd Gamblin*, The International Conference for High Performance Computing, Networking, Storage, and Analysis (SC19), Denver, CO (To Appear).

2019 **Power and Performance Tradeoffs for Visualization Algorithms**, Stephanie Labasan, *Matthew Larsen, Hank Childs, and Barry Rountree*, IEEE International Parallel and Distributed Processing Symposium, Rio de Janeiro, Brazil.

2017 **PaViz: A Power-Adaptive Framework for Optimizing Visualization Performance**, Stephanie Labasan*, Matthew Larsen, Hank Childs, and Barry Rountree*, Eurographics Symposium on Parallel Graphics and Visualization (EGPGV), Barcelona, Spain.

2015 **Exploring Tradeoffs Between Power and Performance for a Scientific Visualization Algorithm**, Stephanie Labasan *and Matthew Larsen and Hank Childs*, IEEE Symposium on Large Data Analysis and Visualization (LDAV), Chicago, IL.

2015 **Volume Rendering Via Data-Parallel Primitives**, *M. Larsen,* S. Labasan*, P. Navrátil, J.S. Meredith, and H. Childs*, Eurographics Symposium on Parallel Graphics and Visualization (EGPGV), Cagliari, Sardinia, Italy.

Patents

2017 **Mitigating Load Imbalances Through Hierarchical Performance Balancing**, S. Labasan*, F. Ardanaz, J. M. Eastep, R. J. Greco*, US Patent Application No: 20170277576A1, Pending patent.

Service

2019 *Scholarship Review Committee Member*, Richard Tapia Celebration of Diversity in Computing

2019 *Committee Track Member*, Computer Systems Engineering, Grace Hopper Celebration of Women in Computing, Anita Borg Institute

2018 *Scholarship Review Committee Member*, Grace Hopper Celebration of Women in Computing, Anita Borg Institute

2017 *Panelist*, "What I Wish I Had Known As An Undergraduate": Advancing Visualization Inclusion and Diversity (AVID), IEEE VIS 2017

2017 *Journal Reviewer*, IEEE Transactions on Computers

2017 *Scholarship Review Committee Member*, Grace Hopper Celebration of Women in Computing, Anita Borg Institute

Professional Memberships

2012–Present Member, Institute of Electrical and Electronics Engineers (IEEE)
Computer Society, Young Professionals

2012–Present Member, Association for Computer Machinery (ACM)
SIGHPC

2008–Present Member, Society of Women Engineers (SWE)

Extracurricular Activities

2014–2015 *Graduate Student Member*, The Duck Store Board of Directors, University of Oregon

2013–2015 *Treasurer*, Alpha Phi Portland Alumnae Chapter, Alpha Phi

2012–2012 *Member*, Mortar Board, University of the Pacific

2011–2012 *Treasurer, Secretary*, Order of Omega, University of the Pacific

2011–2012 *Development Officer*, Center for Community Involvement, University of the Pacific

2009–2012 *President, Vice President of Marketing*, Alpha Phi, University of the Pacific

2009–2011 *Reach Out Coordinator*, Center for Community Involvement, University of the Pacific