ICS-121/ICS-121A

OPERATING MANUAL

Interactive Circuits and Systems Ltd.

December 2004

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ICS Ltd
5430 Canotek Road
Gloucester, Ontario
K1J 9G2 Canada

Tel: (613) 749-9241
USA: (800) 267-9794
Fax: (613) 749-9461

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1 INTRODUCTION

1.1 Summary

The ICS-121 VMEbus analog signal conditioning board is designed to complement the ICS-130 analog input board and the ICS-115 analog output board. It offers the following features:

- 4, 8, 16 or 32 channels;
- differential inputs and outputs;
- gain from +42dB to -12dB individually programmable by channel in steps of 6dB;
- excellent gain and phase match between channels;
- low noise;
- low output offset voltage;
- -90 dB interchannel crosstalk at 1kHz;
- S/(N+D) better than 80dB at 1kHz;
- three-pole anti-alias filter with Butterworth or Bessel characteristic.

A front panel view of the ICS-121 is given in Figure 1.

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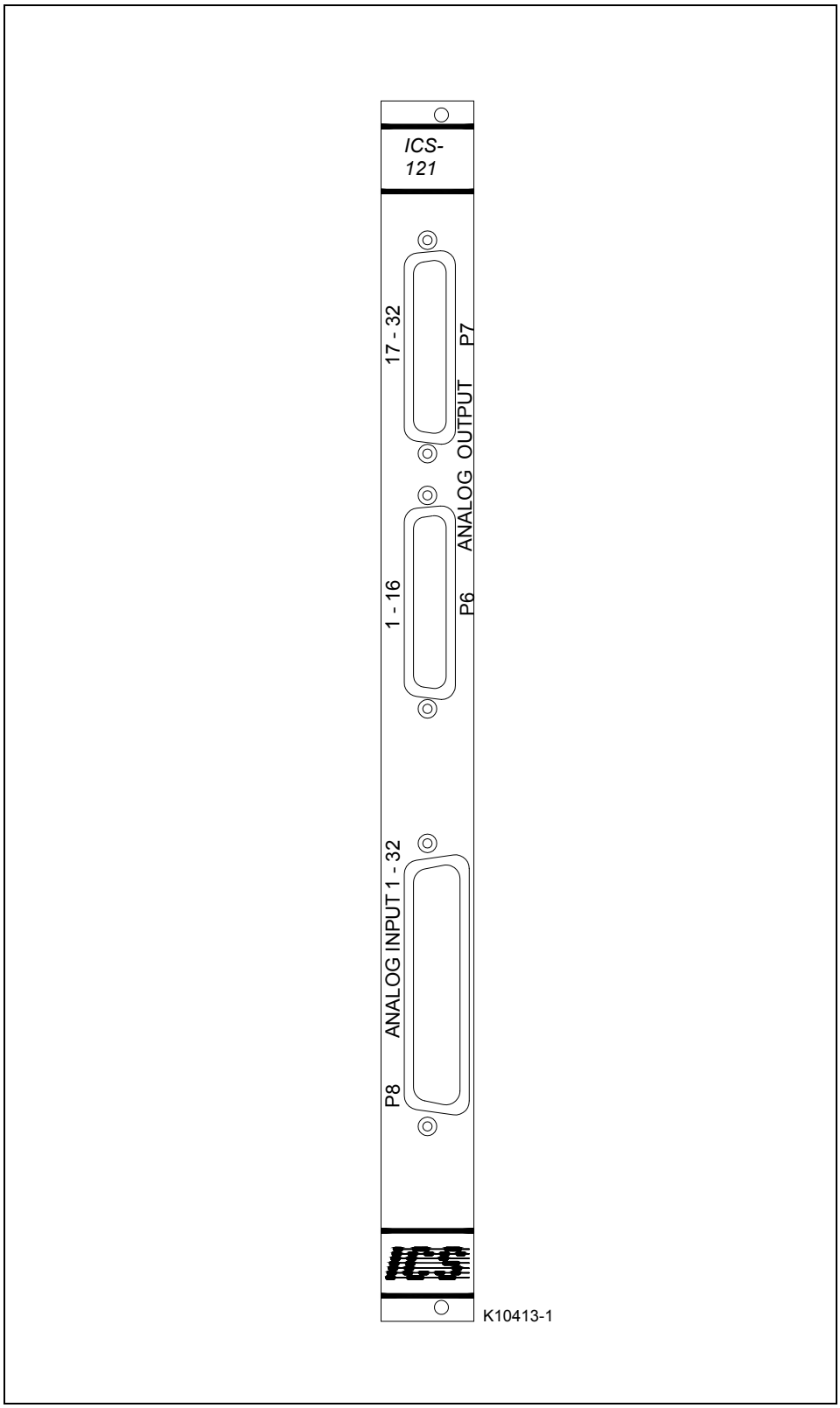

Figure 1 - ICS-121 Front Panel View

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2 SPECIFICATIONS

2.1 ICS-121

Analog	Number of Analog Input Channels :	4, 8, 16 or 32 differential, DC coupled
	Input Impedance :	1 MΩ
	Output Impedance :	10 Ω
	Maximum Input :	30.0 Vpp differential*
	Output :	≤2 Vpp* for linear operation, limited at 4 Vpp* for ADC protection
	Operating Bandwidth :	300 kHz max.
	Output Signal/(Noise + Distortion) :	>80 dB
	Measured at ±1 V, 1 kHz input, 0 dB gain. Noise measurement band 5 Hz to 100 kHz	
	Programmable Gain :	-12 dB to +42 dB in steps of 6 dB
	Filter :	Three pole, Bessel or Butterworth characteristic.
	Filter cut-off frequency, Fc :	≥100 Hz, ≤300 kHz. Specify at time of ordering.
	Output DC Offset (at 25°C) :	±1 mV* max. referred to input, each leg ±25 mV * max. at output referred to input, each leg
	DC Offset temperature coefficient :	<50 μV/°C* referred to input ±200 mV* max. at o/p (0° to 70°C)
	Difference in gain across all channels :	±0.25 dB at Fc
	Difference in phase between any two channels set to same gain at 0.7 Fc :	<1.5° (Bessel Filter) <2.0° (Butterworth Filter)
Bus Interface	VMEbus Interface :	A24/D16, A16/D16 Slave
Environmental		
- Operating :	Temperature :	0° to +50°C
	Humidity :	0 - 95% Rel. Hum., Non-condensing
- Storage :	Temperature :	-25° to +85°C
	Humidity :	0 - 95% Rel. Hum., Non-condensing
Other		
Power :		+5 Volts: 0.5 A maximum +12 Volts: 0.5 A maximum -12 Volts: 0.5 A maximum
Mating Connectors :		
	Input :	Positronic ODD78M... (Quantity 1)
	Output :	Positronic ODD44F... (Quantity 2)
Board Size :		233 x 160 mm VMEbus 6U

* In each differential input or output leg.

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2.2 ICS-121A

Analog	Number of Analog Input Channels :	4, 8, 16 or 32 differential, DC coupled
	Input Impedance :	1 MΩ
	Output Impedance :	10 Ω
	Maximum Input :	30.0 Vpp differential*
	Output :	≤ 2 Vpp* for linear operation, limited at 4 Vpp* for ADC protection
	Operating Bandwidth :	300 kHz max.
	Output Signal/(Noise + Distortion) :	>80 dB
	Measured at ±1 V, 1 kHz input, 0 dB gain.	
	Noise measurement band 5 Hz to 100 kHz	
	Programmable Gain :	-12 dB to +42 dB in steps of 6 dB
	Filter :	Three pole, Bessel or Butterworth characteristic.
	Filter cut-off frequency, Fc :	≥100 Hz, ≤300 kHz. Specify at time of ordering.
	Cut-Off Frequency Amplitude Accuracy:	±1.5 dB of theoretical
	PassBand Flatness DC to 80% of Fc:	±0.5 dB of theoretical
	Output DC Offset (at 25°C) :	±1 mV* max. referred to input, each leg
		±25 mV * max. at output referred to input, each leg
	DC Offset temperature coefficient :	<50 μV/°C* referred to input
		±200 mV* max. at o/p (0° to 70°C)
	Difference in gain across all channels :	±0.25dB at Fc
	Difference in phase between any two channels set to same gain at 0.7 Fc :	<1.5° (Bessel Filter)
		<2.0° (Butterworth Filter)
Bus Interface	VMEbus Interface :	A24/D16, A16/D16 Slave
Environmental		
- Operating :	Temperature :	0° to +50°C
	Humidity :	0 - 95% Rel. Hum., Non-condensing
- Storage :	Temperature :	-25° to +85°C
	Humidity :	0 - 95% Rel. Hum., Non-condensing
Other		
Power :		+5 Volts: 0.5 A maximum
		+12 Volts: 0.5 A maximum
		-12 Volts: 0.5 A maximum
Mating Connectors :		
	Input :	Positronic ODD78M... (Quantity 1)
	Output :	Positronic ODD44F... (Quantity 2)
Board Size :		233 x 160 mm VMEbus 6U

* In each differential input or output leg.

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3 DETAILED DESCRIPTION

The ICS-121 consists of three parts; the mother board, which contains the VMEbus interface and input and output connections, the Programmable Gain Amplifier (PGA) modules and the Filter Modules.

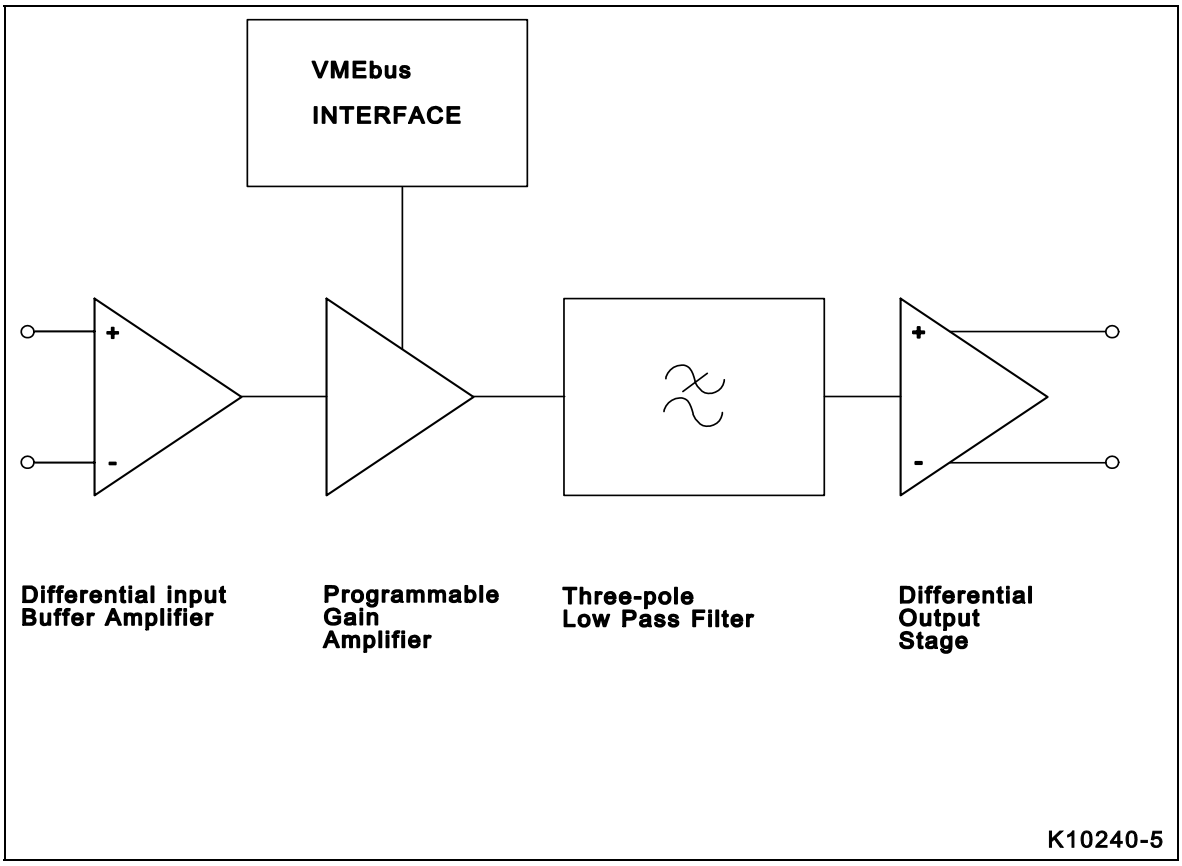

Figure 2 - ICS-121 Block Diagram (One Channel Only Shown)

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3.1 VMEbus Interface

The VMEbus Interface is located on the mother board. The interface allows software control over the gain individually for each channel. It is a slave interface providing a 256 Byte address space, and will respond to A16 or A24 address cycles with Address Modifier (AM) codes 29, 2D, 39, 3B, 3D or 3F. When writing to the board, D16 cycles should be employed. Before attempting to use the board, the user should set the base address using the address switches SW1 and SW2 on the board, and the address mode using jumper JP1, according to the information given in section 4 of this manual.

3.2 Programmable Gain Amplifiers

The Programmable Gain Amplifiers are located on mezzanine modules which are mounted on the ICS-121 mother board; there is one PGA for each channel. On the PGA modules, the differential inputs for the channel are buffered by an instrumentation amplifier of 1MΩ input impedance and converted to a single-ended signal before being applied to the programmable gain amplifier. Here the signal is amplified or attenuated by the value programmed by the user. Each channel may be programmed for a different gain/attenuation value between -12dB and +42dB, inclusive, in steps of 6dB. When power is first applied to the board, the gain of each channel is arbitrary. The user must program the board in order to establish a given gain value.

3.3 Anti-alias Filter

The outputs of each PGA module is applied to a Filter Module having a three-pole low pass function with either Bessel or Butterworth characteristic. The filter characteristic must be specified at time of ordering, together with the desired cut-off frequency. The Filter Modules are located on top of the PGA modules.

3.4 Output Section

The output of each Filter Module is applied to the output stage, which converts the signal to a differential output with an output impedance of 10Ω. This stage also clips the output voltage swing at ∀2V on each wire of the differential pair. Linear operation is provided for output swings up to ∀1V.

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4 HARDWARE PREPARATION

The following section provides information necessary for hardware preparation of the ICS-121.

4.1 VMEbus Board Address and Address Mode

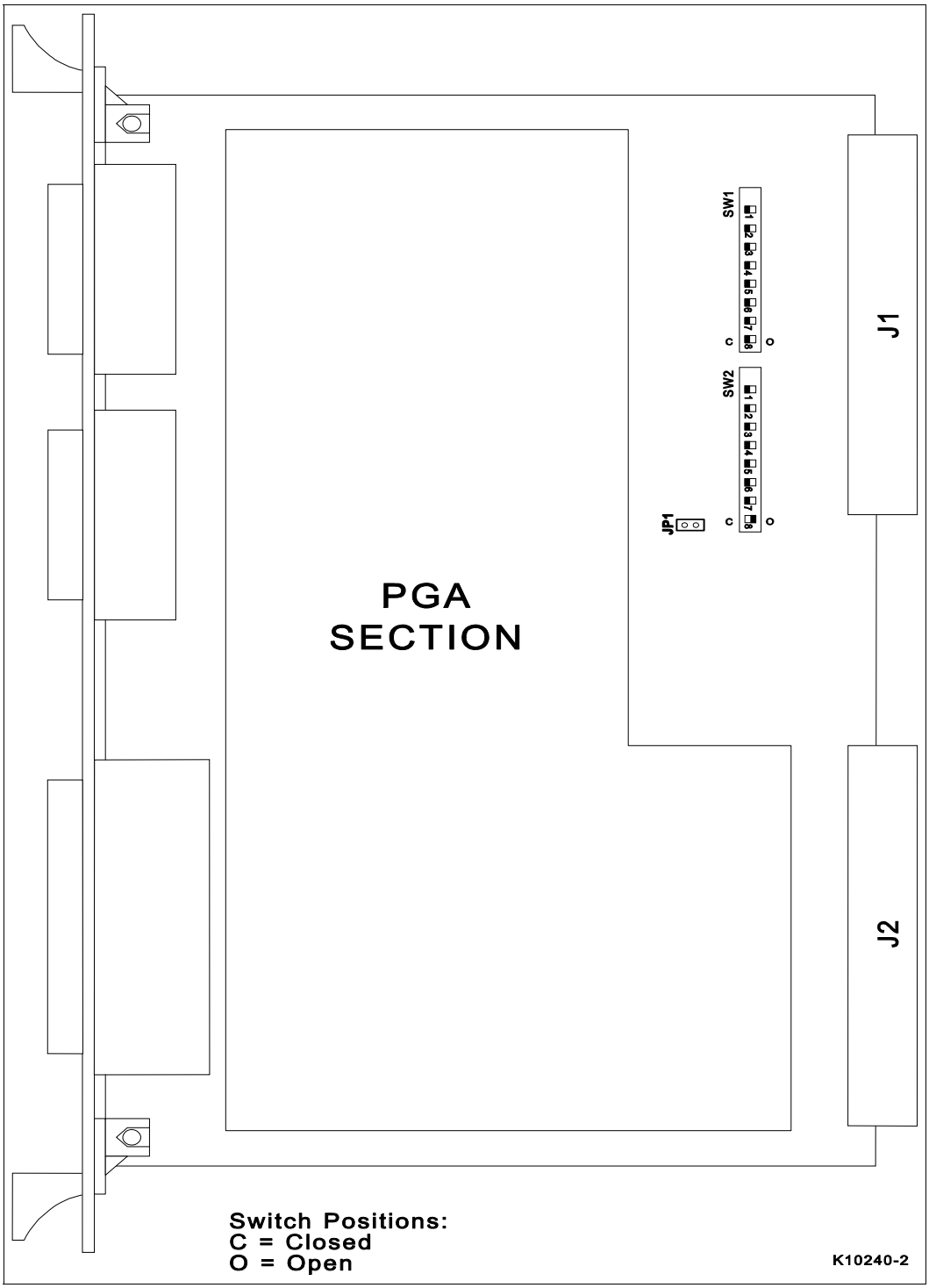

Figure 3 - ICS-121 Switch and Jumper Locations

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The ICS-121 can be configured, by means of Jumper JP1, to reply only to certain AM codes representing short (A16) or standard (A24) addresses during VMEbus accesses. The configurable addressing modes of the ICS-121 are:

Jumper JP1	Address Decoding Scheme
Inserted	A16 addressing, AM codes 29, 2D
Removed	A24 addressing, AM codes 39, 3B, 3D, 3F

The ICS-121 VMEbus base address can be set on any 256 Byte boundary in A16 or A24 physical address space using address bits A08-A23. DIP switch blocks SW1 and SW2 are used to select the VMEbus address as given in the following table; SW1-1 through SW1-8 have no effect when A16 addressing is selected. A closed switch selects a zero for that address bit, while an open switch selects a one. Consult Figure 3 for switch polarities.

Switch	VMEbus Address Bit	Switch	VMEbus Address Bit
SW1-8	A23	SW2-8	A15
SW1-7	A22	SW2-7	A14
SW1-6	A21	SW2-6	A13
SW1-5	A20	SW2-5	A12
SW1-4	A19	SW2-4	A11
SW1-3	A18	SW2-3	A10
SW1-2	A17	SW2-2	A09
SW1-1	A16	SW2-1	A08

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The AM codes referred to above correspond to the following address decoding schemes:

AM Code	Function
29	Short Non-privileged Access
2D	Short Supervisory Access
39	Standard Non-privileged Data Access
3B	Standard Non-privileged Block Transfer
3D	Standard Supervisory Data Access
3F	Standard Supervisory Block Transfer

The default factory settings are shown in Figure 3, and are as follows:

VMEbus Base Address = 0x8000
A16 Addressing, AM codes 29, 2D

4.2 VMEbus Backplane Jumpers

Backplane jumpers for the VMEbus bus grant (BG0 - BG3) signals and the IACKIN/IACKOUT signal may be either in place or removed, as these lines are shorted on the ICS-121 in order to provide continuity for boards further down the daisy chain.

The ICS-121 has no interrupt capability.

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5 MEMORY MAP

The ICS-121 memory map consists of two VMEbus 16-bit registers. The VMEbus memory map is shown in Figure 4. Detailed register descriptions are in the following paragraphs.

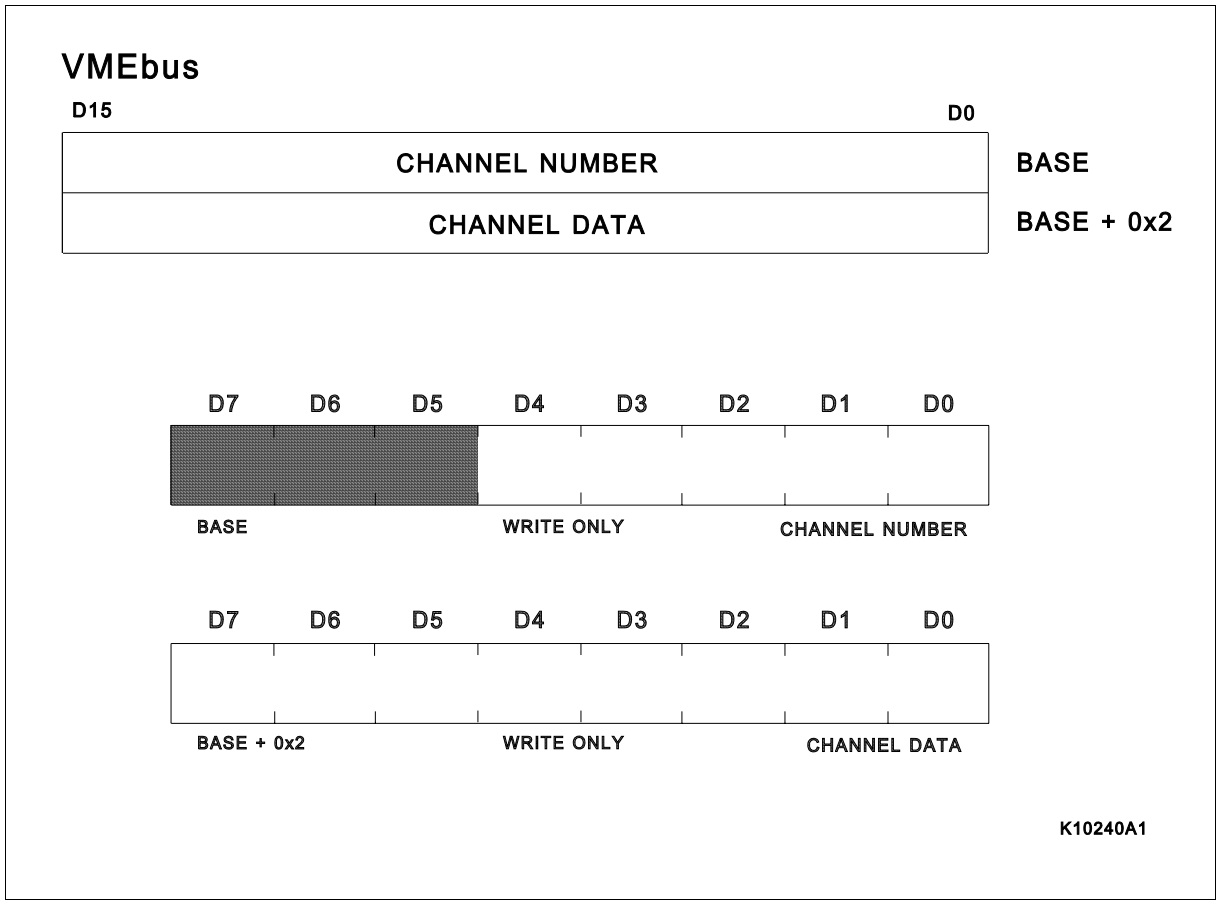

Figure 4 - ICS-121 VMEbus Memory Map

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5.1 Channel Number Register

Write Only

The Channel Number register allows the user to select the channel to be programmed by the next write to the Channel Data register. The value to be written to bits 0-4 of this register is determined from the following table.

Channel	Program Code	Channel	Program Code
1	16	17	0
2	17	18	1
3	18	19	2
4	19	20	3
5	20	21	4
6	21	22	5
7	22	23	6
8	23	24	7
9	24	25	8
10	25	26	9
11	26	27	10
12	27	28	11
13	28	29	12
14	29	30	13
15	30	31	14
16	31	32	15

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5.2 Channel Data Register

Write Only

The Channel Data register is used to program the control data for the channel previously selected using the Channel Number register. The following table describes the programming values required for the various gain settings. The values to be programmed are given as binary, decimal and hexadecimal numbers. The value A is an attenuation offset which is equal to zero dB in the standard product.

After a value has been written to the register, the programmer must ensure that no further data is written either to the Channel Number register or to the Channel Data register for at least 50Φs. This is because channel data is written to the PGA as a serial data stream. Sufficient time must be allowed for this operation to be completed before fresh data is programmed.

Gain (dB)	D7	D6	D5	D4	D3	D2	D1	D0	Dec	Hex
-12 - A	0	0	0	0	1	1	1	1	15	0F
-6 - A	0	0	0	1	1	1	1	1	31	1F
0 - A	0	0	1	1	1	1	1	1	63	3F
+6 - A	0	1	1	1	1	1	1	1	127	7F
+12 - A	1	0	1	1	1	1	1	0	190	BE
+18 - A	1	1	1	1	1	1	1	0	254	FE
+24 - A	1	0	1	1	1	1	0	0	188	BC
+30 - A	1	1	1	1	1	1	0	0	252	FC
+36 - A	1	0	1	1	1	0	0	0	184	B8
+42 - A	1	0	1	1	0	0	0	0	176	B0

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APPENDICES

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6 ANALOG INPUT CONNECTOR

Connector on board: ODD78F4R7NTX
Mating connector: ODD78M..... (consult Manufacturer's data for details)
Manufacturer: Positronic Industries Inc., (417) 866-2322

Figure 5 shows a front panel view of the Analog Input connector. The pin number allocations are given in the tables below.

PIN	DESCRIPTION	PIN	DESCRIPTION
69	CHANNEL 1+	70	CHANNEL 1-
50	CHANNEL 2+	51	CHANNEL 2-
31	CHANNEL 3+	32	CHANNEL 3-
11	CHANNEL 4+	12	CHANNEL 4-
71	CHANNEL 5+	72	CHANNEL 5-
52	CHANNEL 6+	53	CHANNEL 6-
33	CHANNEL 7+	34	CHANNEL 7-
13	CHANNEL 8+	14	CHANNEL 8-
73	CHANNEL 9+	74	CHANNEL 9-
54	CHANNEL 10+	55	CHANNEL 10-
35	CHANNEL 11+	36	CHANNEL 11-
15	CHANNEL 12+	16	CHANNEL 12-
75	CHANNEL 13+	76	CHANNEL 13-
56	CHANNEL 14+	57	CHANNEL 14-
37	CHANNEL 15+	38	CHANNEL 15-
17	CHANNEL 16+	18	CHANNEL 16-

* all other pins are connected to analog ground on the board

PIN	DESCRIPTION	PIN	DESCRIPTION
61	CHANNEL 17+	62	CHANNEL 17-
42	CHANNEL 18+	43	CHANNEL 18-

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23	CHANNEL 19+	24	CHANNEL 19-
3	CHANNEL 20+	4	CHANNEL 20-
63	CHANNEL 21+	64	CHANNEL 21-
44	CHANNEL 22+	45	CHANNEL 22-
25	CHANNEL 23+	26	CHANNEL 23-
5	CHANNEL 24+	6	CHANNEL 24-
65	CHANNEL 25	66	CHANNEL 25-
46	CHANNEL 26+	47	CHANNEL 26-
27	CHANNEL 27+	28	CHANNEL 27-
7	CHANNEL 28+	8	CHANNEL 28-
67	CHANNEL 29+	68	CHANNEL 29-
48	CHANNEL 30+	49	CHANNEL 30-
29	CHANNEL 31+	30	CHANNEL 31-
9	CHANNEL 32+	10	CHANNEL 32-

* all other pins are connected to analog ground on the board

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7 ANALOG OUTPUT 1-16 CONNECTOR

Connector on board: ODD44M.....
Mating connector: ODD44F..... (consult Manufacturer's data for details)
Manufacturer: Positronic Industries Inc., (417)866-2322

Figure 5 shows a front panel view of the Analog Output connectors. The pin number allocations are given in the tables below.

PIN	DESCRIPTION	PIN	DESCRIPTION
32	CHANNEL 1-	33	CHANNEL 1+
18	CHANNEL 2-	19	CHANNEL 2+
3	CHANNEL 3-	4	CHANNEL 3+
34	CHANNEL 4-	35	CHANNEL 4+
20	CHANNEL 5-	21	CHANNEL 5+
5	CHANNEL 6-	6	CHANNEL 6+
36	CHANNEL 7-	37	CHANNEL 7+
22	CHANNEL 8-	23	CHANNEL 8+
7	CHANNEL 9-	8	CHANNEL 9+
38	CHANNEL 10-	39	CHANNEL 10+
24	CHANNEL 11-	25	CHANNEL 11+
9	CHANNEL 12-	10	CHANNEL 12+
40	CHANNEL 13-	41	CHANNEL 13+
26	CHANNEL 14-	27	CHANNEL 14+
11	CHANNEL 15-	12	CHANNEL 15+
42	CHANNEL 16-	43	CHANNEL 16+

* all other pins are connected to analog ground on the board

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8 ANALOG OUTPUT 17-32 CONNECTOR

Connector on board: Positronics ODD44M (see above)
Mating connector: ODD44F..... (consult Manufacturer's data for details)
Manufacturer: Positronic Industries Inc., (417)866-2322

PIN	DESCRIPTION	PIN	DESCRIPTION
32	CHANNEL 17-	33	CHANNEL 17+
18	CHANNEL 18-	19	CHANNEL 18+
3	CHANNEL 19-	4	CHANNEL 19+
34	CHANNEL 20-	35	CHANNEL 20+
20	CHANNEL 21-	21	CHANNEL 21+
5	CHANNEL 22-	6	CHANNEL 22+
36	CHANNEL 23-	37	CHANNEL 23+
22	CHANNEL 24-	23	CHANNEL 24+
7	CHANNEL 25-	8	CHANNEL 25+
38	CHANNEL 26-	39	CHANNEL 26+
24	CHANNEL 27-	25	CHANNEL 27+
9	CHANNEL 28-	10	CHANNEL 28+
40	CHANNEL 29-	41	CHANNEL 29+
26	CHANNEL 30-	27	CHANNEL 30+
11	CHANNEL 31-	12	CHANNEL 31+
42	CHANNEL 32-	43	CHANNEL 32+

* all other pins are connected to analog ground on the board

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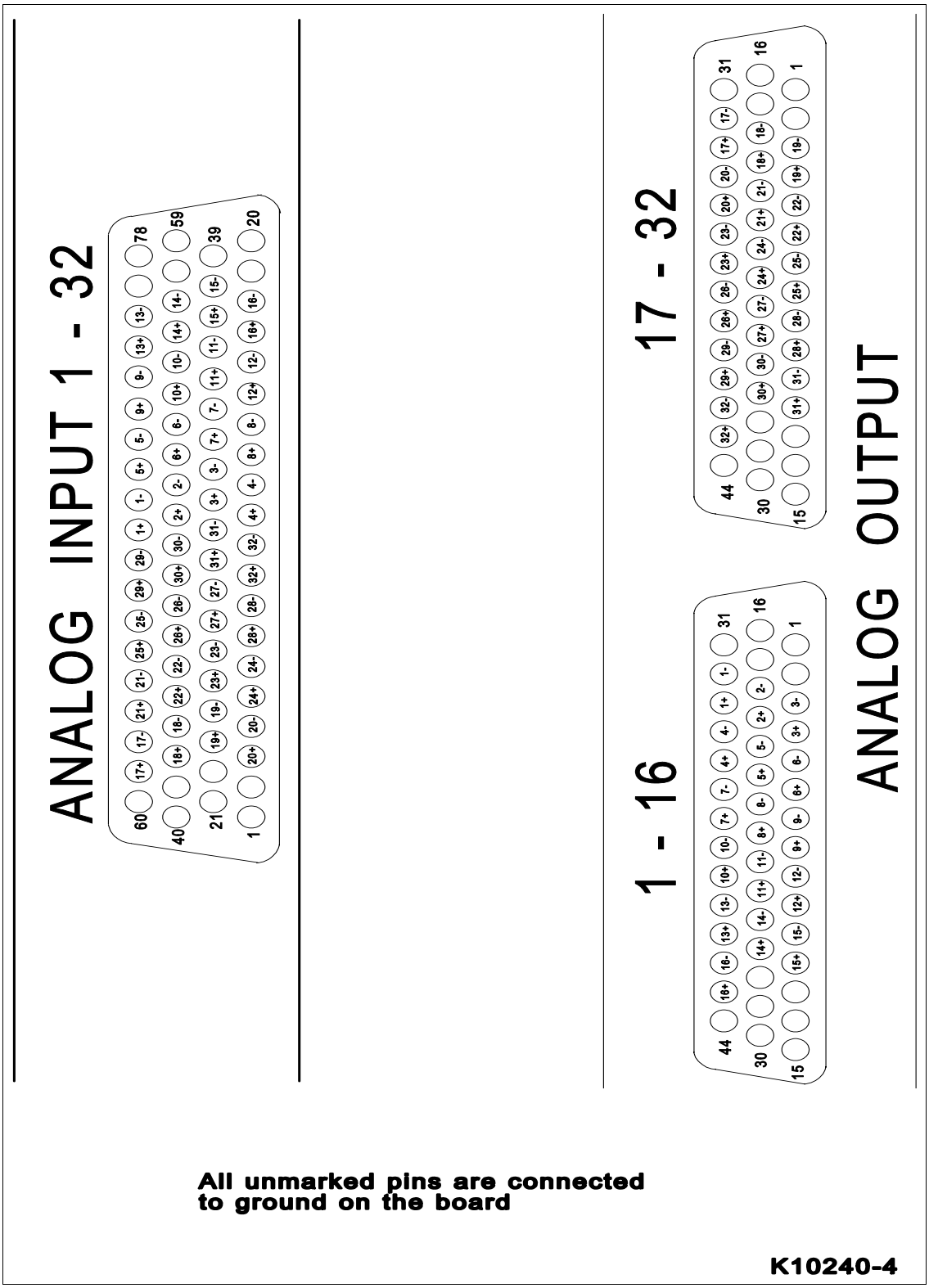

Figure 5 - ICS-121 Front Panel Connector Detail

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