BL0942 datasheet

BL0942 Calibration-Free Metering Chip Data Sheet

Table of contents

1 Product description

1.1 Function introduction

BL0942 is a calibration-free energy metering chip with a built-in clock, suitable for single-phase multi-function energy meters, smart sockets, smart home appliances and other applications, with high cost performance.

BL0942 integrates 2- way high-precision Sigma-Delta ADC , analog circuit modules such as reference voltage, power management, and digital signal processing circuits for processing electrical parameters such as active power, current and voltage RMS.

BL0942 can measure parameters such as current, voltage RMS, active power, active energy, etc., and can output fast current RMS (for overcurrent protection) , as well as waveform output and other functions, and output data through UART/SPI interface, which can fully meet the requirements of intelligent The needs of fields such as sockets, smart home appliances, single-phase multi-function electric energy meters, and big data collection of electricity consumption information.

BL0942 has a patented anti-creep design, combined with a reasonable external hardware design, it can ensure that the noise power is not included in the energy pulse when there is no current.

1.2 main feature

- Two independent Sigma-Delta ADCs , one current and one voltage.
- RMS current range (10mA~30A) @1mohm
- Active energy (1w~6600w) @1mohm@220V
- Can output current, voltage RMS, fast current RMS, active power
- The batch factory gain error is less than 1% , and the external components can be exempted from calibration if they meet certain conditions
- The current channel has an overcurrent monitoring function, and the monitoring threshold and response time can be set
- Voltage / current zero-crossing signal output
- Built-in waveform register, which can output waveform data for load type analysis
- SPI (the fastest rate supports 900KHz) /UART (4800-38400bps) communication method (TSSOP14L Package supports up to 4 slice cascading

  Uart communication)

- Power down monitoring, below 2.7V , the chip enters the reset state
- Built-in 1.218V reference voltage source
- Built-in oscillation circuit, the clock is about 4MHz
- Chip single working power supply 3.3V , low power consumption 10mW (typical value)
- SSOP10L/TSSOP14L encapsulation

1.3 System Block Diagram

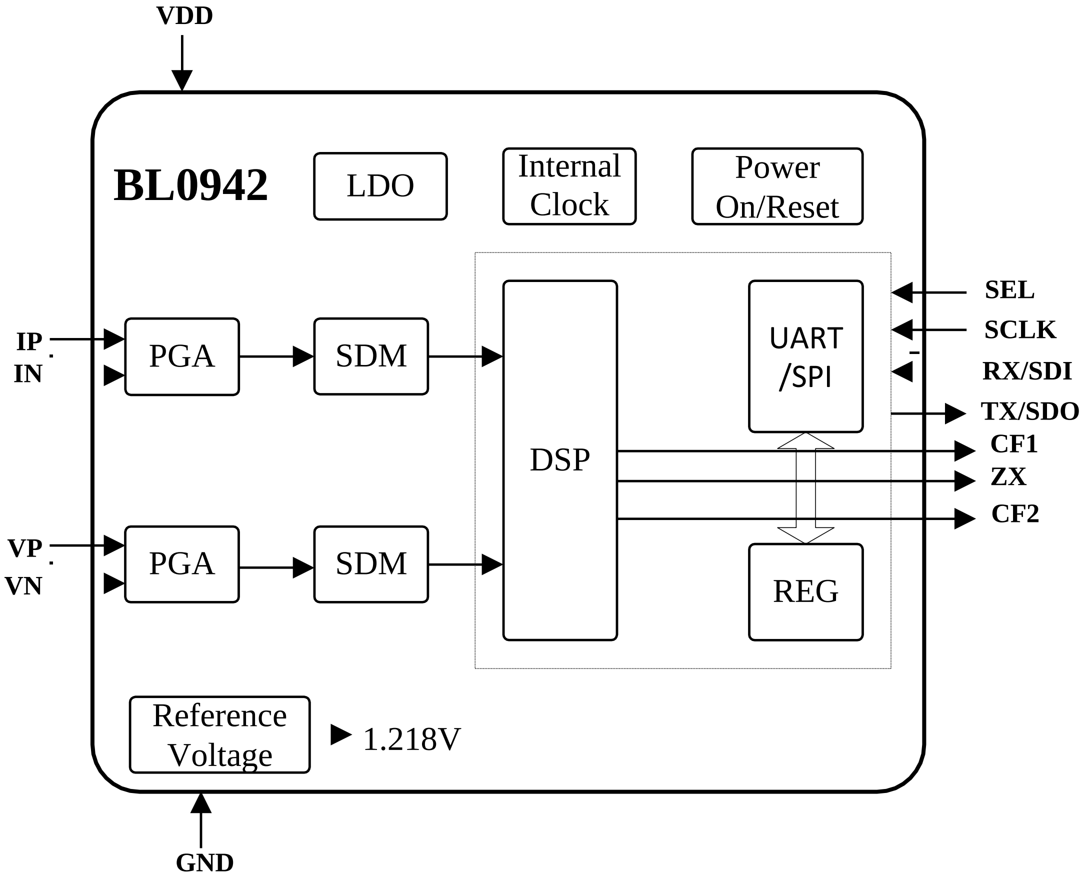


Figure 1

1.4 Package and Pin Description

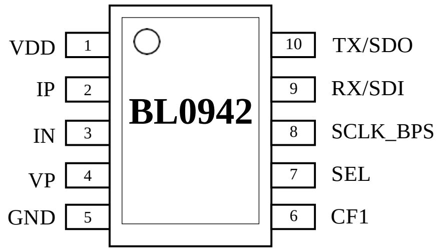


Figure 2

Pin Description (SSOP10L)

pin No	symbol	illustrate
1	VDD	Power supply (+3.3V)
2,3	IP,IN	Current channel analog input, the maximum differential voltage of the pins is ±42mV (30mV rms)
4	VP	Voltage signal input terminal, maximum differential voltage ±100mV (70mV rms)
5	GND	chip ground
6	CF1	Power status output, which can be configured by the OT_FUNX register to output a variety of power information
7	SEL	UART/SPI Communication mode selection (0 : UART 1 : SPI), internal pull-down resistor, Floating is 0 level (UART), and the pin is directly connected to VDD to be high level (SPI)
8	SCLK_BPS	SPI mode clock input, selectable baud rate in UART mode
9	RX/SDI	UART/SPI multiplexing pin, UART RX/SPI DIN , external pull-up is required in UART mode resistance
10	TX/SDO	UART/SPI multiplexed pin, UART TX/SPI DOUT , needs to be connected externally in UART mode pull resistor

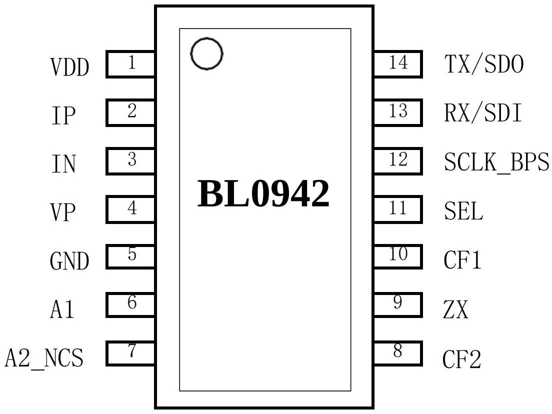


Figure 3

Pin Description（TSSOP14L）

pin number	symbol	illustrate
1	VDD	Power supply（+3.3V）
2,3	IP,IN	Current channel analog input, the maximum differential voltage of the pins at the default gain of 16 is ±42mV (30mV rms)；
4	VP	Voltage signal input terminal, maximum differential voltage ±100mV (70mV rms)
5	GND	chip ground
6	A1	UART mode, it is used as the low address of the chip select function. Internal default dropdown.
7	A2_NCS	UART mode, it is used as the high address of the chip select function. In SPI mode, as CS chip select control, Active low. Internal default dropdown.
8	CF2	Power status output, which can be configured by the OT_FUNX register to output a variety of power information
9	ZX	The zero-crossing monitoring output pin can be configured by the OT_FUNX register to output a variety of electric energy information
10	CF1	Power status output, which can be configured by the OT_FUNX register to output a variety of power information
11	SEL	UART/SPI Communication mode selection（0：UART 1：SPI), there is a pull-down resistor inside , and it is It is 0 level（UART), and the pin is directly connected to VDD, which is high level（SPI）
12	SCLK_BPS	SPI mode clock input, selectable baud rate in UART mode
13	RX/SDI	UART/SPI multiplexing pin, UART RX/SPI DIN, external pull-up resistor is required in UART mode

14	TX/SDO	UART/SPI multiplexing pin, UART TX/SPI DOUT, external pull-up resistor is required in UART mode

1.5 register list

address	name	external read / write	internal read / write	efficient bit	Defaults	describe
Electric parameter register (read only)						
0x01	I_WAVE	R	W	20	0x00000	Current waveform register, signed
0x02	V_WAVE	R	W	20	0x00000	Voltage waveform register, signed
0x03	I_RMS	R	W	twenty four	0x000000	Current RMS register, unsigned
0x04	V_RMS	R	W	twenty four	0x000000	Voltage rms register, unsigned
0x05	I_FAST_RMS	R	W	twenty four	0x000000	Current Fast RMS Register, Unsigned
0x06	WATT	R	W	twenty four	0x000000	Active power register, signed
0x07	CF_CNT	R	W	twenty four	0x000000	Active energy pulse count register, unsigned
0x08	FREQ	R	W	16	0x4E20	LINE VOLTAGE FREQUENCY REGISTER
0x09	STATUS	R	W	10	0x000	status register
User operation register (read and write)						
0x12	I_RMSOS	R/W	R	8	0x00	Current RMS Small Signal Correction Register
0x14	WA_CREEP	R/W	R	8	0x0B	Active power anti-passage register
0x15	I_FAST_RMS_TH	R/W	R	16	0xFFFF	Current Fast RMS Threshold Register
0x16	I_FAST_RMS_CYC	R/W	R	3	0x1	Current Fast RMS Refresh Period Register
0x17	FREQ_CYC	R/W	R	2	0x3	Line Voltage Frequency Refresh Period Register
0x18	OT_FUNX	R/W	R	6	0x24	Output Configuration Register
0x19	MODE	R/W	R	10	0x87	User Mode Select Register
0x1A	GAIN_CR	R/W	R	2	0x2	Current Channel Gain Control Register
0x1C	SOFT_RESET	R/W	R	twen	0x000000	writing 0x5A5A5A, the user area

				ty four		register is reset
0x1D	USR_WRPROT	R/W	R	8	0x00	User write-protect setting register. After writing 0x55, use The user operation register can be written; write other values, the user operation register area cannot be written

Note: The data byte of the communication protocol is 24bit, and the high and invalid bits are filled with 0.

1.6 Special Register Description

User Mode Select Register

0x19	MODE	Operating Mode Register		
No.	name	default value	description	
[1:0]	reserved	b00	reserved	
[2]	CF_EN	b1	Active Energy and Impulse Switches	0：off 1：enable
[3]	RMS_UPDATE_SEL	b0	When the rms register is refreshed choose between	0：400ms 1：800ms
[4]	FAST_RMS_SEL	b00	Fast RMS waveform source selection: 0：Waveform after SINC；1：Waveform after HPF	
[5]	AC_FREQ_SEL	b0	AC frequency selection	0：50Hz 1：60Hz
[6]	CF_CNT_CLR_SEL	b0	CF count register is cleared after read zero enable bit	0：off 1：enable
[7]	CF_CNT_ADD_SEL	b1	CF pulse energy accumulation mode choose	0：algebraic and accumulate 1：Absolute value accumulation
[9:8]	UART_RATE_SEL	b00	UART communication baud rate selection	0x：The baud rate is determined by the hardware pin SCLK_BPS decision, connect 0 to select 4800bps， connect to 1 option 9600bps 10：19200bps 11：38400bps
[23:10]	reserved	b0	reserve	

Output Configuration Register

0x18	OT_FUNX	Output Configuration Register	
No.	name	default value	description
[1:0]	CF1_FUNX_SEL	b00	CF1 output selection bits: b00: output active energy pulse b01: output overcurrent alarm b10: output voltage zero-crossing indication b11: Output current zero-crossing indication
[3:2]	CF2_FUNX_SEL	b01	CF2 output selection bits: b00: output active energy pulse b01: output overcurrent alarm b10: output voltage zero-crossing indication b11: Output current zero-crossing indication
[5:4]	ZX_FUNX_SEL	b10	ZX output selection bit: b00: output active energy pulse b01: output overcurrent alarm b10: output voltage zero-crossing indication b11: Output current zero-crossing indication
[23:6]	reserved	b0	reserve

status register

0x09	STATUS	working status register	
No.	name	default value	description
[0]	CF_REVP_F	b0	Active pulse CF energy reverse indication, set to 1 when negative energy
[1]	CREEP_F	b0	1 when the active power is less than the active anti-creep value
[7:2]	reserved	b0	reserve
[8]	I_ZX_LTH_F	b0	Current zero-crossing output status indication
[9]	V_ZX_LTH_F	b0	Voltage zero-crossing output status indication
[23:10]	reserved	b0	reserve

Current Channel Gain Control Register

0x1A	GAIN_CR	Current Channel Gain Control Register

No.	name	default value	description
[1:0]	GAIN_CR	B10	00： 1 times gain; 01： 4 times gain; 10： 16 times gain (default); 11： 24 times gain;
[23:10]	reserved	b0	reserve

1.7 Performance

1.7.1 Electrical parameter performance

(VDD =3.3V， GND = 0V， on-chip reference voltage source， built-in crystal oscillator, 25 ℃, electric energy is measured through CF output)

Measurement items	symbol	Measurement conditions	the smallest	typical	maximum	unit
Power supply VDD	VDD		3.0		3.6	V
power consumption	Iop	VDD=3.3V		3		mA
Measuring range		4000:1 input drive state range				
Active energy measurement accuracy (big signal)		30A~100mA input @ 1mohm sampling sample resistance		0.2		%
Active energy measurement accuracy (small signal)		100mA~50mA Enter @ 1mohm Sampling resistor		0.4		%
Active energy measurement accuracy (tiny signal)		50mA~10mA output Into @ 1mohm sampling resistor		0.6		%
RMS measurement accuracy (big signal)		30A~100mA input @ 1mohm sampling sample resistance		0.2		%
RMS measurement accuracy (small signal)		100mA~50mA Enter @ 1mohm Sampling resistor		2		%

RMS measurement accuracy (tiny signal)		50mA~10mA input @ 1mohm sampling sample resistance		6		%
Fast RMS response time	50Hz	Can be set to cycle / half cycle	10		160	M
	60Hz		8.3		133	M
Zero-crossing signal output delay				570		u
The phase angle between channels causes measurement errors Poor (capacitive)	PF08err	Phase lead 37 (PF=0.8)			0.5	%
The phase angle between channels causes measurement errors Poor (sensibility)	PF05err	Phase lag 60 (PF=0.5)			0.5	%
AC Power Supply Rejection (Output Frequency rate amplitude change)	ACPSRR	IP/N=100mV			0.1	%
DC power supply rejection (output frequency rate amplitude change)	DCPSRR	VP/N=100mV			0.1	%

Measurement items	symbol	Measurement conditions	the smallest	typical	maximum	unit
Analog input level (current)		Current differential input (peak)			42	mV
Analog input level (voltage)		Voltage differential input (peak)			100	mV
Analog input impedance				370		kΩ _
SEL pull-down resistor		SEL (pull down)		56.9		kΩ _
Analog input bandwidth		(-3dB)		3.5		kHz
Internal Voltage Reference	Vref			1.218		V
logic input high		VDD=3.3V ± 5%	2.6			V
Logic input low		VDD=3.3V ± 5%			0.8	V
logic output high		VDD=3.3V ± 5% IOH=5mA	VDD-0.5			V
Logic output low level		VDD=3.3V ± 5% IOL=5mA			0.5	V

1.7.2 limit range

(T = 25 ° C)

project	symbol	extremum	unit
Power supply voltage VDD	VDD	-0.3 ~ +4	V
Analog input voltage (relative to GND)	IP, VP	-4 ~ +4	V
Digital Input Voltage (relative to GND)	A1, A2_NCS, SEL, SCLK_BPS, RX/SDI	-0.3 ~ VDD+0.3	V
Digital output voltage (relative to GND)	CF1, CF2, ZX, TX/SDO	-0.3 ~ VDD+0.3	V
Operating temperature	Topr	-40 ~ +85	℃
storage temperature	Tstr	-55 ~ +150	℃

2 Functional description

BL0942 is mainly divided into two parts: analog signal processing and digital signal processing. The analog part mainly includes two-channel PGA, two-channel Sigma-Delta ADC, built-in clock (internal clock), power on/reset (Power on/reset), LDO and other related analog module, and the digital part is a digital signal processing module (DSP).

2.1 Current and voltage transient waveform measurement

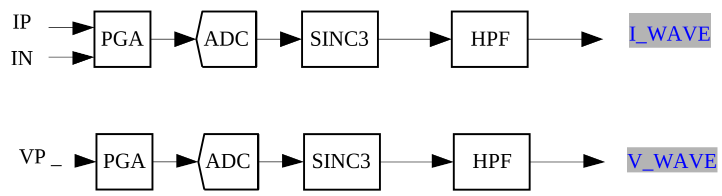


Figure 4

As shown in the figure above, the current and voltage pass through the analog module amplifier (PGA) and high-precision analog-to-digital conversion (ADC) respectively to obtain two 1-bit PDMs for the digital module, and the digital module passes through the down-sampling filter (SINC3) , high-pass filter (HPF) , channel offset correction and other modules to obtain the required current waveform data and voltage waveform data (I_WAVE, V_WAVE) .

The collected load current and voltage waveform data are updated at a rate of 7.8k , each sampled data is a 20bit signed number, and stored in the waveform register (I_WAVE, V_WAVE) respectively , the SPI rate configuration is greater than 375Kbps , and one channel can be read continuously waveform value.

Note: The register is 24bit, if the number of digits is insufficient, high bits are filled with zeros.

address	name	Significant bit	Defaults	describe
0x01	I_WAVE	20	0x00000	Current waveform register, signed
0x02	V_WAVE	20	0x00000	Voltage waveform

				register, signed

2.2 active power

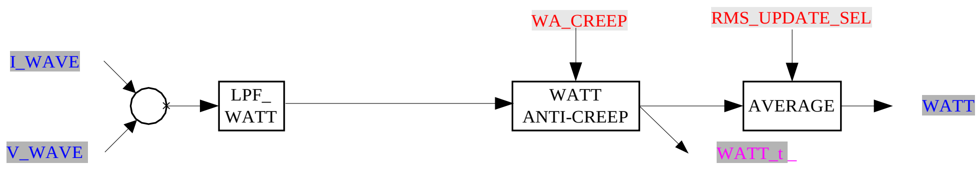


Figure 5

address	name	Significant bit	Defaults	describe
0x06	WATT	twenty four	0x000000	Active power register, signed

Active power calculation formula ： $$WATT = \frac{3537*I(A)*V(V)*COS(\varphi)}{Vref^2}$$

Among them, $I(A)$, $V(V)$ is the effective value (mV) of the channel pin input signal , φ is the phase angle of the I(A) and V(V) AC signals, Vref is the built-in reference voltage, typical value 1.218V ;

This register indicates whether the current active power is positive or negative, Bit[23] is the sign bit, Bit[23]=0, the current power is positive power, Bit[23]=1, the current power is negative power, complement code form.

2.3 Active power anti-creep

BL0942 has a patented power anti-submersion function, which ensures that the board-level noise power will not accumulate power when there is no current input.

The active anti-creep threshold register (WA_CREEP), is an 8bit unsigned number, and the default is 0BH . The corresponding relationship between this value and the active power register value is shown in the following formula. When the absolute value of the input active power signal is less than this value, the output active power is set to 0 . This can make the value output to the active power register be 0 in the case of no load, even if there is a small noise signal, and the electric energy will not accumulate.

address	name	Significant bit	Defaults	describe
0x14	WA_CREEP	8	0x0B	Active power anti-passage register

WA_CREEP can be set according to the value of the power register WATT, and their corresponding relationship:

$$\mathrm{WA\_CREEP} = \mathrm{WATT} * \frac{256}{3125}$$

Note: When the current channel is in the anti-skid state, the current RMS value of this channel is not measured, and it is also cut to **0**.

2.4 Energy Metering

BL0942 provides electric energy pulse metering, the active instantaneous power is integrated according to time, the active energy can be obtained, and the calibration pulse CF can be further output . The CF_CNT register stores the number of output energy pulses CF , as shown in the figure below.

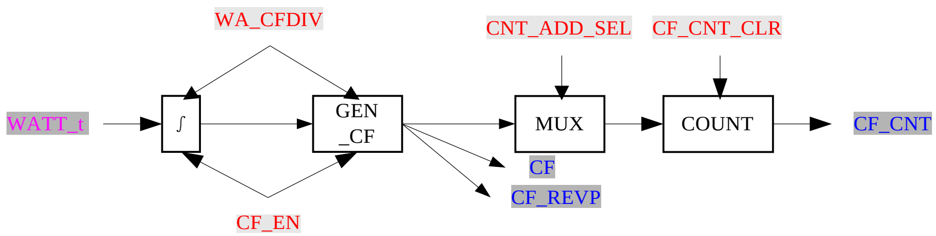


Figure 6

address	name	Significant bit	Defaults	describe
0x07	CF_CNT	twenty four	0x000000	Active energy pulse count, unsigned

consumption can be read directly from the active energy pulse counting register CF_CNT , or the number of pulses can be directly counted from the CF1/CF2/ZX pin by I/O interrupt after configuring the OT_FUNX register . When the cycle of CF is less than 160ms , is a pulse with a 50% duty cycle, and when it is greater than or equal to 160ms , the high-level fixed pulse width is 80ms .

0x19	MODE	Operating Mode Register		
No.	name	default value	description	
[2]	CF_EN	0b1	Active Energy and Impulse Switches	0 : off 1 : enable
[6]	CF_CNT_CLR_SEL	0b0	CF count register is cleared after read zero enable bit	0 : off 1 : enable
[7]	CF_CNT_ADD_SEL	0b1	CF pulse energy accumulation mode choose	0 : algebraic and accumulate 1 : Absolute value accumulation

CF_EN is the main switch for energy pulse output. After it is turned off, CF_CNT stops counting, and CF1/CF2/ZX pins stop outputting energy pulses for counting.

The CF_CNT_CLR_SEL register can be used to select whether the CF count register （ CF_CNT ） is cleared after reading. accessible

CF_CNT_ADD_SEL selects the pulse energy accumulation mode.

Note: The **CF_CNT** register defaults to the energy pulse absolute value accumulation method.

each CF pulse $t_{CF} = \dfrac{1638.4*256}{WATT}$

Where WATT is the corresponding active power register value （ WATT）.

2.5 RMS value of current and voltage

The effective values of the current and voltage channels are shown in the figure below, after a square circuit (X^2), a low-pass filter (LPF_RMS), a root-opening circuit (ROOT), get the instantaneous value RMS_t of the effective value, and then get the average value (I_RMS and V_RMS) of the two channels after averaging .

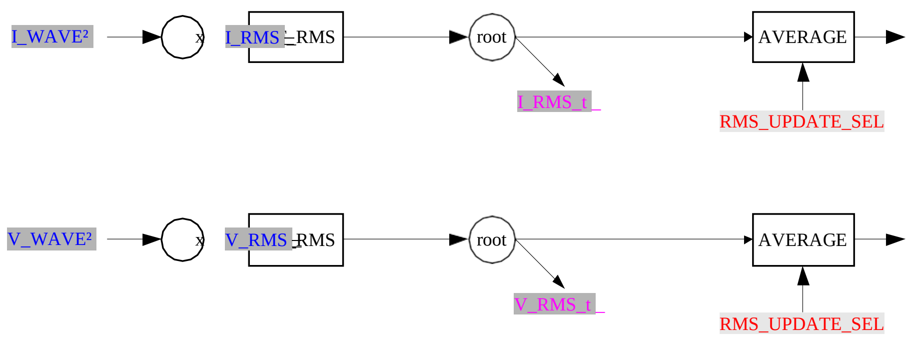


Figure 7

address	name	Significant bit	Defaults	describe
0x03	I_RMS	twenty four	0x000000	Current RMS register, unsigned
0x04	V_RMS	twenty four	0x000000	Voltage rms register, unsigned

<table>
<tr><td>0x19</td><td>MODE</td><td colspan="3">Operating Mode Register</td></tr>
<tr><td>No.</td><td>name</td><td>default value</td><td colspan="2">description</td></tr>
<tr><td rowspan="2">[3]</td><td rowspan="2">RMS_UPDATE_SEL</td><td rowspan="2">0b0</td><td rowspan="2">When the rms register is refreshed time setting</td><td>0： 400ms</td></tr>
<tr><td>1： 800ms</td></tr>
</table>

Set MODE[3].RMS_UPDAT_SEL, you can choose the average refresh time of the effective value to be 400ms or 800ms, and the default is 400ms. When the channel is in the anti-submarine state, the effective value of the current channel is zero.

Current RMS conversion formula: I_RMS = $\frac{305978*I(A)}{Vref}$

Voltage RMS conversion formula: V_RMS = $\frac{73989*V(V)}{Vref}$

$Vref$ is the reference voltage, the typical value is 1.218V.

Note: **I(A)** is the input signal (**mV**) between **IP** and **IN pins**, **V(V)** is the input signal **(mV) of VP** pin .

2.6 overcurrent detection

BL0942 can quickly collect the effective value of the current to realize the function of over-current detection. After I_WAVE_F takes the absolute value, it accumulates the half-cycle or cycle time, stores it in the I_FAST_RMS register, compares it with the current fast RMS threshold register I_FAST_RMS_TH , and outputs an over-current interrupt through the pin.

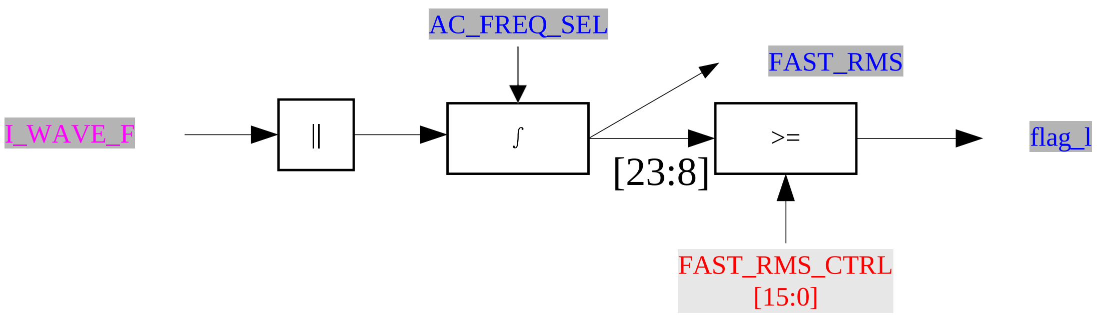


Figure 8

address	name	Significant bit	Defaults	describe
0x15	I_FAST_RMS_TH	16	0xFFFF	Current Fast RMS Threshold Register

Set the fast RMS threshold (that is, the overcurrent threshold) through the I_FAST_RMS_TH fast RMS threshold register.

address	name	Significant bit	Defaults	describe
0x05	I_FAST_RMS	twenty four	0x000000	Current fast rms, unsigned

Compare Bit[23:8] of the I_FAST_RMS register with the overcurrent threshold I_FAST_RMS_TH [15:0] . If it is greater than or equal to the set threshold, the overcurrent alarm output indicator pin CF1/CF2/ZX outputs a high level. CF1/CF2/ZX are set by OT_FUNX output configuration register.

address	name	Significant bit	Defaults	describe	
0x16	I_FAST_RMS_CYC	3	0x1	Current Fast RMS Refresh Period Register	
				000	0.5 cycle
				001	1 cycle
				010	2 cycles
				011	4 cycles
				other	8 cycles

through the I_FAST_RMS_CYC fast effective value refresh cycle register. Among them, Zhou Bo is based on

The setting value of MODE[5] can be 50H or 60Hz. If you choose 50hz, the default is 1 cycle, that is, refresh every 20ms. For example, choose the fastest 0.5

When the cycle is accumulated, the error of the I_FAST_RMS register will be relatively large.

$$I\_FAST\_RMS \approx I\_RMS * 0.363$$

It should be noted that the algorithm of fast effective value and effective value is different. The fast effective value is only used for measurement judgment when the signal is large. Fast rms measurements will be inaccurate due to the inclusion of DC bias components at small signals. If it is desired to remove the DC bias component, set FAST_RMS_SEL(MODE[4])=1, I_WAVE_F selects the waveform after HPF.

0x19	MODE	Operating Mode Register		
No.	name	default value	description	
[4]	FAST_RMS_SEL	0b0	Fast RMS waveform source selection: 0: Waveform after SINC; 1: Waveform after HPF	
[5]	AC_FREQ_SEL	0b0	AC frequency selection	0: 50Hz
				1: 60Hz

Set AC frequency by MODE[5].

2.7 Zero-crossing detection

BL0942 provides voltage and current zero-crossing detection, and the zero-crossing signal can be output by the pin CF1/CF2/ZX . The pin output zero indicates the positive half cycle of the waveform, and the pin output 1 indicates the negative half cycle of the waveform. The time delay with the actual input signal is 570us .

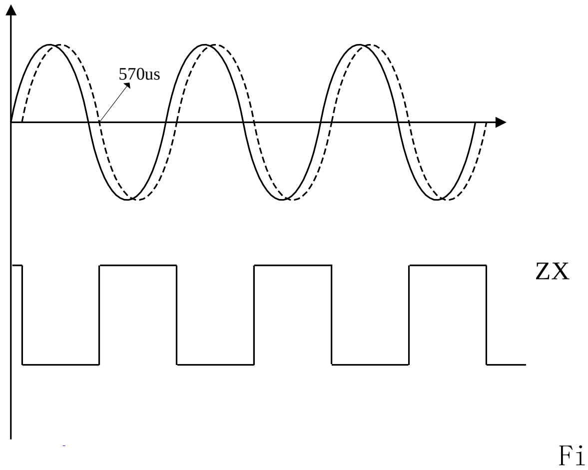


Figure 11

0x18	OT_FUNX	Output Configuration Register	
No.	name	default value	description
[1:0]	CF1_FUNX_SEL	0b00	CF1 output selection bits: b00: output active energy pulse b01: output overcurrent alarm b10: output voltage zero-crossing indication b11: Output current zero-crossing indication
[3:2]	CF2_FUNX_SEL	0b01	CF2 output selection bits: b00: output active energy pulse b01: Output over-current alarm b10: Output voltage zero-crossing indication b11: Output current zero-crossing indication
[5:4]	ZX_FUNX_SEL	0b10	ZX output selection bit: b00: output active energy pulse b01: Output over-current alarm b10: Output voltage zero-crossing indication b11: Output current zero-crossing indication
[23:6]	reserved	0b0	reserve

Configure the output pins through OT_FUNX (the SSOP10L package only has CF1).

0x19	STATUS	working status register		
No.	name	default value	description	
[8]	I_ZX_LTH_F	0b0	Current zero-crossing output state status indication	0: Current zero crossing is above threshold 1: current zero crossing is lower than the threshold
[9]	V_ZX_LTH_F	0b0	Voltage zero-crossing output state status indication	0: Voltage zero crossing is higher than the threshold 1: Voltage zero crossing is lower than the threshold

If the voltage or current RMS value is too low, the zero-crossing detection output signal is unstable.

When the voltage effective value V_RMS High 5 bit it equal to 0 V_ZX_LTH_F _If it is 1 , it means that the effective value of the voltage is too low, less than 1/32 of the full scale , and the zero-crossing indicator of the voltage is turned off and remains at 0 .

RMS current I_RMS _ _high 6 bit equal 0 , I_ZX_LTH_F for 1 , it means that the effective value of the current is too low, less than the full scale 1/64 , the current zero-crossing indicator is turned off and remains at 0 .

2.8 Line voltage frequency detection

BL0942 has a line voltage frequency detection function, which is refreshed every several set cycles (FREQ_CYC), and what is detected is a full-wave voltage waveform.

<table>
<tr><th>address</th><th>name</th><th>Significant bit</th><th>Defaults</th><th colspan="2">describe</th></tr>
<tr><td>0x08</td><td>FREQ</td><td>16</td><td>0x4e20</td><td colspan="2">Line voltage register, unsigned</td></tr>
<tr><td rowspan="5">0x17</td><td rowspan="5">FREQ_CYC</td><td rowspan="5">2</td><td rowspan="5">0x3</td><td colspan="2">Line Voltage Refresh Time Setting Register</td></tr>
<tr><td>00</td><td>2 cycles refresh</td></tr>
<tr><td>01</td><td>4 cycles refresh</td></tr>
<tr><td>10</td><td>8 cycle refresh</td></tr>
<tr><td>11</td><td>16 cycle refresh</td></tr>
</table>

The resolution of line voltage measurement is 2us/LSB (500KHz clock), which is equivalent to 0.01% at 50Hz line frequency or 0.012% at 60Hz line frequency . The conversion relationship between the line voltage register (FREQ) and the actual line voltage frequency:

$$f_{\text{test}} = \frac{2 * f_s}{FREQ}$$

Among them, fs=500KHz in default mode ; for 50Hz mains network, the measured value of FREQ is 20000 (decimal), for 60Hz
The mains network, the measured value of FREQ is 16667 (decimal).

In addition, when the voltage RMS value is lower than the zero-crossing judgment threshold, the line voltage frequency detection is turned off.

3 Communication Interface

BL0942 provides two communication interfaces, SPI and UART, which are multiplexed. The register data is sent in 3 bytes (24bit). For the register data less than 3 bytes, the unused bits are filled with 0, and 3 bytes are sent.

3.1 SPI

- via pin SEL option, with the UART Multiplexing, SEL=1
- work in slave mode
- Half-duplex communication, the communication rate can be configured, the maximum communication rate is 900Khz
- 8-bit data transfer, MSB First, LSB is behind
- Fixed a clock polarity / phase (CPOL=0, CPHA=1)
- Three-wire or four-wire communication, when A2_NCS fixed connection 0 When, it is equivalent to three-wire communication, when A2_NCS When controlled by the host, it is equivalent to four-wire communication.

3.1.1 Operating mode

The master device works in Mode1: CPOL=0, CPHA=1, that is, in the idle state, SCLK is at low level, and the data is sent on the first edge, that is, the transition of SCLK from low level to high level, so the data Sampling is on the falling edge and data transmission is on the rising edge.

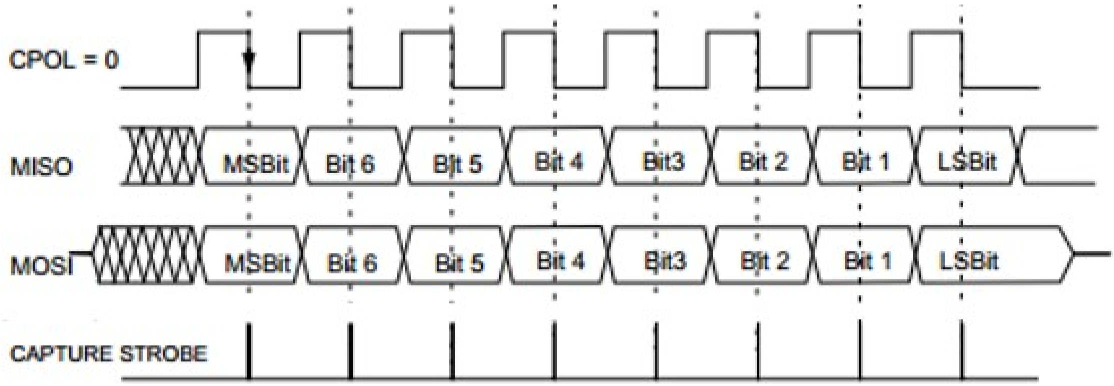


Figure 12

3.1.2 frame structure

In the communication mode, first send 8bit identification byte (0x58) or (0xA8), (0x58) is the identification byte of read operation, (0xA8) is the identification byte of write operation, and then send the register address byte to decide to access the register address (see BL0942 Register List) . The figure below shows the data transfer sequence for read and write operations, respectively. After one frame of data transmission is completed, BL0942 re-enters the communication mode. The number of SCLK pulses required for each read / write operation is 48 bits.

There are two frame structures, which are described as follows:

1) Write operation frame

Write CMD								Register Address								Data_H								Data_L								Checksum							
1	0	1	0	1	0	0	0	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D.5	D4	D3	D.2	D.1	D.0

Among them, the checksum byte CHECKSUM is ((0xA8 + ADDR + Data_H + Data_M+ Data_L) &

0xFF) and then reversed bit by bit. 2) Read operation frame

Read CMD								Register Address							
0	1	0	1	1	0	0	0	A7	A6	A5	A4	A3	A2	A1	A0

Data_H								Data_L								Checksum							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

Among them, the checksum byte CHECKSUM= ((0x58 + ADDR + Data_H + Data_M + Data_L) & 0xFF)

is reversed bit by bit. Note: The data is a fixed 3 bytes (the high byte is in front,

the low byte is in the back, if the data valid byte is less than 3 bytes, the invalid bit

is filled with 0)

3.1.3 Write Operation Timing

The serial write sequence is performed as follows. The frame identification byte {0xA8} indicates that the data communication operation is writing data. ADDR is the address of the register that needs to write data. The MCU will prepare the data bits that need to be written into the BL0942 before the falling edge of SCLK , and start shifting in the register data at the falling edge of the clock of SCLK . All remaining bits of the register data are also shifted left on this falling edge of SCLK (Figure 13).

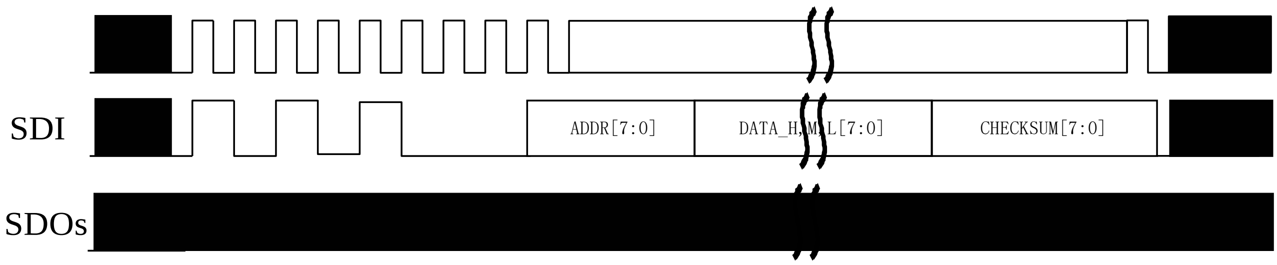


Figure 13

3.1.4 Read Operation Timing

During the data read operation of BL0942 , at the rising edge of SCLK , BL0942 outputs the corresponding data bit to the SDO logic output pin, and the SDO value remains unchanged during the next SCLK is 1 , that is, in the next On the falling edge, an external device can sample the SDO value. When performing data read operation, MCU must first send a read command frame.

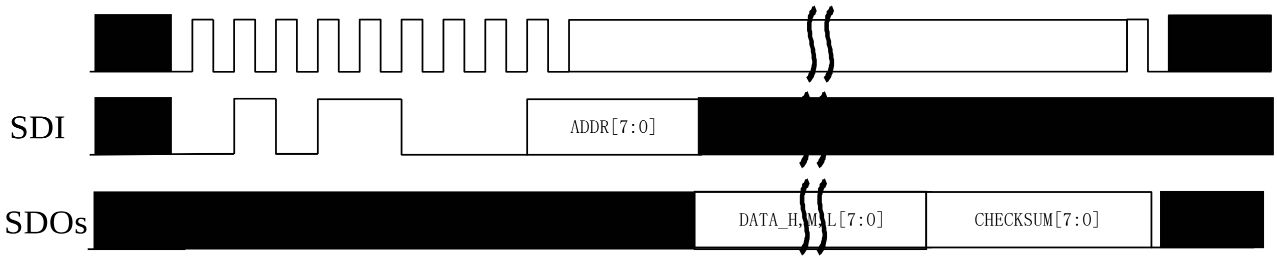


Figure 14

When BL0942 is in the communication mode, the frame identification byte {0x58} indicates that the data communication operation is read data. Then the following byte ADDR is the address of the target register to be read. After receiving the register address, BL0942 begins to shift out the data in the register on the rising edge of SCLK (Figure 14) . All remaining bits of the register data are shifted out on subsequent SCLK rising edges. Therefore, on the falling edge, the external device can sample the output data of the SPI . Once the read operation is complete, the serial interface re-enters communication mode. At this time, the SDO output enters a high-impedance state on the falling edge of the last SCLK signal.

3.1.5 SPI Interface fault tolerance mechanism

The soft reset function of the SPI interface can reset the SPI interface independently by sending 6 bytes of 0xFF through the SPI interface.

3.2 UART

- via pin SEL option, with the SPI Multiplexing, SEL=0
- work in slave mode
- Half-duplex communication, the baud rate can be configured as 4800bps , 9600bps , 19200bps , 38400bps by software and hardware
- 8-bit Data transfer, no parity, stop bit 1
- Support packet reading
- TSSOP14L The package can support device chip select function, the hardware chip select address pins are [A2_NCS , A1] , optional device 0~3 . Can support 4 Sheet BL0942 hang on UART Data communication on the bus, only occupying the MCU A UART of interface.

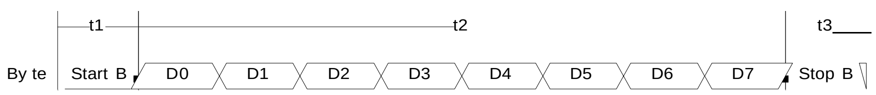
3.2.1 Baud rate configuration

Use mode register UART_RATE_SEL (MODE[9:8]) and pin SCLK_BPS for baud rate configuration.

0x19	MODE	Operating Mode Register			
No.	name	default value	description		
[9:8]	UART_RATE_SEL	0b00	UART communication baud rate selection	00	SCLK_BPS pin = 0: 4800bps
					SCLK_BPS pin = 1: 9600bps
				01	Same as 00
				10	19200bps
				11	38400bps

The RATE_SEL reset value is 0x0 every time the chip is powered on , and the baud rate is determined according to the pin SCLK_BPS at this time .

3.2.2 format per byte



Take the baud rate =4800bps as an example:

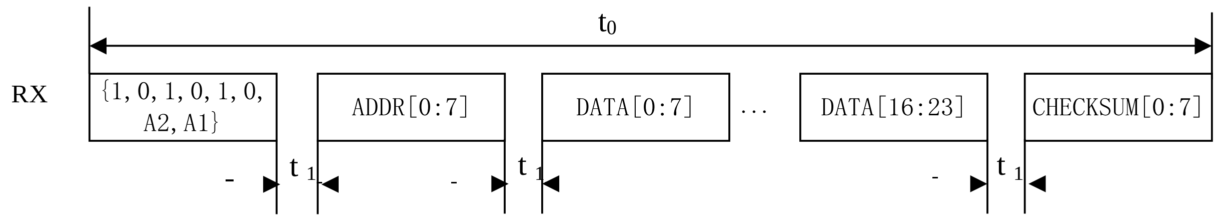
Start bit low level duration t1=208us

Valid data bit time lasts t2=208*8=1664us

Stop bit high level duration t3=208us

3.2.3 write timing

The host UART write data sequence is shown in the figure below. The host first sends the command byte {1,0,1,0,1,0,A2,A1} , and then sends the register byte (ADDR) that needs to be written into the data, and then Send data bytes in sequence (low byte first, high byte later, if the data valid byte is less than 3 bytes, the invalid bit is filled with 0), and finally the checksum byte.



{1,0,1,0,1,0,A2,A1} are frame identification bytes for write operation. Suppose

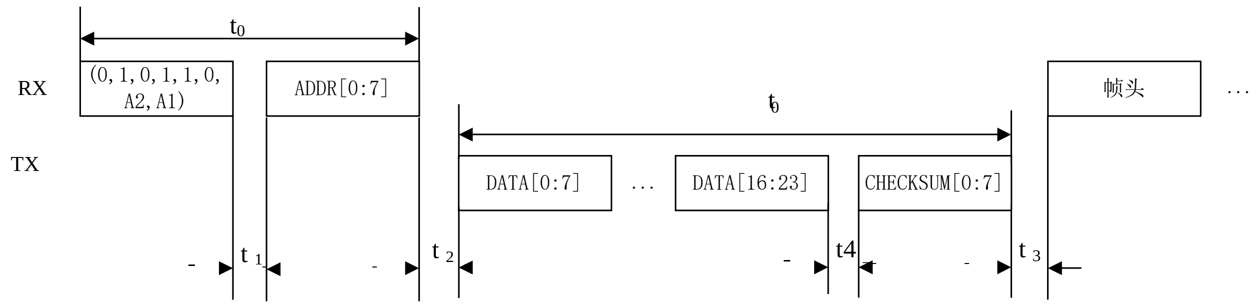
{A2,A1}=10 , the device address is 2 , and the frame identification byte is 0xAA . ADDR is

the internal register address of BL0942 corresponding to the write operation .

CHECKSUM bytes are ({1,0,1,0,1,0,A2,A1}+ADDR+DATA[7:0]+DATA[15:8]+DATA[23:16]) & 0xFF negated.

3.2.4 read timing

The host UART read data sequence is shown in the figure below, the host first sends the command byte {0,1,0,1,1,0,A2,A1} , and then sends the register address byte (ADDR) to be read , and then BL0942 sends the data bytes in sequence (the low byte comes first, the high byte follows, if the data valid byte is less than 3 bytes, the invalid bit is filled with 0), and finally the checksum byte.



{0,1,0,1,1,0,A2,A1} is the frame identification byte of the read operation, assuming that

{A2,A1}=10， the device address is 2， and the frame identification byte is 0x5A .

ADDR is the internal register address of BL0942 corresponding to the read operation ;

CHECKSUM bytes are （ {0,1,0,1,1,0,A2,A1}+ADDR+DATA[7:0]+DATA[15:8]+DATA[23:16] ） & 0xFF negated.

Note: The device address of **SSOP10L** package is **0**， that is, **{A2,A1}=00** .

3.2.5 Timing description

	illustrate	Min	type	Max	unit
t1	Interval time between MCU sending bytes	0		20	M
t2	During the read operation, the MCU sends the register address to the end of the BL0942 sending byte Intervals		150		u
t3	Interframe time	0.5			u
t4	Interval time between bytes sent by BL0942		0		u

3.2.6packet sending mode

Through the command " {0,1,0,1,1,0,A2,A1}+ 0xAA ", BL0942 will return a full electric parameter data packet. A total of 22 packets were returned

bytes, when using 4800bps , it takes about

48ms . Full electric parameter

package format:

	发送字节顺序	内容
HEAD	0	0x55
I_RMS	1	I_RMS[7:0]
	2	I_RMS[15:8]
	3	I_RMS[23:16]
V_RMS	4	V_RMS[7:0]
	5	V_RMS[15:8]
	6	V_RMS[23:16]
I_FAST_RMS	7	I_FAST_RMS[7:0]
	8	I_FAST_RMS[15:8]
	9	I_FAST_RMS[23:16]
WATT	10	WATT[7:0]
	11	WATT[15:8]
	12	WATT[23:16]
CF_CNT	13	CF_CNT[7:0]
	14	CF_CNT [15:8]
	15	CF_CNT [23:16]
FREQ	16	FREQ [7:0]
	17	FREQ [15:8]
	18	0x00
STATUS	19	STATUS [7:0]
	20	0x00
	21	0x00
CHECKSUM	22	

checksum= (({0,1,0,1,1,0,A2,A1} + 0x55 + data1_l + data1_m + data1_h +.......) & 0xff) and invert

3.2.7 UART Interface Protection Mechanism

- Frame timeout reset, if the byte-to-byte interval time exceeds 20ms, the UART Interface reset.
- Manual reset, UART received more than 32 consecutive ″0", UART Interface reset.
- Frame identification byte or checksum If the byte is wrong, the frame data is discarded.

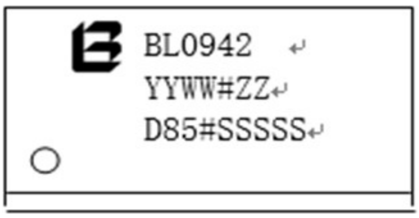
Note: In multi-chip communication in UART mode, each time a frame is sent, wait for a frame timeout or send a manual reset before sending the next frame.

4 order information

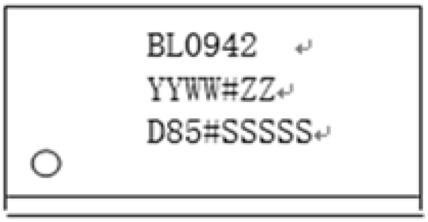
BL0942-X X=SSOP10L: SSOP10L package

X=TSSOP14L: TSSOP14L package

5 silk screen information



TSSOP14L



SSOP10L

″YY″ represents the last two digits of the packaging year

″WW″ stands for package week, 01-52 weeks

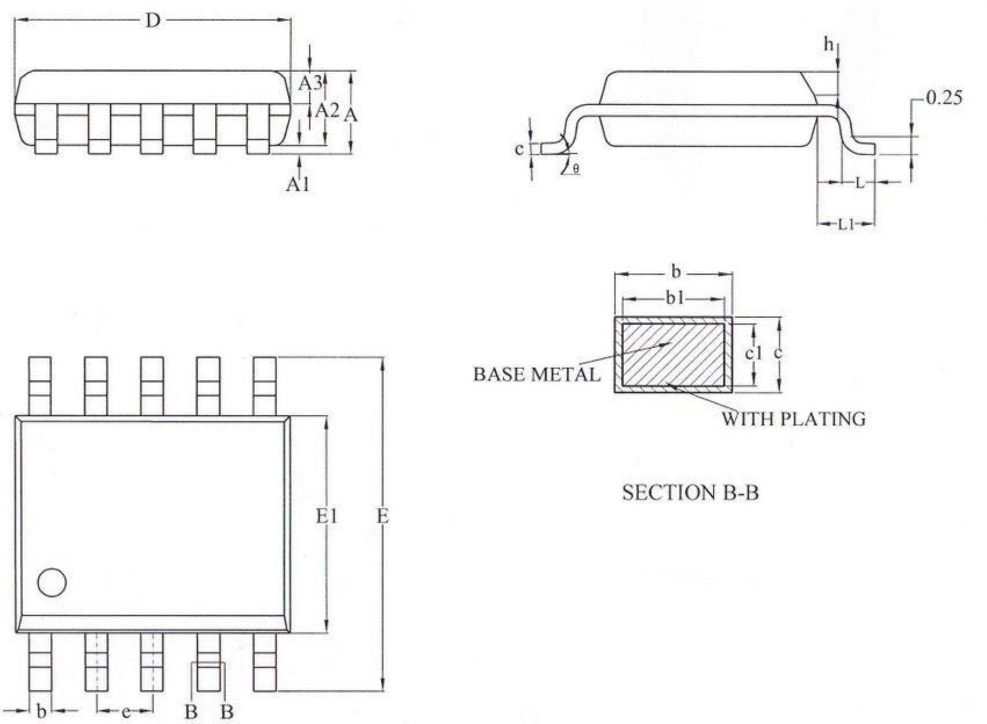
″ZZ″ stands for packaging factory

″#″ stands for space

4th to 8th letters or numbers of the ″SSSSS″ card number (LOT NO.)

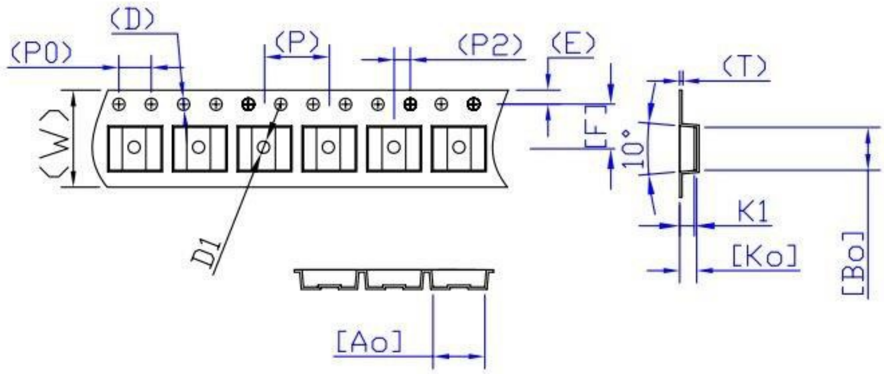
6 encapsulation

Moisture sensitivity level MSL 3
Warranty period of two years
Packing method SSOP10L
taping packaging Min.
packing 3000

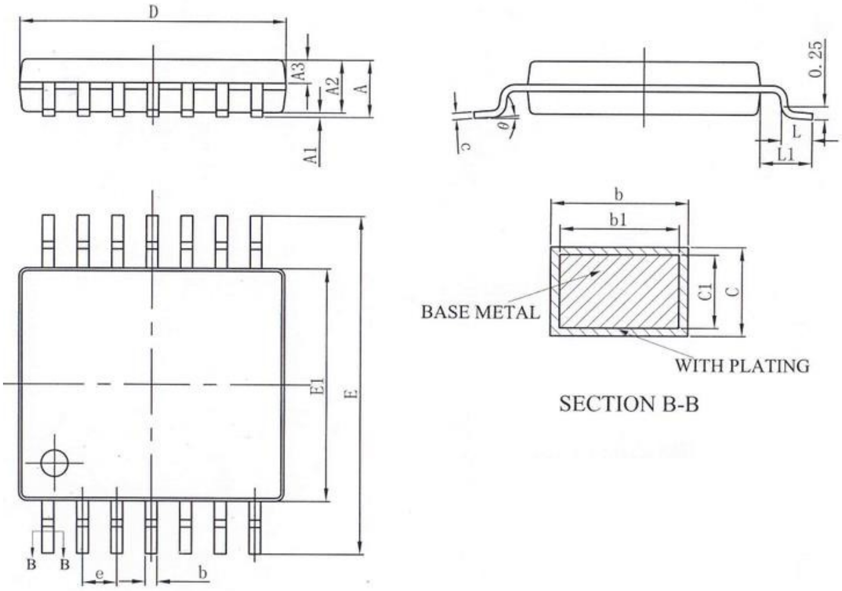


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.00BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

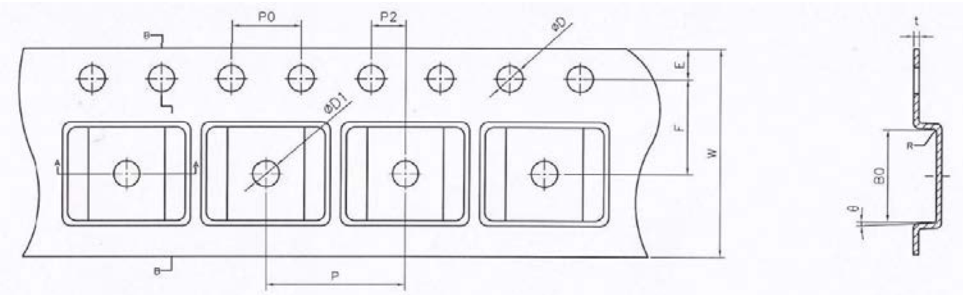
ITEM	W	A0	B0	D	D1	E	F	K1	K0	P0	P2	P	T
DIM	12.0	6.55	5.40	1.5	1.5	1.75	5.50	1.85	2.0	4.0	2.0	8.0	0.30
TOLE	+0.3 -0.3	±0.10	±0.10	+0.1 -0.0	+0.1 -0.0	±0.1	±0.10	±0.05	±0.10	±0.1	±0.1	±0.1	±0.05

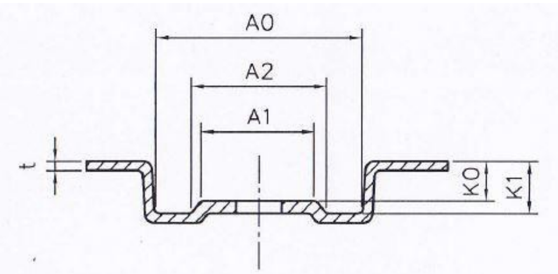


Moisture sensitivity level MSL 3
Warranty period of two years
Packing method TSSOP14L
taping packing Minimum
packing 3000



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°





共同尺寸

外观	尺寸(mm)
E	1.75±0.1
F	5.5±0.1
P2	2.0±0.05
D	$1.5^{+0.1}_{0}$
D1	$1.5^{+0.1}_{0}$
P0	4.0±0.1
R	0.5TYP
10P0	40.0±0.20

口袋尺寸

W	12.0±0.1
P	8.0±0.1
A0	6.8±0.1
B0	5.4±0.1
K0	1.3±0.1
t	0.3±0.05
K1	1.7±0.1
A1	3.8±0.2
A2	4.4±0.2
θ	3° TYP