

A Simple Zero Average Switching Energy Differential SAR ADC

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Introduction

The switching scheme presented here achieves a zero average switching energy with a fully-differential input signal and requires only one clock period per resolved bit. While architectures [1]–[3] and [4]–[6] claim to maintain a constant common-mode voltage, they actually experience a variation when discriminating the least significant bit (LSB). In contrast, the proposed solution introduces a marginal shift for only two specific digital codes during the last transition, representing less than 1 % of the total amount of cases when considering reasonable resolutions (i.e., ≥ 9 bit).

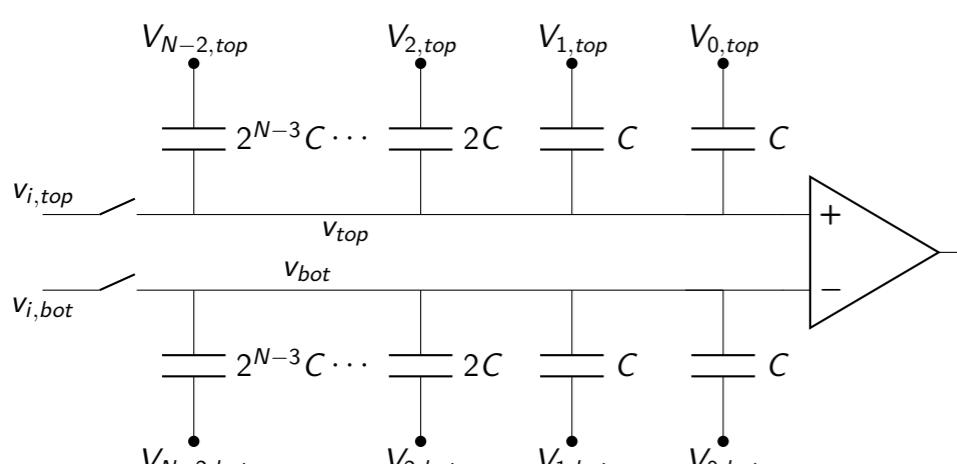


Figure 1. Generic N -bit SAR ADC with labeled binary weighted capacitors and voltages that are set by the SAR logic.

Proposed switching scheme

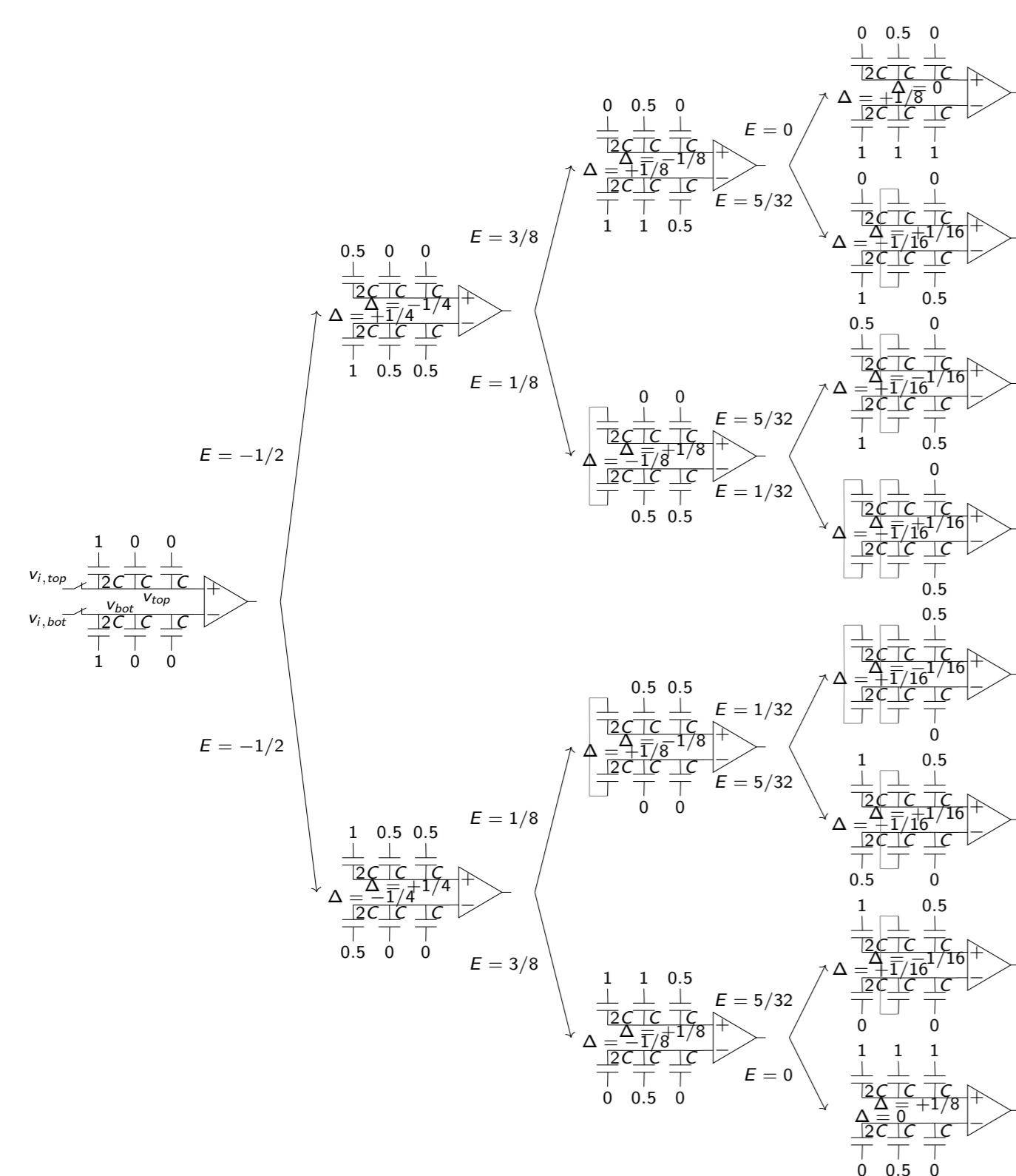


Figure 2. Proposed symmetric switching scheme for a 4-bit SAR ADC. Top sampling is performed. Voltage increments following each transition are visualized at both the top and bottom nodes. The energy values are indicated on the transition arrows, relative to $CV^2 = C$. Up transitions occur when $v_{top} > v_{bot}$.

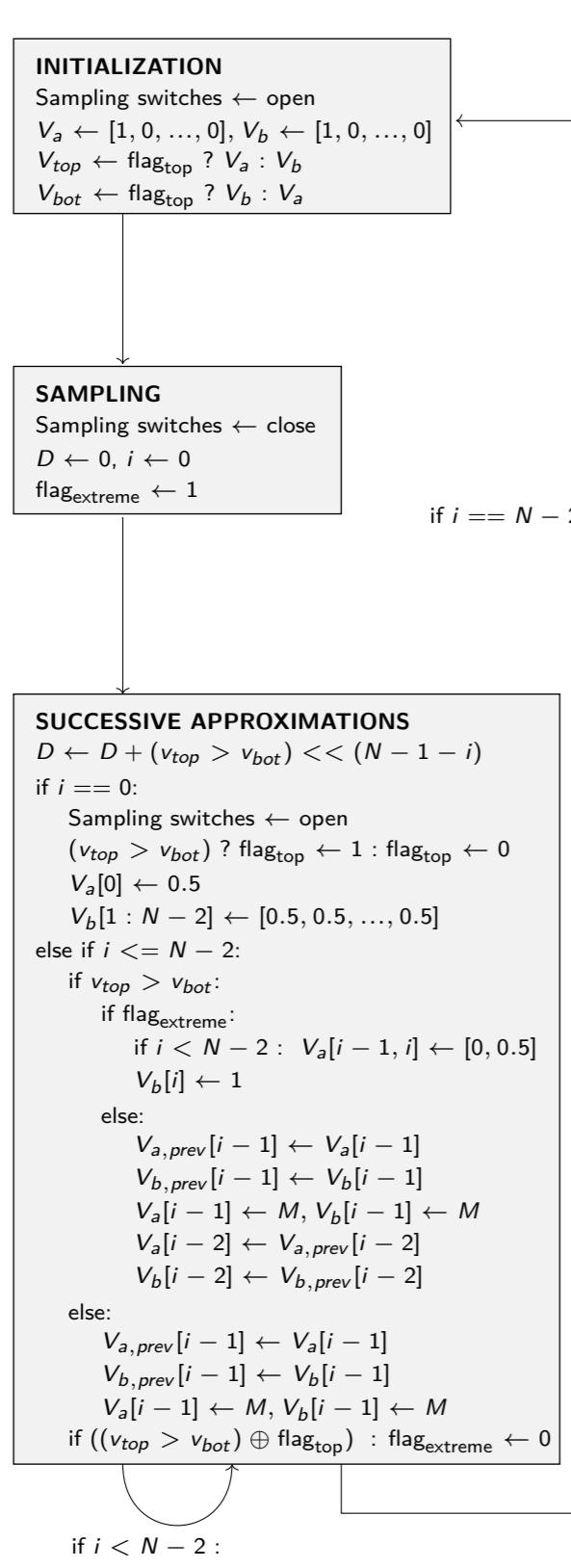


Figure 3. Proposed switching scheme algorithm in pseudocode. D is the resolved code and i the comparison counter that ranges from 0 to $N - 1$. The $<<$ symbol symbolizes the shift left operation. M indicates merging with its counterpart capacitor. Each arrow symbolizes a transition that occurs at the clock edge.

Switching energy general observations

The energy consumed during the switching process in one capacitor array half k (either top or bottom) between two successive steps, as can be generalized from the energy calculations in [7], is as follows:

$$E_k = CV_{0,k}(\Delta V_{0,k} - \Delta v_k) + \sum_{i=0}^{N-3} 2^i CV_{i+1,k}(\Delta V_{i+1,k} - \Delta v_k) . \quad (1)$$

1. Operating multiple switches simultaneously may actually result in lower energy consumption compared to using a single switch [3].
2. Removing the largest capacitors on the CDAC has a notable impact on energy usage, particularly during the initial conversions due to the binary weighting configuration [8]–[10].
3. If $V_{i,k} = 0$ (i.e., ground or negative reference), its contribution to the total switching energy becomes negligible.
4. When capacitor terminals are merged in a specific sequence as demonstrated in [3] and [4], their connection becomes independent of voltage references, resulting in zero energy.

Proposed scheme switching energy

For the specific cases of $N = 4$ and $N = 5$, the transition energies are demonstrated through the following summations:

$$\begin{aligned} E(N=4) &= CV^2 \left(-\frac{1}{2} + \frac{1}{4} + \frac{11}{128} \right), \\ E(N=5) &= CV^2 \left(-1 + \frac{1}{2} + \frac{1}{4} + \frac{55}{512} \right). \end{aligned} \quad (2)$$

As can be noticed from (2), the presence of a negative term in the first transitions plays a crucial role in minimizing the switching energy. By re-writing the equations in (2) as a function of N , the overall switching energy for an N -bit resolution is found to be:

$$E(N) = -CV^2 (2^{-3} + 2^{-N-1} + 2^{-2N+1}) . \quad (3)$$

Behavioral simulations

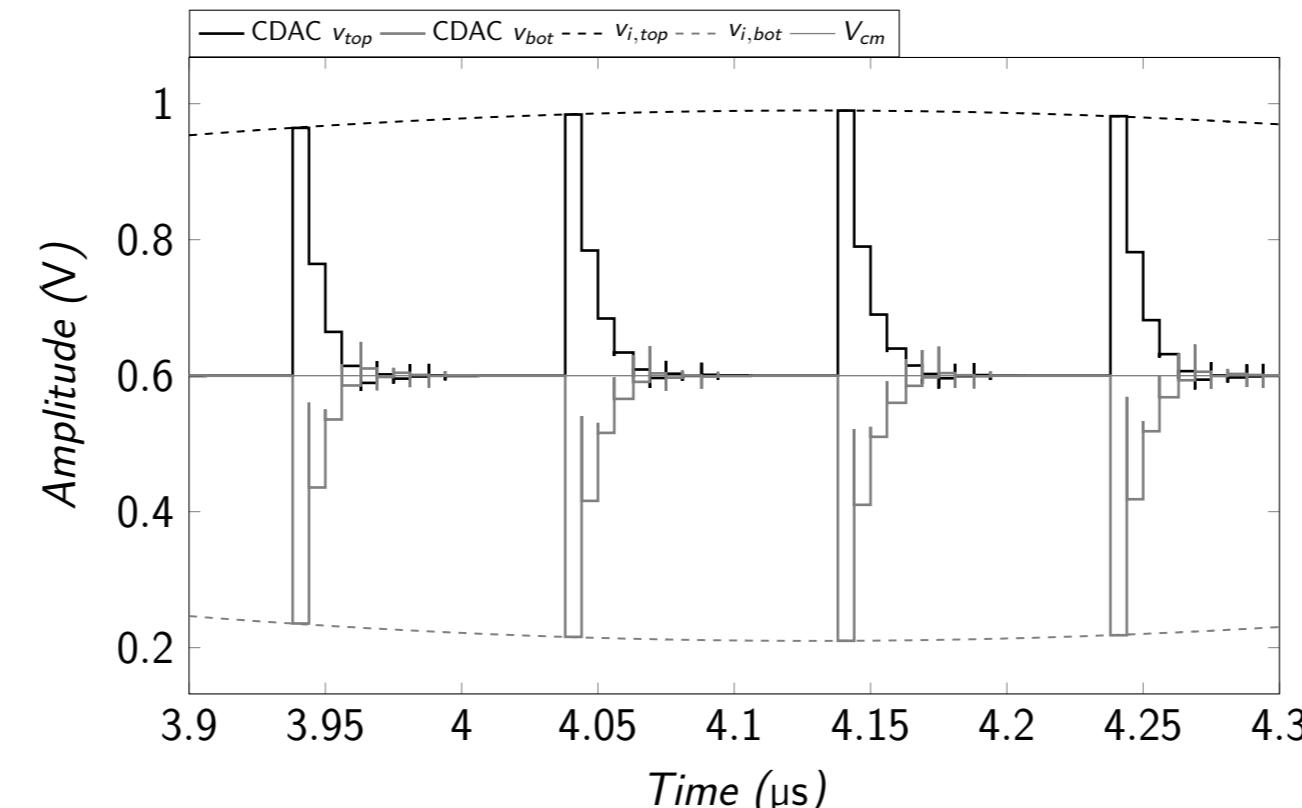


Figure 4. Behavioral simulation of the proposed SAR ADC with a sinusoidal input signal. The displayed waveforms show the transient response of the CDAC (v_{top} , v_{bot}), the input signals ($v_{i,top}$, $v_{i,bot}$) and common-mode voltage (V_{cm}) for a few conversion cycles. The clock frequency is set at 160 MHz, with 4 clock cycles allocated to sampling, 2 for idle states, and 10 for the actual switching operation. This configuration yields a sampling rate of 10 MSPS.

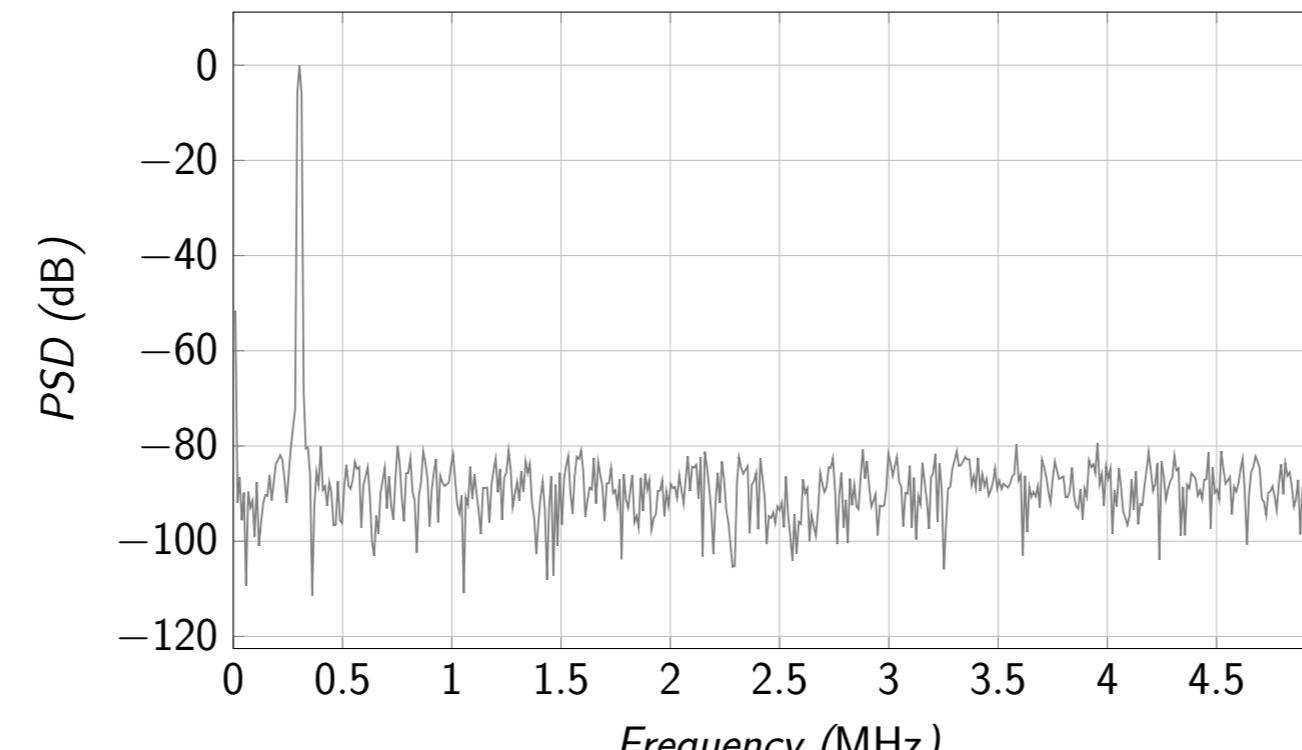


Figure 5. Power spectral density (PSD) of the proposed 10-bit SAR ADC with a sinusoidal input signal of 0.395 V and ~ 302.74 kHz frequency. The simulated SNR is 62 dB, aligning with an ideal 10-bit resolution. The sampling rate is 10 MSPS with 1024 FFT points.

Comparison

This section provides a comparison between the proposed switching scheme of Figure 2 and state-of-the-art 10-bit SAR ADC solutions. Table 1 summarizes the performance metrics, focusing on recent techniques that exhibit exceptionally low energy switching: $E/(CV^2) < 32$. The comparison specifically emphasizes architectures utilizing binary weighted configurations without the use of bridge capacitor techniques and, similar to other schemes considered in this analysis, the parasitic capacitors and energy consumed during the reset phase are not taken into account. The conventional SAR is used as the standard reference to assess energy and area efficiency for all techniques. It is worth mentioning that the switching energy is influenced by the input analog value. While Table 1 displays the expected switching energy of multiple switching techniques assuming all input values are equally probable, Figure 6 shows $E(D)$, i.e., the energy for each digital output code.

Table 1. Comparison with recent solutions for 10-bit SAR ADC.

	Avg. Energy $E/(CV^2)$	E Saving (%)	Capacitor DAC	Area Red. (%)	V_{cm} Variation	# Ref.
[10]	31.88	97.66	512	75	0.5Vref (High)	3
[9]	21.30	98.40	512	75	0.75Vref (Very high)	2
[4]	21.30	98.40	512	75	0.5LSB (Low)	2
[5]	21.08	98.45	512	75	0.5LSB (Low)	3
[6]	21.08	98.45	512	75	0.5LSB (Low)	3
[11]	0	100	1532	25.19	< 0.25Vref (High)	3
[12]	0 ¹	100	248	87.89	0	3
This	-0.12549	100	512	75	0.5LSB (Very low)²	3

¹ It requires a more complex digital logic implementation and additional clock cycles during conversion.

² 0.5 LSB in the 2 most extreme cases out of 2^{N-1} cases, 0 LSB in the rest. No additional clocks.

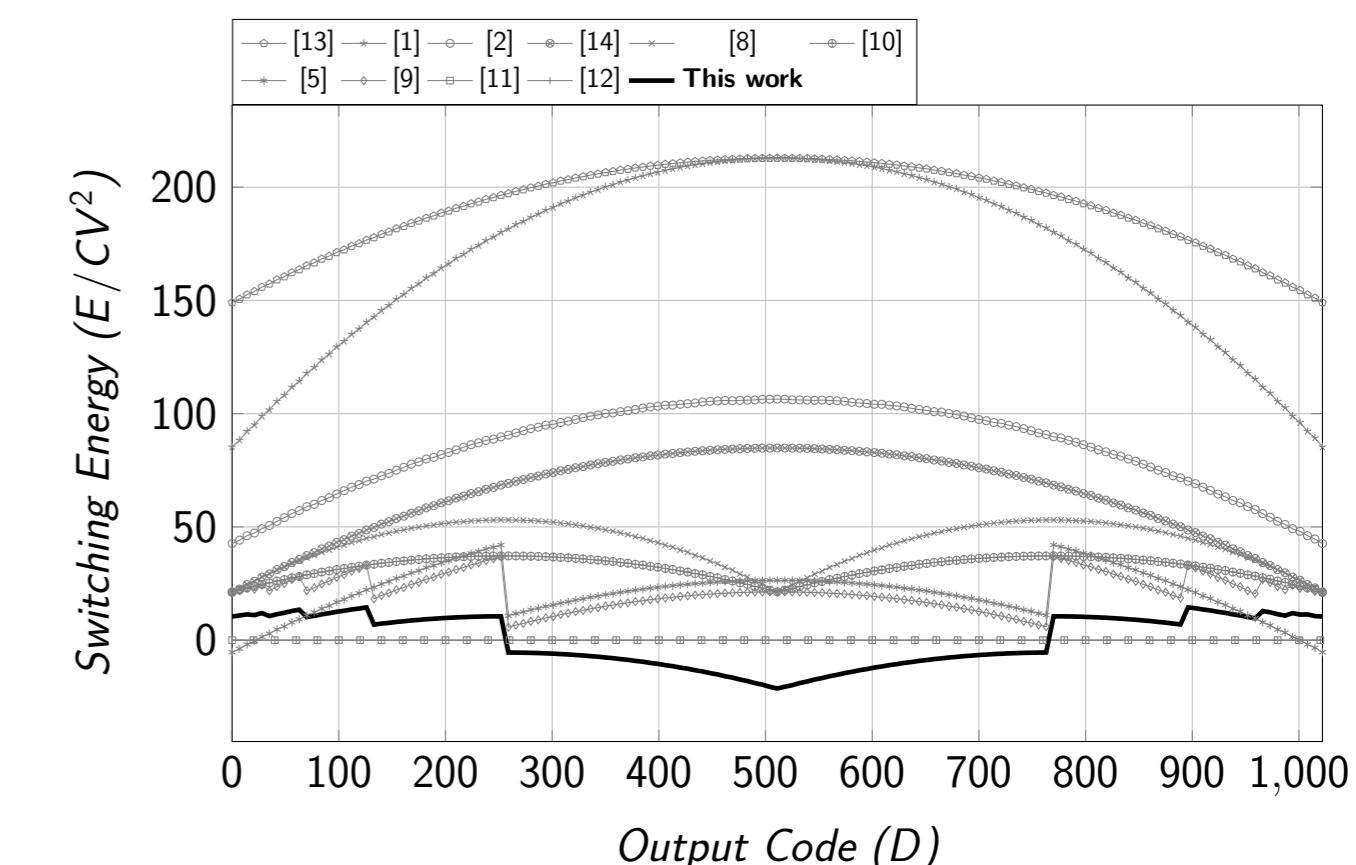


Figure 6. $E(D)$ comparison with state-of-the-art 10-bit SAR ADCs.

Summary and future work

Acknowledgements

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