

A Simple Zero Average Switching Energy Differential SAR ADC

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Introduction

The successive approximation register (SAR) analog-to-digital converter (ADC) has emerged as a dominant architecture for low-power applications. This is attributed to its superior energy efficiency, compact form factor, and seamless compatibility with technology scaling. Recent advancements have notably focused on refining the switching logic. Remarkable energy savings exceeding 98% have been demonstrated in prior works [1]–[4] while maintaining common-mode voltage variations and overall performance. However, with recent advancements, it is now achievable to reach 100% energy savings at the cost of a large capacitive DAC as in [5] or complexity and extra clock cycles as in [6]. The proposed switching scheme achieves a zero average switching energy with a fully-differential input signal, an almost constant common-mode voltage and requires only one clock period per resolved bit.

Proposed switching scheme

- Symmetric operation.
- Zero energy during successive approximations.
- Almost constant common-mode voltage.
- Compact capacitive DAC.
- No additional clock cycles.

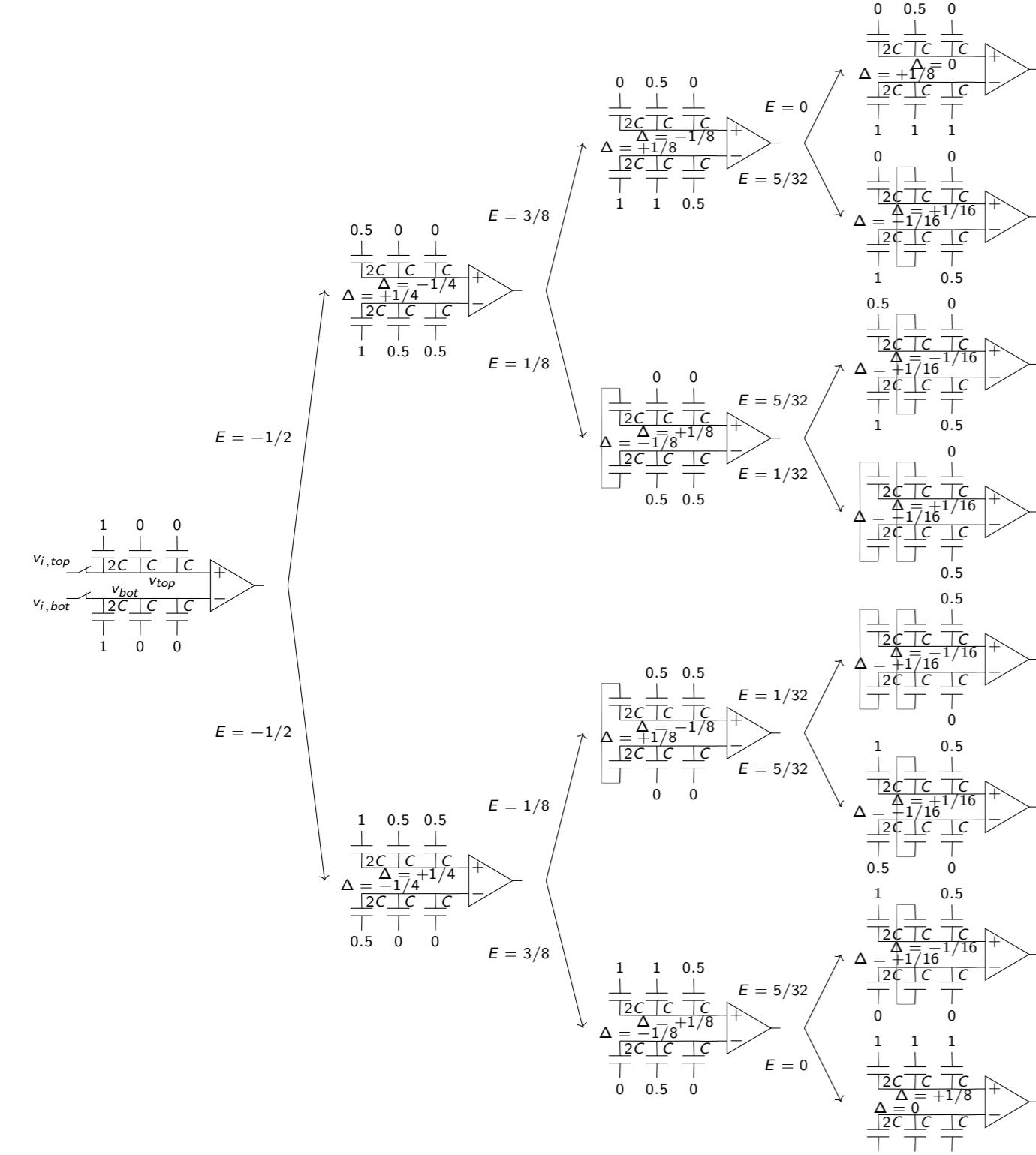


Figure 1. Proposed symmetric switching scheme for a 4-bit SAR ADC. Top sampling is performed. Voltage increments following each transition are visualized at both the top and bottom nodes. The energy values are indicated on the transition arrows, relative to $CV^2 = C$. Up transitions occur when $v_{top} > v_{bot}$.

Proposed switching scheme algorithm

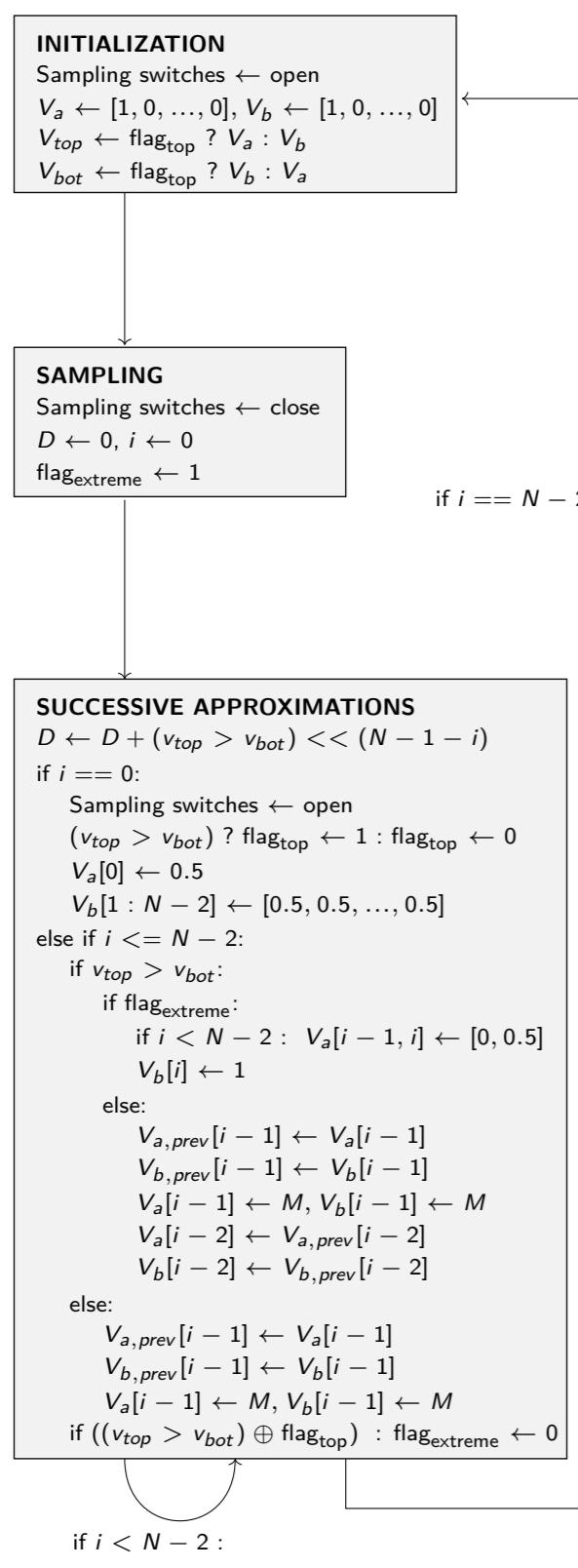


Figure 2. Proposed switching scheme algorithm in pseudocode. D is the resolved code and i the comparison counter that ranges from 0 to $N - 1$. The \ll symbolizes the shift left operation. M indicates merging with its counterpart capacitor. Each arrow symbolizes a transition that occurs at the clock edge.

Switching energy general observations

The energy consumed during the switching process in one capacitor array half k (either top or bottom) between two successive steps, as can be generalized from the energy calculations in [7], is as follows:

$$E_k = CV_{0,k}(\Delta V_{0,k} - \Delta v_k) + \sum_{i=0}^{N-3} 2^i CV_{i+1,k}(\Delta V_{i+1,k} - \Delta v_k) . \quad (1)$$

Some main design strategies can be derived from this:

1. Operating multiple switches simultaneously may actually result in lower energy consumption compared to using a single switch [8].
2. Removing the largest capacitors on the CDAC has a notable impact on energy usage, particularly during the initial conversions due to the binary weighting configuration [9]–[11].
3. If $V_{i,k} = 0$ (i.e., ground or negative reference), its contribution to the total switching energy becomes negligible.
4. When capacitor terminals are merged in a specific sequence as demonstrated in [8] and [1], their connection becomes independent of voltage references, resulting in zero energy.

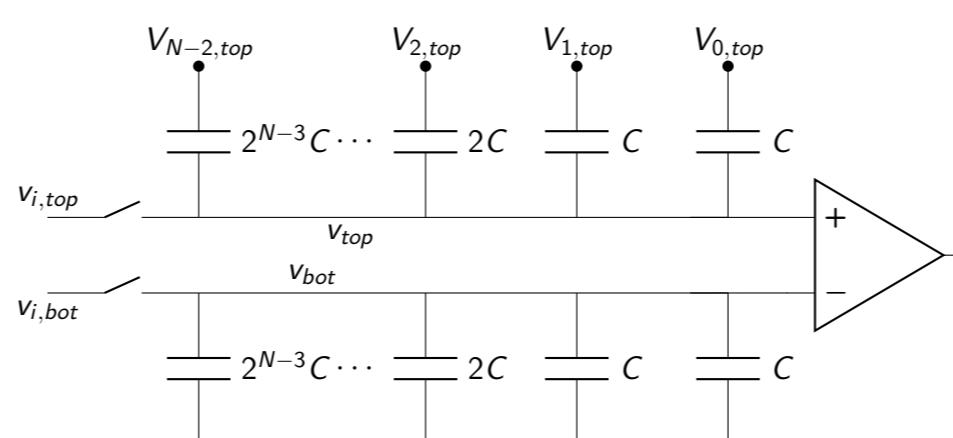


Figure 3. Generic N -bit SAR ADC with labeled binary weighted capacitors and voltages that are set by the SAR logic.

Proposed scheme switching energy

For the specific cases of $N = 4$ and $N = 5$, the transition energies are demonstrated through the following summations:

$$\begin{aligned} E(N=4) &= CV^2 \left(-\frac{1}{2} + \frac{1}{4} + \frac{11}{128} \right), \\ E(N=5) &= CV^2 \left(-1 + \frac{1}{2} + \frac{1}{4} + \frac{55}{512} \right). \end{aligned} \quad (2)$$

As can be noticed from (2), the presence of a negative term in the first transitions plays a crucial role in minimizing the switching energy. By re-writing the equations in (2) as a function of N , the overall switching energy for an N -bit resolution is found to be:

$$E(N) = -CV^2 (2^{-3} + 2^{-N-1} + 2^{-2N+1}) . \quad (3)$$

Negative energies $E(N)$ are possible when there is a positive energy in the reset phase.

Behavioral simulations

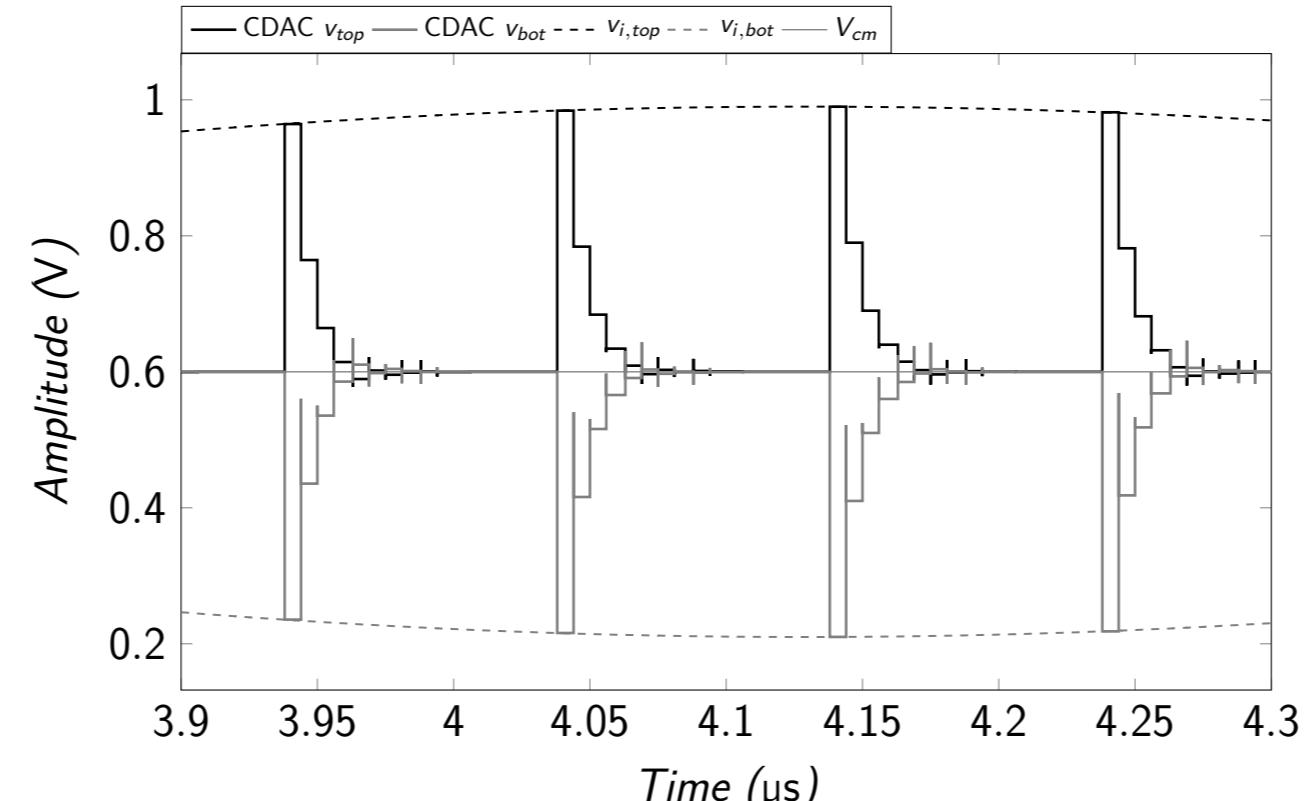


Figure 4. Behavioral simulation of the proposed SAR ADC with a sinusoidal input signal. The displayed waveforms show the transient response of the CDAC (v_{top} , v_{bot}), the input signals ($v_{i,top}$, $v_{i,bot}$) and common-mode voltage (V_{cm}) for a few conversion cycles. The clock frequency is set at 160 MHz, with 4 clock cycles allocated to sampling, 2 for idle states, and 10 for the actual switching operation. This configuration yields a sampling rate of 10 MSPS.

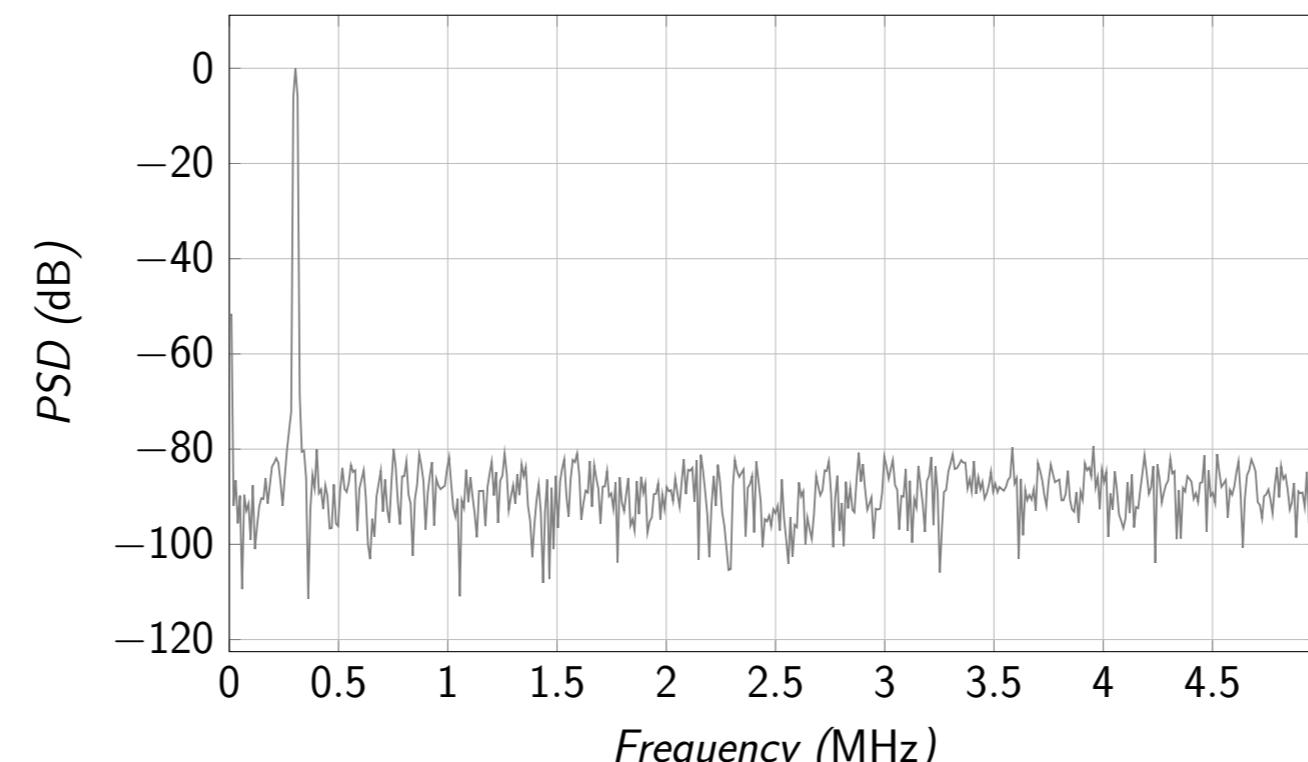


Figure 5. Power spectral density (PSD) of the proposed 10-bit SAR ADC with a sinusoidal input signal of 0.395 V and ~ 302.74 kHz frequency. The simulated SNDR is 62 dB, aligning with an ideal 10-bit resolution. The sampling rate is 10 MSPS with 1024 FFT points.

Comparison

The section compares the proposed switching scheme of Figure 1 with state-of-the-art 10-bit SAR ADC solutions. Table 1 showcases the performance metrics against techniques with low energy switching: $E/(CV^2) < 32$. The comparison specifically emphasizes architectures utilizing binary weighted configurations without the use of bridge capacitor techniques. Similar to other schemes presented in this analysis, parasitic capacitors and energy consumed during the reset phase are not considered. The conventional SAR is used as the standard reference. Table 1 displays the expected switching energy of multiple switching techniques and Figure 6 shows $E(D)$, i.e., the energy for each digital output code.

Table 1. Comparison with recent solutions for 10-bit SAR ADC.

	Avg. Energy $E/(CV^2)$	E Saving (%)	Capacitor DAC	Area Red. (%)	V_{cm} Variation	# Ref.
[11]	31.88	97.66	512	75	0.5Vref (High)	3
[10]	21.30	98.40	512	75	0.75Vref (Very high)	2
[1]	21.30	98.40	512	75	0.5LSB (Low)	2
[2]	21.08	98.45	512	75	0.5LSB (Low)	3
[3]	21.08	98.45	512	75	0.5LSB (Low)	3
[5]	0	100	1532	25.19	< 0.25Vref (High)	3
[6]	0 ¹	100	248	87.89	0	3
This	-0.12549	100	512	75	0.5LSB (Very low)²	3

¹ It requires a more complex digital logic implementation and additional clock cycles during conversion.

² 0.5 LSB in the 2 most extreme cases out of 2^{N-1} cases, 0 LSB in the rest. No additional clocks.

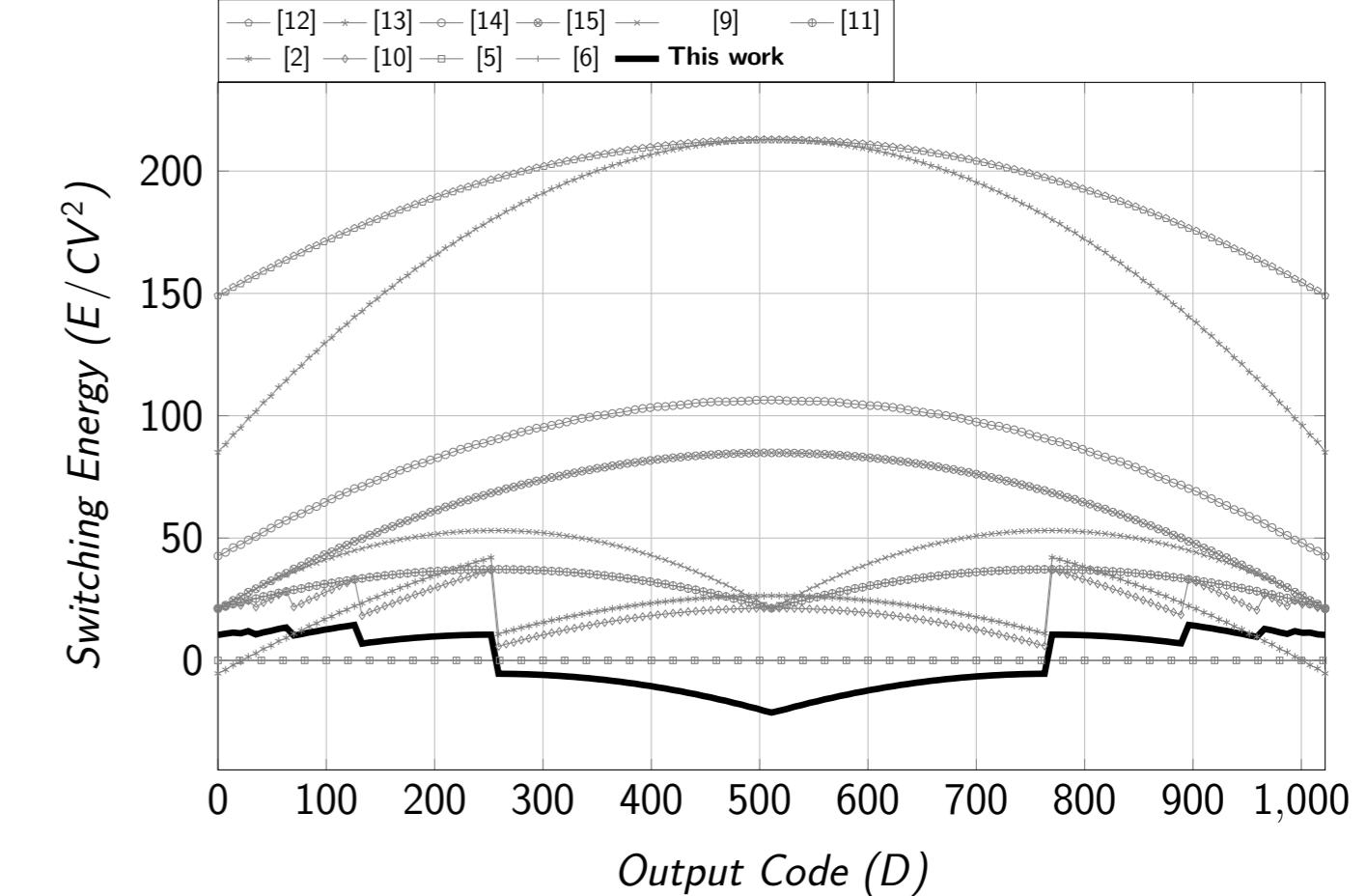


Figure 6. $E(D)$ comparison with state-of-the-art 10-bit SAR ADCs.

Summary and future work

A simple SAR ADC with zero average switching energy has been introduced. The proposed scheme keeps a constant common-mode voltage, minimizes the capacitor area and requires only one clock per transition. Each individual cell of the SAR is prepared for implementation at the transistor level, and as part of future development, exploration of a 28nm CMOS process is underway. It has been demonstrated that by carefully selecting connections at the capacitor terminals a simple architecture achieves a zero power consumption during the successive approximations conversion phase.

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