16-Channel Cryo Detector Frequency Tracking Algorithm (FTA) CMB Version

Author: J. Dusatko

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# Registers

The Cryo Mux Processor presently contains up to 2048 “Configuration” registers which the app can read and write, and up to 2048 “Status” registers which are read-only to the app. All registers are 32-bits wide. Registers are defined below; more registers will be defined eventually.

### Configuration Registers

The Configuration Registers are used by the app to configure and operate the FPGA PLL

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Configuration Registers (R/W)** | | | | |
| **AXI addr** | **Word** | **Size (bits)** | **Function** | **Comments** |
| 0x800 | 0 |  | Control Register | See bit-by-bit definition below |
| 0x804 | 1 | 1 | Feedback enable | D[0] = 1 to enable overall feedback  (each channel must be individually enabled as well) |
| 0x808 | 2 | 16 | Feedback gain | D[7:0] unsigned 16\_12 e.g 0x1000 = nominal gain / min nonzero gain = 1/4096, max gain = 16  This value is multiplied by the calculated frequency error value to increase the overall error magnitude |
| 0x80c | 3 | 8 | Reference delay | D[7:0] Adjusts the delay of the reference signal to match that of the overall system (sensor, cables, RF front & back ends)  8 bits in steps of 3.2552 ns, range 0 to 830.08 ns |
| 0x810 | 4 | 16 | Output amplitudes | A0 D[31:16] Amplitude of central lines 0xffff= = 0.1 = full scale (unsigned 16\_16)  This setting value is multiplied with the output of each channel’s LO output, prior to summation with all of the other channels, which are then presented to the frequency shifter block (which shifts to DAC band). |
| 0x814 | 5 | 16 | FB limit | D[31:16] Max frequency excursion for FB  Loop filter offset frequency 307.2MHz/216 =4.6875 kHz per LSB |
| 0x818 | 6 | 16 | Bandwidth | D[15:0] Bandwidth assumed for each notch. 16 bits in increments of 307.2MHz/216 ~= 4.6875 kHz  (functionally another feedback gain) |
| ~~0x81c~~ | ~~7~~ |  | ~~Synch threshold~~ | ~~Signed 16\_15 threshold on ADC 1 for signaling flux ramp synch when using function generator~~ |
| ~~0x820~~ | ~~8~~ |  | ~~Phase ref lowpass control~~  ~~Freq Error lowpass control~~ | ~~wPhiRef (15:0) unsigned 16\_16~~  ~~wdPhi (31:16) 1.0🡺no filtering (see Note 1 below)~~ |
| 0x824 –0x8f8 | 9 -62 | -- | unused/reserved |  |
| 0x8fc | 63 | 1 | Command Reg | D[0] = 1 to reset loop filter (non-toggling, must be set back to 0) |
| 0x900 –0x93C | 64-95 | 25 | Enable FBi  Initial Resonator Line Frequency Fi | Fi [24]: FBeni enable ith feedback (1=ena,0=disa)  Fi [23:0] Initial frequency of ith line, unsigned 24 bits, units of 307.2MHz/224 ~= 18.31 Hz per LSB |
| 0x940 –0x9FC |  |  | unused/Reserved |  |
| 0xA00 –0xA7C | 96-127 | 32 | eta I&Q channel calibration constants | D[31:0] / Floating point value / paired:  Addr, Addr+4: Chan(n) I, Chan(n) Q  n: 0=ch0, 1 = ch1 … |
| 0xA80 -- 0xAFC |  |  | Unused/Reserved |  |
| 0XB00 –0xB3C | 128-143 | 16s | DAC IF Band Frequency shift LO tune word | D[15:0] / Sets the tuning frequency of the DAC signal up-mixer to shift the output into the desired DAC freq band (for its internal up converter). Set value = (FLO x 2^16)/307.2MHz, where FLO = desired freq |
|  |  |  |  |  |
|  |  |  |  |  |

Notes:

1. Registers are write-only unless otherwise noted
2. Registers are addressed as 4-byte entities
3. Registers are 32-bits, but not all bits may be used in a particular register
4. The Configuration Registers are write-only to the high-level app (unless otherwise noted)
5. Unless otherwise noted, the given register setting applies to all lines/channels in the system

#### Control Register Bit Definition (address 0x800)

|  |  |  |
| --- | --- | --- |
| **bit** | **function** | **comment** |
| 0 | RF output enable | 0 🡺 off | 1 🡺 RF output enabled |
| 1 | Reference source | 0 🡺 use ADC ref input | 1 🡺 use internal reference (not implemented, always uses internal reference) |
| 2 | ~~Notch simulator enable~~ | ~~1 🡺 enable internal notch simulator~~ (not yet implemented) |
| 3 | ~~White noise~~ | ~~1 🡺 generate white noise in band around each output line~~ (not yet implemented) |
| 4 | Feedback polarity | 0 🡺 normal polarity | 1 🡺 inverted |
| [7:5] | Unused/reserved |  |
| [15:8] | Status mux | Selects a channel/line for which status registers 7:0 (see next section) provide debug information |
| [23:16] | Debug mux setting | Maps internal signals for channel (n) to debug ports  Debug port 0: Channel(n) loop filter output value  Debug port 1: Channel(n) frequency error value  D[23:16] = (n) = channel # (0…15) |
| 24 | Ch0 band A I/Q swap | Swap I/Q datapaths on incoming 32b data stream from the ADC DDC channel (two per physical ADC channel)  0: I=Din[15:0], Q=Din[31;16]  1: Q=Din[15:0], I=Din[31;16] |
| [31:25] | unused/reserved |  |

Notes:

1. Bits are write-only unless otherwise noted

### Status Registers

Status registers, read-only to high-level apps, provide status info from the Laser Locker module.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Status Registers (Read-only)** | | | | | |
| **AXI addr** | **Word** | **Size (bits)** | **Function** | **Comments** | |
| 0x000 | 0 | 24 | Freq | Debug :  Select nth line/channel viaConfig Register\_0 bits [15:8] | D[23:0] Frequency of channel/line / (307.2MHz/2^24 = 18.31Hz/LSB) |
| 0x004 | 1 | 32 | delta F | Freq error for line (32 bits signed / 32\_30 format: 307.2MHz/2^30 = 0.286Hz/LSB (fractional)) |
| 0x008 | 2 |  | ~~Signal amplitude~~ | Currently hard-wired to Ch0 Initial Frequency (register 0x900) value for initial test & debug |
| 0x00C | 3 |  | ~~Reference amplitude~~ |
| 0x010 | 4 |  | ~~Minus sideband amplitude~~ |
| 0x014 | 5 |  | ~~Minus sideband reference~~ |
| 0x018 | 6 |  | ~~Plus sideband amplitude~~ |
| 0x01C | 7 |  | ~~Plus sideband reference~~ |
| 0x020 | 8 |  | unused/reserved |  |
| 0x024 | 9 |  | unused/reserved |
| 0x028 | 10 |  | unused/reserved |  |
| 0x02c | 11 |  | unused/reserved |
| 0x030 | 12 |  | unused/reserved |  | |
| 0x034-0x0ff | 13-63 |  | unused/reserved |  | |
| 0x100-0x17C | 64-95 | 24, 32 | Frequency & Frequency Error value pairs per channel | Present frequency of nth line, 24bits signed, 18.31Hz/LSB  Frequency error of nth line, (32 bits signed / 32\_30 format: 307.2MHz/2^30 = 0.286Hz/LSB (fractional))  Addr, Addr+4: Chan(n) I, Chan(n) Q  n: 0=ch0, 1 = ch1 … | |
| 0x200-  0xEFC |  |  | unused/reserved |  | |
| 0xF00 |  | 32 | FTA version # | Version/Revision of the current frequency tracking algorithm loaded | |
| 0xF04 |  | 32 | Scratchpad Write | Simple writable register for test/debug / write side | |
| 0xF08 |  | 32 | Scratchpad Read | Read side of above | |

Notes:

1. All registers are read-only, unless otherwise noted
2. For the current FTA, there are 16 lines/channels and therefore that many status channels