

Chapter 8

TRANSISTORS

In chapter 6, we have read that a transistor is a single crystalline semiconducting material with three differently doped regions as NPN and PNP structure. Accordingly there are two types of transistors, namely : (i) NPN transistor and (ii) PNP transistor. Thus, a transistor is a three terminal device, namely the emitter, base and collector. The emitter is always kept in forward bias relative to the base, while the collector is kept in reverse bias relative to the base. The base-emitter junction thus offers a low resistance for the emitter current, while the base-collector junction offers a high resistance in the collector circuit. The base is made thinner than the emitter, while collector is wider than both the emitter and base. The emitter is heavily doped, base is lightly doped, while collector is moderately doped. The emitter current I_E , base current I_B and collector current I_C are related as $I_E = I_B + I_C$.

8.1. Different Configurations of a Transistor

While connecting a transistor in an electric circuit, we need four terminals – two for the input circuit and two for the output circuit. But there are only three terminals namely emitter, base and collector, in a transistor. Hence one of the three terminals emitter (E), base (B) or collector (C) is earthed and is kept common in both the input and output circuits. Thus, one terminal of the transistor is kept common to both the input and output circuits. In this way, there are the following three modes of connecting a transistor in an electric circuit :

- (i) **Common base (CB) mode** in which the base is kept common to both the input and output circuits.
- (ii) **Common emitter (CE) mode** in which the emitter is kept common to both the input and output circuits.
- (iii) **Common collector (CC) mode** in which the collector is kept common to both the input and output circuits.

The graphs plotted between different currents and voltages in each mode, are called the characteristic curves of a transistor. Here we shall study the three main characteristic curves in each mode : (a) input characteristic curve, (b) output characteristic curve, and (c) current transfer characteristic curve.

8.2. Characteristics of a Transistor in Common Base (CB) Mode

The electric circuit for the NPN transistor and PNP transistor in CB mode are shown in Fig. 8.1 (a) and (b) respectively. The emitter-base junction is in forward bias and the collector-base junction is in reverse bias. The emitter current I_E , voltage V_{EB} at the emitter-base junction, collector current I_C and the voltage V_{CB} at the collector-base junction, all the four quantities, are variable. The input signal is applied in the emitter circuit, therefore a graph plotted between the emitter current I_E and the emitter-base voltage V_{EB} , at a constant collector-base voltage V_{CB} is called the *input characteristic curve*. Similarly, the output signal is obtained in the collector circuit, therefore a graph

plotted between the collector current I_C and the collector-base voltage V_{CB} , keeping the emitter current I_E constant, is called the *output characteristic curve*.

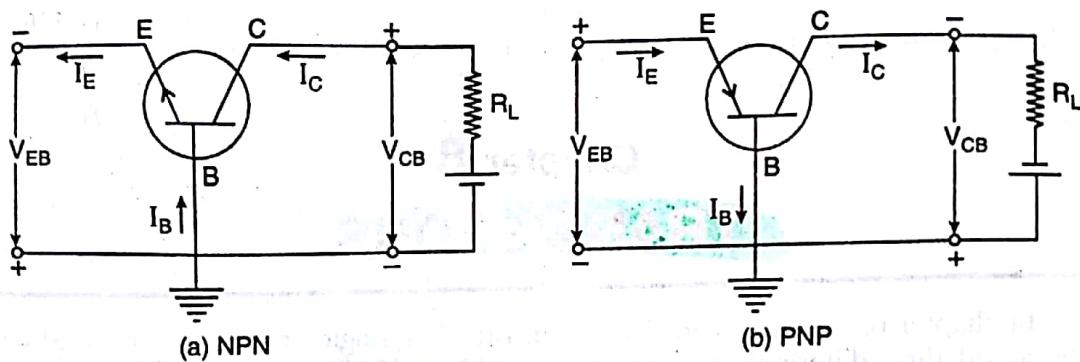


Fig. 8.1. CB mode

Fig. 8.2 (a) and (b) respectively represent the electric circuits for the NPN and PNP transistors in CB mode, required to draw the characteristic curves. A voltage V_{EB} is applied between the emitter E and the base B through a battery B_1 and a rheostat Rh_1 . This voltage is read with the voltmeter V_1 . The emitter current I_E can be changed

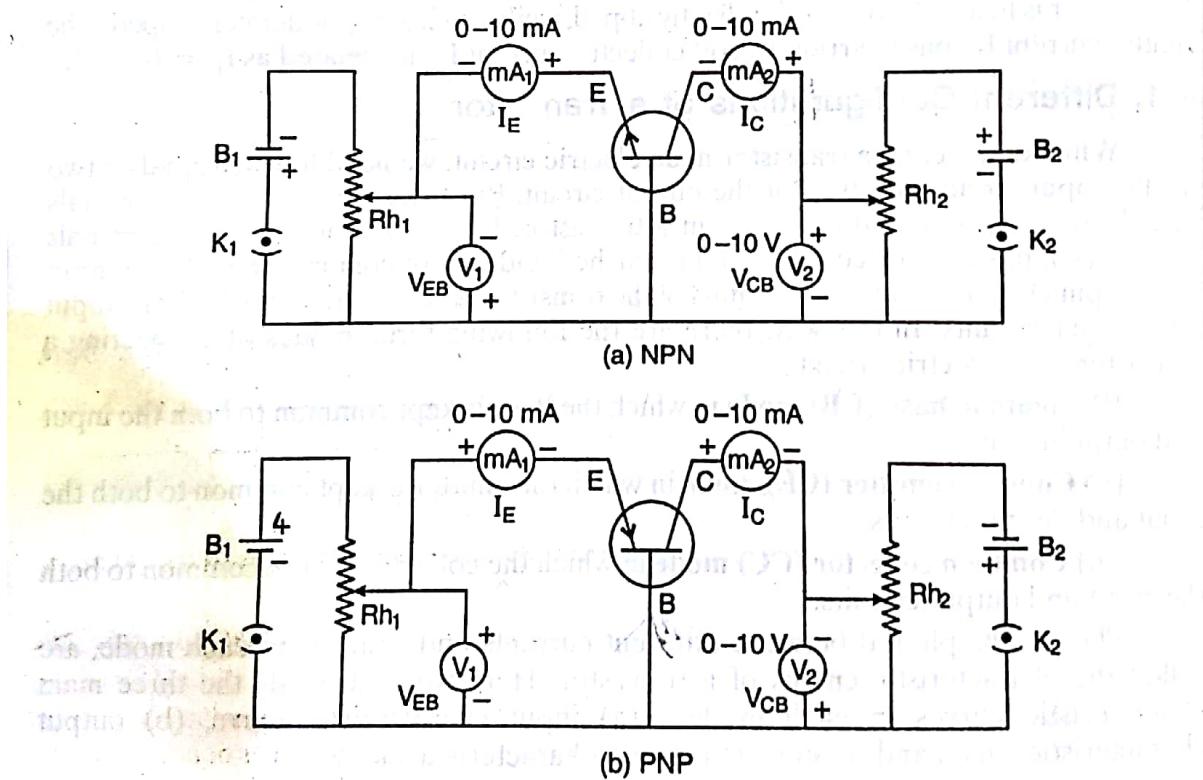


Fig. 8.2. Electric circuit to draw characteristic curves in CB mode

with the rheostat Rh_1 and its value is read with the milli-ammeter mA_1 . A voltage V_{CB} is applied between the collector C and the base B by using the battery B_2 as a potential divider with the help of rheostat Rh_2 . This voltage is read with the voltmeter V_2 and the collector current I_C is read with the milli-ammeter mA_2 .

(1) **Input characteristics**—For this characteristics, the collector-base voltage V_{CB} is kept constant and the emitter current I_E is changed with the help of rheostat Rh_1 and corresponding to each value of emitter current, the emitter-base voltage V_{EB}

is read with the voltmeter V_1 . Then a graph is plotted for the emitter current I_E versus the emitter-base voltage V_{EB} . The experiment is repeated for different constant collector-base voltages V_{CB} . Fig. 8.3. shows the input characteristic curves. Since the emitter-base junction is in forward bias, these characteristic curves are similar to those of P-N junction diode in the forward bias. From the characteristic curves, we note that the emitter current I_E increases rapidly with the small increase in emitter-base voltage V_{EB} .

The slope of input characteristic curve is equal to the reciprocal of *input dynamic resistance*.

Thus, input dynamic resistance

$$R_{in} = \frac{\Delta V_{EB}}{\Delta I_E} \text{ (when } V_{CB} \text{ is constant)} \quad \dots(8.1)$$

Its value is of the order of 20 ohm to 50 ohm.

(2) Output characteristics – For this characteristics, the emitter current I_E is kept constant and the collector-base voltage V_{CB} is varied with the help of the rheostat R_{h2} . Corresponding to each value of V_{CB} , the collector current I_C is read with the milli-ammeter mA_2 . Then a graph is plotted for the collector current I_C versus collector-base voltage V_{CB} . The experiment is repeated for different values of emitter current I_E . Fig. 8.4 shows the output characteristics. From these curves we note that

(i) The collector current I_C varies with the collector-base voltage V_{CB} only at a very low voltage (below 1 volt).

(ii) When the collector-base voltage is raised above 1 volt, the collector current I_C is nearly independent of the collector-base voltage V_{CB} . This region is nearly a straight line parallel to the V_{CB} axis. The slope of the curve in this region is equal to the reciprocal of the *output dynamic resistance*.

Thus, output dynamic resistance

$$R_{out} = \frac{\Delta V_{CB}}{\Delta I_C} \text{ (when } I_E \text{ is constant)} \quad \dots(8.2)$$

Since for a constant value of emitter current I_E , there is a very small change in collector current I_C for a very large change in collector-base voltage V_{CB} , therefore the output dynamic resistance in this mode is very large ($\approx 1.0 M\Omega$).

A transistor is commonly used as an amplifier in this region.

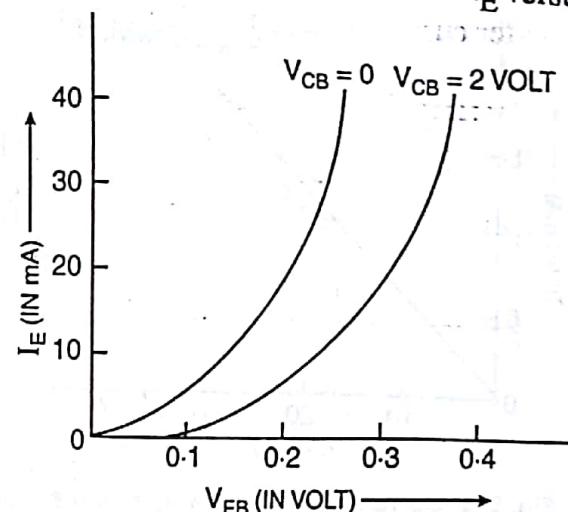


Fig. 8.3. Input characteristics in CB mode

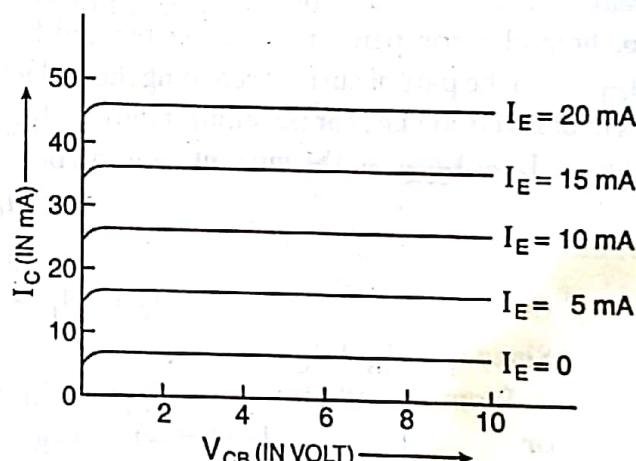


Fig. 8.4. Output characteristics in CB mode

(3) Current transfer characteristics— Keeping the collector-base voltage V_{CB} constant, a graph plotted between the emitter current I_E and the corresponding collector current I_C is called the current transfer characteristics, which is a straight line as shown in Fig. 8·5. The slope of this straight line is called the *current gain* in the common base mode.

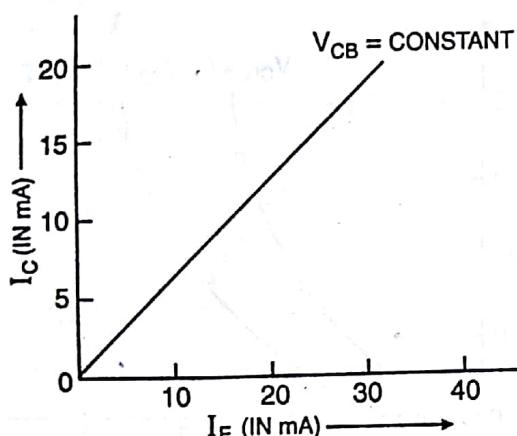


Fig. 8·5. Current transfer characteristics in CB mode

Thus, current gain in CB mode

$$\alpha = \left(\frac{\Delta I_C}{\Delta I_E} \right)_{V_{CB}} \quad \dots (8.3)$$

Its value is of the order of 0·98.

Relationship for the collector current—In the common base mode, the base current I_B is the input current and the collector current I_C is the output current.

$$\text{Since } I_E = I_B + I_C \quad \therefore \quad I_C = I_E - I_B$$

When the emitter is in open circuit and the collector-base junction is in reverse bias condition, a small collector current ($\approx \mu A$) exists which is called the *collector-base leakage current* and is represented as I_{CBO} . This current arises due to thermal generation of hole-electron pairs in the collector and base regions. Thus I_C must be the sum of I_{CBO} and the part of current reaching the collector from the emitter current when emitter is in close circuit i.e., for the emitter current I_E , the part of current reaching the collector will be $I_C - I_{CBO}$, so the current gain will be

$$\alpha = \frac{I_C - I_{CBO}}{I_E}$$

or

$$I_C = \alpha I_E + I_{CBO} \quad \dots (8.4)$$

$$\text{Since } I_E = I_B + I_C$$

∴ From eqn. (8.4),

$$I_C = \alpha (I_B + I_C) + I_{CBO}$$

or

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

or

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CBO} \quad \dots (8.5)$$

8·3. Characteristics of a Transistor in Common Emitter (CE) Mode

The electric circuits for the NPN and PNP transistors in the CE mode are shown in Fig. 8·6 (a) and (b) respectively in which emitter is kept in the forward bias and collector in the reverse bias.

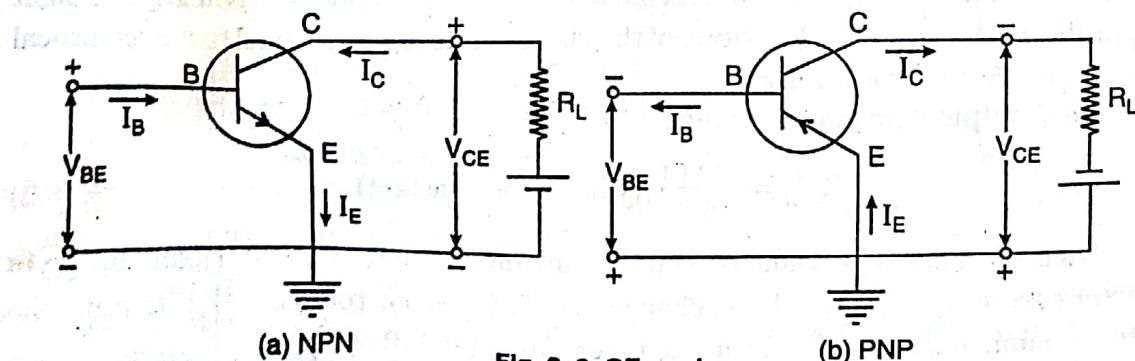
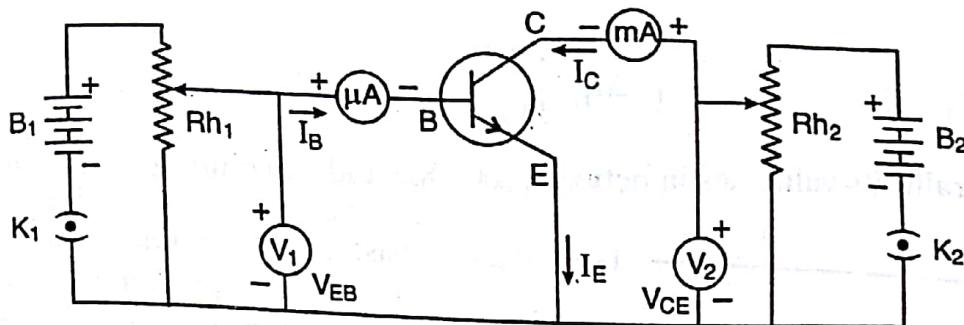
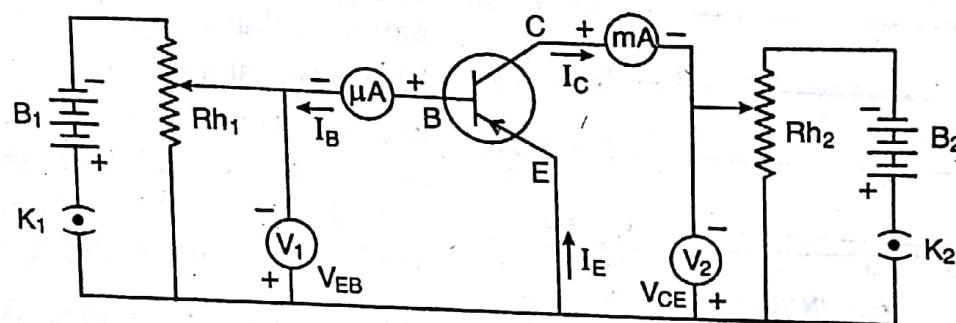


Fig. 8·6. CE mode

Obviously, the base current I_B and the emitter-base voltage V_{EB} are in the input circuit. Hence, a graph plotted between the base current I_B and the emitter-base voltage V_{EB} , keeping the collector-emitter voltage V_{CE} constant, is called the *input characteristic*



(a) NPN



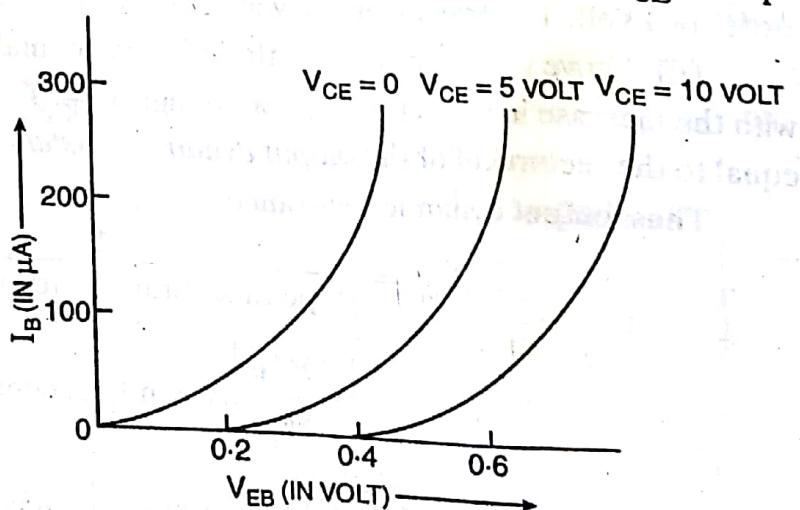
(b) PNP

Fig. 8.7. Electric circuit for characteristic curves in CE mode

curve. Similarly, the collector current I_C and the collector-emitter voltage V_{CE} are in the output circuit, therefore a graph plotted between the collector current I_C and the collector-emitter voltage V_{CE} at a constant base current I_B is called the *output characteristics*. Fig. 8.7 (a) and (b) show respectively the electric circuit diagrams for drawing the characteristic curves of a NPN and PNP transistors in CE mode.

(1) Input characteristics

— For this, the collector-emitter voltage V_{CE} is kept constant and the emitter-base voltage V_{EB} is varied with the help of rheostat R_{h1} and corresponding to each voltage V_{EB} , the corresponding base current I_B is read with the help of micro-ammeter. Then a graph is plotted for the base current I_B versus the emitter-base voltage V_{EB} . The experiment is repeated for the different constant collector-emitter voltage V_{CE} . Fig. 8.8 represents the input characteristics. These curves

**Fig. 8.8. Input characteristics in CE mode**

are identical to those of a P-N junction diode in the forward bias. It may be noted that the increase in base current I_B with increase in emitter-base voltage V_{EB} is less rapid. The slope of the linear part of this curve is equal to the reciprocal of the *input dynamic resistance*.

Thus, input dynamic resistance

$$R_{in} = \frac{1}{\text{Slope of the input characteristic curve}}$$

$$= \left(\frac{\Delta V_{BE}}{\Delta I_B} \right)_{V_{CE}} \quad \dots(8.6)$$

Generally, its value lies in between 200 ohm and 800 ohm (which is quite large as compared to the input dynamic resistance of common base mode).

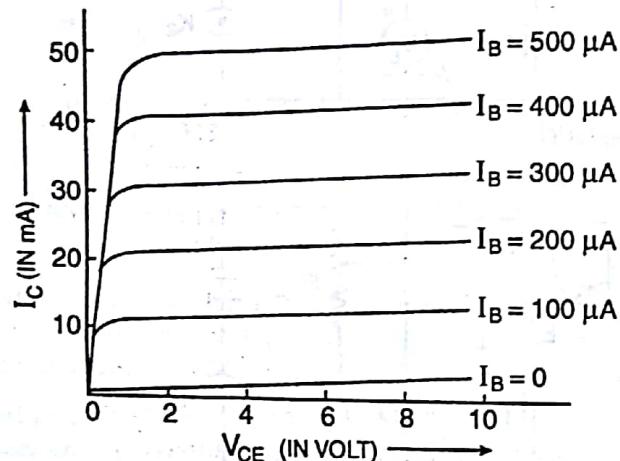


Fig. 8.9 Output characteristics in CE mode

values of base current I_B . Fig. 8.9 shows the output characteristic curves.

From these curves we note that

- (i) For a given constant base current I_B , the collector current I_C varies with the collector-emitter voltage V_{CE} only upto 1 volt, after which the collector current I_C almost becomes constant and independent of collector-emitter voltage V_{CE} . The value of V_{CE} at which I_C becomes nearly constant is called the *knee voltage* (V_{knee}) which is of the order of 1 volt. The transistor is always operated in CE mode above the knee voltage.
- (ii) Above the knee voltage, there is a very small increase in collector current I_C with the increase in collector-emitter voltage V_{CE} . The slope of this part of the curve is equal to the reciprocal of the *output dynamic resistance*.

Thus, output dynamic resistance

$$R_{out} = \frac{1}{\text{slope of saturated part of the curve}}$$

$$= \left| \frac{\Delta V_{CE}}{\Delta I_C} \right| \text{ when } I_B \text{ is constant} \quad \dots(8.7)$$

Its value is of the order of 20 kilo-ohm (which is very small in comparison to that in CB mode).

- (iii) At a given collector-emitter voltage V_{CE} , more the base current I_B , more is the collector current I_C .

(3) Current transfer characteristics—Keeping the collector-emitter voltage V_{CE} constant, a graph plotted between the base current I_B and the corresponding

collector current I_C is called the current transfer characteristics which is a straight line as shown in Fig. 8.10. The slope of the line is called the *current gain* in CE mode.

Thus, current gain in CE mode

$$\beta = \left\{ \frac{\Delta I_C}{\Delta I_B} \right\}_{V_{CE}} \quad \dots(8.8)$$

Its value is nearly 49, which is very large as compared to the current gain α in the common base mode. This is why while using a transistor as an amplifier, CE mode is preferred over the CB mode.

Relationship for the collector current : In the common emitter mode, the base current I_B is the input current and the collector current I_C is the output current.

$$\text{Since } I_E = I_B + I_C \therefore I_C = I_E - I_B$$

When the base is in open circuit and the collector-emitter junction is in reverse bias condition, a small collector current flows which is called the *collector-emitter leakage current* and is represented as I_{CEO} . This current is larger than the collector-base leakage current I_{CBO} . Thus, when the base is in close circuit, the current I_C is the sum of I_{CEO} and the part of current reaching the collector from the emitter current I_E i.e., for the emitter current I_E , the part of current reaching the collector will be $I_C - I_{CEO}$. Then current gain in CE mode will be

$$\beta = \frac{I_C - I_{CEO}}{I_B}$$

$$I_C = \beta I_B + I_{CEO} \quad \dots(8.9)$$

8.4 Characteristics of a Transistor in Common Collector (CC) Mode

The electric circuits for the NPN and PNP transistors in the common collector mode are shown in Fig. 8.11 (a) and (b) in which emitter is kept in forward bias and collector in reverse bias. It is clear that the base current I_B and the base-collector voltage V_{BC} are in the input circuit, hence keeping the emitter-collector voltage V_{EC} constant,

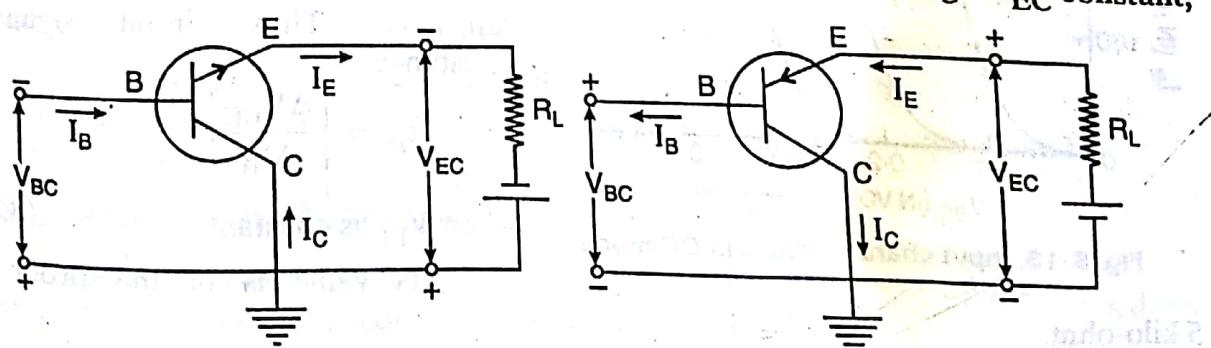


Fig. 8.11. Common collector (CC) mode

a graph plotted between the base current I_B and the base-collector voltage V_{BC} is called the *input characteristic curve*. Similarly, the emitter current I_E and the emitter-collector voltage V_{EC} are in the output circuit, therefore, at a constant base current I_B , a graph plotted between the emitter current I_E and the emitter-collector voltage V_{EC} , is called the *output characteristic curve*.

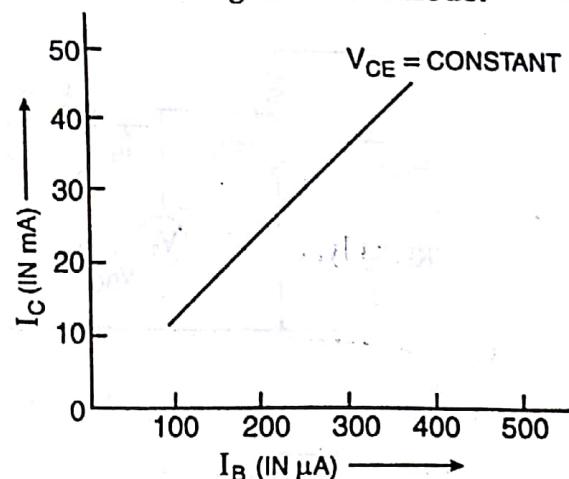


Fig. 8.10. Current transfer characteristics in CE mode

Fig. 8.12 (a) and (b) respectively show the electric circuit diagrams for drawing the characteristic curves of a NPN and PNP transistors in CC mode.

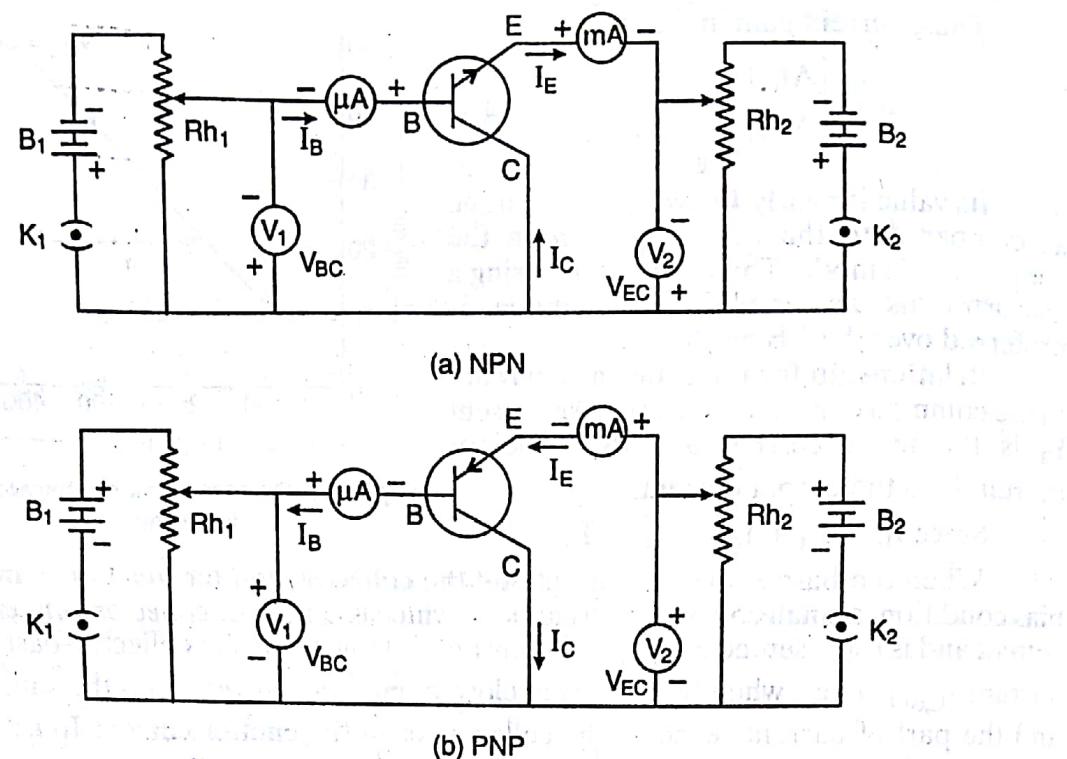


Fig. 8.12. Electric circuit for characteristics curves in CC mode

(1) Input characteristics—For this, a graph is plotted for the base current I_B versus the base-collector voltage V_{BC} , keeping the emitter-collector voltage V_{EC} constant.

The input characteristic curves are shown in Fig. 8.13 in which the base current becomes saturated at a small base voltage. Thus, these characteristic curves are similar to those of a P-N junction diode in the reverse bias. The slope of this curve is equal to the reciprocal of the *input dynamic resistance*. Thus, input dynamic resistance

$$R_{in} = \left| \frac{\Delta V_{BC}}{\Delta I_B} \right|$$

when V_{EC} is constant ... (8.10)

Its value is of the order of

5 kilo-ohm.

(2) Output characteristics—For this, keeping the base current I_B constant at a particular value, the emitter-collector voltage V_{EC} is changed and corresponding to each value of V_{EC} , the emitter current I_E is read. Then a graph is plotted between the emitter current I_E and the emitter-collector voltage V_{EC} . The experiment is repeated for different values of base current I_B . The output characteristic curves are shown in Fig. 8.14 which are similar to the output characteristic curves obtained in common

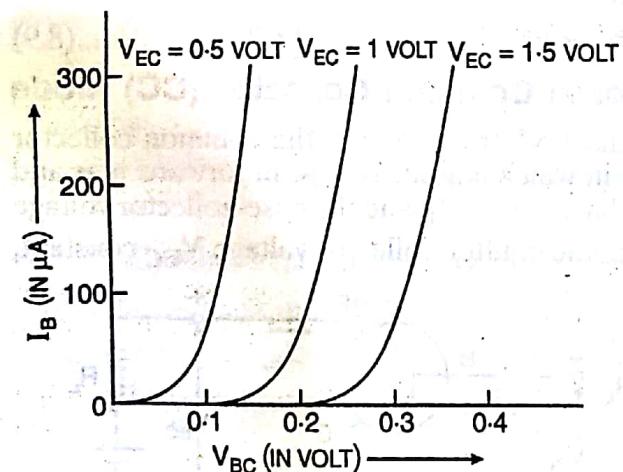


Fig. 8.13. Input characteristics in CC mode

emitter mode. From these curves we note that for a given base current I_B , the emitter current I_E increases with the increase in emitter-collector voltage V_{EC} only upto 1 volt and then becomes almost constant. The slope of the curve in the initial part when the emitter current increases with increase in emitter-collector voltage, is equal to the reciprocal of output dynamic resistance.

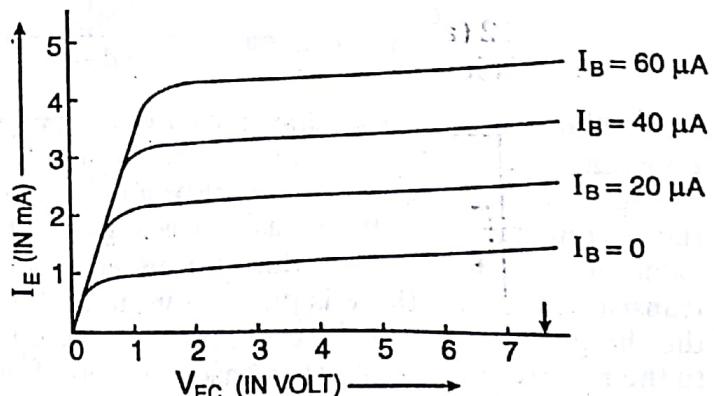


Fig. 8.14. Output characteristics in CC mode

Thus, output dynamic resistance

$$R_{out} = \left| \frac{\Delta V_{EC}}{\Delta I_E} \right| \quad \dots(8.11)$$

when I_B is constant. Obviously, it is very small.

(3) Current transfer characteristics : Keeping the emitter-collector voltage V_{EC} constant, a graph plotted between the base current I_B and emitter current I_E is called the current transfer characteristics which is a straight line as shown in Fig. 8.15. The slope of this line is called the *current gain* in the common collector mode.

Thus, current gain in common collector mode

$$\gamma = \left| \frac{\Delta I_E}{\Delta I_B} \right| \text{ when } V_{EC} \text{ is constant} \quad \dots(8.12)$$

Its value is nearly 50 (which is nearly equal to the current gain in the common emitter mode).

It is also clear that in this mode, any variation in the output circuit (emitter) depends on the variation that occurs in the input circuit (base), hence we can say that the emitter is the follower of the base. Due to this property, the transistor used in common collector mode is also called the *emitter follower*.

Relationship for the emitter current : In the common collector mode, the input current is I_B and the output current is I_E where $I_E = I_C + I_B$... (8.13)

8.5. Current Amplification Factors

Depending upon the different modes of use of transistor, there are following three current amplification factors of a transistor :

- (i) current gain in common base mode α ,
- (ii) current gain in common emitter mode β , and
- (iii) current gain in common collector mode γ .

(i) **Current gain in common base mode α** — In the common base mode, at constant collector-base voltage, the ratio of change in collector current I_C to the corresponding change in emitter current I_E is called the *current gain* α . If the change in collector current is ΔI_C due to change in emitter current ΔI_E , keeping the collector-base voltage V_{CB} constant, then

$\alpha = \frac{\Delta I_C}{\Delta I_E}$... (8.14)

$\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_C}{\Delta I_B + \Delta I_E} = \frac{\Delta I_C}{\Delta I_B}$... (8.15)

$\alpha = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_B}$... (8.16)

$\alpha = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_B}$... (8.17)

$$\text{Current gain } \alpha = \left(\frac{\Delta I_C}{\Delta I_E} \right) \text{ when } V_{CB} \text{ is constant} \quad \dots(8.14)$$

Since some of the charge carriers coming in the base region from the emitter combine with the majority charge carriers present in the base region, therefore, the change in collector current is slightly smaller than the change in emitter current. Thus, the current gain α of the transistor is slightly smaller than 1 (≈ 0.95 to 0.995). If the value of α is less than 1, it does not mean that there is no power amplification by the transistor. Actually there is power amplification by the transistor, since in a transistor, the charge carriers move from the forward biased emitter-base junction of low resistance to the reverse biased collector-base junction of high resistance.

It may be mentioned here that the current amplification factor α is a constant. It has no unit.

(ii) **Current gain in common emitter mode β** —In a common emitter mode, the ratio of change in collector current I_C to the change in base current I_B , keeping the collector-emitter voltage V_{CE} constant, is called the current gain β . If at a constant collector-emitter voltage V_{CE} , the change in collector current is ΔI_C due to change in base current ΔI_B , then

$$\text{Current gain } \beta = \left(\frac{\Delta I_C}{\Delta I_B} \right) \text{ when } V_{CE} \text{ is constant} \quad \dots(8.15)$$

It also has no unit. Its value lies between 20 to 150.

(iii) **Current gain in common collector mode γ** —In a common collector mode, the ratio of change in emitter current I_E to the change in base current I_B , keeping the emitter-collector voltage V_{EC} constant, is called the current gain γ . If at a constant value of V_{EC} , the change in emitter current is ΔI_E due to change in base current ΔI_B , then

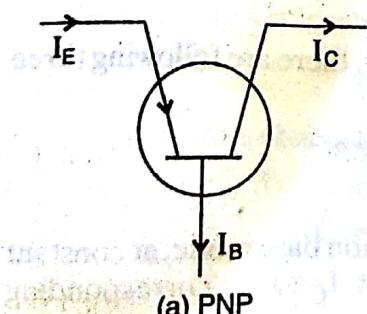
$$\text{Current gain } \gamma = \left(\frac{\Delta I_E}{\Delta I_B} \right) \text{ when } V_{EC} \text{ is constant} \quad \dots(8.16)$$

It also has no unit. Its value is nearly equal to that of β .

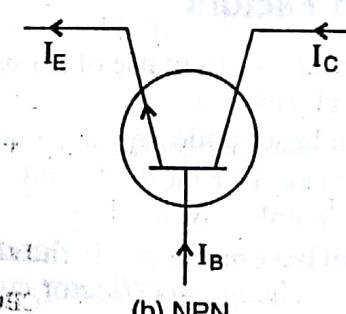
8.6. Relationship Between the Current Gains of a Transistor in Various Configurations

Relationship between α and β —We have read that as shown in Fig. 8.16, the emitter current I_E , the base current I_B and the collector current I_C are related as

$$\begin{aligned} I_E &= I_C + I_B \\ \text{or} \quad \Delta I_E &= \Delta I_C + \Delta I_B \quad \text{or} \quad \Delta I_B = \Delta I_E - \Delta I_C \end{aligned} \quad \dots(8.17)$$



(a) PNP



(b) NPN

$$\text{But } \beta = \frac{\Delta I_C}{\Delta I_B}$$

Substituting the value of ΔI_B from eqn. (8.17),

$$\begin{aligned} \beta &= \frac{\Delta I_C}{\Delta I_E - \Delta I_C} \\ &= \frac{\Delta I_C / \Delta I_E}{1 - (\Delta I_C / \Delta I_E)} \end{aligned}$$

Fig. 8.16. Direction of currents in PNP and NPN transistors

$$\text{But } \alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$\therefore \beta = \frac{\alpha}{1-\alpha} \quad \dots(8.18)$$

Thus, if the current gain in common base mode is $\alpha = 0.98$, the current gain in common emitter mode will be

$$\beta = \frac{0.98}{1-0.98} = 49$$

Relationship between α and γ — From Fig. 8.16, $I_E = I_C + I_B$

or

$$\Delta I_E = \Delta I_C + \Delta I_B \quad \text{or} \quad \Delta I_B = \Delta I_E - \Delta I_C$$

Hence

$$\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} = \frac{1}{1 - (\Delta I_C / \Delta I_E)}$$

$$\text{But } \frac{\Delta I_C}{\Delta I_E} = \alpha$$

$$\therefore \gamma = \frac{1}{1-\alpha} \quad \dots(8.19)$$

If the current gain in common base mode α is 0.98, the current gain in the common collector mode will be

$$\gamma = \frac{1}{1-0.98} = \frac{1}{0.02} = 50$$

Relationship between β and γ — From Fig. 8.16, $I_E = I_C + I_B$

$$\Delta I_E = \Delta I_C + \Delta I_B$$

Hence

$$\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_C + \Delta I_B}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_B} + 1 = \beta + 1 \quad \dots(8.20)$$

If the current gain in common emitter mode is $\beta = 49$, the current gain in the common collector mode will be $\gamma = 49 + 1 = 50$.

Relationship between the collector-emitter leakage current I_{CEO} and collector-base leakage current I_{CBO}

In CB mode : From eqn. (8.4),

$$I_C = \alpha I_E + I_{CBO}$$

and from eqn. (8.5),

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$\text{But } \beta = \frac{\alpha}{1-\alpha}$$

$$\therefore I_C = \beta I_B + (\beta + 1) I_{CBO} \quad \dots(8.21)$$

In CE mode : From eqn. (8.9),

$$I_C = \beta I_B + I_{CEO}$$

$$I_{CEO} = (\beta + 1) I_{CBO} \quad \dots(8.22)$$

or

$$I_{CEO} = \frac{1}{(1-\alpha)} I_{CBO} \quad \dots(8.23)$$

8.7 Voltage Gain and Power Gain of a Transistor in Different Configurations

Voltage gain – The voltage gain in a mode is the ratio of change in output voltage across the load to the change in input voltage. Thus,

Voltage gain in common base mode

$$A_v = \frac{\Delta I_C \times R_L}{\Delta I_E \times R_{in}} = \alpha \times \frac{R_L}{R_{in}}$$

Voltage gain in common emitter mode

$$A_v = \frac{\Delta I_C \times R_L}{\Delta I_B \times R_{in}} = \beta \times \frac{R_L}{R_{in}}$$

and voltage gain in common collector mode

$$A_v = \frac{\Delta I_E \times R_L}{\Delta I_B \times R_{in}} = \gamma \times \frac{R_L}{R_{in}}$$

Power gain – The power gain in a mode is the product of voltage gain and current gain in that mode. Thus,

Power gain in the common base mode

$$A_p = \alpha \times A_v = \alpha^2 \times \frac{R_L}{R_{in}}$$

Power gain in the common emitter mode

$$A_p = \beta \times A_v = \beta^2 \times \frac{R_L}{R_{in}}$$

Power gain in the common collector mode

$$A_p = \gamma \times A_v = \gamma^2 \times \frac{R_L}{R_{in}}$$

8.8. Comparison of Properties of a Transistor in Different Configurations

The table below gives a comparison of properties of a transistor in the different modes.

Properties of a transistor in different modes

Property	CB mode	CE mode	CC mode
1. Input resistance R_{in}	Very small ($\approx 50 \Omega$)	Large (≈ 200 to 800Ω)	Very large ($\approx 5 k\Omega$)
2. Output resistance R_{out}	Very large ($10^6 \Omega$)	Large ($\approx 20 k\Omega$)	Very small ($\approx 20 \Omega$)
3. Current gain	Less than 1	Large (≈ 49)	Large (≈ 50)
4. Voltage gain	High ≈ 100	Very high $\approx 10^3$	Less than 1
5. Power gain	Medium	Very large	Medium

It may be mentioned here that while using the transistor as an amplifier, out of the three modes, it is generally used in the common emitter mode. This is because (i) the current gain in this mode is very large, (ii) the voltage and power gains are large, and (iii) the ratio of input impedance to the output impedance is nearly 50 which is quite appropriate for the multi-stage coupling.

On the other hand, in the common collector mode, the input resistance of a transistor is very high and its output resistance is very low. Hence a transistor is used for impedance matching in this mode.

8.9. Graphical Analysis of CE Configuration

We have read that in CE configuration, the emitter is grounded (or earthed) and the input is applied at the base-emitter junction, while the output is obtained at the collector-emitter junction. The base current I_B is the function of base-emitter voltage V_{BE} and collector-emitter voltage V_{CE} i.e., $I_B = f(V_{BE}, V_{CE})$, while the collector current I_C is the function of base current I_B and collector-emitter voltage V_{CE} i.e., $I_C = f(I_B, V_{CE})$. Thus, we get the graphs : (i) $I_B - V_{BE}$ graph at a constant V_{CE} and (ii) $I_C - V_{CE}$ graph at a constant I_B .

(i) $I_B - V_{BE}$ graph at a constant V_{CE} – The curves representing the variation of base current I_B with the base-emitter voltage V_{BE} at a constant collector-emitter voltage V_{CE} are called the *input characteristic curves* in CE configuration and they are shown in Fig. 8.17. When $V_{CE} = 0$, the emitter-base junction is forward biased, so the curve is like a junction diode in forward bias. As V_{CE} increases, the width of depletion layer at the collector-base junction will increase. As a consequence, the effective width of base will decrease, so the base current decreases. Further we note that a change in V_{CE} does not result in much deviation of the curves. The reciprocal of the slope of the curve at any point gives the input resistance of transistor at that point.

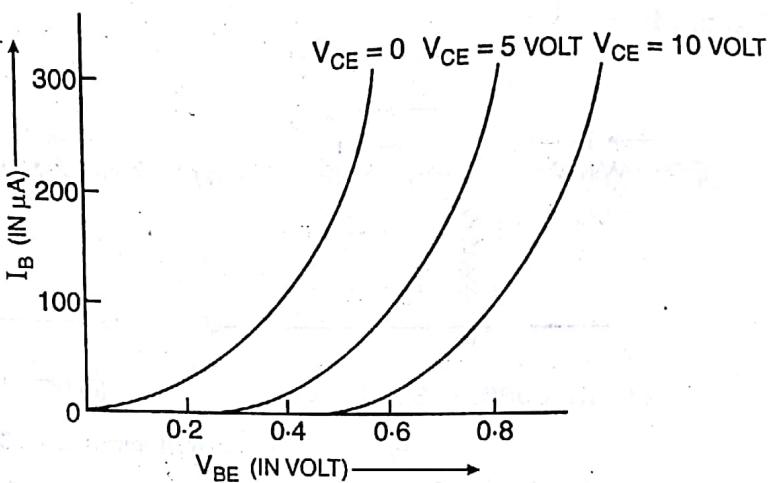


Fig. 8.17. $I_B - V_{BE}$ graphs in CE configuration

(ii) $I_C - V_{CE}$ graph at a constant I_B – The curves representing the variation of collector current I_C with the collector-emitter voltage V_{CE} at a constant base current I_B are called the *output characteristic curves* in CE configuration and they are shown in Fig. 8.18.

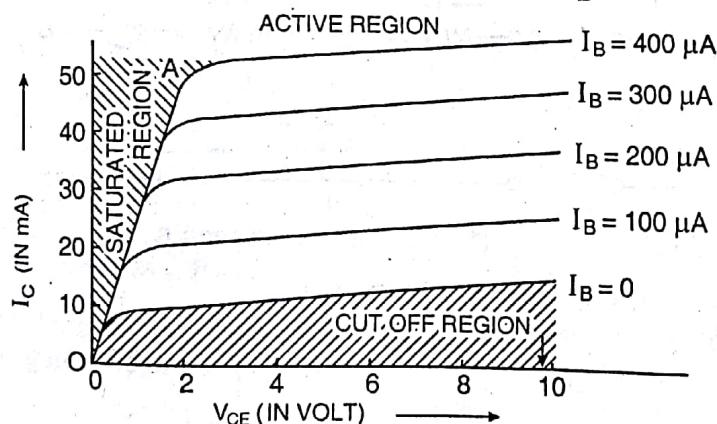


Fig. 8.18. $I_C - V_{CE}$ graphs in CE configuration

collector both are reverse biased, so it is considered as the off condition of the transistor.

(b) **Saturated region** : It is the region enclosed between the line OA and the current axis. In this region the emitter is forward biased and the collector is very small reverse biased. The collector is not able to collect the charge carriers coming from the emitter. In this region, the collector current I_C does not depend on the base current I_B .

(c) **Active region** : The central part in which the collector current I_C is nearly constant with increase in collector-emitter voltage V_{CE} is called the active region. In this

$$h_{rE} = \left(\frac{\partial V_B}{\partial V_C} \right)_{I_B} \quad \dots(8.45)$$

(c) **Forward current gain** – At constant collector potential V_C , the ratio of change in collector current to the corresponding change in base current, is called the forward current gain. i.e.,

$$h_{fE} = \left(\frac{\partial I_C}{\partial I_B} \right)_{V_C} \quad \dots(8.46)$$

(d) **Input impedance** – At constant collector voltage V_C , the ratio of change in base potential to the corresponding change in base current, is called the input impedance i.e.,

$$h_{iE} = \left(\frac{\partial V_B}{\partial I_B} \right)_{V_C} \quad \dots(8.47)$$

Importance of h Parameters

h parameters of a transistor determine its characteristics and are useful because of the following reasons :

- (i) h parameters are the real numbers at audible frequencies.
- (ii) The values of h parameters can be easily determined.
- (iii) h parameters are more useful for the circuit analysis and circuit construction.
- (iv) Input impedance, output impedance, current gain, voltage gain and power gain can easily be obtained with the help of these parameters.
- (v) Generally the manufacturer provides the values of h parameters of the transistor.

8.15. Use of Transistor as an Amplifier and Concept of Load Line

The process of magnifying the amplitude of an electric signal (voltage, current or power) is called the *amplification*. The device used to increase the magnitude of voltage, current or power is called the *amplifier*. A transistor can be used as an amplifier because in a transistor, the charge carriers move from the forward biased input circuit of low resistance to the reverse biased output circuit of high resistance and so by a small change in current in the input circuit, a large change in current is obtained in the output circuit. Thus, a transistor changes a weak signal into a strong signal and can be used as an amplifier.

A transistor is used as an amplifier mainly in CE configuration. Fig. 8.26 (a) shows a transistor used in CE configuration when no a.c. signal is applied in the input circuit and Fig. 8.26 (b) shows its output characteristic curves (i.e., the curves plotted between the collector current I_C versus collector-emitter voltage V_{CE} at constant base current I_B).

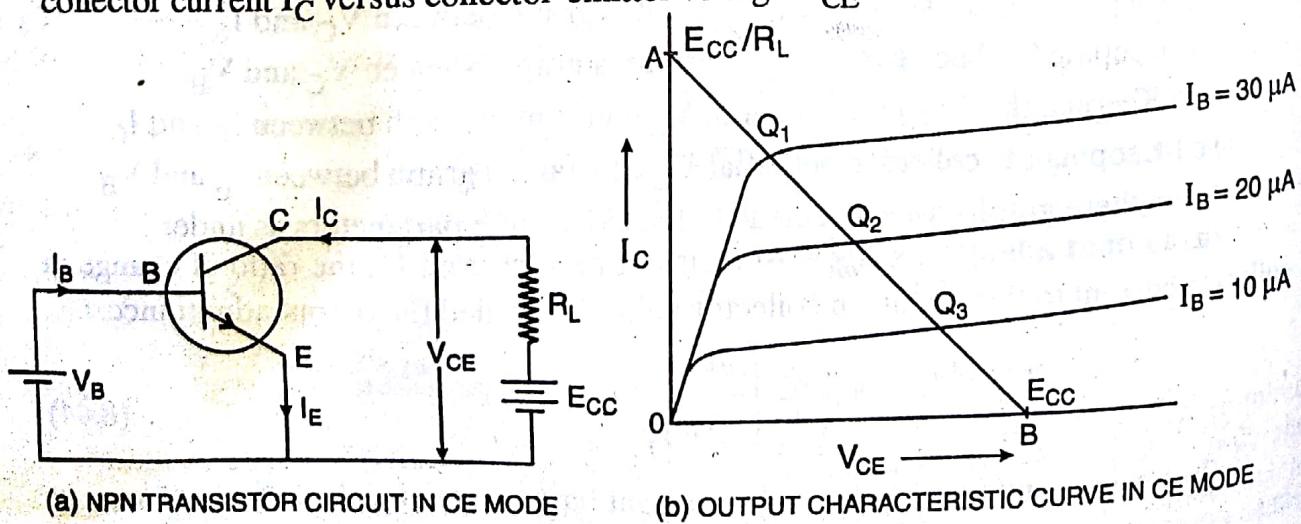


Fig. 8.26. NPN transistor in CE mode and its output characteristic curve

Let for the base current I_B , a current I_C flows through the load resistance R_L in the collector-emitter circuit. The value of I_C depends on the supply voltage E_{CC} , load resistance R_L and the voltage drop V_{CE} between the collector and emitter of the transistor.

From Fig. 8.26 (a), by Kirchhoff's voltage law

$$E_{CC} = I_C R_L + V_{CE}$$

or

$$I_C = \frac{E_{CC}}{R_L} - \frac{V_{CE}}{R_L} \quad \dots(8.48)$$

It is clear from eqn. (8.48) that a graph plotted between I_C and V_{CE} is a straight line of slope $= -1/R_L$ which has an intercept equal to E_{CC}/R_L on the I_C -axis (since on I_C -axis, $V_{CE} = 0$, $\therefore I_C = E_{CC}/R_L$) and an intercept equal to E_{CC} on the V_{CE} -axis (since on V_{CE} -axis, $I_C = 0$, $\therefore V_{CE} = E_{CC}$). This straight line is called the *load line*.

The points of intersection of the output characteristic curves and the load line are called the *operating points* Q_1, Q_2, Q_3, \dots as shown in Fig. 8.26 (b). In absence of the input signal, these points are called simply the Q points or the *quiescent points*. The selection of the Q point, at which the input signal is applied, depends on the value of the base current I_B .

SOLVED EXAMPLES

Ex. 1. The current gain of a transistor in the common base mode is 0.98. What will be the change in collector current if the change in emitter current is 5.0 mA? What will be the change in base current?

Sol. Given : $\alpha = 0.98$

But

$$\alpha = \left(\frac{\Delta I_C}{\Delta I_E} \right)$$

If $\Delta I_E = 5.0$ mA, then change in collector current

$$\Delta I_C = \alpha \Delta I_E = 0.98 \times 5.0 \text{ mA} = 4.9 \text{ mA}$$

$$\text{Now } I_E = I_C + I_B \quad \therefore \quad \Delta I_E = \Delta I_C + \Delta I_B$$

$$\text{Hence change in base current } \Delta I_B = \Delta I_E - \Delta I_C = 5.0 - 4.9 = 0.1 \text{ mA.}$$

Ex. 2. The current gain α of a transistor is 0.98. What will be its current gain in common emitter mode? In the CE mode, calculate the change in collector current and emitter current corresponding to a change in base current by 0.2 mA.

Sol. Current gain in CE mode is $\beta = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = \frac{0.98}{0.02} = 49$

But $\beta = \left(\frac{\Delta I_C}{\Delta I_B} \right)$. If $\Delta I_B = 0.2$ mA, then

$$\text{Change in the collector current } \Delta I_C = \beta \Delta I_B = 49 \times 0.2 \text{ mA} = 9.8 \text{ mA}$$

$$\text{Change in emitter current } \Delta I_E = \Delta I_C + \Delta I_B = 9.8 + 0.2 = 10 \text{ mA.}$$

Ex. 3. The current gain of a transistor in CB mode is 0.98. If the base current is 0.48 μ A, find the emitter current and the collector current. What will be the current gain in the common collector mode?

Chapter 9

FIELD EFFECT TRANSISTORS

9.1. Introduction

We have read that the current flow in a junction transistor is due to flow of both the electrons and holes. This is why a junction transistor is also called a bipolar junction transistor or BJT. There are two drawbacks in a junction transistor : (i) the internal resistance (or the input impedance) in CE mode is very small due to which base current is not negligible, (ii) the noise level is high. Both of these drawbacks are removed in the field effect transistor. *Field effect transistor (or FET) is that semi-conducting device in which output current is controlled by the electric field.* The current flow in FET is only due to the flow of one type of charge carriers (either electrons or holes). Hence, it is also called the *unipolar transistor*. Generally, two types of FET are used : (i) junction field effect transistor or JFET and (ii) metal oxide semiconductor field effect transistor or MOSFET. It is also called the insulated gate field effect transistor (IGFET).

9.2. Construction of JFET

The junction field effect transistor (JFET) is constructed in the following two ways :

(1) N channel JFET and (2) P channel JFET.

(1) **N channel JFET** : It consists of a thin bar of N type semiconductor with two junctions with the P type semiconductor near the centre, at opposite sides of the bar. Thus we get two P-N junctions on either side of the bar (Fig. 9.1). Both the P type

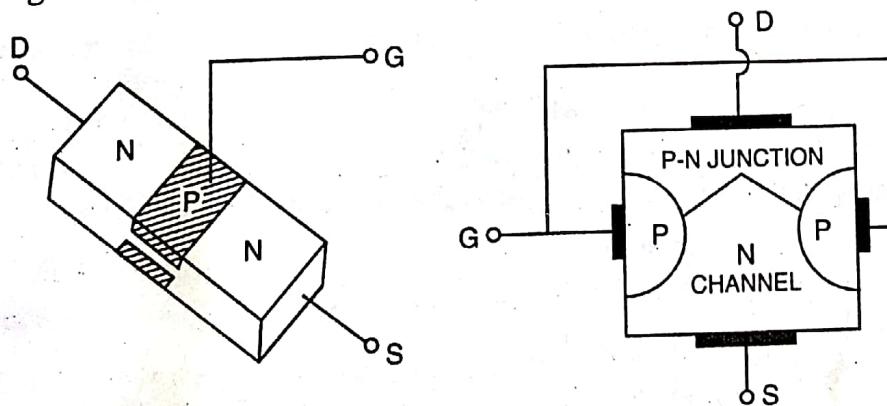


Fig. 9.1. N channel JFET

semiconductors are internally connected together (*i.e.*, both have the common one terminal). This terminal is called the *gate* and is represented by the letter G. When this terminal is given a potential, the P type semiconductors of both the junctions are at the same potential. The region between the two junctions is called the *channel*. The terminals from the either ends of the N type semiconductor are called the *source* and *drain* which are represented by the letters S and D respectively. When a potential difference is applied between the drain D and the source S, the majority charge carriers of N channel (*i.e.*, electrons) move in accordance with the applied potential. As a result, current flows through the channel.

(2) P channel JFET : It consists of a thin bar of P type semiconductor with two junctions with the N type semiconductor near the centre, at opposite faces of the bar. Thus we get two P-N junctions on either side of the bar (Fig. 9.2). Both the N type semiconductors are connected internally. The common terminal is called the *gate G*. The

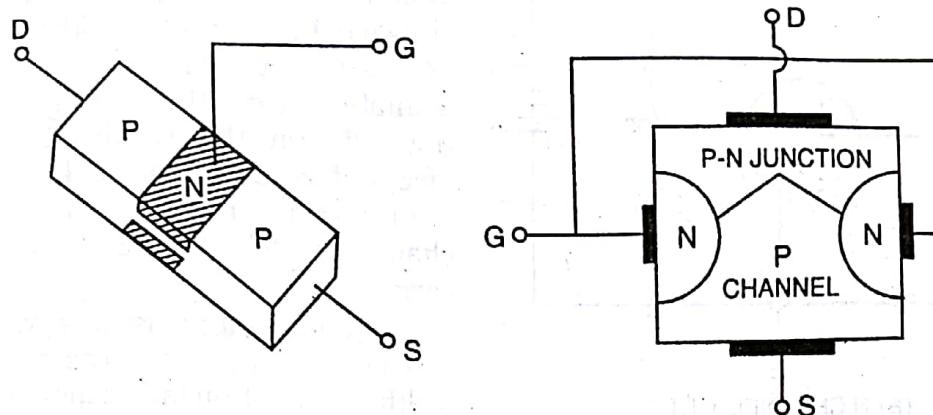


Fig. 9.2. P channel JFET

terminals extending out of the two ends of the P semiconductor are called the *source S* and *drain D*. When a potential difference is applied between the drain D and the source S, the majority charge carriers of P channel (*i.e.*, holes) move in accordance with the applied potential. As a result, the current flows through the channel.

Thus, there are three electrodes (or three terminals) in a JFET just like a transistor. They are : (i) source S, (ii) drain D and (iii) gate G.

(i) **Source S** — This is the terminal through which the majority charge carriers enter the channel region.

(ii) **Drain D** — This is the terminal through which the majority charge carriers exit from the channel region.

(iii) **Gate G** — This is the terminal which joins the impurity junctions on either side of the bar. In the N channel JFET, the gate is P type, while in a P channel JFET, the gate is N type.

Fig. 9.3 shows the symbols for the N channel and P channel JFET. To distinguish between them, an arrow is marked on the gate terminal which represents the direction of gate current, when the gate-source junction is in forward bias. In the N channel JFET, the arrow is from gate towards the channel (since the gate is P type), while in the P channel JFET, the arrow is from channel towards the gate (since the gate is N type). It may be mentioned here that in actual circuits the gate-source junction is kept in reverse bias, so actually there is no gate current.

9.3. Operation of JFET

Fig. 9.4 (a) and (b) show respectively the circuit diagrams for the N channel JFET and P channel JFET in which V_{GS} and V_{DS} are respectively the gate voltage and drain voltage applied by means of voltage sources X and Y.

Initially, when no potential difference is applied between the drain and source or gate and source, depletion layers are formed at the P-N junctions. Now if a potential difference V_{DS} is applied between the source and the drain by means of the source Y,

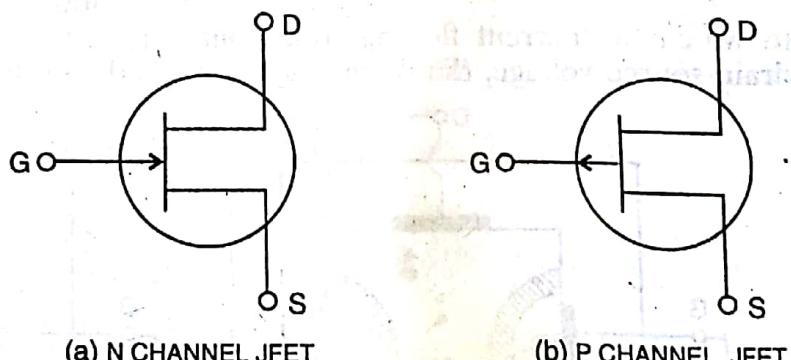


Fig. 9.3. Symbols of N channel and P channel JFET

while the gate is kept at zero potential, then the charge carriers (electrons in N channel and holes in P channel) begin to flow from the source to drain through the channel between the depletion layers as shown in Fig. 9·5. The width (or the area of cross-section) of the channel available for the charge carriers depends on the width of depletion layers. Obviously, more the width of depletion layers, less is the width of channel available for the motion of charge carriers.

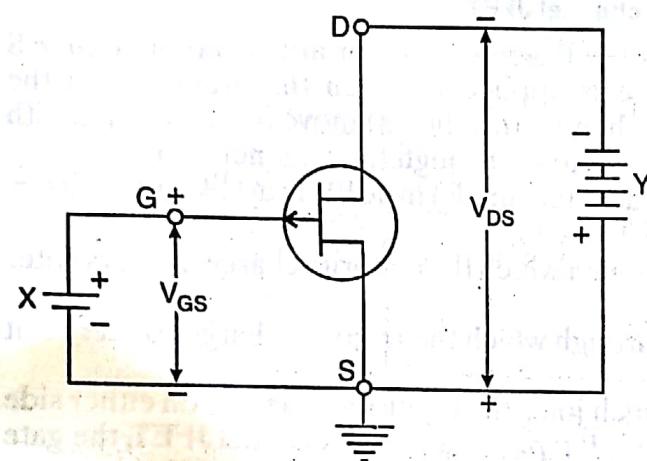
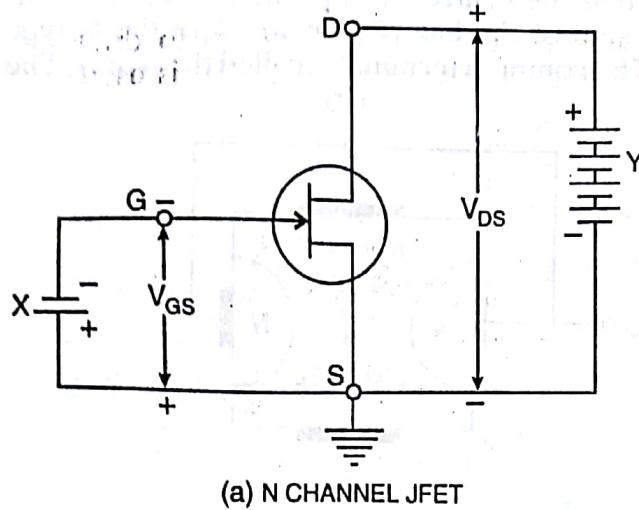


Fig. 9·4. Electric circuits for N channel and P channel JFET's

to which the current flowing from source to drain increases. Thus for a constant drain-source voltage, the drain current depends on the gate-source voltage. In other

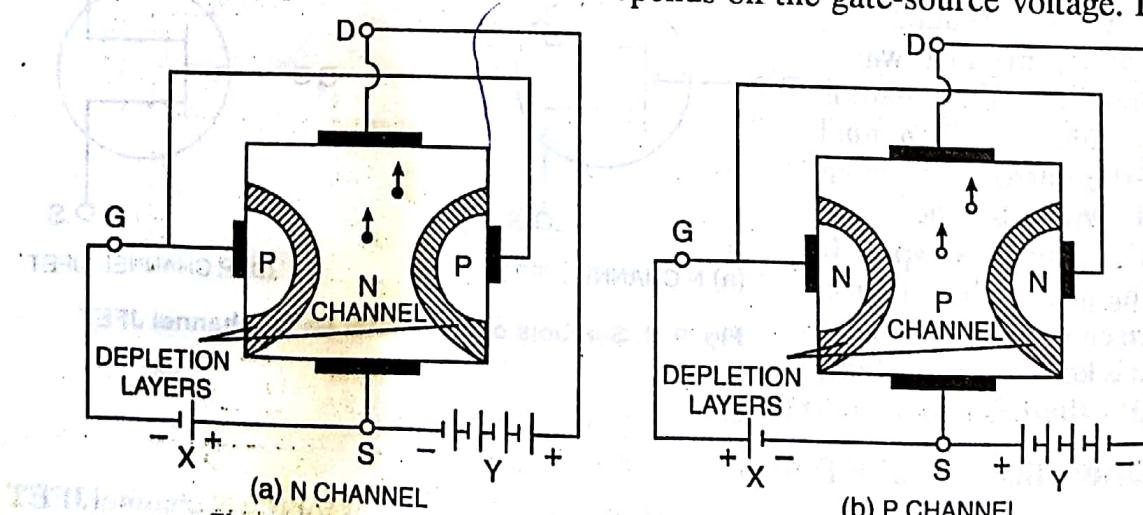


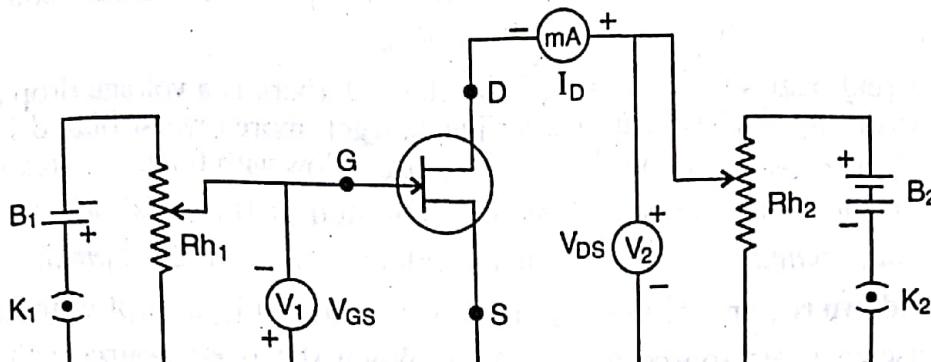
Fig. 9·5. Formation of depletion layers in N and P channel JFET's

words, the voltage applied on the gate controls the drain current. Obviously, since the gate-source is in reverse bias, therefore the current drawn by the gate is very low, i.e., the input resistance of the JFET between the gate and source is very high.

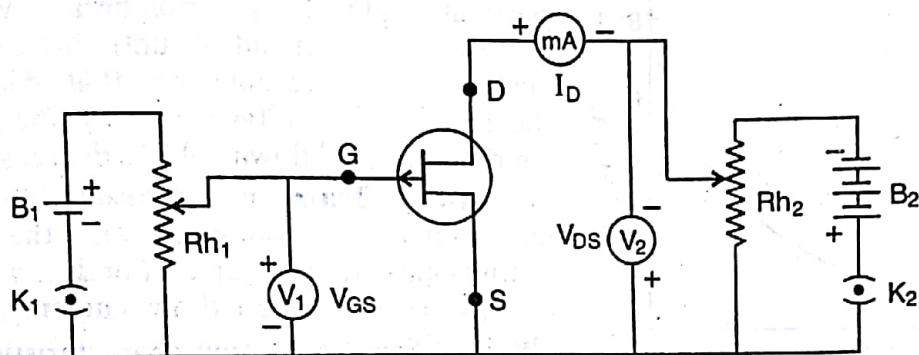
Thus the voltage applied at the gate (i.e., electric field) controls the drain current. This is why it is called the *field effect transistor*.

9.4. Characteristic (Volt-Ampere) Curves of JFET

Fig. 9.6 (a) and 9.6 (b) show respectively the circuit diagrams to draw the characteristics of N channel and P channel JFET's. Here the battery B_1 is used as a



(a) N CHANNEL



(b) P CHANNEL

Fig. 9.6. Circuit diagrams for N and P channel JFET's to draw the characteristic curves

potential divider with the help of a rheostat Rh_1 to apply a voltage V_{GS} between the gate G and source S so as to keep the gate G reverse biased. The voltage V_{GS} can be read by means of voltmeter V_1 . Similarly, the battery B_2 is used as a potential divider by means of a rheostat Rh_2 to apply a voltage V_{DS} between the drain D and source S. The voltage V_{DS} is read by means of voltmeter V_2 . The drain current I_D is read by means of milliammeter mA.

We can draw the following two characteristics curves of JFET.

- (i) Output characteristic curve, and
- (ii) Transfer characteristic curve.

(i) **Output characteristics**— Keeping the gate-source voltage V_{GS} constant, a graph plotted between the drain current I_D and drain-source voltage V_{DS} is called the output characteristics. It is as shown in Fig. 9.7. These curves can be divided in the following three regions : (a) ohmic or linear region, (b) saturated region and (c) breakdown region,

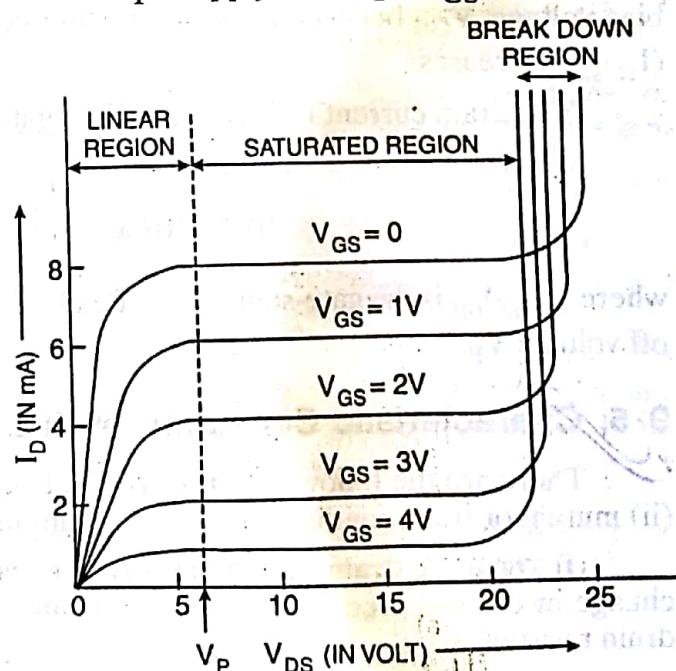


Fig. 9.7. Output characteristic of JFET

(a) **Ohmic or linear region**—When V_{DS} is very low, the drain current is directly proportional to the drain-source voltage (*i.e.*, $I_D \propto V_{DS}$). In this region, the channel bar behaves like an ohmic conductor.

(b) **Saturated region**—When the drain current I_D almost becomes constant and it does not depend on the drain-source voltage V_{DS} .

When current begins to flow through the channel, there is a voltage drop along the length of the bar, due to which the gate-source junction gets more reverse biased. Hence the effective area of cross-section of the channel decreases. Now with further increase in V_{DS} , when $V_{DS} = V_p$, the drain current I_D becomes saturated. In this condition, the channel is said to be in the *pinched off condition* and the voltage V_p is called the *pinch off voltage*.

(c) **Breakdown region**—In this region, the drain current I_D abruptly increases with a small increase in drain-source voltage V_{DS} . When the drain-source voltage V_{DS}

becomes large, with further increase in V_{DS} at a particular value, the junction breakdown occurs and the drain current abruptly increases. It is clear from the different curves that on increasing the reverse bias voltage between the gate and source, the breakdown voltage decreases.

(ii) **Transfer characteristics**—This characteristics is obtained with the help of output characteristic curves. For different values of V_{GS} , the saturated drain current $(I_D)_{sat}$ is obtained from the output characteristic curves. Then a graph is plotted between $(I_D)_{sat}$ and V_{GS} , which is called the transfer characteristics.

It is shown in Fig. 9·8. Obviously, as the reverse bias voltage V_{GS} between the gate and source increases, the saturated drain current $(I_D)_{sat}$ decreases.

The drain current I_D is related to the gate-source voltage V_{GS} as follows :

$$I_D = (I_D)_{sat} \times \left(1 - \frac{V_{GS}}{(V_{GS})_{off}}\right)^2 \quad \dots(9.1)$$

where $(V_{GS})_{off}$ is the gate-source cut off voltage which is numerically equal to the pinch off voltage V_p .

9·5. Characteristic Constants of JFET and Their Relationship

There are the following three constants of a JFET : (i) dynamic drain resistance, (ii) mutual or trans conductance and (iii) amplification factor.

(i) **Dynamic drain resistance**—At a constant gate-source potential, the ratio of change in drain-source potential to the change in drain current is called the dynamic drain resistance, *i.e.*,

$$r_d = \left(\frac{\Delta V_{DS}}{\Delta I_D} \right)_{V_{GS}} \quad \dots(9.2)$$

Its unit is ohm and its value lies between $10 \text{ k}\Omega$ and $1 \cdot 0 \text{ M}\Omega$.

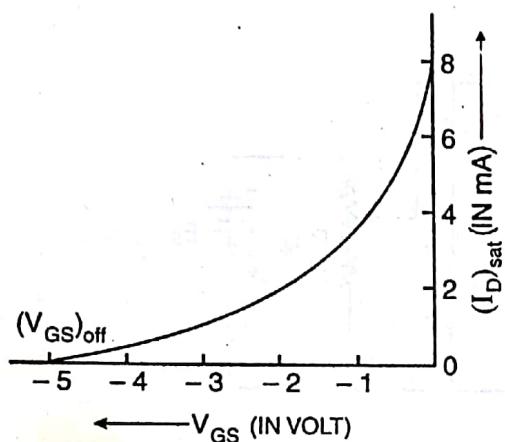


Fig. 9·8. Transfer characteristics of JFET

bias voltage V_{GS} between the gate and source increases, the saturated drain current $(I_D)_{sat}$ decreases.

(ii) **Mutual or trans conductance**—At a constant drain-source potential, the ratio of change in drain current to the corresponding change in gate-source potential, is called the mutual or trans conductance. i.e.,

$$g_m \text{ or } g_{fe} = \left(\frac{\Delta I_D}{\Delta V_{GS}} \right)_{V_{DS}} \quad \dots(9.3)$$

Its unit is ohm^{-1} or mho. It is of the order of 3 milli mho.

(iii) **Amplification factor**—For a constant drain current, the ratio of change in drain-source potential to the corresponding change in gate-source potential, is called the amplification factor. i.e.,

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta V_{GS}} \right)_{I_D} \quad \dots(9.4)$$

It has no unit. It is of the order of 50.

Relationship between the JFET's constants

We know that

$$\begin{aligned} \mu &= \frac{\Delta V_{DS}}{\Delta V_{GS}} \\ &= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} \end{aligned}$$

$$\text{But } \frac{\Delta V_{DS}}{\Delta I_D} = r_d \text{ and}$$

$$\frac{\Delta I_D}{\Delta V_{GS}} = g_{fe}$$

$$\mu = r_d \times g_{fe} \quad \dots(9.5)$$

or Amplification factor = dynamic drain resistance \times trans conductance

9.6. Comparison Between a JFET and Bipolar Transistor

(i) In a JFET, there is only the one type of charge carriers (electrons in a N channel JFET and holes in a P channel JFET), while in a transistor, the current flow is due to motion of both types of charge carriers (i.e., electrons and holes). Thus JFET is a unipolar device, while transistor is a bi-polar device.

(ii) In a JFET, the input circuit (i.e., gate-source) is kept in reverse bias due to which its input impedance is very high, while in a transistor, the input circuit is in forward bias due to which its input impedance is relatively low.

(iii) In a JFET, since the gate is kept in reverse bias, hence the gate current is negligible and the potential applied on the gate controls the drain current while in a transistor, the input current controls the output current. In other words, JFET is a device working on the basis of potential, while transistor is a device working on the basis of current.

(iv) In a JFET, the flow of current is through the channel (either P type or N type) and not through the P-N junction, hence the noise level is very low. On the other hand, in a transistor, the current flow is through the P-N and N-P junctions, hence the noise level is high.

~~9.7. Advantages of JFET~~

A JFET is a voltage controlled constant current device in which output current is controlled by the variations in input voltage. Some of the advantages of JFET are given below:

(i) Its input impedance is very high ($\approx 100 \text{ M}\Omega$), so the current drawn by gate is quite negligible.

- (ii) The noise level is very low.
- (iii) Its temperature coefficient of resistance is negative, so there are no chances of thermal runaway.
- (iv) Its power gain is very high.
- (v) It is smaller in size and it has a high efficiency and longer life.

9.8. JFET Biasing

We have read that for the proper operation of JFET, its gate is kept with respect to source in reverse bias condition. For this, either a battery can be used in the gate circuit or a circuit can be joined with the gate or source terminal, which is called the biasing circuit.

There are two methods of biasing : (i) self bias method, and (ii) voltage divider bias method.

(i) **Self bias method** : Fig 9.9 (a) and (b) show respectively the electric circuit with self biasing for the N channel and P channel JFET's. The resistance R_s connected with condenser C_s in parallel is the biasing circuit connected with the source S. The resistance

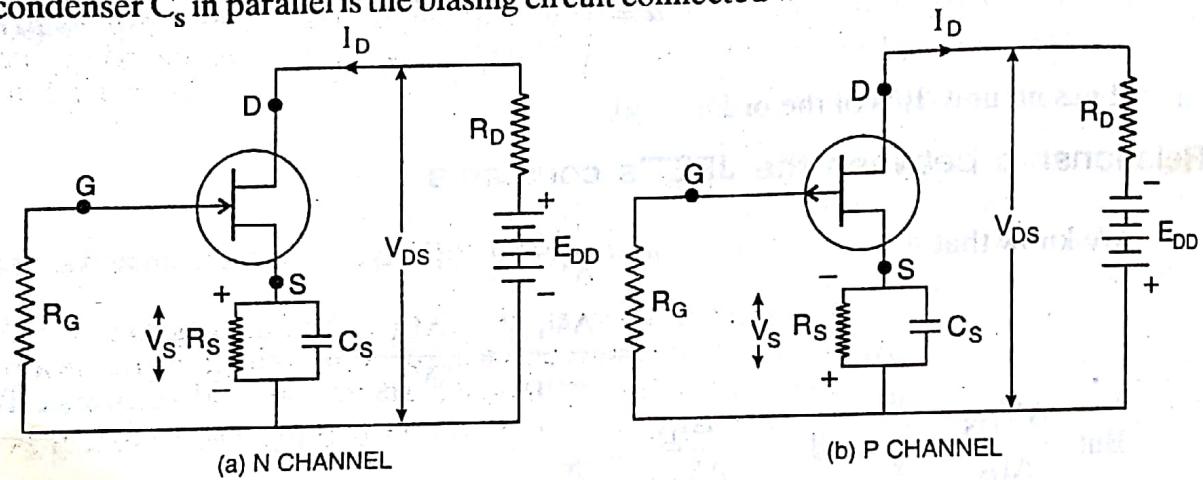


Fig. 9.9. Self biasing of JFET's

R_s is called the bias resistance. The d.c. component of drain current I_D flowing through the resistance R_s produces the desired bias voltage. The condenser C_s by passes the a.c. component of the drain current. Thus voltage across R_s is $V_s = I_D R_s$

$$\text{Since } V_G = 0, \therefore V_{GS} = V_G - V_s = 0 - I_D R_s = -I_D R_s \quad \dots(9.6)$$

Thus the gate is in reverse bias condition with respect to the source.

(ii) **Voltage divider bias method** : Fig. 9.10 (a) and (b) show respectively the circuit diagrams with voltage divider bias for the N channel and P channel JFET's. Here the resistances R_1 and R_2 provide the voltage divider. The voltage developed across the resistance R_1 provides the forward biasing at the gate while the voltage developed across the resistance R_S due to the d.c. component of drain current provides the reverse biasing at the gate. The condenser C_s by passes the a.c. component of drain current.

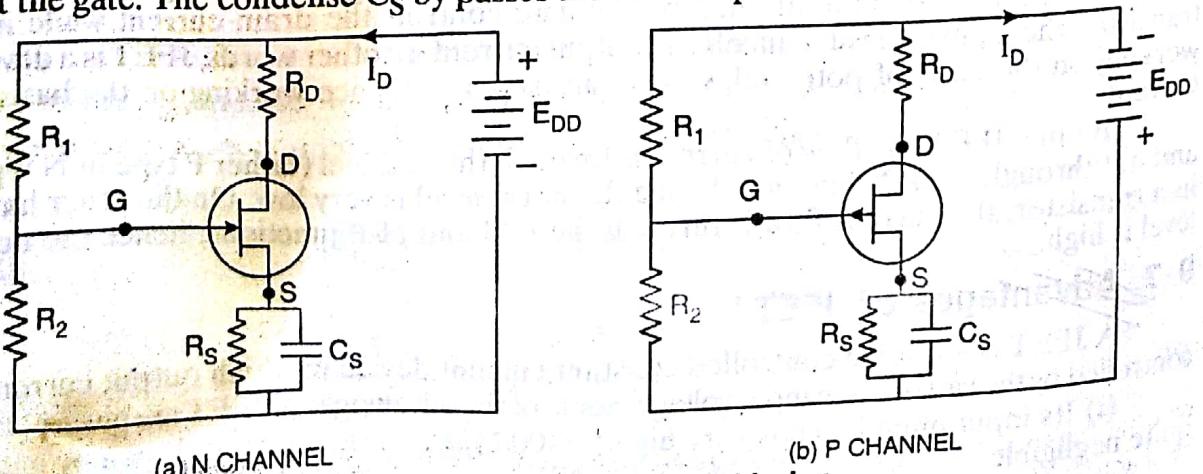


Fig. 9.10. Voltage divider biasing

Potential drop across the resistance R_2 is $\frac{E_{DD}}{(R_1 + R_2)} \times R_2$ which provides the forward biasing at the gate and potential drop across R_S is $I_D R_S$ which provides the reverse biasing at the gate. So the gate-source bias voltage is

$$V_{GS} = \frac{E_{DD}}{R_1 + R_2} \times R_2 - I_D R_S \quad \dots(9.7)$$

The parameters are so chosen that V_{GS} is negative i.e., $I_D R_S > \frac{E_{DD}}{R_1 + R_2} \times R_2$ so that the resultant bias at the gate-source junction is reverse.

9.9. A. C. Operation of JFET and Source Follower

We have read that there are three terminals in a JFET, namely the source S, gate G and drain D. When JFET is to be connected in a circuit, we require two terminals for the input and two terminals for the output. Therefore, it becomes essential to keep one terminal common to both the input and output. Thus, a JFET can be connected in a circuit in the following *three* ways :

- (i) Common source connection,
- (ii) Common gate connection, and
- (iii) Common drain connection.

Out of these, the most common way in which a JFET is used, is the common source connection.

Fig. 9.11 (a) and (b) show respectively the electric circuit diagrams for the N channel and P channel JFET's in common source connection with a.c. signal as input between the gate and source. The output is obtained across the load resistance R_L between the drain and the source. E_{DD} is the drain supply battery. The reverse bias at

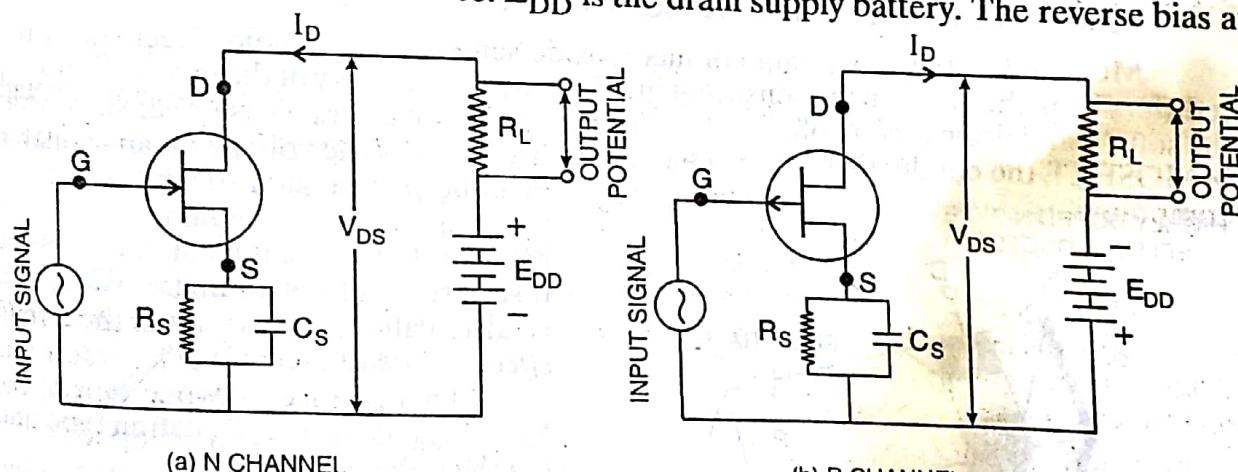


Fig. 9.11. Common source terminal JFET connections

the gate with respect to source is obtained by the self biasing method for which a resistance R_s in parallel with condenser C_s is connected in the source circuit. The voltage drop across the resistance R_s due to d.c. component of drain current I_D provides the gate bias voltage V_{GS} . The condenser C_s bypasses the a.c. component of drain current.

Obviously,

$$V_{GS} = -I_D R_s \quad \dots(9.8)$$

Further by Kirchhoff's law, $V_{DS} = E_{DD} - I_D (R_L + R_s)$

The drain current is given as

$$I_D = (I_D)_{sat} \left[1 - \frac{V_{GS}}{(V_{GS})_{off}} \right]^2 \quad \dots(9.10)$$

where $(V_{GS})_{off}$ is the gate-source cut off voltage of JFET which is known from its transfer characteristics.

Thus, using the eqns. (9.9) and (9.10), the operating point (*i.e.*, the values of I_D and V_{DS} at zero signal) can be obtained.

In this connection, the input impedance is high, voltage gain is good and output impedance is moderate. Further output signal is 180° out of phase of the input signal.

Source follower : When JFET is used with common drain terminal, it is called the source follower. The circuit diagrams for N channel and P channel JFET's with common drain terminal are shown in Fig. 9.12.

It has (i) voltage gain less than 1, (ii) no phase change in output, (iii) high input impedance and (iv) low output impedance.

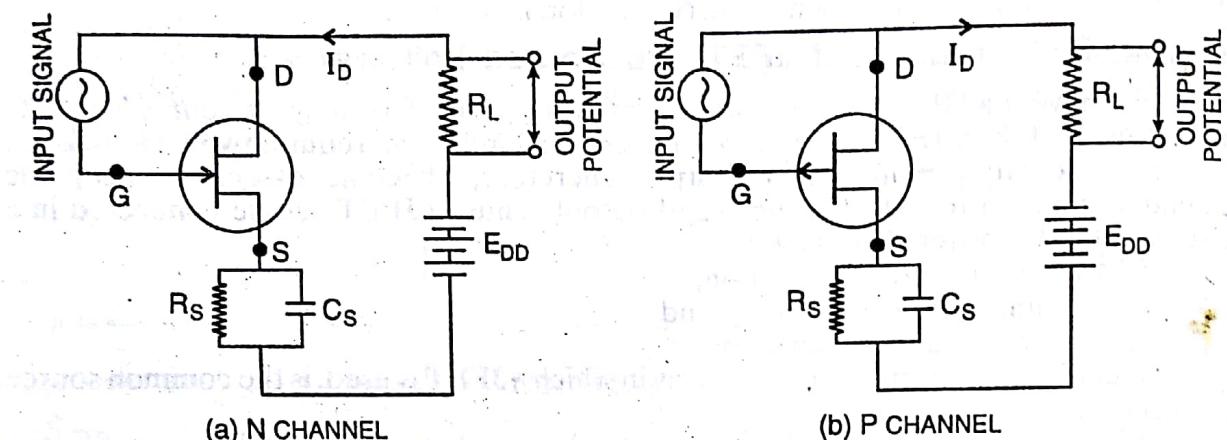


Fig. 9.12. JFET as a source follower

9.10. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) : Depletion and Enhancement Modes

MOSFET is the short name of metal oxide semiconductor field effect transistor. It differs from the JFET in the sense that in JFET, the conductivity of the channel between the source and drain is controlled by the width of depletion layers on its either side, while in MOSFET, the conductivity of the channel is controlled by the voltage on an insulated

metallic plate called the gate, lying on the top of the channel. Thus in MOSFET, the gate is insulated from the rest part by a layer of metal oxide, so it is also called the *insulated gate field effect transistor* (IGFET).

There are two types of MOSFET's : (i) the depletion type and (ii) the enhancement type.

(i) Depletion type MOSFET

Construction : Fig. 9.13 shows a depletion type N channel MOSFET. It has a lightly doped thin rod of P type semiconductor which acts as *substrate*. On one side of this rod, at the either ends two highly doped N type semiconductors are diffused which form the *drain D* and the *source S*. A lightly doped N type semiconductor is then diffused into the substrate as *channel* to connect the source and drain. On the other side of channel, there is an insulating thin layer of metal oxide

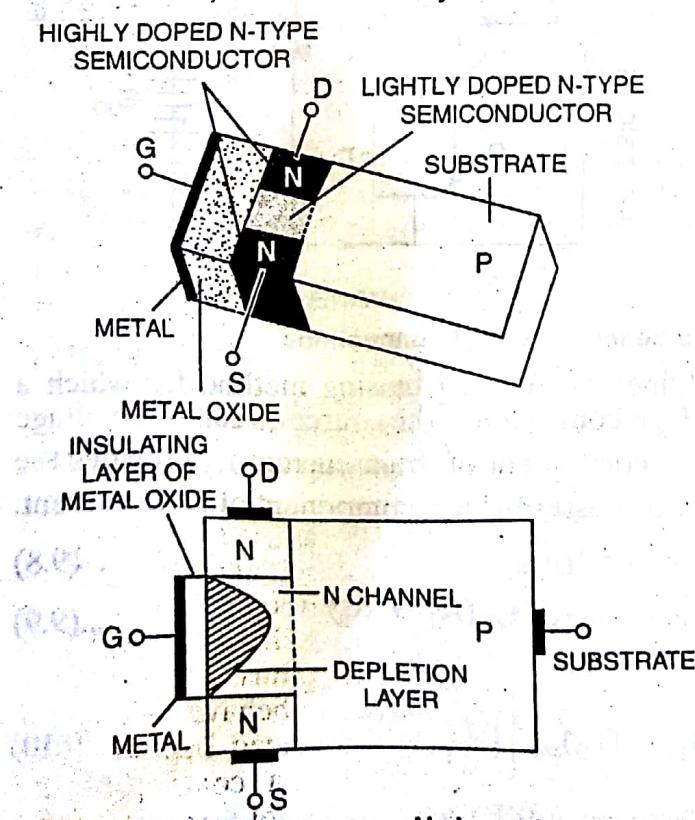


Fig. 9.13. Depletion type N channel MOSFET

(SiO_2) and then a layer of metal which acts as *gate G*. The insulating layer keeps the gate *G* isolated from the channel. Thus, this MOSFET also has three terminals like JFET, namely the source *S*, drain *D* and gate *G*.

Note that in P channel depletion type MOSFET, the substrate will be of N type semiconductor and the drain, source, channel each will be of P type semiconductor.

Working : Fig. 9.14 shows the circuit diagram to understand the working of depletion type N channel MOSFET. It is clear that there is no P-N junction between the gate and channel in a MOSFET as it is in case of JFET. In MOSFET, the gate and channel act like a condenser with gate and channel as plates and the insulating layer (SiO_2) as the dielectric.

Initially, when no potential is applied at the gate *G* by the battery *X* and a potential V_{DS} is applied by means of the battery *Y*, the drain current I_D begins to flow between the source and drain through the channel. In this condition the gate *G* is at -ve potential with respect to the drain *D* and so negative charges accumulate on the metal plate. This negative charge induces a positive charge inside the channel (Since the metal plate and the channel behave as two plates of a condenser) which causes depletion of mobile electrons inside the channel. The shape of depletion region inside the channel is generally wedge shaped as shown in Fig. 9.14.

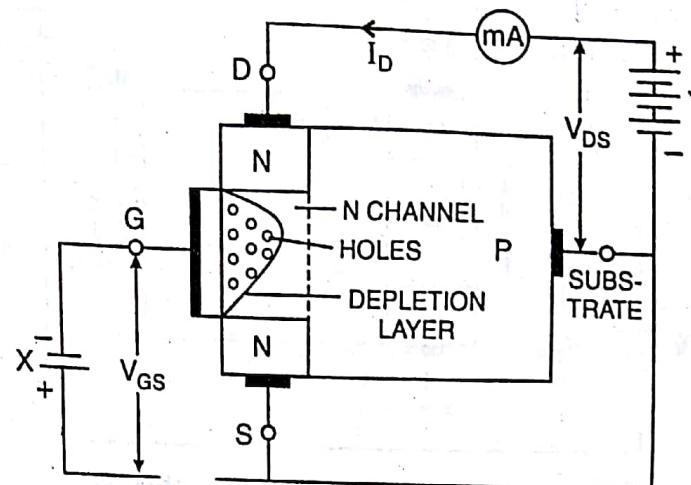


Fig. 9.14. Circuit diagram for depletion type N channel MOSFET

Now when gate *G* is kept at negative bias, the positive charges induced in the channel increase due to which the depletion region becomes more wide. As a result, the drain current decreases. Ultimately, when gate is made sufficiently negative, drain current ceases to flow.

But if positive potential is applied on the gate *G* by reversing the terminals of the battery *X*, electrons will get induced in the channel which will increase the number of majority charge carriers in the N channel and hence the conductivity of the channel will increase, due to which drain current increases.

Thus at a constant drain-source voltage, the drain current depends on the gate potential (i.e., the applied potential or the applied electric field controls the drain current). Further we notice that the depletion MOSFET works both at the positive as well as negative gate potentials.

(ii) Enhancement type MOSFET

Construction : Fig. 9.15 shows an enhancement type P channel MOSFET. It

consists of a lightly doped thin rod of P type semiconductor which acts as *substrate*. This rod on its one side has two highly doped N type semiconductors diffused on either side which act as *drain D* and the *source S*. The *channel* between the drain and source is the rod itself which is of P type semiconductor. Thus, the source, channel and drain behave as two N-P junction diodes placed back to back. The channel has a coating of thin insulating layer of metal oxide

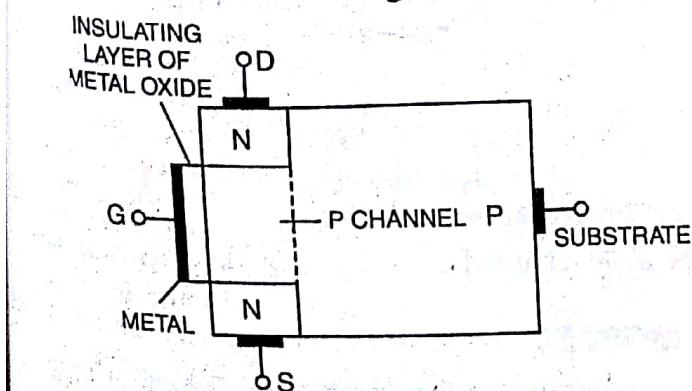


Fig. 9.15. P channel enhancement type MOSFET

(generally SiO_2) and over it there is a layer of metal (say, Al) which serves as the *gate G*. Thus, there are three terminals drain D, source S and gate G.

Note that in N channel enhancement type MOSFET, the channel and substrate are of N type semiconductor, while drain and source are of P type semiconductor.

Working : Fig. 9.16 shows the circuit diagram to understand the working of enhancement type P channel MOSFET.

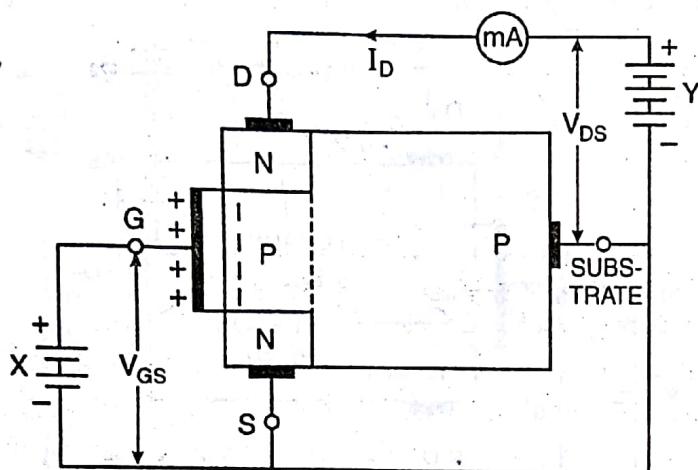


Fig. 9.16. Electric circuit for P channel enhancement type MOSFET

Thus, a conduction channel is formed between the N type source S and N type drain D. As a result, drain current I_D begins to flow. As the positive potential on gate is increased, the thickness of conduction channel formed between the source S and drain D increases and so the drain current also increases.

On the other hand, if gate G is at negative potential, then also no drain current flows.

Thus in the enhancement type MOSFET, no drain current flows when the gate is at zero or negative potential.

It may be mentioned here that as the gate forms a condenser, the gate current is quite negligible whether the gate is at positive potential or negative potential. So the input impedance of MOSFET is very high in the range of $10^4 \text{ M}\Omega$ to $10^6 \text{ M}\Omega$. The MOSFET can be used in any of the circuits where JFET is used.

Fig. 9.17 (a) and (b) respectively show the symbols for N channel and P channel depletion type MOSFET's.

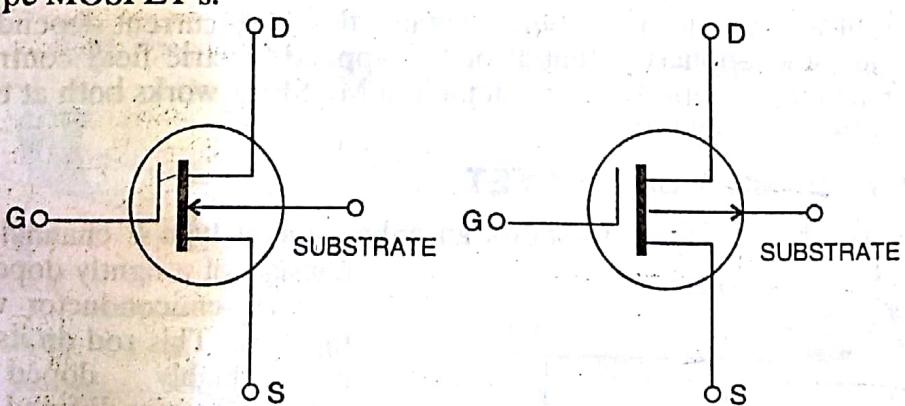


Fig. 9.17. Symbols for N and P channel MOSFET's.

Here the arrow is made inwards in N channel MOSFET, while outwards in P channel MOSFET on the substrate.

9.11. Characteristic Curves of MOSFET

Fig. 9.18 shows the electric circuit diagram for the N channel depletion type MOSFET to draw the characteristic curves. Here the battery B_1 is used as a potential

divider by means of a rheostat Rh_1 to apply either the negative potential or positive potential at the gate through a commutator C. The gate-source voltage V_{GS} can be read

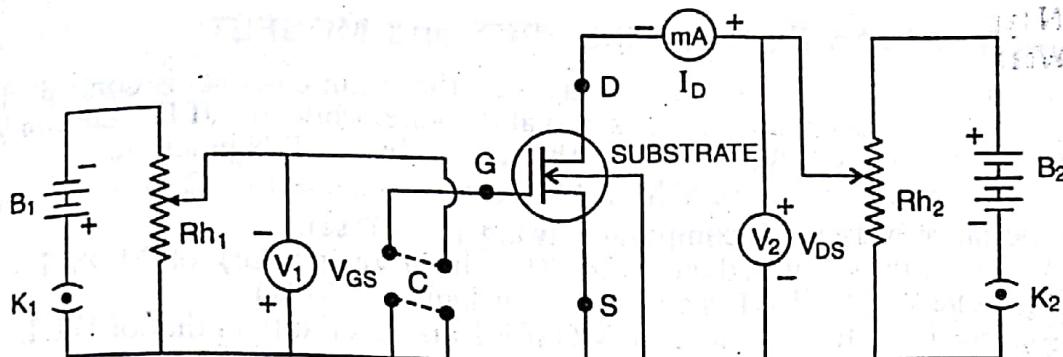


Fig. 9.18. Electric circuit for N channel depletion type MOSFET to draw the characteristic curves

by the voltmeter V_1 . The battery B_2 is used as a potential divider by means of a rheostat Rh_2 to apply a potential between the drain and the source. The drain-source voltage V_{DS} can be read by the voltmeter V_2 and the drain current I_D can be read by the milli-ammeter (mA).

In experiment, the gate-source voltage V_{GS} is kept fixed and by varying the drain-source voltage V_{DS} , the corresponding drain current I_D is noted. Then a graph is plotted for the drain current I_D versus the drain-source voltage V_{DS} . The experiment is then repeated for the different fixed gate-source voltage V_{GS} . The curves so obtained are called the output characteristic curves of MOSFET. They are shown in Fig. 9.19.

From these curves, we note that

- (i) When $V_{GS} = 0$, the drain current I_D is not zero.

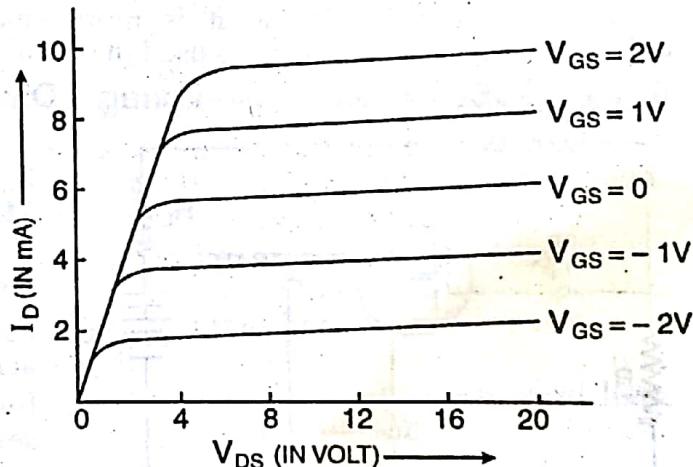


Fig. 9.19. Output characteristics of N channel depletion type MOSFET

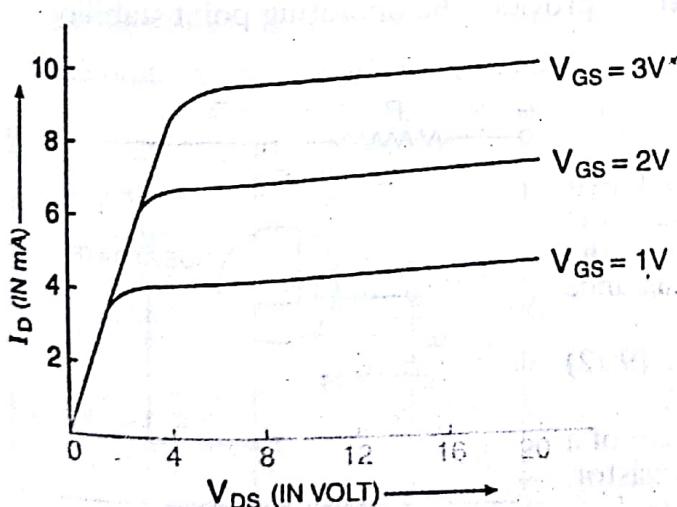


Fig. 9.20. Output characteristic curves of P channel enhancement type MOSFET

(ii) With increase in drain-source voltage V_{DS} , the drain current I_D first increases and then becomes nearly constant, at each gate-source voltage V_{GS} .

(iii) For a given drain-source voltage, drain current I_D is more when the gate-source voltage V_{GS} is more positive.

It may be noted that a similar

enhancement type MOSFET which are shown in Fig. 9.20. These curves differ from the curves of depletion type MOSFET in the sense that in enhancement type MOSFET, no drain

current is obtained when V_{GS} is zero or negative. The smallest value of V_{GS} at which the drain current starts flowing is called the *threshold voltage*.

9.12. Comparison Between the JFET and MOSFET

(1) In a MOSFET, the conductivity (*i.e.*, the drain current) is controlled by the electric field across the condenser formed at the gate, while in a JFET, the conductivity is controlled by the electric field across the reverse biased P-N junction.

(2) The input impedance of MOSFET is very high ($\approx 10^{10} \Omega$ to $10^{12} \Omega$), while the input impedance of JFET is comparatively low ($\approx 10^8 \Omega$).

(3) The output impedance (*i.e.*, the drain resistance) of MOSFET is low ($\approx k \Omega$), while that of JFET is comparatively high ($\approx M \Omega$).

(4) The characteristic curves of MOSFET are less flat than that of JFET.

(5) The depletion type MOSFET can be operated both at the negative and positive gate voltage, while JFET can only be operated at the negative gate voltage.

(6) In MOSFET, the input signal is applied between the gate and substrate, while in JFET, the input signal can be applied between any of the two terminals *i.e.*, the gate and source (if source is kept common) or gate and drain (if drain is kept common) or source and gate (if gate is kept common).

Advantages of MOSFET – As the input resistance of MOSFET is excessively high, it can be used in any of the circuit of JFET. It is easier to construct MOSFET, so it is more widely used than JFET. It is less expensive and it can be constructed in an extensively small space, so it is more suited for micro electronic circuits. The enhancement type MOSFET is used in digital circuits.

SOLVED EXAMPLES

Ex. 1. For a JEFT, the saturated drain current is 32 mA and gate-source cut off voltage is -8 volt. Find the drain current at gate-source voltage $V_{GS} = -4.5$ volt.

Sol. Given, $(I_D)_{sat} = 32 \text{ mA}$, $(V_{GS})_{off} = -8 \text{ V}$, $V_{GS} = -4.5 \text{ V}$

From relation $I_D = (I_D)_{sat} \left[1 - \frac{V_{GS}}{(V_{GS})_{off}} \right]^2$

$$I_D = 32 \left[1 - \frac{(-4.5)}{(-8)} \right]^2 \text{ mA}$$

$$= 6.125 \text{ mA.}$$

Ex. 2. If saturated drain current of a JFET is 10 mA, pinch off voltage is 6 V, find the gate-source voltage when the drain current is 5 mA.

Sol. Given, $(I_D)_{sat} = 10 \text{ mA}$, $V_p = 6 \text{ V}$, $\therefore (V_{GS})_{off} = -6 \text{ V}$, $I_D = 5 \text{ mA}$

From relation $I_D = (I_D)_{sat} \left[1 - \frac{V_{GS}}{(V_{GS})_{off}} \right]^2$

$$5 = 10 \left[1 - \frac{V_{GS}}{(-6)} \right]^2$$

or $1 + \frac{V_{GS}}{6} = \frac{1}{\sqrt{2}} = 0.707$

or $V_{GS} = 6(0.707 - 1) = -1.76 \text{ V}$

Ex. 3. Show that for JFET, the trans conductance is expressed as

$$g_{fe} = -2(I_D)_{sat} \left[1 - \frac{V_{GS}}{(V_{GS})_{off}} \right]$$

Sol. The drain current is given as

$$I_D = (I_D)_{sat} \left[1 - \frac{V_{GS}}{(V_{GS})_{off}} \right]^2$$

$$\therefore g_{fe} = \left(\frac{\Delta I_D}{\Delta V_{GS}} \right)_{V_{DS}} = -2(I_D)_{sat} \left[1 - \frac{V_{GS}}{(V_{GS})_{off}} \right]$$

Ex. 4. In a JFET, when a reverse gate voltage of 15 V is applied, the gate current is $0.001 \mu\text{A}$. Find the resistance between the gate and source.

Sol. Given, $V_{GS} = 15 \text{ V}$, $I_G = 0.001 \mu\text{A} = 10^{-9} \text{ A}$

$$\text{Resistance between the gate and source} = \frac{V_{GS}}{I_G} = \frac{15}{10^{-9}} \Omega = 15000 \text{ M}\Omega$$

Ex. 5. At a constant gate-source voltage, the drain current changes by 0.02 mA when the drain-source voltage is changed by 2 V. Find the dynamic drain resistance of JFET.

Sol. Given, $\Delta I_D = 0.02 \text{ mA} = 2 \times 10^{-5} \text{ A}$, $\Delta V_{DS} = 2 \text{ V}$

$$\text{Dynamic drain resistance } r_d = \left(\frac{\Delta V_{DS}}{\Delta I_D} \right)_{V_{GS}} = \frac{2}{2 \times 10^{-5}} \Omega = 10^5 \Omega$$

Ex. 6. In a JFET, the drain current changes from 1 mA to 1.3 mA when the gate-source voltage is changed from -3.1 V to -3 V . The dynamic drain resistance of JFET is 100 kilo ohm. Find : (i) the trans conductance and (ii) the amplification factor of JFET.

Sol. Given, $\Delta I_D = 1.3 - 1 = 0.3 \text{ mA} = 0.3 \times 10^{-3} \text{ A}$, $\Delta V_{GS} = -3 - (-3.1) = 0.1 \text{ V}$, $r_d = 100 \text{ kilo ohm} = 10^5 \text{ ohm}$.

$$(i) \text{Trans conductance } g_{fe} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3 \times 10^{-3} \text{ A}}{0.1 \text{ V}} = 3 \times 10^{-3} \text{ mho}$$

$$(ii) \text{Amplification factor } \mu = r_d \times g_{fe} = 10^5 \times 3 \times 10^{-3} = 300$$

Ex. 7. From the following observations, find : (i) a.c. drain resistance, (ii) trans conductance and (iii) amplification factor of JFET.

V_{GS} (in volt)	0	0	-0.2
V_{DS} (in volt)	7	15	15
I_D (in mA)	10	10.25	9.65

$$\text{Sol. (i) A.C. drain resistance } r_d = \left(\frac{\Delta V_{DS}}{\Delta I_D} \right)_{V_{GS}}$$

$$\text{At } V_{GS} = 0; \Delta V_{DS} = 15 - 7 = 8 \text{ V}, \Delta I_D = 10.25 - 10 = 0.25 \text{ mA} = 0.25 \times 10^{-3} \text{ A}$$

$$\therefore r_d = \frac{8}{0.25 \times 10^{-3}} \Omega = 32 \text{ k}\Omega$$

$$(ii) \text{Trans conductance } g_{fe} = \left(\frac{\Delta I_D}{\Delta V_{GS}} \right)_{V_{DS}}$$

$$\text{At } V_{DS} = 15 \text{ V}, \Delta I_D = 9.65 - 10.25 = -0.60 \text{ mA} = -0.6 \times 10^{-3} \text{ A} \text{ and}$$

$$\Delta V_{GS} = -0.2 - 0 = -0.2 \text{ V}$$

$$\therefore g_{fe} = \frac{-0.6 \times 10^{-3} \text{ A}}{-0.2 \text{ V}} = 3 \times 10^{-3} \text{ mho}$$

$$(iii) \text{Amplification factor } \mu = r_d \times g_{fe}$$

$$= (32 \times 10^3) \times (3 \times 10^{-3}) = 96$$

Ex. 8. In a MOSFET, the drain current is given as

$$I_D = K [V_{GS} - (V_{GS})_{\text{threshold}}]^2$$

If $(V_{GS})_{\text{threshold}} = 3 \text{ V}$ and drain current I_D is 8 mA when the gate-source voltage V_{GS} is 5 V , find the drain current at gate-source voltage 8 V .

Sol. Given, $(V_{GS})_{\text{threshold}} = 3 \text{ V}$, and $I_D = 8 \text{ mA}$, $V_{GS} = 5 \text{ V}$

$$\therefore 8 = K (5 - 3)^2 \quad \text{or} \quad K = 2 \text{ mA/V}^2$$

Now $V_{GS} = 8 \text{ V}$ and $I_D = ?$

Substituting the value of K , we get

$$I_D = 2 (8 - 3)^2 \text{ mA} = 50 \text{ mA}$$

Chapter 10

AMPLIFIERS

10.1. Bipolar Transistors as Amplifier

The process of magnifying the amplitude of an electric signal (voltage, current or power) is called the *amplification*. The device used to increase the magnitude of voltage, current or power is called the *amplifier*. A transistor can be used as an amplifier because in a transistor, the charge carriers move from the forward biased input circuit of low resistance to the reverse biased output circuit of high resistance and so by a small change in current in the input circuit, a large change in current is obtained in the output circuit. Thus, a transistor changes a weak signal into a strong signal and it can be used as an amplifier.

We have read that a transistor has only the three terminals : emitter, base and collector. But to connect a transistor in an electric circuit, we require four terminals : two for the input circuit and two for the output circuit. Hence out of the three terminals, emitter (E), base (B) and collector (C) of a transistor, one terminal is earthed and it is kept common in between the remaining two terminals. In other words, one terminal of transistor is made common to both the input and output circuits. Thus, a transistor can be used as an amplifier in the following three configurations :

- (i) In *common base configuration* or *CB mode* in which base is made common to both the input and output circuits.
- (ii) In *common emitter configuration* or *CE mode* in which emitter is made common to both the input and output circuits.
- (iii) In *common collector configuration* or *CC mode* in which collector is made common to both the input and output circuits.

10.2. Classification of Amplifiers

Amplifiers are classified on the basis of following six criterion :

(1) on the basis of aim, (2) on the basis of frequency range, (3) on the basis of biasing, (4) on the basis of coupling, (5) on the basis of load, and (6) on the basis of configuration.

(1) Classification on the basis of aim : The amplifiers are divided in the following three classes on the basis of aim.

(a) Voltage amplifier — It amplifies a weak voltage signal without any distortion. It is also called the *small signal amplifier*.

(b) Current amplifier — It amplifies a weak current signal to a strong current signal.

(c) **Power amplifier**—It amplifies a weak power signal. It is also called the large signal amplifier.

(2) **Classification on the basis of frequency range** : On the basis of frequency range, the amplifiers are divided into the following four classes :

(a) **Audio or low frequency amplifier**—It amplifies the signal of audible frequency (20 Hz to 20 kilo-Hz) without any distortion (for example, to amplify the signal obtained from a microphone).

(b) **Radio frequency amplifier**—It amplifies the signal of radio frequency of the order of MHz, (for example to amplify the signal for transmission at the radio-station).

(c) **Video frequency amplifier**—It amplifies the signal of frequency from 20 kHz to 5 MHz, (for example to amplify the video signal in a television).

(d) **D. C. amplifier**—It amplifies the d.c. signal also alongwith the a.c. signal.

(3) **Classification on the basis of biasing** : On the basis of biasing in the input circuit, the amplifiers are divided in the following four classes :

(a) **Class A amplifier**—It provides output current in the complete cycle of input signal and the output current has the amplified wave form exactly similar to that of input current.

(b) **Class AB amplifier**—It provides output current for more than half cycle (but less than the complete cycle) of the input signal.

(c) **Class B amplifier**—It provides output current only for half cycle of input signal.

(d) **Class C amplifier**—It provides output current for less than half cycle of input signal.

(4) **Classification on the basis of coupling** : Generally a signal is not amplified in a single stage, but it is amplified in multiple stages. For this, a number of amplifiers are coupled in cascade such that the output signal of one stage is again supplied as input signal to the next stage. On the basis of coupling, the amplifiers are divided in the following four classes :

(a) d-c or direct coupled amplifier,

(b) R-C or resistance-capacitance coupled amplifier,

(c) L-C or inductance-capacitance coupled amplifier,

(d) Transformer coupled amplifier.

(5) **Classification on the basis of load** : Depending upon the load connected with the amplifier, they are divided in the following two classes :

(a) Untuned voltage or power amplifier, and

(b) Tuned voltage or power amplifier.

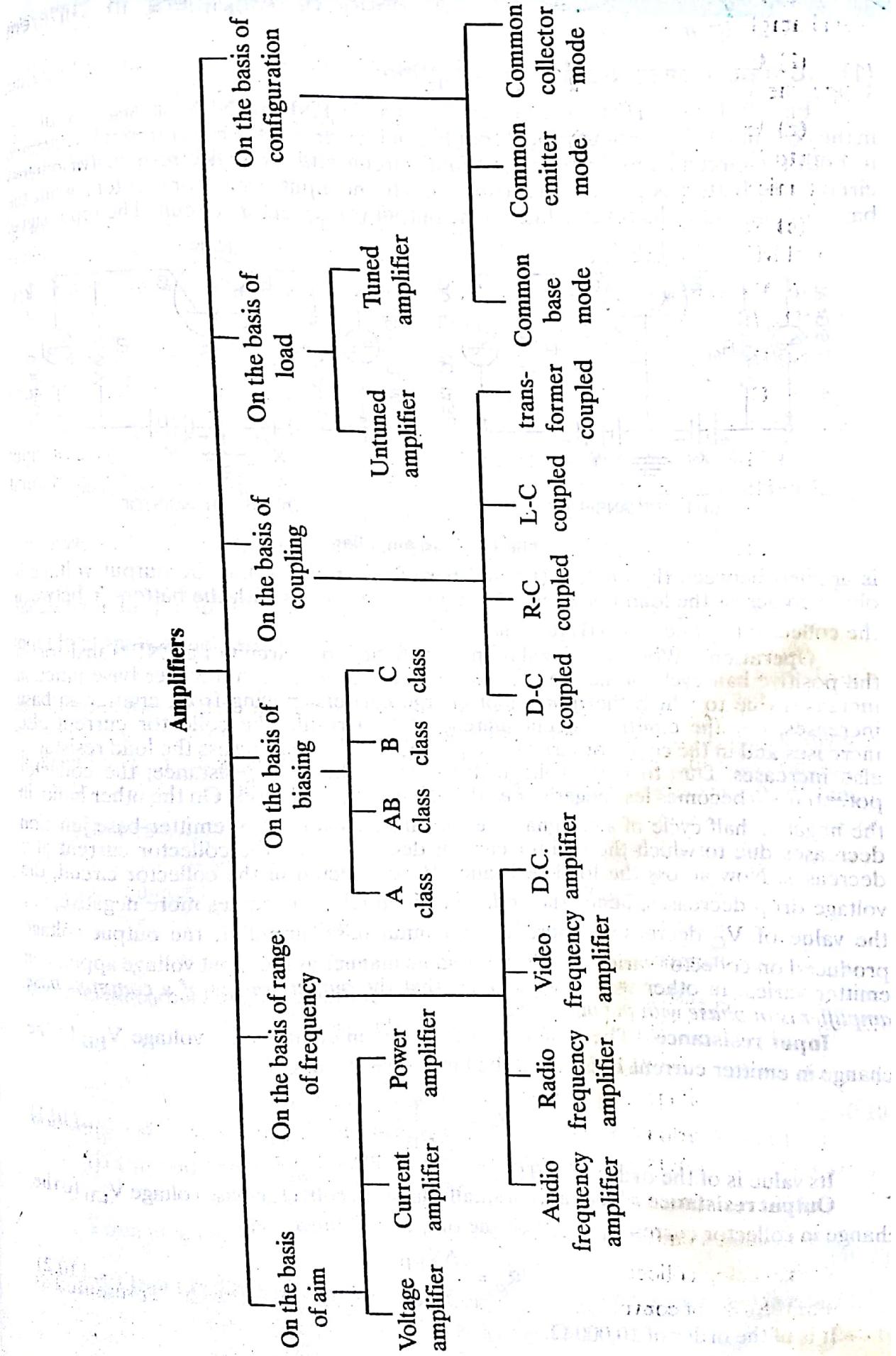
(6) **Classification on the basis of configuration** : On the basis of configuration, the transistor amplifiers are divided in the following three classes :

(a) Common base amplifier,

(b) Common emitter amplifier, and

(c) Common collector amplifier.

For the sake of convenience, the classification of amplifiers can be represented as ahead.



10·3. General Principles of Operation of Amplifiers in Different Configurations

(1) Common base transistor amplifier

Fig. 10·1(a) and (b) respectively represent the PNP and NPN transistor amplifiers in the common base configuration. From Fig., it is clear that the base terminal is common to both the circuits emitter-base (or input) circuit and the collector-base (or output) circuit. The battery X provides a forward bias to the input circuit (or emitter), while the battery Y provides the reverse bias to the output (or collector) circuit. The input signal

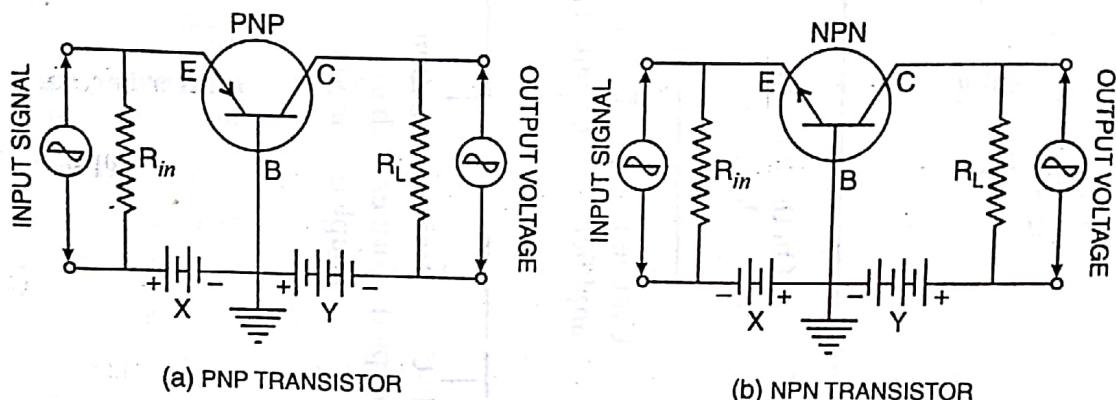


Fig. 10·1. CB amplifier

is applied between the emitter (E) and base (B) terminals and the output voltage is obtained across the load resistance R_L connected in series with the battery Y between the collector (C) and base (B) terminals.

Operation — When a.c. signal is applied in the input circuit of a PNP transistor, in the positive half cycle of a.c. signal, the forward bias voltage of emitter-base junction increases due to which the number of charge carriers moving from emitter to base increases, i.e., the emitter current increases. As a result, the collector current also increases and in the collector circuit, the potential difference across the load resistance also increases. Due to more voltage drop across the load resistance, the collector potential V_C becomes less negative i.e., the value of V_C increases. On the other hand, in the negative half cycle of a.c. signal, the forward bias voltage of emitter-base junction decreases due to which the emitter current decreases and the collector current also decreases. Now across the load resistance R_L connected in the collector circuit, the voltage drop decreases, hence the collector potential V_C becomes more negative, i.e., the value of V_C decreases. Thus, in a common base amplifier, the output voltage produced on collector varies exactly in the same manner as the input voltage applied on emitter varies. In other words, we can say that the *output voltage of a common base amplifier is in phase with the input voltage*.

Input resistance — The ratio of small change in emitter-base voltage V_{EB} to the change in emitter current I_E is called the input resistance. i.e.,

$$R_i = \frac{\Delta V_{EB}}{\Delta I_E} \quad \dots(10.1)$$

Its value is of the order of 100Ω .

Output resistance — The ratio of small change in collector-base voltage V_{CB} to the change in collector current I_C is called the output resistance. i.e.,

$$R_o = \frac{\Delta V_{CB}}{\Delta I_C} \quad \dots(10.2)$$

It is of the order of $10,000\Omega$.

Since the resistance of the forward biased emitter circuit is very low ($\approx 100 \Omega$) and the resistance of reverse biased collector circuit is very high ($\approx 10,000 \Omega$), hence corresponding to a small change in emitter voltage, a high a.c. voltage is obtained across the load (i.e., the signal gets amplified). Thus, a transistor in common base mode is used as a voltage amplifier.

Current gain — At a constant collector-base voltage, the ratio of change in collector current to the corresponding change in emitter current is called the current gain of the common base amplifier. It is represented by the symbol α . Thus

$$\text{Current gain } \alpha = \left(\frac{\Delta I_C}{\Delta I_E} \right)_{V_{CB} = \text{constant}} \quad \dots(10.3)$$

Its value is slightly less than 1 because nearly 2% to 5% of emitter current is lost in base.

Voltage gain — The ratio of change in output voltage to the change in input voltage is called the voltage gain. It is represented by the symbol A_v . Thus

$$\text{Voltage gain } A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{R_L \Delta I_C}{R_{in} \Delta I_E} = \frac{R_L}{R_{in}} \times \left(\frac{\Delta I_C}{\Delta I_E} \right) = \alpha \frac{R_L}{R_{in}} \quad \dots(10.4)$$

Power gain — By definition, power gain = current gain \times voltage gain.

$$\text{or } A_p = \alpha \times \alpha \times \frac{R_L}{R_{in}} = \alpha^2 \frac{R_L}{R_{in}} \quad \dots(10.5)$$

Mathematical analysis using h parameters : The hybrid equivalent circuit of CB amplifier is shown in Fig. 10.2. Here the resistor R_{in} has been neglected since it does not affect the a.c. operations. R_S is the internal resistance of source.

The hybrid equations of the equivalent circuit are

$$V_E = h_{rB} V_C + h_{iB} I_E \quad \dots(10.6)$$

$$\text{and } I_C = h_{fB} I_E + h_{oB} V_C \quad \dots(10.7)$$

(Note that h_{oB} is the output admittance, so $1/h_{oB}$ will be the output impedance)

$$V_E = e_s - I_E R_S \quad \dots(10.8)$$

$$V_C = -I_C R_L \quad \dots(10.9)$$

Substituting the value of V_C from eqn. (10.9) in eqn. (10.7), we get

$$I_C = h_{fB} I_E - h_{oB} I_C R_L$$

$$\text{or } I_C = \frac{h_{fB} I_E}{1 + h_{oB} R_L} \quad \dots(10.10)$$

$$(i) \text{ Current gain } -A_{iB} = \frac{\text{Output current}}{\text{Input current}} = \frac{I_C}{I_E}$$

$$\text{From eqn. (10.10), } A_{iB} = \frac{h_{fB}}{1 + h_{oB} R_L} \quad \dots(10.11)$$

(ii) **Input resistance** — Substituting the value of V_C from eqn. (10.9) in eqn. (10.6),

$$V_E = -h_{rB} I_C R_L + h_{iB} I_E$$

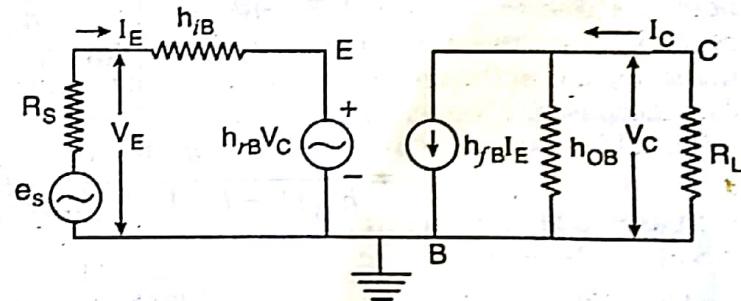


Fig. 10.2. Hybrid equivalent circuit of CB amplifier

Now putting the value of I_C from eqn. (10.10),

$$V_E = \frac{-h_{rB}h_{fB}I_E R_L}{1 + h_{oB}R_L} + h_{iB}I_E$$

$$\text{or } V_E = I_E \left[h_{iB} - \frac{h_{rB}h_{fB}R_L}{1 + h_{oB}R_L} \right]$$

$$\therefore \text{Input resistance } R_{iB} = \frac{\text{Input voltage}}{\text{Input current}} = \frac{V_E}{I_E}$$

$$= h_{iB} - \frac{h_{rB}h_{fB}R_L}{1 + h_{oB}R_L} \quad \dots(10.12)$$

$$\text{(iii) Voltage gain} - \text{Voltage gain } A_{vB} = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \text{Current gain} \times \frac{R_L}{R_{iB}}$$

$$= A_{iB} \frac{R_L}{R_{iB}}$$

Now substituting the values of A_{iB} and R_{iB} from eqns. (10.11) and (10.12), we get

$$\begin{aligned} A_{vB} &= \frac{h_{fB}}{1 + h_{oB}R_L} \times \frac{R_L}{\left[h_{iB} - \frac{h_{rB}h_{fB}R_L}{1 + h_{oB}R_L} \right]} \\ &= \frac{h_{fB}R_L}{h_{iB}(1 + h_{oB}R_L) - h_{rB}h_{fB}R_L} \\ &= \frac{h_{fB}R_L}{h_{iB} + R_L(h_{iB}h_{oB} - h_{rB}h_{fB})} \quad \dots(10.13) \end{aligned}$$

$$\text{(iv) Power gain} - \text{Power gain} = \text{Voltage gain} \times \text{Current gain}$$

$$A_{pB} = A_{vB} \times A_{iB}$$

$$\begin{aligned} &= \frac{h_{fB}R_L}{h_{iB} + R_L(h_{iB}h_{oB} - h_{rB}h_{fB})} \times \frac{h_{fB}}{1 + h_{oB}R_L} \\ &= \frac{h_{fB}^2 R_L}{\{h_{iB} + R_L(h_{iB}h_{oB} - h_{rB}h_{fB})\}(1 + h_{oB}R_L)} \quad \dots(10.14) \end{aligned}$$

$$\text{(v) Output resistance} - \text{Output resistance } R_{oB} = \frac{\text{Output voltage}}{\text{Output current}} = \frac{V_C}{I_C} \text{ when the input signal source is replaced by its internal resistance } R_s \text{ and the output voltage source } V_C \text{ is connected in place of the load resistance } R_L.$$

Then $V_C = (I_C - h_{fB} I_E) \times \frac{1}{h_{oB}}$ (since h_{oB} is the output admittance, so output impedance $= \frac{1}{h_{oB}}$)

and

$$I_E = \frac{-h_{rB} V_C}{h_{iB} + R_S}$$

On solving these equations, we get

$$h_{oB} V_C = I_C + \frac{h_{fB} h_{rB} V_C}{h_{iB} + R_S}$$

or

$$V_C = \frac{I_C}{h_{oB} - \frac{h_{fB} h_{rB}}{h_{iB} + R_S}}$$

$$\begin{aligned} \text{Hence output resistance } R_{oB} &= \frac{V_C}{I_C} = \frac{1}{h_{oB} - \frac{h_{fB} h_{rB}}{h_{iB} + R_S}} \\ &= \frac{h_{iB} + R_S}{h_{oB} (h_{iB} + R_S) - h_{fB} h_{rB}} \end{aligned} \quad \text{2006} \quad \dots(10.15)$$

✓ Imp

(2) Common Emitter Transistor Amplifier

Fig. 10.3 (a) and (b) show respectively the PNP and NPN transistor amplifiers in common-emitter configuration. From Fig., it is clear that the emitter terminal is common to both input (base-emitter) and output (collector-emitter) circuits. The input circuit (base) is kept in forward bias by the battery X, while the output circuit (collector) is kept

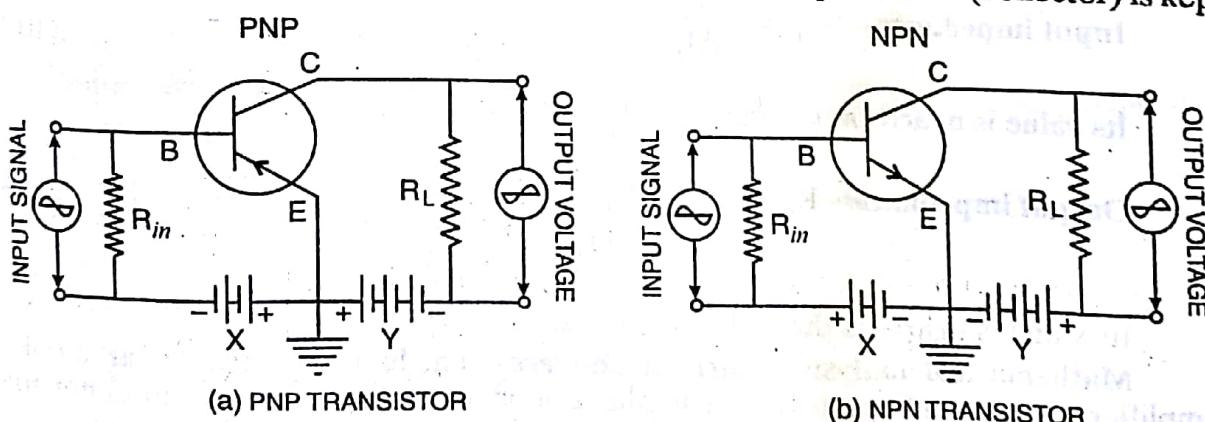


Fig. 10.3. CE amplifier

in reverse bias by the battery Y. The input signal is applied between the terminals of base (B) and emitter (E) and the output voltage is obtained across the load resistance R_L connected in series with the battery Y in between the collector (C) and emitter (E) terminals.

Operation – On applying the a.c. signal in the input circuit, in a PNP transistor, in the positive half cycle of signal, the forward bias voltage of base-emitter junction decreases due to which the collector current also decreases and the voltage drop across the load resistance R_L decreases. As a result, the collector voltage becomes more

negative (*i.e.*, decreases). On the other hand, in the negative half cycle of input a.c. signal, the forward bias voltage of base-emitter junction increases due to which collector current also increases and the voltage drop across the load resistance R_L increases, *i.e.*, the collector voltage becomes less negative (*i.e.*, increases). Thus, in a common emitter amplifier, the output voltage is in opposite phase to the input voltage (*i.e.*, there is a phase difference of 180° between the output and input voltages).

Obviously, in a common emitter amplifier, the collector current is governed by the base current (not by the emitter current) but in a transistor, corresponding to a very low base current, the collector current is very high hence in a common emitter amplifier, due to a small variation in base current, a large variation is obtained in the collector current (*i.e.*, a high current gain is obtained). So it is commonly used as a current amplifier.

Current gain—At a constant collector-emitter voltage, the ratio of change in collector current to the corresponding base current, is called the current gain by a common emitter amplifier and it is represented by the symbol β . Thus

$$\text{Current gain } \beta = \left(\frac{\Delta I_C}{\Delta I_B} \right)_{V_{CE} = \text{constant}} \quad \dots(10.16)$$

Its value is generally 49.

Voltage gain—Voltage gain of a common emitter amplifier

$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{R_L \Delta I_C}{R_{in} \Delta I_B} = \frac{R_L}{R_{in}} \times \left(\frac{\Delta I_C}{\Delta I_B} \right) = \beta \frac{R_L}{R_{in}} \quad \dots(10.17)$$

Power gain—By definition, power gain = current gain \times voltage gain

$$\text{or } A_p = \beta \times \beta \left(\frac{R_L}{R_{in}} \right) = \beta^2 \frac{R_L}{R_{in}} \quad \dots(10.18)$$

$$\text{Input impedance } R_{in} = \left(\frac{\Delta V_B}{\Delta I_B} \right)_{V_C} \quad \dots(10.19)$$

Its value is nearly in between 200Ω to 800Ω .

$$\text{Output impedance } R_{out} = \left(\frac{\Delta V_C}{\Delta I_C} \right)_{I_B} \quad \dots(10.20)$$

Its value is nearly of the order of $20 \text{ k}\Omega$.

Mathematical analysis using h parameters—The hybrid equivalent circuit of CE amplifier is shown in Fig. 10·4. Here R_{in} has not been considered since it does not affect

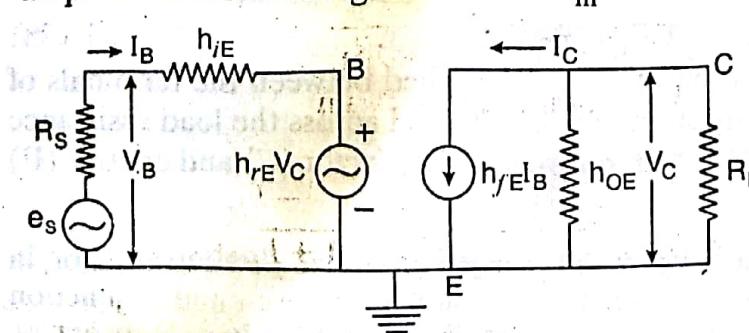


Fig. 10·4. Hybrid equivalent circuit of CE amplifier

the a. c. operation. R_s is the internal resistance of the source.

The hybrid equations of the equivalent circuit are

$$V_B = h_{iE} I_B + h_{rE} V_C \quad \dots(10.21)$$

$$I_C = h_{fE} I_B + h_{oE} V_C \quad \dots(10.22)$$

$$V_B = e_s - I_B R_s \quad \dots(10.23)$$

$$V_C = - I_C R_L \quad \dots(10.24)$$

Substituting the value of V_C from eqn. (10.24) in eqn. (10.22),

$$I_C = h_{fE} I_B + h_{oE} (-I_C R_L)$$

$$\text{or } I_C = \frac{h_{fE} I_B}{1 + h_{oE} R_L}$$

$$(i) \text{ Current gain } - A_{iE} = \frac{\text{Output current}}{\text{Input current}} = -\frac{I_C}{I_B}$$

Here negative sign shows that the collector current I_C is in phase opposite to the base current I_B . From eqn. (10.25),

$$A_{iE} = \frac{-h_{fE}}{1 + h_{oE} R_L} \quad \dots(10.26)$$

(ii) Input resistance — Substituting the value of V_C from eqn. (10.24) in eqn. (10.21),

$$V_B = h_{iE} I_B - h_{rE} I_C R_L$$

Now putting the value of I_C from eqn. (10.24),

$$V_B = h_{iE} I_B - \frac{h_{rE} h_{fE} I_B R_L}{1 + h_{oE} R_L}$$

$$= I_B \left[h_{iE} - \frac{h_{rE} h_{fE} R_L}{1 + h_{oE} R_L} \right]$$

$$\therefore \text{Input resistance } R_{iE} = \frac{V_B}{I_B} = h_{iE} - \frac{h_{rE} h_{fE} R_L}{1 + h_{oE} R_L} \quad \dots(10.27)$$

$$(iii) \text{ Voltage gain } - A_{vE} = \frac{\text{Output voltage}}{\text{Input voltage}} = \text{Current gain} \times \frac{R_L}{R_{iE}}$$

$$= \frac{A_{iE} R_L}{R_{iE}}$$

Substituting the values of A_{iE} and R_{iE} from eqns. (10.26) and (10.27), we get

$$A_{vE} = \frac{-h_{fE}}{1 + h_{oE} R_L} \times \frac{R_L}{\left\{ h_{iE} - \frac{h_{rE} h_{fE} R_L}{1 + h_{oE} R_L} \right\}}$$

$$= \frac{-h_{fE} R_L}{h_{iE}(1 + h_{oE} R_L) - h_{rE} h_{fE} R_L}$$

$$= \frac{-h_{fE} R_L}{h_{iE} + (h_{iE} h_{oE} - h_{rE} h_{fE}) R_L} \quad \dots(10.28)$$

(iv) Power gain — Power gain = voltage gain \times current gain

$$A_{pE} = A_{vE} \times A_{iE}$$

$$= \frac{-h_{fE} R_L}{h_{iE} + (h_{iE} h_{oE} - h_{rE} h_{fE}) R_L} \times \frac{-h_{fE}}{1 + h_{oE} R_L}$$

$$= \frac{h_{fE}^2 R_L}{\{h_{iE} + (h_{iE} h_{oE} - h_{rE} h_{fE}) R_L\} (1 + h_{oE} R_L)} \quad \dots(10.29)$$

(v) Output resistance—Output resistance $R_{oE} = \frac{\text{Output voltage}}{\text{Output current}} = \frac{V_C}{I_C}$ (when the input signal source e_S is replaced by its internal resistance R_S and the voltage source V_C is applied at the output terminals instead of load R_L).

Then $V_C = (I_C - h_{fE} I_B) \times \frac{1}{h_{oE}}$ (since h_{oE} is the output admittance, so output impedance $= \frac{1}{h_{oE}}$)

and

$$I_B = -\frac{h_{rE} V_C}{h_{iE} + R_S}$$

On solving these equations, $h_{oE} V_C = I_C + \frac{h_{fE} h_{rE} V_C}{h_{iE} + R_S}$

or

$$V_C = \frac{I_C}{h_{oE} - \frac{h_{fE} h_{rE}}{h_{iE} + R_S}}$$

Hence output resistance

$$R_{oE} = \frac{1}{h_{oE} - \frac{h_{fE} h_{rE}}{h_{iE} + R_S}} = \frac{h_{iE} + R_S}{h_{oE}(h_{iE} + R_S) - h_{fE} h_{rE}} \quad \dots(10.30)$$

(3) Common Collector Transistor Amplifier

Fig. 10.5 (a) and (b) show respectively the PNP and NPN transistor amplifiers in the common collector configuration. From Fig., it is clear that the collector terminal is common to both the input (base-collector) and output (emitter-collector) circuits. The

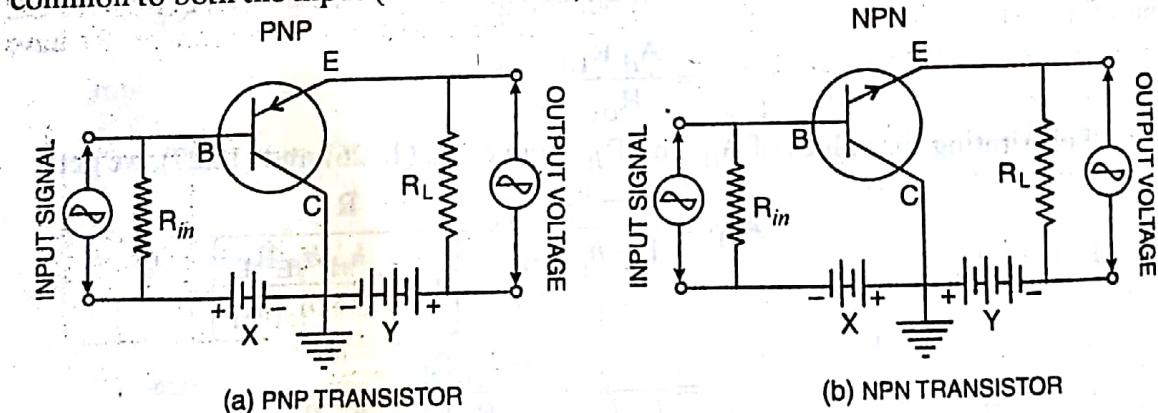


Fig. 10.5. CC amplifier (Emitter follower)

collector in the input circuit is kept in the reverse bias by the battery X, while the emitter in the output circuit is kept in the forward bias by the battery Y. The input signal is applied between the base B and collector C terminals, while the output voltage is obtained across the load resistance R_L connected in series with the battery Y in between the emitter E and collector C terminals.

Operation—On applying the a.c. signal in the input circuit, in a PNP transistor in positive half cycle of signal, the base voltage increases due to which the collector current increases and the output voltage across the load resistance also increases. On the other hand, in the remaining half cycle of input signal, the base voltage decreases due to which the output voltage across load resistance R_L also decreases. Thus, the emitter voltage follows the base voltage. This is why, a common collector transistor amplifier is also called

the *emitter follower*. Obviously, in the common collector transistor amplifier, the output voltage is in same phase as the input voltage.

Current gain — At a constant emitter-collector voltage, the ratio of change in emitter current to the corresponding change in base current is called the current gain of the common collector amplifier. It is represented by the symbol γ . Thus

$$\text{Current gain } \gamma = \left(\frac{\Delta I_E}{\Delta I_B} \right)_{V_{EC} = \text{constant}} \quad \dots(10.31)$$

Its value is nearly 50.

Voltage gain —

$$A_v = \frac{\text{Change in output potential}}{\text{Change in input potential}}$$

$$= \frac{\Delta I_E \times R_L}{\Delta I_B \times R_{in}} = \gamma \frac{R_L}{R_{in}} \quad \dots(10.32)$$

Power gain — $A_p = \text{current gain} \times \text{voltage gain}$

$$= \gamma \times \gamma \frac{R_L}{R_{in}} = \gamma^2 \frac{R_L}{R_{in}} \quad \dots(10.33)$$

Input impedance —

$$R_{in} = \left(\frac{\Delta V_B}{\Delta I_B} \right)_{V_E} \quad \dots(10.34)$$

Its value is very large ($\approx 1 \text{ M}\Omega$)

Output impedance —

$$R_{out} = \left(\frac{\Delta V_E}{\Delta I_E} \right)_{I_B} \quad \dots(10.35)$$

Its value is very low ($\approx 20 \text{ ohm}$).

Chapter 11

OSCILLATORS

In chapter 10, we have read that an oscillator is basically a positive feed back amplifier. Here first we shall reconsider the principle of feed back in amplifiers.

11.1. Principle of Feed back in Amplifiers

When a part of the output voltage of an amplifier is feed back into the input circuit, feed back is said to exist. When the feed back voltage is in phase with the input voltage, the feed back is said to be *positive or regenerative feed back*, but if the feed back voltage is in opposite phase with the input voltage, the feed back is said to be *negative or degenerative feed back*. The voltage feed back from the output of an amplifier into the input may be either proportional to the voltage across the load or it may be proportional to the current in the load. Depending upon it, the feed back is of two types : (i) voltage feed back (when the feed back voltage is proportional to the voltage across the load) and (ii) current feed back (when the feed back voltage is proportional to current in the load). Here we shall consider the principle of voltage feed back.

Fig. 11.1 illustrates the principle of voltage feed back. Let the voltage gain of an ordinary amplifier be A and the feed back part of the output voltage be B . If the input voltage is V_1 and the output voltage is V_2 , then the feed back voltage will be BV_2 .

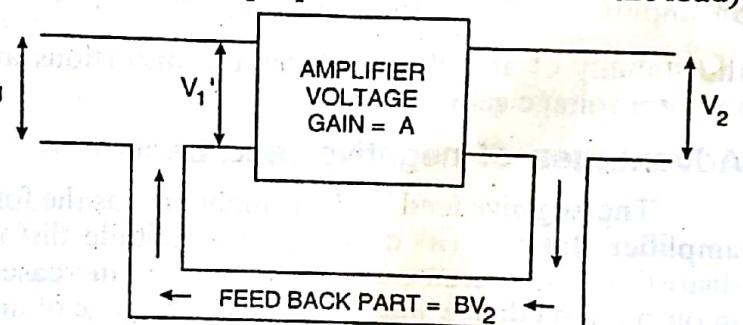


Fig. 11.1. Principle of voltage feed back

Hence the total input voltage to the amplifier is $V_1' = V_1 + BV_2$

$$\text{Voltage gain of ordinary amplifier (without feed back), } A = \frac{V_2}{V_1}$$

$$\text{Voltage gain of amplifier with feed back, } A_f = \frac{V_2}{V_1'}$$

$$\text{or } A_f = \frac{V_2}{V_1' - BV_2} = \frac{V_2/V_1'}{1 - B(V_2/V_1')} = \frac{A}{1 - BA} \quad \dots(11.1)$$

This expression relates the voltage gain A_f of feed back amplifier with the voltage gain A of the ordinary amplifier (without feed back).

It is clear that

- (i) If A is very large (i.e., $BA >> 1$), then $A_f = -\frac{1}{B}$ i.e., the voltage gain becomes independent of A . This provides a stable voltage gain.

(ii) If $|1 - BA| < 1$, i.e., B is +ve, then $A_f > A$

This is only possible when the feed back voltage increases the effective value of input voltage i.e., the feed back is positive. Thus for positive feed back $A_f = \frac{A}{1 - BA}$

(iii) If $|1 - BA| = 0$, then $A_f = \infty$ i.e., the output signal is obtained without any input signal. This is the principle of oscillator circuit.

(iv) If $|1 - BA| > 0$, i.e., B is negative, then $A_f < A$.

This is only possible if the feed back is negative. Thus for negative feed back

$$A_f = \frac{A}{1 + BA}$$

Effect of feed back on amplifier characteristics

From eqn. (11.1), it is clear that the positive feed back ($B = +ve$) in an amplifier increases its voltage gain from A to $\frac{A}{1 - BA}$ (i.e., $A_f > A$) and if the positive feed back is too much so that $1 - BA = 0$ or $B = 1/A$, the voltage gain of the amplifier becomes infinite (i.e., $A_f = \infty$). In such a case, the amplifier becomes unstable and the output can be obtained with no external input voltage i.e., the amplifier becomes an oscillator. However the positive feed back increases the distortions and noises, but it reduces the range of uniform voltage gain. On the other hand, the negative feed back ($B = -ve$) in an amplifier decreases the voltage gain from A to $\frac{A}{1 + BA}$ (i.e., $A_f < A$), but it increases the stability of amplifier, reduces the distortions and noises, increases the range of uniform voltage gain.

Advantages of negative feed back

The negative feed back in amplifiers has the following advantages : (i) increase in amplifier stability, (ii) decrease in amplitude distortion, (iii) decrease in frequency distortion, (iv) decrease in output noise, (v) increase in input impedance, (vi) decrease in output impedance and (vii) increase in range of uniform voltage gain.

(i) **Increase in amplifier stability** : The voltage gain of a negative feed back amplifier is $A_f = \frac{A}{1 + BA}$... (11.2)

If $BA > 1$, then $A_f \approx \frac{1}{B}$ i.e., independent of A .

Thus the effect of changes in supply voltage or transistor parameters etc., may have large effect on voltage gain A without feed back, but they have no effect on voltage gain A_f with negative feed back. Hence the stability of amplifier increases.

(ii) **Decrease in amplitude distortion** : Let D be the distorted output voltage of an amplifier without feed back and D' be the distorted output voltage of amplifier with negative feed back. The feed back voltage will be BD' which is amplified by the amplifier to ABD' . This amplified voltage will be in opposite phase with the voltage D . So the output voltage with negative feed back will be

$$D' = D - ABD' \text{ or } D' = \frac{D}{1 + BA} \quad \dots (11.3)$$

Obviously $D' < D$ i.e., the negative feed back decreases the amplitude distortion.

(iii) **Decreases the frequency distortion** : With negative feed back, voltage gain

$$A_f = \frac{A}{1 + BA}$$

If $BA \gg 1$, $A_f = \frac{1}{B}$. Since B is independent of frequency, so the negative feed back reduces the frequency distortion in the output.

(iv) **Decrease in noise**: The noises present in the output of amplifier are fed back to the input in opposite phase, so the noises in the output get reduced.

(v) **Increase in input impedance**: The input impedance Z_{if} with negative feed back and Z_i without feed back are related as

$$Z_{if} = (1 + BA) Z_i \quad \dots(11.4)$$

Thus the input impedance is increased.

(vi) **Decrease in output impedance**: The output impedance Z_{of} with negative feed back and Z_o without feed back are related as

$$Z_{of} = \frac{Z_o}{1 + BA} \quad \dots(11.5)$$

Thus the output impedance is reduced.

(vii) **Increase in region of uniform voltage gain**: The negative feed back in amplifiers decreases the lower cut off frequency from f_1 to f'_1 and increases the upper cut off frequency from f_2 to f'_2 . Thus it increases the band width (i.e., the frequency range) of constant voltage gain. Fig. 11.2 compares the frequency response curves with negative feed back and without feed back.

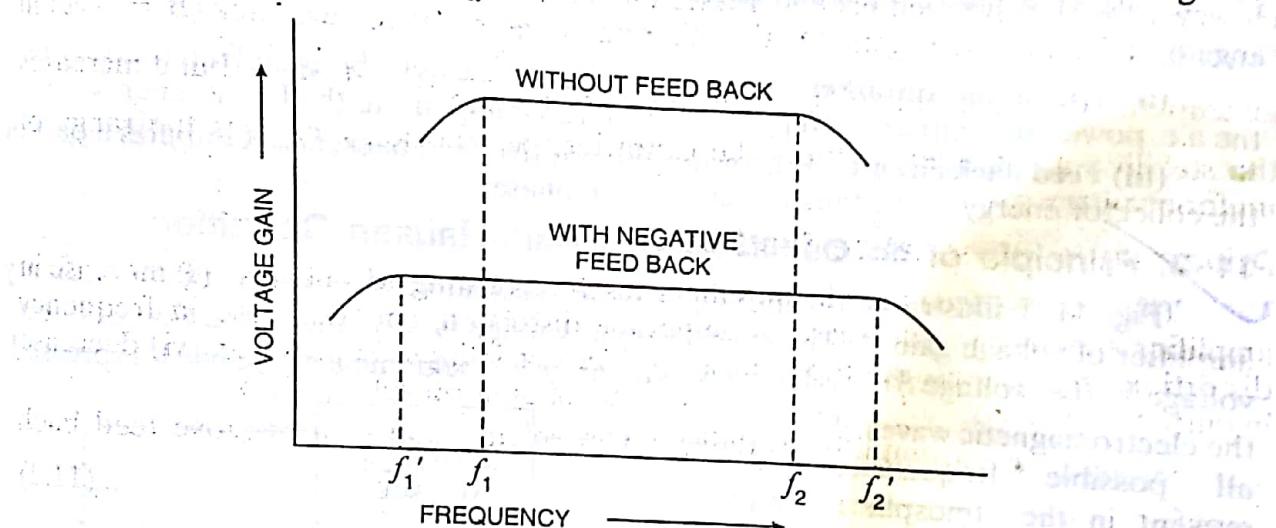


Fig. 11.2 Frequency response curves with and without negative feed back

11.2. Transistor As An Oscillator

An oscillator is a device by which we obtain the continuous electrical oscillations (i.e., alternating current or voltage) of a definite frequency (in the range from few hertz to 100 mega-hertz). Actually, it converts the d.c. power into a.c. power. In an oscillator, we obtain an alternating output signal of a particular frequency without applying any external input signal. In an oscillator, the input voltage is obtained from the d.c. source of the circuit and the output signal is obtained so long as the d.c. source is connected. Fig. 11.3 shows the difference between an amplifier and an oscillator. In

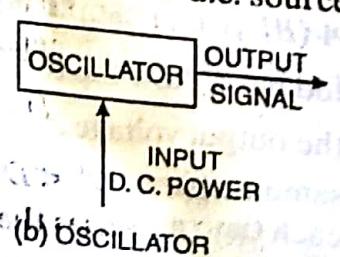
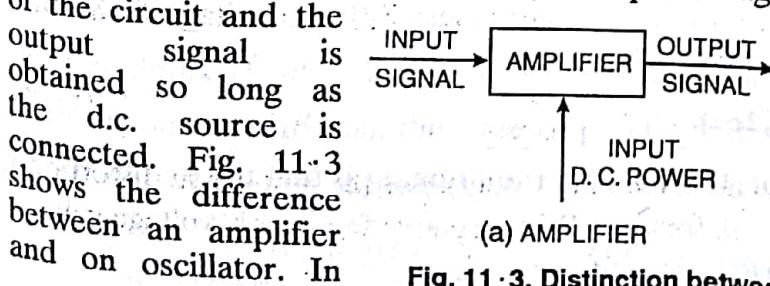


Fig. 11.3 Distinction between an amplifier and an oscillator

Fig. 11·3 (a), the a.c. output of an amplifier is obtained when input a.c. signal is applied and d.c. power is used, while in Fig. 11·3 (b), the output a.c. signal is obtained from an oscillator from the input d.c. power without any input a.c. signal.

In principle, an oscillator is a positive feed back amplifier whose voltage gain is infinite. In an amplifier, a very low external input signal is converted into a high output signal. If a part of output voltage is fed back in same phase with the input signal, it is again amplified. In this condition, the amplifier works even without any external input a.c. voltage signal, i.e., the amplifier then works as an oscillator. Thus, *an oscillator is an amplifier in which the input signal is not obtained from a separate a.c. source, but it is obtained by the positive feed back of its own output signal.*

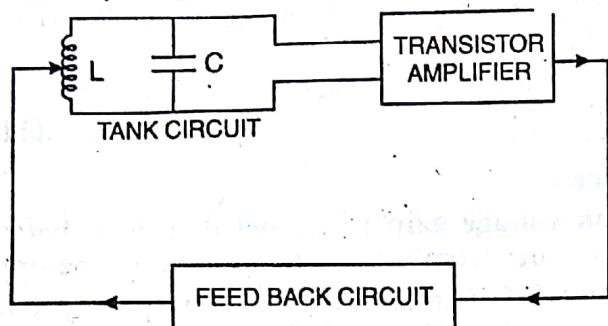


Fig. 11·4. Main parts of an oscillator

circuit.

(ii) **Transistor amplifier**—It converts the d.c. power obtained from battery into the a.c. power and imparts it to the tank circuit to compensate the loss in energy.

(iii) **Feed back circuit**—It provides the positive feed back, i.e., it imparts a part of the collector energy to the tank circuit in same phase.

11·3. Principle of an Oscillator and Bark-Hausen Condition

Fig. 11·5 illustrates the principle of an oscillator. It consists of an ordinary amplifier of voltage gain A . The primary input voltage is zero and B fraction of output voltage V_2 (i.e., voltage BV_2) is fed back as input. In the beginning, as the key K is pressed, the electromagnetic waves of all possible frequencies present in the atmosphere cause electrical pulses in the circuit, which are amplified by the amplifier and we get the output voltage V_2 . Now B fraction of the output voltage V_2 (i.e., voltage BV_2) is fed back to the input so that the total input voltage now is BV_2 , which is again amplified and the output voltage is $A(BV_2) = ABV_2$. Again a fraction B of this voltage ABV_2 [i.e., $B(ABV_2) = AB^2V_2$] is fed back. Now the total input voltage is AB^2V_2 which is amplified by the amplifier to get the output voltage $A(AB^2V_2) = A^2B^2V_2$. This process continues. But to obtain waves of same amplitude from an oscillator, the essential requirement is that the output voltage each time must be the same, i.e.,

$$V_2 = ABV_2 = A^2B^2V_2 = \dots$$

Fig. 11·4 shows the main parts of an oscillator. Its main parts are :

- (i) Tank or resonant circuit,
- (ii) Transistor amplifier and (iii) Feed back circuit.

(i) **Tank or resonant circuit**—In this circuit, an inductive coil L is connected in parallel with a condenser C . The values of L and C determine the frequency of oscillations of the

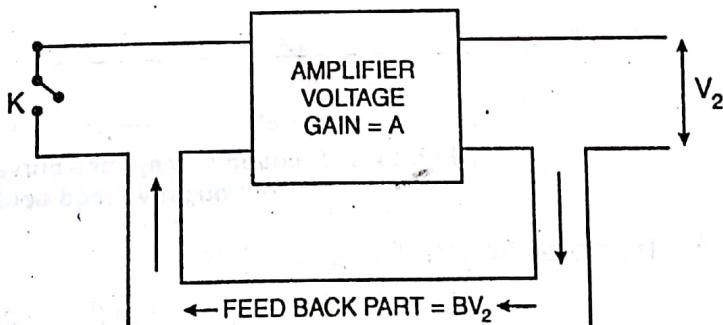


Fig. 11·5. Principle of an oscillator

$$\text{or } AB = 1 \text{ or } B = 1/A$$

Thus without any input voltage, to obtain oscillations of same amplitude, the essential condition is $AB = 1$. This is called the *Bark-Hausen's condition* for self maintained oscillations.

It is clear from the above discussion that on pressing the key K , there can be waves of each possible frequency at the input and output terminals. But from an oscillator, we want to obtain oscillations only of a definite (particular) frequency at the output terminals. In addition, we require that the frequency of these oscillations must be prior known and if needed, it could be adjusted. For this purpose, a resonant circuit (such as LC circuit) is used with the oscillator. When an inductance L and a condenser C are connected in series or in parallel and an electrical disturbance is created by on or off of oscillations are produced in the circuit (*i.e.*, charging and discharging of condenser takes place. While charging of condenser, whole of the energy is stored in form of electrostatic potential energy of condenser and while discharging, this energy is stored in form of magnetic potential energy of inductance). The frequency of these oscillations is

$f = \frac{1}{2\pi\sqrt{LC}}$ (if ohmic resistance of circuit is zero). If the ohmic resistance of circuit is zero, the amplitude of oscillations remains constant. But in actual practice, there is some loss of energy due to resistance of circuit, therefore the amplitude of these electrical oscillations continuously decreases and the frequency of oscillations also decreases to

$$f = \frac{1}{2\pi} \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \text{ where } R \text{ is the ohmic resistance of the circuit.}$$

Now if the same amount of energy is continuously supplied to the circuit as the amount of energy loss, the amplitude of electrical oscillations will remain constant. In an oscillator, due to amplification action of transistor, the circuit continuously gets energy. This energy is compensated by the positive feed back of a part of output signal and then by its amplification.

The frequency of output oscillations can be adjusted, as required, by changing the value of either L or C in the resonant circuit.

11.4. Requirements For An Oscillator

Following are the main requirements for an oscillator circuit :

- (1) Transistor amplifier in class *A* condition and in common emitter mode* connected with a positive feed back circuit such that its feed back ratio $B = 1/A$ where A is the voltage gain of ordinary amplifier. It provides energy to the tank circuit for maintaining the sustained oscillations.
- (2) A non-linear circuit to fix the amplitude of oscillations.

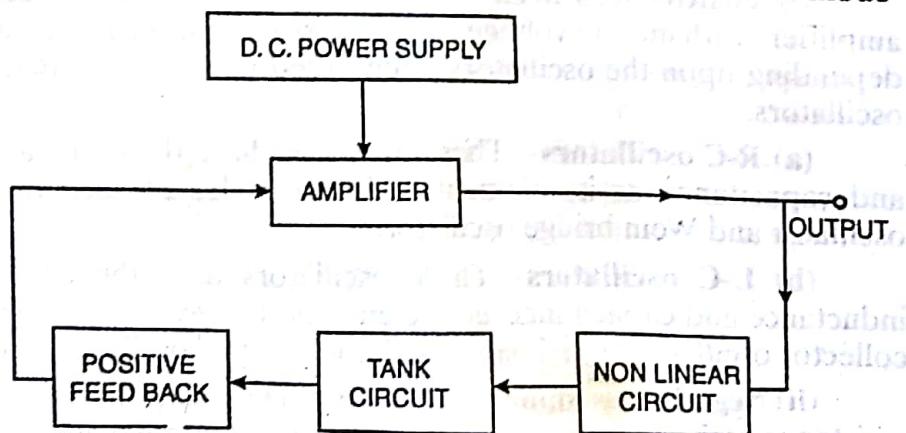


Fig. 11.6. Block diagram of an oscillator

* In the CE mode, since there is a phase difference of 180° between the output voltage and the input voltage of a single transistor amplifier, therefore to have the input voltage and the output voltage in the same phase (*i.e.*, phase difference either 0° or 360°), CE transistor amplifiers are used in two stages.

(3) A resonant circuit (also called the tank circuit) to produce oscillations of a constant frequency.

(4) A d.c. power supply in form of source of energy.

The block diagram of an oscillator is shown in Fig. 11·6.

Use of oscillators—Oscillators are mainly used in radio and television transmitter, receiver, radar and other communication devices.

11·5. Classification of Oscillators

Oscillators are divided on two basis : (A) on the basis of frequency range and (B) on the basis of wave form produced by them.

(A) According to the frequency range, oscillators are divided in the following classes :

	Class	Frequency range
(i)	Audio frequency oscillators (A. F. oscillators)	Few hertz to 20 kilo-hertz
(ii)	Radio frequency oscillators (R. F. oscillators)	20 kHz to 30 MHz
(iii)	Very high frequency oscillators (V. H. F. oscillators)	30 MHz to 300 MHz
(iv)	Ultra high frequency oscillators (U. H. F. oscillators)	300 MHz to 3000 MHz
(v)	Micro-wave oscillators	Above 3000 MHz

(B) Depending upon the wave form produced, the oscillators are divided into two categories :

(1) Sinusoidal oscillators and (2) Non-sinusoidal oscillators.

(1) **Sinusoidal oscillators**—These oscillators generate the oscillations of sine wave form of a definite frequency. Depending upon the mechanism used, they are further classified in the following four groups : (i) positive feed back oscillators, (ii) negative resistance oscillators, (iii) crystal oscillators and (iv) magneto-striction oscillators.

(i) **Positive feed back oscillators**—These oscillators are the positive feed back amplifiers with infinite voltage gains. These oscillators are further divided in two groups depending upon the oscillatory circuit used in them : (a) R-C oscillators and (b) L-C oscillators.

(a) **R-C oscillators**—These oscillators have the oscillatory circuit with resistance and capacitance as its elements. The examples of such oscillators are phase shift oscillator and Wein bridge oscillator.

(b) **L-C oscillators**—These oscillators have the oscillatory tank circuit with inductance and capacitance as its elements. The examples of such oscillators are tuned collector oscillator, tuned base oscillator, Hartley oscillator and Colpitt oscillator.

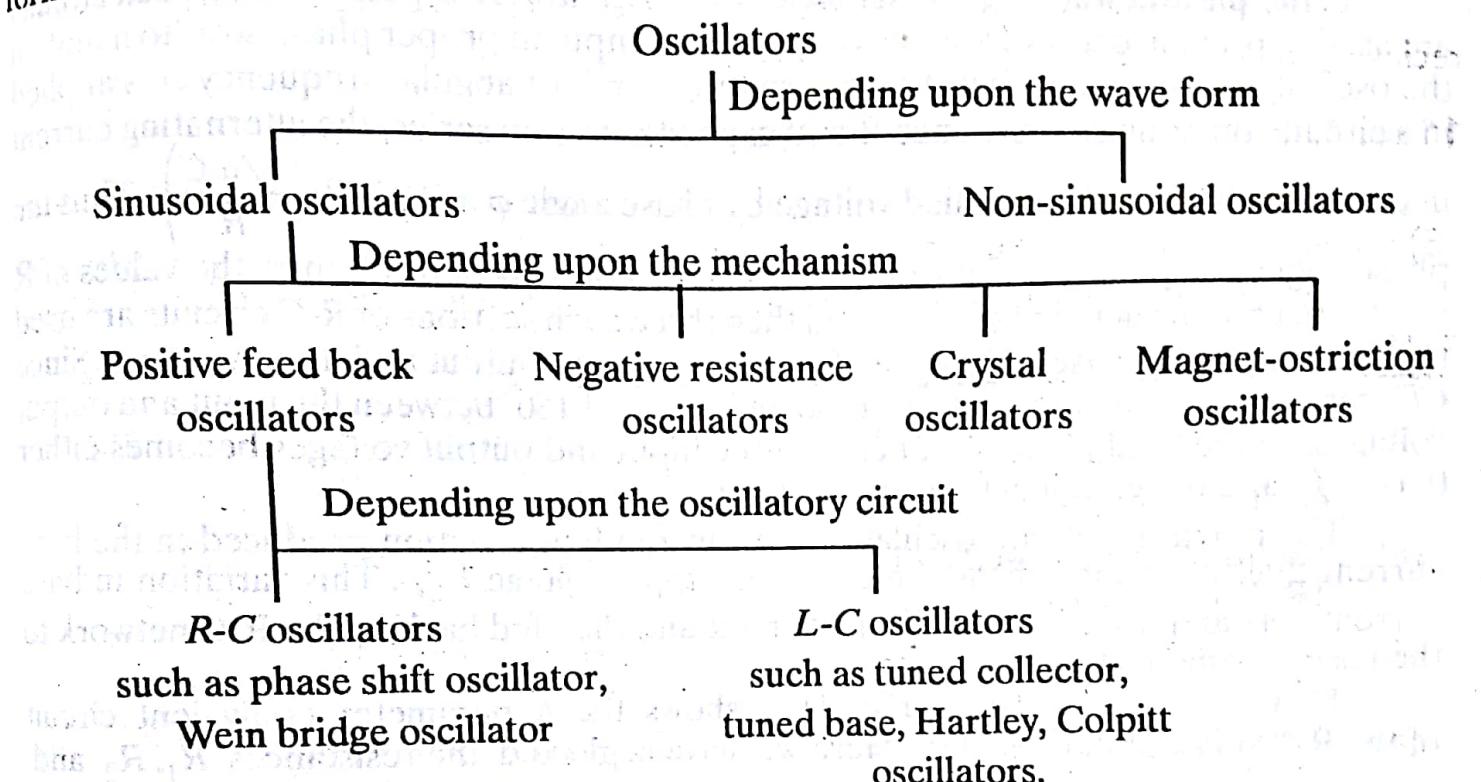
(ii) **Negative resistance oscillators**—These oscillators employ a device of negative resistance such as tunnel diode, thyristor etc., in parallel with the tank circuit.

(iii) **Crystal oscillators**—These oscillators use crystals such as quartz, tourmaline etc., and are based on piezo electric effect. They maintain the oscillations to a fixed frequency.

(iv) **Magneto-striction oscillators**—These oscillators are based on the principle that when there is change in magnetisation of a magnetic substance, the substance either contracts or expands.

(2) **Non-sinusoidal oscillators** – These oscillators generate oscillations of non-sinusoidal wave form such as square or sawtooth wave form. Such oscillators are used in television, radar, oscilloscope etc. as electronic control circuits.

For the sake of convenience, the classification of oscillators depending upon wave form can be represented as follows :



Here we shall limit ourselves only to the positive feed back oscillators.

11.10. Hartley Oscillator

The Hartley oscillator is one of the most frequently used oscillator as a local oscillator in radio receiver. There are two forms of Hartley oscillator : (i) series fed Hartley oscillator and (ii) shunt fed Hartley oscillator.

(i) **Series fed Hartley oscillator**—The circuit diagram of series fed Hartley oscillator is shown in Fig. 11.17 in which the transistor has been used in the common emitter mode and a single tapped coil L having two parts L_1 and L_2 is used in the tank

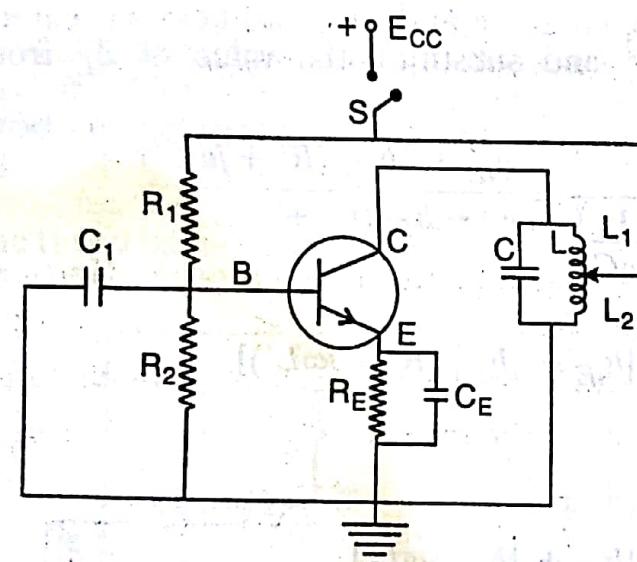


Fig. 11.17. Series fed Hartley oscillator

supply voltage E_{CC} provide the necessary bias conditions for the circuit.

(ii) **Shunt fed Hartley oscillator**—The circuit diagram of a shunt fed Hartley oscillator is shown in Fig. 11.18 in which the resistances R_1 , R_2 and R_E and the supply voltage E_{CC} provide the required biasing to the transistor. The resonant or tank circuit used in it has a variable condenser C and two inductive coils L_1 and L_2 . The coils L_1 and L_2 are coupled together inductively and their combination forms an auto-transformer. The condenser C_2 prevents the d.c. component from the collector in going to the tank circuit and provides the path for the a.c. component. The radio frequency

circuit. The part L_1 of the coil is in the collector circuit and the part L_2 is in the base circuit. The amount of feed back is determined by the ratio L_2/L_1 ($= n_2/n_1$ i.e., the ratio of number of turns in L_2 and L_1). The feed back voltage is fed to the base through the condenser C_1 which blocks the d.c. from the collector to base through the inductance L_2 . The coil L and the condenser C forms the tank circuit which determines the frequency of oscillations. The coil L is tapped at the proper point to sustain oscillations in the tank circuit. The resistances R_1 , R_2 , R_E and the

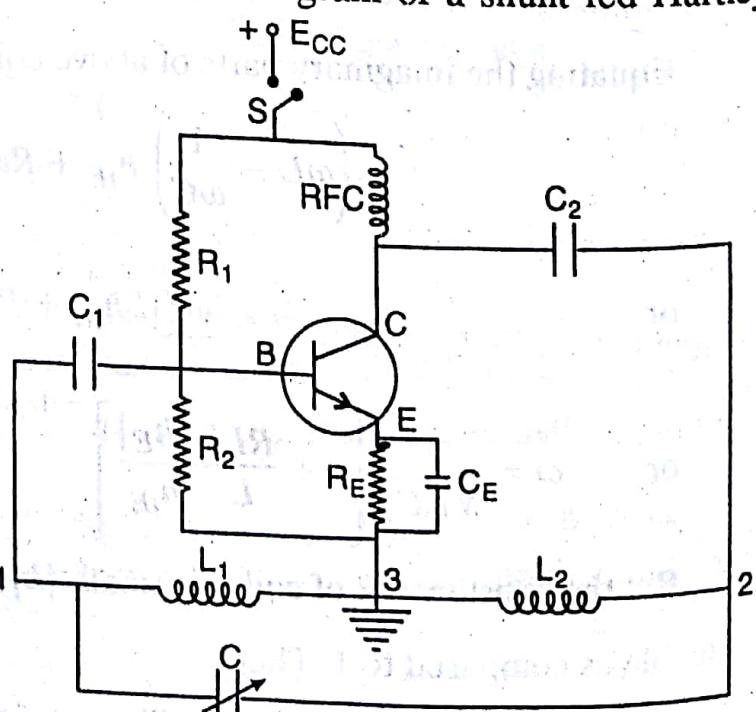


Fig. 11.18. Shunt fed Hartley oscillator

choke RFC behaves like a d.c. load for the collector and prevents the a.c. component to pass to the supply voltage E_{CC} . The condenser C_1 is the blocking condenser for the base circuit and obstructs it from going to the resistance R_E .

The shunt fed Hartley oscillator is considered to be superior than the series fed Hartley oscillator.

Working—As the switch S of the collector supply voltage E_{CC} is made on, the transistor gets biased through the resistances R_1 and R_2 . As a result, the collector current starts increasing which charges the condenser C . When the condenser C is fully charged, it starts discharging through the coils L_1 and L_2 , due to which damped oscillations start in the tank circuit. The voltage produced across the coil L_1 due to flow of the oscillatory current in the tank circuit gets applied at the base-emitter junction of the transistor which is obtained in the collector circuit after amplification. The feed back part from the output circuit (collector-emitter) reaches the input circuit (base-emitter) by the auto transformer action. Thus, the energy in the tank circuit is fed back by the mutual inductance M between the coils L_1 and L_2 . This energy compensates the loss in energy during the damped oscillations. As a result, steady and maintained oscillations occur in the circuit. The frequency of oscillations is given by the following relation :

$$f = \frac{1}{2\pi \sqrt{LC}} \text{ where } L = L_1 + L_2 + 2M \quad \dots(11 \cdot 32)$$

Here M is the mutual inductance between the coils L_1 and L_2 .

Mathematical analysis : Fig. 11.19 shows the equivalent circuit of the Hartley oscillator in which Z_1 , Z_2 and Z_3 represent the inductive and capacitive reactances namely $Z_1 = j\omega L_1 + j\omega M$, $Z_2 = j\omega L_2 + j\omega M$ and $Z_3 = -j/\omega C$ (where M is mutual inductance between the coils L_1 and L_2). Assuming the reverse voltage parameter h_{rE} of the transistor to be negligible, the feed back source of e.m.f. $h_{rE} V_0$ has not been considered. Further the output admittance h_{oE} in parallel with Z_2 has been neglected, since the output admittance parameter h_{oE} is very small (so impedance $1/h_{oE}$ is very large.) In the Fig. I_B , I_C , I_1 and I_2 are base current, collector current, output and input currents respectively.

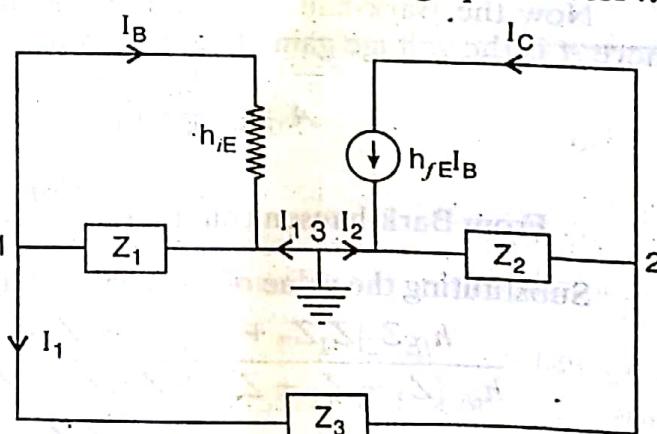


Fig. 11.19. Equivalent circuit of Hartley oscillator

From Fig. 11.19, it is clear that the input resistance h_{iE} and impedance

Z_1 are in parallel, their equivalent impedance is $Z' = \frac{Z_1 h_{iE}}{Z_1 + h_{iE}}$

The equivalent impedance Z' is in series with Z_3 and then in parallel with Z_2 . Thus the load impedance Z_L between the output terminals 2 and 3 is given as

$$\frac{1}{Z_L} = \frac{1}{Z' + Z_3} + \frac{1}{Z_2}$$

$$\begin{aligned}
 \text{or } \frac{1}{Z_L} &= \frac{1}{Z_1 h_{iE}} + \frac{1}{Z_2} \\
 &= \frac{Z_1 + h_{iE}}{Z_1 h_{iE} + Z_3 (Z_1 + h_{iE})} + \frac{1}{Z_2} \\
 &= \frac{Z_2 (Z_1 + h_{iE}) + Z_1 h_{iE} + Z_3 (Z_1 + h_{iE})}{Z_2 [Z_1 h_{iE} + Z_3 (Z_1 + h_{iE})]} \\
 &= \frac{Z_2 [Z_1 Z_3 + h_{iE} (Z_1 + Z_3)]}{h_{iE} (Z_1 + Z_2 + Z_3) + Z_1 (Z_2 + Z_3)} \quad \dots(11.33)
 \end{aligned}$$

Now output voltage across the terminals 2 and 3 is

$$\begin{aligned}
 V_0 &= -I_1 (Z' + Z_3) = -I_1 \left[\frac{Z_1 h_{iE}}{Z_1 + h_{iE}} + Z_3 \right] \\
 &= -I_1 \left[\frac{Z_1 Z_3 + h_{iE} (Z_1 + Z_3)}{Z_1 + h_{iE}} \right] \quad \dots(11.34)
 \end{aligned}$$

The feed back voltage to the input terminals 1 and 3 is

$$BV_0 = -I_1 Z' = -I_1 \frac{Z_1 h_{iE}}{Z_1 + h_{iE}} \quad \dots(11.35)$$

From eqns. (11.34) and (11.35),

$$\text{Feed back ratio } B = \frac{Z_1 h_{iE}}{Z_1 Z_3 + h_{iE} (Z_1 + Z_3)} \quad \dots(11.36)$$

Now the Bark-hausen condition for the maintenance of oscillations is $AB = 1$, where A is the voltage gain of the CE amplifier without feed back which is given as

$$A = -\frac{h_{fE}}{h_{iE}} Z_L$$

$$\therefore \text{From Bark-hausen condition } \frac{-h_{fE}}{h_{iE}} Z_L \times \frac{Z_1 h_{iE}}{Z_1 Z_3 + h_{iE} (Z_1 + Z_3)} = 1$$

Substituting the value of Z_L from eqn. (11.33), we get

$$\frac{h_{fE} Z_2 [Z_1 Z_3 + h_{iE} (Z_1 + Z_3)]}{h_{iE} (Z_1 + Z_2 + Z_3) + Z_1 (Z_2 + Z_3)} \times \frac{Z_1}{Z_1 Z_3 + h_{iE} (Z_1 + Z_3)} = -1$$

$$\frac{h_{fE} Z_1 Z_2}{h_{iE} (Z_1 + Z_2 + Z_3) + Z_1 (Z_2 + Z_3)} = -1$$

$$\text{or } \frac{h_{iE} (Z_1 + Z_2 + Z_3) + Z_1 (Z_2 + Z_3)}{h_{iE} (Z_1 + Z_2 + Z_3) + Z_1 (Z_2 + Z_3)} = -h_{fE} Z_1 Z_2$$

$$\text{or } h_{iE} (Z_1 + Z_2 + Z_3) + Z_1 Z_2 (1 + h_{fE}) + Z_1 Z_3 = 0 \quad \dots(11.37)$$

This is the general equation of L-C oscillator.

Now substituting the values of Z_1, Z_2 and Z_3 (i.e., $Z_1 = j\omega L_1 + j\omega M$, $Z_2 = j\omega L_2 + j\omega M$ and $Z_3 = -j/\omega C$), we get

$$\begin{aligned}
 h_{iE} \left[(j\omega L_1 + j\omega M) + (j\omega L_2 + j\omega M) - \frac{j}{\omega C} \right] \\
 + (j\omega L_1 + j\omega M) (j\omega L_2 + j\omega M) (1 + h_{fE}) + (j\omega L_1 + j\omega M) \times \left(\frac{-j}{\omega C} \right) = 0
 \end{aligned}$$

$$\text{or } j\omega h_{fE} \left[L_1 + L_2 + 2M - \frac{1}{\omega^2 C} \right] - \omega^2 (L_1 + M)(L_2 + M)(1 + h_{fE}) + \frac{L_1 + M}{C} = 0$$

$$\text{or } j\omega h_{fE} \left[L_1 + L_2 + 2M - \frac{1}{\omega^2 C} \right] - \omega^2 (L_1 + M) \left[(L_2 + M)(1 + h_{fE}) - \frac{1}{\omega^2 C} \right] = 0$$

...(11.38)

Equating the imaginary parts on both sides of eqn. (11.38), we get

$$L_1 + L_2 + 2M - \frac{1}{\omega^2 C} = 0$$

$$\text{or } \omega^2 C = \frac{1}{L_1 + L_2 + 2M}$$

$$\text{or } \omega = \frac{1}{\sqrt{(L_1 + L_2 + 2M) C}}$$

$$\therefore \text{Frequency of oscillation } f = \frac{1}{2\pi \sqrt{(L_1 + L_2 + 2M) C}} \quad \dots(11.39)$$

Now equating the real parts on both sides of eqn. (11.38), we get

$$(L_2 + M)(1 + h_{fE}) - \frac{1}{\omega^2 C} = 0$$

$$\text{or } 1 + h_{fE} = \frac{1}{\omega^2 C (L_2 + M)}$$

$$\text{But } \omega^2 C = \frac{1}{L_1 + L_2 + 2M}$$

$$\therefore 1 + h_{fE} = \frac{L_1 + L_2 + 2M}{L_2 + M} = \frac{(L_1 + M) + (L_2 + M)}{(L_2 + M)}$$

$$= \frac{L_1 + M}{L_2 + M} + 1$$

$$\text{or } h_{fE} = \frac{L_1 + M}{L_2 + M} \quad \dots(11.40)$$

This gives the condition for the sustained oscillations in Hartley oscillator. Thus, the oscillations can be adjusted just by changing the tapping point of the coil which does not disturb the frequency of oscillation since $(L_1 + L_2)$ remains the same.

Uses — The Hartley oscillator is widely used as the local oscillator. The reasons are : (i) the frequency of oscillations can be easily varied by using the variable capacitor C and (ii) a single coil can be easily designed.

11.11. Colpitt Oscillator

Colpitt oscillator is similar to the shunt fed Hartley oscillator with the only difference that in the Hartley oscillator, the inductive coil of the tank circuit is tapped in two parts L_1 and L_2 whereas in Colpitt oscillator, two capacitors C_1 and C_2 are used with a common coil L in the tank circuit and the two capacitors are tapped at the centre. Fig. 11.20 shows the NPN transistor in CE mode used as Colpitt oscillator.

Circuit—Fig. 11·20 shows the circuit of Colpitt oscillator.

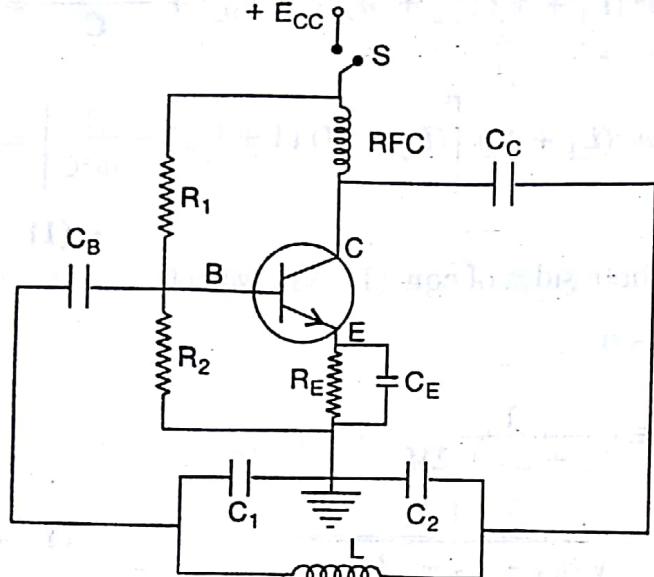


Fig. 11·20. Colpitt oscillator

The resistances R_1 , R_2 and R_E provide proper biasing to the transistor. C_E is the emitter by pass capacitor. The radio frequency choke coil RFC behaves as load in the collector circuit and it prevents a.c. component of current from the collector supply voltage E_{CC} . The tank circuit is composed of condensers C_1 and C_2 tapped at its centre and coil L . The condenser C_C in the collector circuit obstructs the d.c. component of current and passes only the a.c. component of current from collector to the tank circuit. The condenser C_B is used to feed back the voltage across the coil L from collector circuit to the base circuit.

Operation—As the switch S is closed, the collector current begins to increase due to which the condensers C_1 and C_2 begin to charge. When they get fully charged, they discharge through the coil L and thus oscillations start in the tank circuit. The oscillatory current in the tank circuit produces an a.c. voltage across the condenser C_1 which is fed back at the base-emitter junction and gets amplified by the transistor. This amplified voltage in the collector circuit overcomes the loss of energy in the tank circuit.

Mathematical analysis—Fig. 11·21 shows the equivalent hybrid parameter circuit of the Colpitt oscillator which is identical to that of Hartley oscillator.

In Fig. 11·21, $Z_1 = \frac{1}{j\omega C_1}$, $Z_2 = \frac{1}{j\omega C_2}$ and $Z_3 = j\omega L$

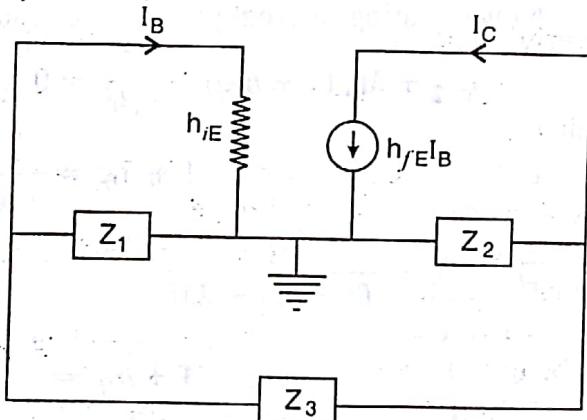


Fig. 11·21. Equivalent h parameter circuit of Colpitt oscillator

From eqn. (11·37), the general equation of L-C oscillator is

$$h_{fE} (Z_1 + Z_2 + Z_3) + Z_1 Z_2 (1 + h_{fE}) + Z_1 Z_3 = 0$$

Substituting the values of Z_1 , Z_2 and Z_3 , we get

$$\begin{aligned} h_{fE} \left[\frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} + j\omega L \right] + \frac{1}{j\omega C_1} \times \frac{1}{j\omega C_2} (1 + h_{fE}) + \frac{1}{j\omega C_1} \times j\omega L &= 0 \\ \text{or } -jh_{fE} \left[\frac{1}{\omega C_1} + \frac{1}{\omega C_2} - \omega L \right] - \frac{(1 + h_{fE})}{\omega^2 C_1 C_2} + \frac{L}{C_1} &= 0 \end{aligned} \quad (11·41)$$

Equating the imaginary parts of eqn. (11.41), we get

$$\frac{1}{\omega C_1} + \frac{1}{\omega C_2} - \omega L = 0 \text{ or } \frac{1}{C_1} + \frac{1}{C_2} = \omega^2 L$$

$$\text{or } \omega^2 = \frac{C_1 + C_2}{LC_1 C_2} \quad \text{or } \omega = \sqrt{\frac{C_1 + C_2}{LC_1 C_2}}$$

$$\therefore \text{Frequency of oscillations } f = \frac{1}{2\pi} \sqrt{\frac{C_1 + C_2}{LC_1 C_2}} \quad \dots(11.42)$$

Equating the real part of eqn. (11.41), we get

$$-\frac{(1 + h_{fE})}{\omega^2 C_1 C_2} + \frac{L}{C_1} = 0 \text{ or } 1 + h_{fE} = \omega^2 L C_2$$

$$\therefore h_{fE} = \frac{(C_1 + C_2)}{LC_1 C_2} \times LC_2 - 1 = \frac{C_1 + C_2}{C_1} - 1 = \frac{C_2}{C_1} \quad \dots(11.43)$$

This is the condition for self maintained oscillations.

Uses – The Colpitt oscillator is widely used in commercial signal generators above 1 MHz and also sometimes as a local oscillator in radio receiver.

Relative merits and demerits of R-C and L-C oscillators

1. The frequency stability of R-C oscillators is good, but it is not good in L-C oscillators.
2. R-C oscillators can only be used to generate low frequencies, while L-C oscillators cannot be used to generate the low (audible) frequencies.
3. R-C oscillators do not require inductive coils or transformers, whereas the L-C oscillators need them.
4. R-C oscillators cannot be used to generate high frequencies, but L-C oscillators can be used to generate high frequencies.
5. In R-C oscillators, it is difficult to change the frequency of oscillations, while it is easy to change the frequency of oscillations in L-C oscillators.

SOLVED EXAMPLES

Ex. 1. The voltage gain of an amplifier without feed back is 3000. If a negative feed back is applied with feed back factor 0.01, find the voltage gain with feed back.

Sol. Given, $A = 3000, B = 0.01$

With negative feed back

$$A_f = \frac{A}{1 + BA} = \frac{3000}{1 + (0.01 \times 3000)} = \frac{3000}{31} = 96.8$$

Ex. 2. The voltage gain of a transistor amplifier is 40 and its input resistance is $2 \text{ k}\Omega$. Calculate the voltage gain and input resistance when 10% negative feed back is given to the amplifier.

Sol. Given, $A = 40, B = \frac{10}{100} = 0.1, Z_i = 2 \text{ k}\Omega$

$$\text{With negative feed back, } A_f = \frac{A}{1 + BA} = \frac{40}{1 + (0.1 \times 40)} = \frac{40}{5} = 8$$

$$\begin{aligned} \text{Input resistance with feed back } Z_{if} &= Z_i (1 + BA) = 2 [1 + (0.1 \times 40)] \text{ k}\Omega \\ &= 10 \text{ k}\Omega \end{aligned}$$