

Treble

The treble control has a range of +12dB to -12 dB in 3 dB steps. The treble is set using bits D0-D3. **IMPORTANT:** Bits D4 - D7 must be set to 1.

dB	D3-D0
12	F
:	:
12	A
:	:
0	6
:	:
-12	2
:	:
-12	0

Register #7

Output Mode

D7	D6	D5	D4	D3	D2	D1	D0
1	1	MU	ST-MONO		SOURCE		

Register #8

This register controls the final output. This final output section takes as its input the output from the mixing section. SOURCE indicates which channels from the mixer are selected for final output. If only one input channel is selected, it is directed to both output channels. Stereo input results in stereo output.

SOURCE	Channels
6	Left and right
4	Right only
2	Left only

ST-MONO selects the type of effect applied to the final output:

ST-MONO	Effect
3	Spatial stereo
2	Pseudo stereo
1	Linear stereo
0	Forced mono

Linear stereo is ordinary, stereo output with no effects added. The spatial and pseudo stereo effects will be useful primarily when the original sources are monophonic. If the surround option is present, the output signal is modified after mixing and the attributes of this register are then applied.

Setting MU enables muting; clearing it disables muting.

IMPORTANT: Bits D6 and D7 must be set to 1.

Mixing Volumes

Registers 9 through 10h are individual volume control registers and constitute the mixing section of the card. 128 different linear volume levels are possible, ranging from 128 (silent) to 255 (maximum gain). Note that writing values less than 128 will result in a signal with negative polarity and should be avoided because the resulting signal may cancel out another signal of opposite polarity.

Audio Selection

D7	D6	D5	D4	D3	D2	D1	D0
X	X	SPKR	X	MFB	XMO	FLT0	FLT1

Register #11h

The Gold card uses antialiasing filters during sampling and playback to ensure maximum audio quality. Because these operations are mutually exclusive on a given channel, the same antialiasing filter is used for sampling and playback. When FLT0 is set, the filter for Channel 0 (left) is set for input (recording); clearing the bit sets the filter for output (playback). FLT1 operates similarly, but is applied to Channel 1 (right).

Normally, the Aux input on the card is sampled in stereo on both channels at the same time. This stereo input can be turned monophonic and sampled on Channel 0 by setting XMO. Clearing XMO returns Aux input to its normal state.

When the telephone option of the Gold card is present, microphone input is directed to both the loudspeaker output as well as the telephone when MFB is cleared. However, this could cause feedback to occur. When MFB is set, the microphone signal is not directed to the loudspeaker output, thus eliminating possible causes of feedback. Although this feature is intended for use with the telephone option, it is operational at all times so that setting MFB always removes the microphone from the final output.

The internal audio speaker from the PC can be mixed directly with the final audio signal of the Gold Card. When SPKR is cleared, the signal is disconnected; when set it is connected.

Register 12h

Register 12h is unused and should be ignored or set to 0 otherwise.

Audio IRQ/DMA Select - Channel 0

D7	D6	D5	D4	D3	D2	D1	D0
DENO	DMA SEL 0		AEN		INT SEL A		

Register #13h

Audio interrupts (FM, sampling and telephone) are enabled when AEN is set. The following values for INT SEL A select the corresponding interrupt line:

Mixer and Setup Features

Register Reference

INT SEL A	IRQ
0	3
1	4
2	5
3	7
4	10
5	11
6	12
7	15

Only IRQ 3, 4, 5, and 7 are available on model Gold 1000. All listed interrupts are available on the Gold 2000 and the Gold 2000MC.

DMA for sampling channel 0 is enabled when DEN0 is set. The following values for DMA SEL 0 select the corresponding DMA line:

DMA SEL 0	DMA Line
0	0
1	1
2	2
3	3

Only DMA 1, 2 and 3 are available on model Gold 1000. All listed DMA lines are available on the Gold 2000 and the Gold 2000MC.

DMA Select - Channel 1

D7	D6	D5	D4	D3	D2	D1	D0
DEN1		DMA SEL 1		X	X	X	X

Register #14

DMA for sampling channel 1 is enabled when DEN1 is set. The following values for DMA SEL 1 select the corresponding DMA line:

DMA SEL 1	DMA Line
0	0
1	1
2	2
3	3

Only DMA 1, 2 and 3 are available on the model Gold 1000. All listed DMA lines are available on the Gold 2000 and the Gold 2000MC.

Audio Relocalisation

D7	D6	D5	D4	D3	D2	D1	D0
X	AUDIO RELOCATE						

Register #15h

This register indicates the port address for the audio section (FM, sampling, control chip). Writing here immediately relocates the audio section to the specified address. The AUDIO RELOCATE value is the port address divided by eight. This forces the address to be on an 8-byte boundary.

The audio section uses 8 port addresses. It is the first of these 8 addresses which is used in this register. Note that the control chip address is considered to be part of the audio section, so that the address of the control chip changes as soon as this register is modified.

The following is the default configuration for the audio section:

Address	Section
388h, 389h	FM Bank 0
38Ah, 38Bh	FM Bank 1, Control Chip
38Ch, 38Dh	Sampling Channel 0
38Eh, 38Fh	Sampling Channel 1

Mixer and Setup Features

Register Reference

SCSI IRQ/DMA Select

D7	D6	D5	D4	D3	D2	D1	D0
DENS		DMA SEL S		SIEN		INT SEL S	

Register #16h

SCSI interrupts are enabled when SIEN is set. The following values for INT SEL S select the corresponding interrupt line:

INT SEL S	IRQ
0	3
1	4
2	5
3	7
4	10
5	11
6	12
7	15

Only IRQ 3, 4, 5, and 7 are available on the model Gold 1000. All listed interrupts are available on the Gold 2000 and the Gold 2000MC.

SCSI DMA is enabled when DENS is set. The following values for DMA SEL S select the corresponding DMA line:

DMA SEL S	DMA Line
0	0
1	1
2	2
3	3

Only DMA 1, 2 and 3 are available on model GOLD 1000. All listed DMA lines are available on the Gold 2000 and the Gold 2000MC.

SCSI Relocalization

D7	D6	D5	D4	D3	D2	D1	D0
X	SCSI RELOCATE						

Register #17h

This register indicates the port address for the SCSI section. Writing here immediately relocates the SCSI section to the specified address. The SCSI RELOCATE value is the port address divided by eight. This forces the address to be on an 8-byte boundary. The SCSI section uses 8 port addresses. It is the first of these 8 addresses which is used in this register. The default configuration has the SCSI section at addresses 390h to 397h.

Surround

D7	D6	D5	D4	D3	D2	D1	D0
SURROUND							

Register #18h

The surround sound option of the card is accessed via this register. It will be documented at a later date.

This chapter explains the features of the new FM synthesis chip, the YM262, on the Ad Lib Gold cards. This chip is similar to the YM3812, the chip on the original Ad Lib card, and contains a compatibility mode to emulate the YM3812. Because of this similarity, the first part of this section discusses the features of the YM3812. Those of you who are already familiar with this chip may wish to skip this section and proceed to *Programming the YM262*, which discusses the differences between the two chips.

Programming the YM3812

(NOTE: This section is reproduced from the original Ad Lib Synthesizer Card Programmer's Manual. It is necessary for understanding the functioning of the new FM chip, the YMF262. If you are already familiar with this material, you may wish to proceed to the following section which discusses the YMF262.)

This section provides information about the Ad Lib Music Synthesizer Card for advanced programmers who wish to program it directly. There is information on the components of the card, a technical description of the operators, the input / output map and a register reference section.

The Ad Lib Music Synthesizer Card

The card is equipped with a vibrato oscillator, an amplitude oscillator (tremolo), a noise generator which allows for the combination of a number of frequencies, two programmable timers, composite sine wave synthesis and 18 operators.

A white noise generator is used to create rhythm sounds. This white noise generator uses voices 7 and 8 (melodic voices), frequency information (Block, F-Number, Multi), and the proper phase output. Various rhythm sounds are produced by combining this output signal with white noise. The resulting signal is then sent to the operators. Experience has shown that the best ratio for the two frequencies is 3:1 (melodic voice 7 frequency = 3 times melodic voice 8 frequency). Finally, envelope information is multiplied with the wave table output. As the envelope is set for one operator which corresponds to a single rhythm instrument, the values which express that instrument's characteristics are set in the parameter registers in the same manner as for melody instruments.

Programming the Synthesizer

Operators

Operators

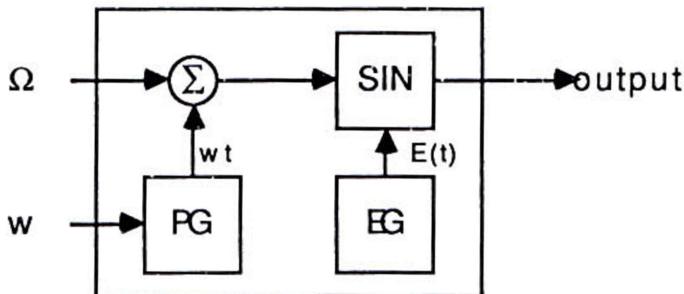
The ALMSC uses pure sine waves that interact together to produce the full harmonic spectrum for any voice. Each digital sine wave oscillator is combined with its own envelope generator to form an "operator".

An operator has 2 inputs and 1 output. One input is the pitch oscillator frequency and the other is for the modulation data. The frequency and modulation data (phases) are added together and converted to a sine wave signal. The phase generator (PG) converts the frequency (w) into a phase by multiplying it by time (t). An envelope generator (EG) produces a time variant amplitude signal (ADSR). The EG's output is then multiplied by the sine wave and output to the outside world.

The operator output can be expressed as a mathematical expression:

$$F(t) = E(t) \sin(wt + \Omega)$$

$E(t)$ is the output from the EG, w is the frequency, t is time and Ω is the phase modulation.



The operators can be connected in three different ways: additive, frequency modulation and composite sine wave.

- **FM synthesis**

FM synthesis uses two operators in series. The first operator, the modulator, modulates the second operator via its modulation input. The name given to the second operator is the carrier. The modulator can feed back its output into its modulation data input;

$$F_m(t) = E_m(t) \sin(w_m t + \beta F_m(t)) \quad \text{Modulator and feedback}$$

$$F_c(t) = E_c(t) \sin(w_c t + F_m(t)) \quad \text{Carrier and Modulator}$$

- **Additive synthesis**

Additive synthesis connects two operators in parallel, adding both outputs together. This method of synthesis is not as interesting as FM synthesis, but it can generate good organ type sounds.

The simplified formula for the additive synthesis is:

$$F(t) = E_1(t) \sin(wt + \Omega_1) + E_2(t) \sin(wt + \Omega_2)$$

- **Composite sine wave synthesis**

Composite sine wave synthesis (CSW) may be used to generate speech or other related sounds by playing all voices simultaneously. When using this mode the card cannot generate any other sounds. This mode is not used because other methods have proved to provide better quality speech.

ALMSC Input / Output Map

The ALMSC is located at address 388H in the i/o space. The card decodes two addresses: 388H and 389H. The first address is used for selecting the register address and the second is used for writing data to the selected register. There also exists the possibility of using three other addresses: 218H, 288H and 318H. The port address is currently hard-wired, but address jumpers may be added in the future so you may want to take into account the possibility of using different addresses when programming. Here is a register map of the ALMSC:

Programming the Synthesizer

ALMSC Input/Output Map

REG	D7	D6	D5	D4	D3	D2	D1	D0
01			WSE				TEST	
02							TIMER-1	
03							TIMER-2	
04	RST	T1	mask	T2				start/stop T2 T1
08	CSM	SEL						
20-35	AM	VIB	EG	KSR			MULTI	
40-55		KSL					TL	
60-75			AR				DR	
80-95			SL				RR	
A0-A8				FN			F-NUMBER (L)	
B0-B8			KON		BLOCK			F-NUM (H)
BD	DEP AM	DEP VIB	R	BD	SD	TOM	TC	HH
C0-C8							FB	C
E0-F5								WS

Because of the nature of the card, you must wait 3.3 μ sec after a register select write and 23 μ sec for a data write. Only the status register located at address 388H can be read.

For many parameters, there is one register per operator. However, there are holes in the address map so that the operator number cannot be used as an offset into the map. The operator offsets are as follows:

	Operator Address Offset									
Opr.	1	2	3	4	5	6	7	8	9	
Off. (hex)	00	01	02	03	04	05	08	09	0A	
Opr.	10	11	12	13	14	15	16	17	18	
Off. (hex)	0B	0C	0D	10	11	12	13	14	15	

For example, the KSL/TL registers are at 40H-55H. If we wish to access the register for operator 8, we must write to register 49H (NOT 48H).

Register Reference

Test Register/WSE

This register must be initialized to zero before taking any action. The wave select enable/disable bit (WSE) is D5. If set to 1, the value in the WS register will be used to select the wave form used to generate sound. If the WSE is set to 0, the value in the WS register will be ignored and the chip will use a sine wave. (The available waveforms are detailed later in this section).

Timers

The timers are not wired on the card. However, the following information is included since the timers can be used to detect the presence of our card in the computer.

Timer-1 is an upward 8 bit counter with a resolution of 80 μ sec. If an overflow occurs, the status register flag FT1 is set, and the preset value (address = 02) is loaded into Timer-1. Timer-2 (address = 03) is an upward 8 bit counter just like Timer-1 except that the resolution is 320 μ sec.

$$T_{\text{overflow}}(\text{ms}) = (256-N) * K$$

N is the preset value and K is the timer constant equal to 0.08 for Timer-1 and 0.32 for Timer-2. Register address 04 controls the operation of both timers. ST1 and ST2 (start/stop T1 or T2) bits start or stop the timers. When the corresponding bit is 1 the counter is loaded and counting starts, but when 0 the counter is held.

The Mask bits are used to gate the status register timer flags. If a mask bit is 1 then the corresponding timer flag bit is kept low (0) and is active when the mask bit is cleared (0). The most significant bit (MSb) is called IRQ-RESET. It resets timer flags and IRQ flag in the status register to zero. All other bits in the control register are ignored when the IRQ-RESET bit is 1.

Status Register

Reading at address 388H yields the following byte of information:

- D0 - D4 are unused.
- D5 Timer 2 flag: Set to 1 when the preset time in Timer 2 has elapsed. The flag remains until reset.
- D6 Same as D5, except for Timer 1.
- D7 IRQ flag: set if D5 or D6 are 1.

As mentioned earlier, the timer interrupts are not connected, but the timers can be used to detect the presence of the board as follows:

1. Reset T1 and T2: write 60H to register 4.
2. Reset the IRQ: write 80H to register 4 (this step must NOT be combined with Step #1).
3. Read status register: read at 388H. Save the result.
4. Set timer-1 to FFH: write FFH to register 2.
5. Unmask and start timer-1: write 21H to register 4.
6. Wait (in a delay loop) for at least 80 μ sec.
7. Read the status register and save the result.
8. Reset T1, T2 and IRQ as in steps #1 and #2.
9. Test the results of the two reads: the first should be 0, the second should be C0H. If either is incorrect, then an ALMSC board is not present. (NOTE: You should AND the result bytes with E0H as the unused bits are undefined.)

CSM/Keyboard Split

This register (address = 08) will determine if the card is to function in music mode (CSM = 0) or speech synthesis mode (CSM = 1) as well as the keyboard split point.

When using composite sine wave speech synthesis mode all voices should be in the KEY-OFF state. The bit NOTE-SEL (D6) is used to control the split point of the keyboard. When 0, the keyboard split is the second bit from the MSb (bit 8) of the F-Number. The MSb of the F-number is used when

NOTE-SEL = 1. This is illustrated in the following table:

NOTE-SEL = 0

BLOCK/OCT	0	1	2	3	4	5	6	7
FNUM(MSb)	X	X	X	X	X	X	X	X
FNUM(8)	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1
Split Num.	0 1	2 3	4 5	6 7	8 9	10 11	12 13	14 15

NOTE-SEL = 1

BLOCK/OCT	0	1	2	3	4	5	6	7
FNUM(MSb)	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1
FNUM(8)	X X	X X	X X	X X	X X	X X	X X	X X
Split Num.	0 1	2 3	4 5	6 7	8 9	10 11	12 13	14 15

X = Ignored

AM/VIB/EG-TYP/KSR/Multiple

This group of registers (addresses 20H to 35H), one per operator, controls the frequency conversion factor and modulating wave frequencies corresponding to the frequency components of music.

The MULTI 4-bit field determines the multiplication factor applied to the input pitch frequency in the PG section. That is, an operator's frequency will automatically be multiplied according to the value in this field. The multiplication factors are given in the following table:

Programming the Synthesizer

Register Reference

MULTI	Factor
0	1/2
1	1
2	2
3	3
4	4
5	5
6	6
7	7

MULTI	Factor
8	8
9	9
10	10
11	10
12	12
13	12
14	15
15	15

The operator output can then be expressed, with "d" as the multiplication factor, as follows:

$$F(t) = E_c(t) \sin(\partial_c w_{ct} + E_m \sin(\partial_m w_{mt}))$$

The KSR bit (position = D4) changes the rates for the envelope generator (EG). This parameter makes it possible to gradually shorten envelope length (increase EG rates) as higher notes on the keyboard are played. This is particularly useful for simulating the sound of stringed instruments such as piano and guitar, in which the envelope of the higher notes is noticeably shorter than the lower notes. The actual rate is then equal to the ADSR value plus an offset:

$$\text{Actual rate} = 4 * \text{Rate} + \text{KSR offset}$$

The KSR offset is specified in the following table:

Rate	KSR=0	KSR=1
0	0	0
1	0	1
2	0	2
3	0	3
4	1	4
5	1	5
6	1	6
7	1	7

Rate	KSR=0	KSR=1
8	2	8
9	2	9
10	2	10
11	2	11
12	3	12
13	3	13
14	3	14
15	3	15

The EG-Type activates the sustaining part of the envelope when the EG-Type is set (1). Once set, an operator's frequency will be held at its sustain level until a KEY-OFF is done.

The VIB parameter toggles the frequency vibrato (1 = on, 0 = off). The frequency of the vibrato is 6.4 Hz and the depth is determined by the DEP VIB bit in register 0BDH.

The AM parameter is similar to the VIB parameter except that it is an amplitude vibrato (tremolo) of frequency 3.7Hz. The amplitude vibrato depth is determined by the DEP AM bit in register 0BDH.

KSL/Total Level

These registers (addresses 40H to 55H, 1 per operator) control the attenuation of the operator's output signal. The KSL parameter produces a gradual decrease in note output level towards higher pitch notes. Many acoustic instruments exhibit this gradual decrease in output level. The KSL is expressed on 2 bits (value 0 through 3). The corresponding attenuation is given below:

D7	D6	Attenuation
0	0	0
1	0	1.5dB/oct
0	1	3.0dB/oct
1	1	6.0dB/oct

The Total Level (TL) attenuates the operator's output. In FM synthesis mode, varying the output level of an operator functioning as a carrier results in a change in the volume of that operator's voice. Attenuating the output from a modulator will change the frequency spectrum produced by the carrier. In additive synthesis, varying the output level of any operator varies the volume of its corresponding voice. The TL value has a range of 0 through 63 (6 bits). To convert this value into an output level, apply the following formula:

$$\text{Output level} = (63 - \text{TL}) * 0.75\text{dB}$$

ADSR

These values change the shape of the envelope for the specified operator by changing the rates or the levels. The attack (AR) and the decay (DR) rates are at addresses 60H to 75H (1 per operator). The Sustain Level (SL) and Release Rate (RR) are located at addresses 80H to 95H. All of these values are 4 bits in length (range 0 to 15). Refer to the diagram on page 11 for more information.

The attack rate (AR) determines the rising time for the sound. The higher the value in this register, the faster the attack.

The decay rate (DR) determines the diminishing time for the sound. The higher the value in the DR register, the shorter the decay.

The sustain level (SL) is the point at which the sound ceases to decay and changes to a sound having a constant level. The sustain level is expressed as a fraction of the maximum level. When all bits are set, the maximum level is reached. Note that the EG-Type bit must be set for this to have an effect.

The release rate (RR) determines the rate at which the sound disappears after a Key-Off. The higher the value in the RR register, the shorter the release time.

BLOCK/F-Number

These parameters determine the pitch of the note played. The Block parameter determines the octave while the F-Number (10 bits) further specifies the frequency. The following formula is used to determine the value of F-Number and Block:

$$F\text{-Num} = F_{\text{mus}} * 2^{(20-b)} / 49.716 \text{kHz}$$

In this formula, F_{mus} is the desired frequency (Hz) and "b" is the block value (0 to 7). Refer to Appendix C for a table of note frequencies.

The D5 bit in the register that contains the BLOCK information is called KEY-ON (KON) and determines if the specified voice (0 to 8) is enable (1) or disable (0). The lower bits of F-Number are at location A0H through A8H (1 per voice) and the 2 MSb are at positions D0 and D1 of addresses B0H to B8H.

REG	D7	D6	D5	D4	D3	D2	D1	D0
A0H-								F-Number
A8H	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
B0H-			KEY ON		Block		F-Number	
B8H				2 ²	2 ¹	2 ⁰		2 ⁹ 2 ⁸

Rhythm/AM Dep/VIB Dep

This register allows for control over AM and VIB depth, selection of rhythm mode and ON/OFF control for various rhythm instruments. Bit D5 (R) is used to change the mode from melodic (0) to percussive (1). When in percussive mode, bits D0 through D4 are the KEY-ON/KEY-OFF controls for the rhythm instruments listed below. The KEY-ON bit in registers B6H, B7H and B8H must always be 0 when in percussive mode.

D0	Hi-Hat
D1	Cymbal
D2	Tom-Tom
D3	Snare Drum
D4	Bass Drum

The AM Depth is 4.8dB when D7 is 1 and 1dB when 0. The VIB Depth is 14 cents when D6 is 1, and 7 cents when zero. (A "cent" is 1/100th of a semi-tone.)

FeedBack/Connection

These two parameters influence the way the operators are connected together and the β factor in the feedback loop of the modulator. These parameters are assigned 1 per voice at locations C0H through C8H. The Connection bit (C) determines if the voice will be functioning in Additive synthesis mode (C = 1) or in Frequency modulation mode (C = 0). The other parameter, Feedback (FB), gives the modulation factor, β , for the feedback loop:

Programming the Synthesizer

Register Reference

	0	1	2	3	4	5	6	7
β	0	$\pi / 16$	$\pi / 8$	$\pi / 4$	$\pi / 2$	π	2π	4π

Wave Select

- The WS parameter enables the card to generate other kinds of wave shapes. This is done by changing the sine function of the specified operator. (Note that the WSE bit must be set in order to use this feature.) The addresses of this feature are E0H to F5H. The following figure gives the corresponding wave forms:

D1	D0	Wave Form
0	0	 Sine
0	1	 Half-sine
1	0	 Abs-sine
1	1	 Pulse-sine

Programming the YMF262

This section explains the differences between the Ad Lib Gold Sound Adapter and the original Ad Lib Music Synthesizer Card as regards FM synthesis. A previous knowledge of the original Ad Lib card is assumed. If you are unfamiliar with the original card, you should first read the following section: "Programming the Synthesizer", which is reproduced from the original Programmer's Manual .

You can see from the register map on the following page that the new FM section is quite similar to the original FM chip but with extra features added. Register Array 0 is accessed by writing to addresses x and x+1 (388H and 389H by default). Register Array 1 is accessed by writing to addresses x+2 and x+3 (38AH and 38BH by default). This scheme allows for complete compatibility with older software which recognizes only the original Ad Lib card.

All registers are cleared at reset. The TEST registers at 01 should be cleared or not accessed at all. Bits in the register map which are not designated should be left in their cleared state.

Register Array 0

Register Array 0 emulates the original chip and will be used as such by software written for the original card. However, there are several changes to be noted.

The Wave Select Enable bit (WSE, D5 at 01) no longer exists. Wave Select is now "on" permanently. Writing 1 to D5 at 01 has no effect so that compatibility is thereby maintained.

The CSM bit (D7 at 08) found on the original chip is no longer present. Although this bit was documented on the original chip, it was non-functional. Compatibility is, therefore, not an issue.

The timers are now functional. How to program them is explained in the *Timers* section of *Programming the Synthesizer*.

New FM Features

Register Map

Register Map, FM Array 0

REG	D7	D6	D5	D4	D3	D2	D1	D0				
01	TEST											
02	TIMER-1											
03	TIMER-2											
04	RST	mask T1	T2					start/stop T2 T1				
05												
08		SEL										
20-35	AM	VIB	EG	KSR	MULTI							
40-55	KSL		TL									
60-75	AR				DR							
80-95	SL				RR							
A0-A8	F-NUMBER (L)											
B0-B8			KON	BLOCK			F-NUM (H)					
BD	DEP AM	DEP VIB	R	BD	SD	TOM	TC	HH				
C0-C8		SRL	STR	FB			C					
E0-F5						WS						

Register Map, FM Array 1

REG	D7	D6	D5	D4	D3	D2	D1	D0
01								TEST
02								
03								
04								CONNECTION SELECT
05								NEW
08								
20-35	AM	VIB	EG	KSR				MULTI
40-55	KSL							TL
60-75		AR						DR
80-95		SL						RR
A0-A8					F-NUMBER (L)			
B0-B8		KON		BLOCK				F-NUM (H)
BD								
C0-C8		SRL	STR		FB			C
E0-F5								WS

New FM Features

4-Operator Voices

Each voice now has two bits which control stereo output: STL and STR (D5/D4 at C0-C8). Setting STL enables output to the left channel. Setting STR enables output to the right channel. Clearing both bits will result in no output for a given voice. However, for these bits to have effect, the NEW bit (explained in the next section) must be set. If NEW is not set (its default state), then the STL and STR bits are ignored and sound is output to both channels. This maintains compatibility with older software which ignores the existence of the stereo bits.

The stereo bits affect pairs of operators, which creates a particularity in percussive mode. The stereo bits in C7 simultaneously affect the Hi-Hat and Snare Drum; C8 affects the Tom-Tom and Cymbal similarly. The Bass Drum (C6) uses two operators and functions the same as a melodic voice.

The Wave Select has been expanded to 3 bits, thus allowing for a total of 8 different waveforms. The waveforms are shown below.

D2 - D0	Waveform
0	Sine
1	Half-sine
2	Abs-sine
3	Pulse-sine
4	Square
5	Triangle
6	Square
7	Square

Register Array 1

Register Array 1 is similar to Register Array 0 with some omissions and additions. The timer registers are unused or are used for other purposes. Register Array 1 does not offer percussive voices, so the bits relating to percussive mode are not present.

The SEL, DEP AM and DEP VIB bits are globally affective and so are found only in the first register array. Setting any one of these three bits will affect both register arrays.

The NEW bit (D0 at 05) enables the new features of the new chip. If this bit is zero, then writes to any other register in Register Array 1 will be blocked. When NEW is zero, Register Array 0 functions as if it were the original chip: the stereo bits will be ignored and the high bit of the wave select will be ignored.

IMPORTANT: All software should enable the NEW bit during its initialization sequence. However, it should clear the NEW bit when exiting. This is so that if an older piece of software is subsequently run, the card will be in the mode which emulates the original card.

The CONNECTION SELECT bits control the 4-operator voice, as explained in detail in the next section.

4-Operator Voices

A significant new feature of the FM section of the Ad Lib Gold card is the presence of 4-operator voices, which are capable of creating a large variety of rich timbres. To enable a 4-operator voice, you must set the appropriate bit in the CONNECTION SELECT register. The following table shows which bit corresponds to which 4-operator voice and the pair of 2-operator voices which correspond to the 4-operator voice.

Connection Select (05H, Register Array 1):

	D5	D4	D3	D2	D1	D0
4-op voice	6	5	4	3	2	1
2-op voices	3,6	2,5	1,4	3,6	2,5	1,4
	Array 1				Array 0	

New FM Features

4-Operator Voices

With 2-operator voices, the connection bit at C0-C8 specifies one of two possible methods for connecting the operators. With 4-operator voices, there are 4 methods of connecting the operators. This is done by using both connection bits of the pair of 2-operator voices involved. The following table shows the relationship between the 4-operator voice and its connection bits. The diagram on the next page illustrates the connection methods.

Connection bit (C) addresses for 4-operator voices:

4-op voice	1	2	3	4	5	6
C addresses	C0,C3	C1,C4	C2,C5	C0,C3	C1,C4	C2,C5
Array 0				Array 1		

Note that even if all six 4-operator voices are used, there are still three 2-operator voices available on Register Array 1 and three 2-operator or five percussive voices available on Register Array 0. The CONNECTION SELECT register allows you to selectively use 4-operator voices so that you can mix 2 and 4-operator voices as you wish.

The following table is a combination of the preceding two tables. You may find it useful for reference purposes.

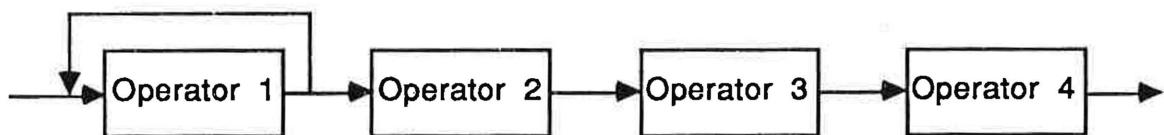
Connect Sel	D5	D4	D3	D2	D1	D0
4-op voice	6	5	4	3	2	1
2-op voices	3,6	2,5	1,4	3,6	2,5	1,4
C addresses	C2,C5	C1,C4	C0,C3	C2,C5	C1,C4	C0,C3
Array 1				Array 0		

Feedback in a 4-operator voice is applied to the first operator only, as indicated by the loop around Operator 1 in the diagram on the following page. The feedback value is determined by the value written in the register for the first register pair (Cx). The value in the second register pair (Cx+3) is ignored.

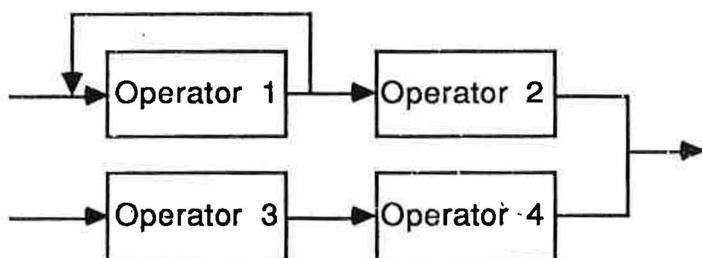
Similarly, the F-NUMBER, KON, and BLOCK parameters for a 4-operator voice are determined by the values written in the registers for the first register pairs (Ax and Bx). The values in the second register pairs (Ax+3 and Bx+3) are ignored.

Note that the state of the STL and STR bits for a 4-operator voice must be the same for both register pairs (Cx and Cx+3) or else the output of all four operators will be disabled. For example, if STL at C0 is 1 and STL at C3 is 0, then this 4-operator voice will not be output to the left channel.

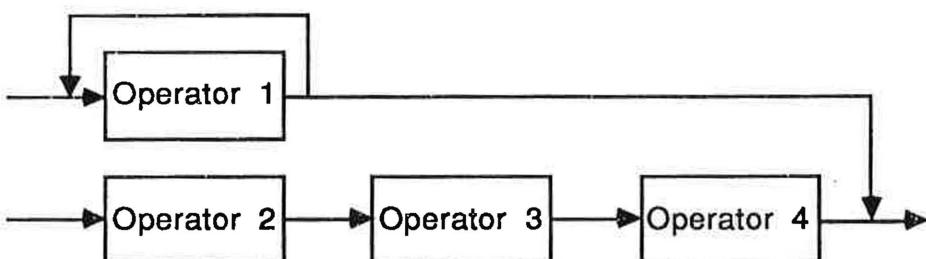
Cx=0, Cx+3=0



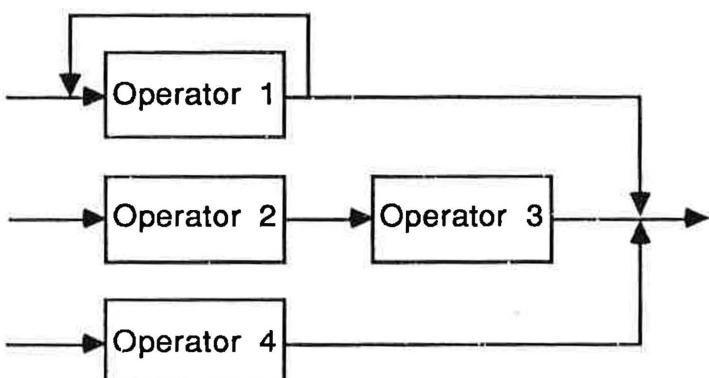
Cx=0, Cx+3=1



Cx=1, Cx+3=0



Cx=1, Cx+3=1



Connection Methods

7.3

Digital Input and Output (Digital Audio and MIDI)

The digital I/O functions are handled by the YMZ263 chip, also known as the MMA. The MMA handles the following functions:

- 2 channels of digital audio input and output
- MIDI input and output
- Three high-speed timers

The digital I/O functions are accessed via three addresses. The first address is located four bytes past the address of FM Array 0 (38CH by default).

Accessing a MMA register is done in two steps:

- 1) write the index of the register to be accessed to the "register select" port, located at 38CH
- 2) write or read the desired value for the selected register, either in the channel 0 port, located at 38DH or in the Channel 1 port located at 38FH

A 470 nanosecond delay is necessary between read/write at any address of the MMA

Digital Input and Output

Register Map

REG		D7	D6	D5	D4	D3	D2	D1	D0
01	-								TEST
02	W								TIMER-0 (L)
03	W								TIMER-0 (H)
04	W								BASE COUNTER (L)
05	W								BASE COUNTER (H)
06	RW								TIMER 2 (L)
07	RW								TIMER 2 (H)
08	W	SBY	T2M	T1M	T0M	STB	ST2	ST1	ST0
09	W	RST	R	L	FREQ	PCM	P/R		GO
0A	W								VOLUME CONTROL
0B	RW								PCM DATA
0C	W	ILV	DATA FMT					MSK	ENB
0D	W		MSK POV	MSK MOV	MDI TRS RST	MSK TRQ	MDI RCV RST	MSK RRQ	
0E	RW								MIDI DATA

Register Map, Channel 0

Digital Input and Output

Register Map

REG		D7	D6	D5	D4	D3	D2	D1	D0
01	-								
02	W								
03	W								
04	W								
05	W								
06	RW								
07	RW								
08	W								
09	W	RST	R	L	FREQ	PCM	P/R	GO	
0A	W	VOLUME CONTROL							
0B	RW	PCM DATA							
0C	W		DATA FMT		FIFO INT		MSK	ENB	
0D	W								
0E	RW								

Register Map, Channel 1

Register Reference

Status Register

Reading the port at address 38CH returns the following information:

D7	D6	D5	D4	D3	D2	D1	D0
OV	T2	T1	T0	TRQ	RRQ	FIF1	FIFO

Status Byte

OV becomes 1 when a MIDI receive overrun error or a PCM/ADPCM record or playback overrun error occurs.

T0, T1 and T2 become 1 when the specified time elapses in the corresponding timer.

TRQ becomes 1 when the MIDI transmit FIFO buffer is empty.

RRQ becomes 1 when the MIDI receive FIFO buffer has data in it.

FIFO and FIF1 become 1 when the PCM/ADPCM FIFO reaches the status that was specified in FIFO INT. FIFO corresponds to channel 0; FIF1 to channel 1.

Register 00H: Test Register

Register #1, Channel 0 is used for testing the LSI. It should not be accessed.

Registers 02H - 07H: Timer Counters

Timer 0 (Registers #1 and 2, Channel 0) is a 16-bit programmable down counter with 1.88964 usec resolution. This constant will be referred to as **clockFreq**. In the following examples. The interrupt is triggered when the counter value reaches 0. The time **t0**, in usec, until IRQ is generated may be calculated as follows:

$$t0 = \text{TIMER0(H)} * (256 * \text{baseFreq}) + \text{TIMER0(L)} * \text{baseFreq}$$

The BASE COUNTER (Register #4 and 5, Channel 0) is a 12-bit counter that supplies the period for each tick of TIMER1 and TIMER2. The base counter has a resolution of 1.89 usec. The period **bc**, in usec, may be calculated as follows:

$$bc = \text{BASE COUNTER(H)} * (256 * \text{baseFreq}) + \text{BASE COUNTER(L)} * \\ \text{baseFreq}$$

Timer 1 (Register #5, Channel 0) is a 4-bit programmable down counter that is controlled by the base counter clock. . The 4-bit value is placed in the high nibble of the register. The interrupt is triggered when the counter value reaches 0. The time **t1**, in usec, until IRQ is generated may be calculated as follows:

$$t1 = \text{TIMER1} * bc$$

Timer 2 (Register #6 and 7, Channel 0) is a 16-bit programmable down counter that is controlled by the base counter clock. The interrupt is triggered when the counter value reaches 0. The time **t2**, in usec, until IRQ is generated may be calculated as follows:

$$t2 = (\text{TIMER2(H)} * 256 + \text{TIMER2(L)}) * bc$$

TIMER2 may be read to determine the count value. When TIMER2(L) is read the 16-bit count value is latched and the latched value of TIMER2(L) is output. Subsequently, when TIMER2(H) is read, the latched value of TIMER2(H) is output. (Latching a value means taking a "snapshot" of that value at a given moment.) TIMER2(L) must be read first as it is this read which triggers the latching mechanism.

Digital Input and Output

Select Frequency

Register 08H: Timer Control

D7	D6	D5	D4	D3	D2	D1	D0
SBY	T2M	T1M	T0M	STB	ST2	ST1	ST0

Register #8: Channel 0

Stand-by Mode

Setting SBY to 1 reduces the internal clock frequency in order to minimize power consumption. This must be set to 0 when doing any I/O operations.

Timer Interrupt Masks

Setting T0M, T1M or T2M disables the interrupt generated by the corresponding timer. Hence, the bit must be cleared if you wish to use the interrupt timer.

Timer Controls

ST0, ST1, ST2 and STB (base counter) control the start and stop of each timer. Setting a bit loads the reload value and starts counting down. Clearing the bit stops the timer.

Register 09H: Playback and Recording Control

D7	D6	D5	D4	D3	D2	D1	D0
RST	R	L	FREQ		PCM	P/R	GO

Register #9: Channels 0 & 1

Reset PCM/ADPCM

RST bit is used to reset PCM and ADPCM playback for the channel. Resetting a channel clears the FIFO buffers and resets the FIFO flags. In order for reset to operate properly, all other bits should be 0. The sequence for a channel reset should then be: 1) write 80H to register 9 2) write the desired values to register 9.

Select Output Channel

Setting L or R enables output from the left or right channel respectively. Clearing the bit disables output.

Select Frequency

FREQ selects the PCM/ADPCM frequency as indicated below:

FREQ	Sampling Frequency (KHz.)	
	PCM Mode	ADPCM Mode
0	44.1	22.05
1	22.05	11.025
2	11.025	7.35
3	7.35	5.5125

PCM/ADPCM Selection

Setting PCM selects PCM mode (data is not compressed). Clearing PCM selects ADPCM mode (data is compressed to 4-bits).

Select Record/Playback

Clear P/R to record; set it to playback.

Start/Stop Record/Playback

In playback, the FIFO buffers should never be empty when the GO bit is set. To start playback, the proper procedure is: 1) write data into the FIFO buffer for the channel. The FIFO should be filled to a level exceeding the FIFO interrupt level (see register 0CH description) 2) Set the GO bit to start playback.

Register 0AH: Output Volume Control

VOLUME CONTROL (Register #0Ah, both channels) sets the output attenuation value. A value of 0 is the minimum output volume, a value of FF is the maximum output volume.

Register 0BH: PCM/ADPCM Data

Register #0Bh (both channels) is used for writing data into the FIFO buffer and reading data from the FIFO buffer. . Each channel has its own buffer. Data written into this register is transferred into the FIFO buffer, and data transferred from the FIFO buffer is written into this register. In PCM mode, 12-bit data is accessed in one or two passes. The data format for this access follows the specification of the FORMAT register. In ADPCM mode, each access inputs or outputs two 4-bit data. The high 4 bits and the low 4 bits are each ADPCM data. The high data is followed immediately by the low data.

Register 0CH: Sampling Format and Control

D7	D6	D5	D4	D3	D2	D1	D0
ILV	DATA FORMAT		FIFO INT		MSK	ENB	

Register #0Ch: Channels 0 & 1

Interleaving

Setting ILV (Channel 0 *only*) to 1 will cause the chip to do interleaving. Data will be alternately input/output from each channel. Channel 0 initiates the transfer. ENB must be 1 for both channels, otherwise the data transfer is not performed. Both channels operate in the same mode so that the P/R,FREQ and GO bits will be controlled by the values set for channel 0.

Set Data Format

There are 3 possible data formats for sampling input and output. The format is selected by writing 0, 1 or 2 to the DATA FORMAT register. "3" is an invalid format... This is ignored in ADPCM mode.

Format 0 is an 1-byte format which contains the 8 most significant bits of the sample.

Format 1 is a 2-byte format. The first byte contains the 8 least significant bits. The lower nibble of the second byte contains the 4 most significant bits of the sample. The MSB of the sample is repeated in all bits of the upper nibble.

Format 2 is a 2-byte format as well. The upper nibble of the first byte contains the 4 LSBs of the sample. The lower nibble is zero. The second byte contains the 8 MSB's.

FORMAT	PCM Data Byte 1	PCM Data Byte 2
0	MSB b10 b9 b8 b7 b6 b5 b4	There is no 2nd byte
1	b7 b6 b5 b4 b3 b2 b1 b0	MSB MSB MSB MSB MSB b10 b9 b8
2	b3 b2 b1 b0 0 0 0 0	MSB b10 b9 b8 b7 b6 b5 b4

PCM Data Formats

Set FIFO Interrupt

The FIFO INT register is used to specify when an interrupt will be generated while the 128-byte FIFO buffer is being filled or emptied. The following table documents the possible interrupt points.

FIFO INT	Interrupt Generation Point (bytes)
0	112
1	96
2	80
3	64
4	48
5	32
6	16
7	Prohibited

FIFO Interrupt Mask

Setting MSK disables the FIFO interrupt.

DMA Mode Specification

Set ENB to enable the DMA mode. Clear ENB when not using DMA to transfer data.

Register 0DH: MIDI and Interrupt Control

D7	D6	D5	D4	D3	D2	D1	D0
		MSK POV	MSK MOV	MDI TRS RST	MSK TRQ	MDI RCV RST	MSK RRQ

Register #0Dh: Channel 0

Mask Digital Overrun Error

Set POV to disable interrupt signals generated by overrun errors during PCM/ADPCM recording and playback.

Mask MIDI Overrun Error

Set MOV to disable interrupt signals generated by overrun errors during MIDI reception or transmission.

Reset MIDI transmit circuit

Set MDI TRS RST to 1 to reset the MIDI transmit circuit and clear the MIDI transmit FIFO buffer. Zero MDI TRS RST to terminate the reset status.

Mask MIDI transmit FIFO Interrupts

Set MSK TRQ to disable interrupt signals generated by the MIDI transmit FIFO. When interrupts are enabled, an interrupt is generated when the MIDI transmit FIFO buffer is emptied.

Reset MIDI Receive Circuit

Set MDI RCV RST to 1 to reset the MIDI receive circuit and clear the MIDI receive FIFO buffer. Zero MDI RCV RST to terminate the reset status.

Mask MIDI Receive FIFO Interrupts

Set MSK RRQ to disable interrupt signals generated by the MIDI receive FIFO buffer. When interrupts are enabled, an interrupt is generated on reception of a MIDI byte.

Register 0EH: MIDI Data

This register is used for writing data into the MIDI FIFO buffer and reading data from the MIDI FIFO buffer. Data written in this register is transferred to the transmit FIFO buffer and data transferred from the receive FIFO buffer can be read from this register.

MMA Programming Tips

- Reset a MMA channel after each sample (using the RST bit in register 9), after stopping the sample playback. This makes sure that the FIFO buffer for the channel is emptied.
- In playback mode, when processing a FIFO interrupt, a situation occurs where your application is filling in the FIFO while the playback mechanism is emptying the FIFO at the same time. In some cases this can cause "false triggers" of the FIFO interrupt. In order to avoid this, a simple trick is to temporarily lower the FIFO level, while your application fills in the FIFO, and restore the original level before leaving the interrupt procedure.
- A similar situation can occur in recording mode.
- To avoid the same situation during playback and recording using DMA transfers, you can double-check if the interrupt is valid by reading the DMA controller's counters or status register. they should indicate that data transfer is over.
- The MMA FIFO buffers should never be left to empty themselves during playback (that is when GO bit is set) This implies that the FIFO buffers should be filled to a level exceeding the FIFO interrupt level before the GO bit is set.

Special care should be taken during high-speed transfers (44.1K, 12 bit stereo samples, for example) on slower computers.

- All masks (mask T2, T1, T0, FIFO, POV, MOV, TRQ and RRQ) have no effect whatsoever on the status register. They are only used to disable the hardware interrupt.
- Respect the 470ns delay between writes to the MMA registers.

YAMAHA
**Gold Sound
Standard**

March 17, 1992

Contents

Introduction	1
Overview	2
GSS Implementation.....	3
MMA: Digital Audio, MIDI, and Game Port	4
OPL3: FM Synthesis	6
Mixer and Set-up Section	9
Software Issues	11
Mixer and Set-up Function Implementation	12
Access Method	12
Status Register	13
Index Register Map	14
Register Reference	15
Conclusion	28

Introduction

The rapid evolution of multimedia has necessitated an audio standard to be defined. Although Windows alleviates some of the need for compatibility, it is important that an audio standard is established for DOS, game, and "edutainment" applications. The implementation of an audio multimedia standard lessens the concerns of both hardware and software developers.

This document describes recommended procedures and practices for implementing multimedia audio hardware using the "Magic" chip set from YAMAHA. By conforming to the Gold Sound Standard, hardware manufacturers can be assured that software written for Gold Sound Standard compatible cards will run on their product.

The Gold Sound Standard is a hardware implementation specification, as well as the requirements of hardware compatibility at the register level for the mixer and set up functions. This ensures that software, which writes directly to the hardware, will run on any Gold Sound Standard implementation. This also means that any Gold Sound Standard driver kit for DOS or Windows will be capable of driving any Gold Sound Standard hardware. The Gold Sound Standard provides a safe development path for both software and hardware designers.

Overview

The Gold Sound Standard (GSS) is composed of the YAMAHA "Magic" chip set and a form of mixer and set up circuitry. In the case of the YAMAHA "Magic" chip set, this document will summarize its functions. A more detailed reference for the individual registers of the "Magic" chip set may be found in the YAMAHA reference manual for the particular chip.

Only the minimum requirements are defined in this document. The individual hardware designer may implement additional features. The GSS provides the necessary functionality to be Level 1 MPC compatible.

The "Magic" chip set is designed as a highly integrated solution to developing a Level-1 MPC compatible audio subsystem. The following sections illustrate design concerns when using the "Magic" chip set. They also provide the I/O register map requirements to be Gold Sound Standard compatible.

