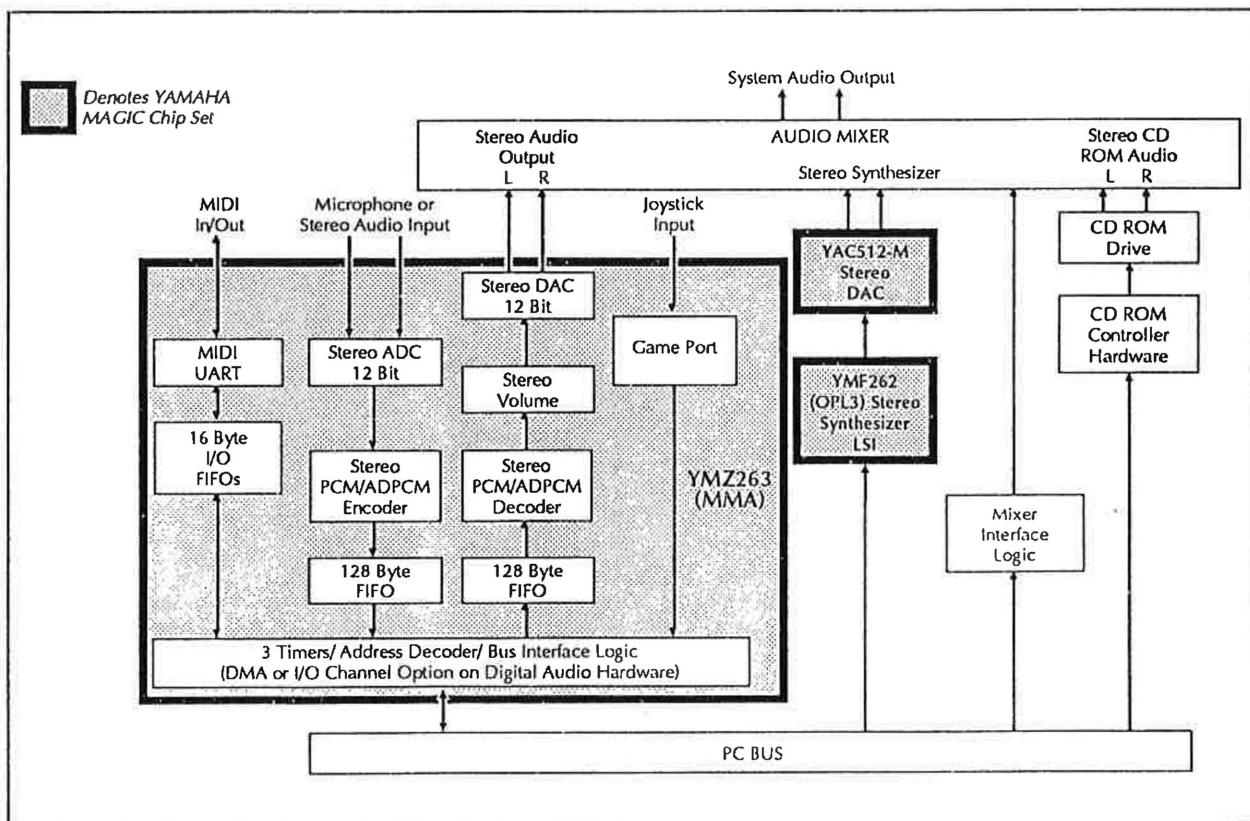


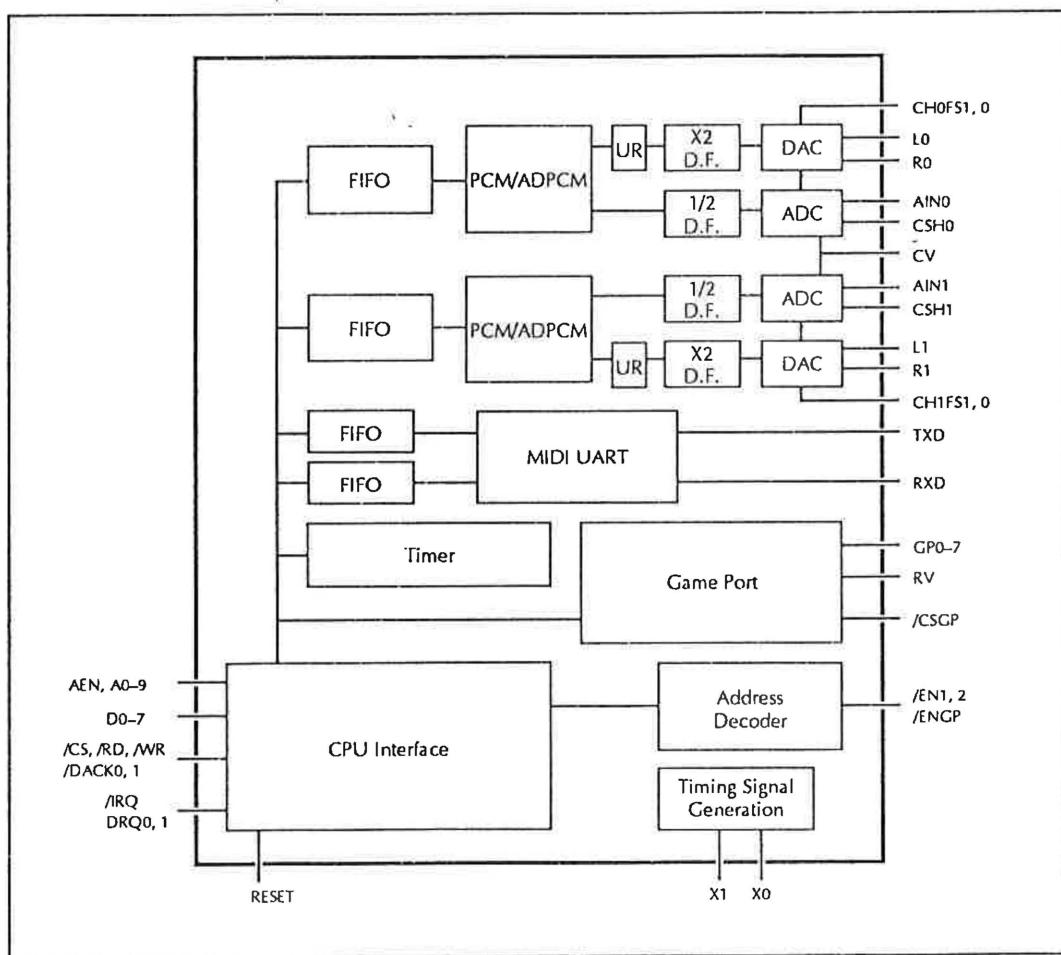
GSS Implementation

The basic features of GSS compatible hardware are a MIDI port, microphone input, stereo input/output, joystick input, and a mixer to produce the stereo audio output. Optionally, a SCSI interface may be implemented for use with CD-ROM drives. A hardware design conforming to the GSS will allow software that directly accesses the hardware to run on all GSS compatible cards. The design concerns are minimized by implementing the "Magic" chip set, which includes the YMZ263 (MMA) Multimedia Audio LSI, the YMF262 (OPL3) Advanced Algorithm Synthesizer LSI, and the YAC512-M Stereo Serial DAC. The following figure illustrates the hardware components of a typical Level 1 multimedia PC using the "Magic" chip set.



MMA: Digital Audio, MIDI, and Game Port

The MMA integrates a stereo digital audio, game port, and MIDI interface into one LSI. The MMA also contains internal bus decode logic, two DMA channels, and two FIFOs. The internal block diagram illustrates the various portions of control circuitry.



The CPU interface is directly connectable to the address, data, and I/O control lines of the PC bus. The interrupt line is connected to the PC bus and may either be asserted when there is data in the input FIFOs, when the output FIFOs are able to receive more data, or if a timer interrupt is generated.

The DMA channels may be programmed to provide two methods of operation, allowing simultaneous record and playback. The first method uses a separate DMA channel for each channel. The second method is to interleave channel information using one DMA.

A PAL device may be used to decode jumper block settings, allowing DMA channel and IRQ level selection.

The direct ISA bus interface of the MMA contains an address decoder for built in fixed addresses. The I/O address the MMA will respond to is determined by the state of the /EN1, /EN2, and /ENGP signals. The recommended default I/O address for the MMA is from 38CH to 38FH (Channel 0: 38CH-38DH, Channel 1: 38EH-38FH). The MMA uses two port addressing for each channel. The first address of a channel is the address register, which is used to access the desired internal register. The second register is the data register. The data written to this register will be sent to the register specified by the index written to the address register.

The two inputs to the wave audio section of the MMA are a low impedance stereo microphone or a high impedance stereo audio. These inputs are A/D converted at twice the selected sampling frequency and decimated before being fed into the PCM/ADPCM encoder. External capacitors are attached to pins CSH1 and CSH2, which stabilize the analog signals during sample hold operations. A reference center voltage for the A/D converter is supplied through the CV pin of the MMA.

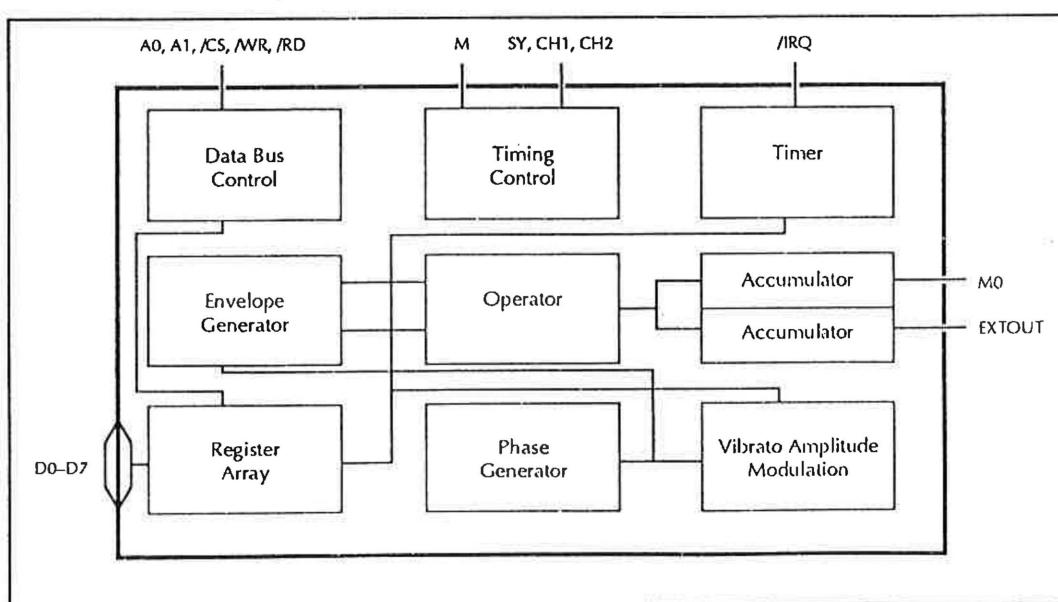
The buffered PCM/ADPCM decoder output is amplified and over sampled at twice the selected frequency (except for 44.1 kHz PCM mode) before passing through the DAC. The DAC output signals are fed through a series of operational amplifiers ending with a low pass reconstruction filter before final output.

The MMA contains a MIDI subsystem with three timers, an asynchronous UART, and two 16 byte FIFOs for sending and receiving MIDI data. The MIDI output channel (TXD) is inverted and sent through an external 5 mA current loop to the external MIDI output connector. The external MIDI input connector's RXD signal is optically isolated to avoid ground loops. An optional MIDI thru port may be added by transferring the MIDI input signal through two inverters out an additional MIDI output port.

The game port interface of the MMA uses internal voltage comparison circuitry to isolate changes in the signals from the game port connector.

OPL3: FM Synthesis

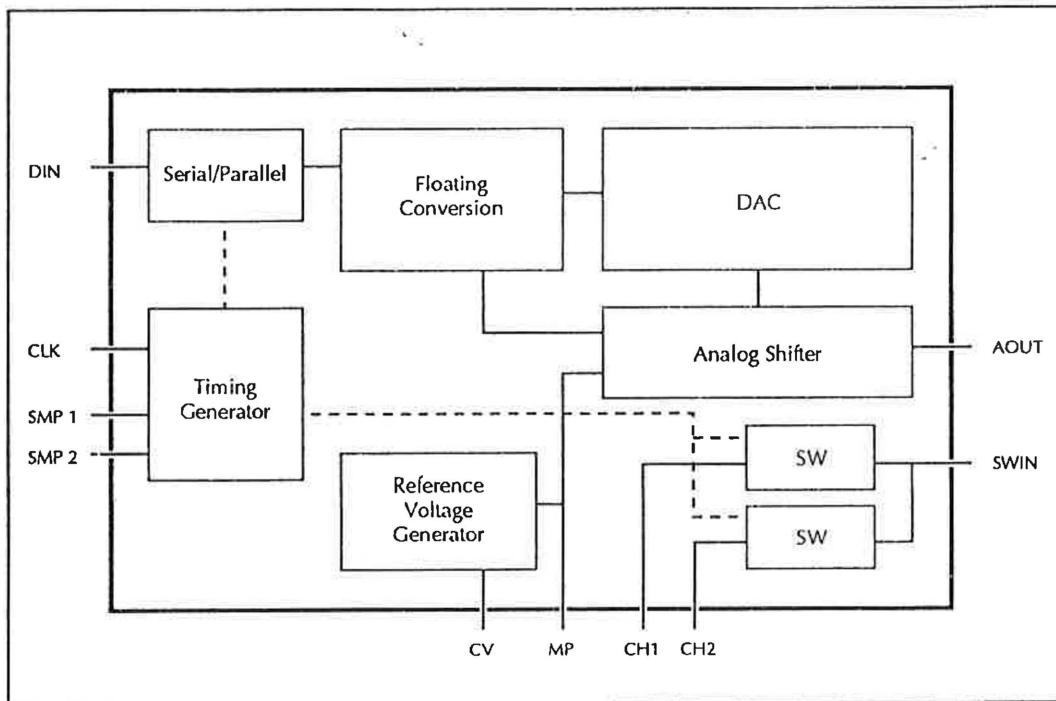
The FM synthesis is produced by the OPL3 and uses the YAC512-M stereo DAC for output. The OPL3 is backward compatible with the YM3812 (OPL2) used in most popular PC audio cards, yet offers much higher quality synthesized sound. The OPL3 was designed to be directly controlled by software. The following diagram illustrates the internal functions of the OPL3.



The OPL3 requires a 14.3127 MHz oscillator, which is taken directly from the PC bus. The address, data, and I/O control lines are also taken directly from the PC bus.

The recommended default base address of the OPL3 is 388H. The OPL3 also uses two port addressing for each channel and the internal register access is identical to the procedure used with the MMA. Channel 0 will be accessed at 388H and Channel 1 at 38AH.

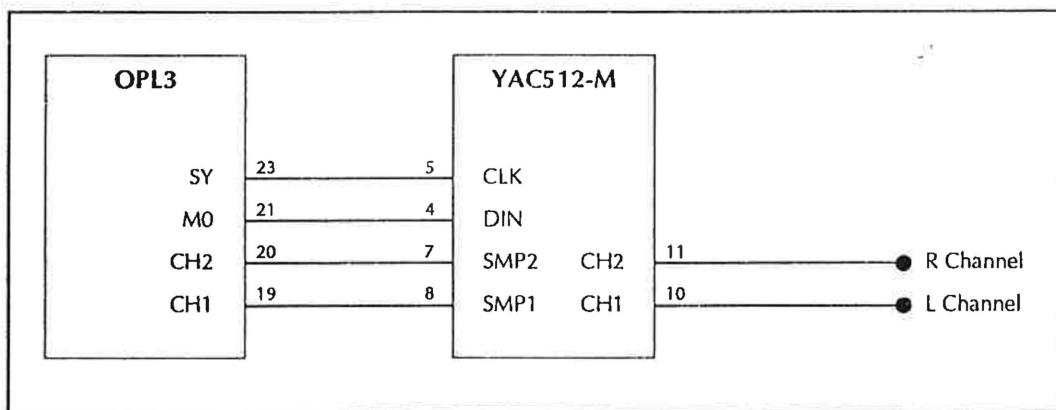
The internal block diagram of the YAC512-M is shown below.



The serial data output and sample/hold channel signals are directly connected to the YAC512-M. The serial data between the OPL3 and the YAC512-M is synchronized using the OPL3's SY clock signal. This data is then latched when the channel sampling lines of the OPL3 fall.

The data is converted to floating point with the mantissa being processed by the DAC and the exponent by the analog shifter. This process produces effectively 16 bit resolution . The data is then converted into a D/A voltage which is sent out the AOUT terminal. This signal passes through a buffer operational amplifier for sample holding and is used for channel 1/2 common input.

The YAC512-M converts the digital serial stream into an analog signal. The YAC512-M requires external capacitors for stabilizing the analog output. The stereo output of the YAC512-M is ready for mixing with the MMA's stereo audio output. The block diagram below illustrates the simple connections between the OPL3 and the YAC512-M.



Mixer and Set-up Section

The mixer section is where the hardware designer may differentiate their audio implementation. The Gold Sound Standard implementation allows software to control the individual volumes of the mixer inputs.

The GSS allows for relocation of the MMA and OPL3. Software should not assume an absolute address. This document will use the default base address of the OPL3 (388H) and the MMA (38CH). The mixer section may be accessed by outputting an invalid index address to the second channel address register of the OPL3.

This access method uses the second channel of the OPL3 for the mixer registers. When the mixer registers are enabled, an index into the internal mixer registers is written to 38AH, or OPL3 base address +2, with the desired register data written to 38BH, or OPL3 base address +3.

In order to avoid the problem of hardware reentrance when accessing the mixer registers the software must push the flags and disable interrupts. Then by writing a value of FFH to port 38AH, or OPL3 base address +2, the hidden mixer registers will appear on top of the second channel of the OPL3.

The next output to port 38AH or OPL3 base address +2 will be an index into the internal registers. The specified internal register is ready for read/write operations. Multiple reads or writes may be made without continually resetting the address register. Once all accesses are complete, the internal register access is disabled by writing a FEH to port 38AH, or OPL3 base address +2. This access method is illustrated by the listing below.

```
PUSHF           ; Push the CPU status flags.  
CLI             ; Disable Interrupts  
OUT  OPL3_base +2, FFH    ; Switch to mixer register access  
OUT  OPL3_base +2, 02H    ; Select register 2, Left Smpl Gain  
OUT  OPL3_base +3, 34H    ; Set gain level to 34H  
...  
OUT  OPL3_base +2, FEH    ; Close access to internal mixer  
                           ; registers.  
  
POPF           ; Restore interrupt status.
```

This approach minimizes the address space occupied by the GSS implementation and reduces the risk of hardware conflicts with other resources.

The implementation allows access to the address and data I/O registers of the first channel of the OPL3, while accessing the internal mixing registers. The address decoding being handled by the mixer section should have no influence on the operation of the second channel of the OPL3.

As is the case with all other aspects of the GSS hardware, special care must be taken for the possibility of reentrance when separate applications access the mixer section and the OPL3 chip simultaneously. This is discussed in the section entitled "Software Issues" below.

Software Issues

In the GSS architecture, hardware reentrance may be possible. Applications may be using the MMA to record and play back samples while the timer or MIDI functions are being used by other applications. Multiple operations are required to access the OPL3 and the MMA. There is a possibility of an interrupt occurring during these accesses, which would cause problems.

In a single-task system (such as DOS), this reentrance may be handled by disabling interrupts during accesses to the GSS hardware.

This reentrance may be handled through the use of an asynchronous queue manager, which would handle mixer register requests when appropriate.

The GSS hardware implementation will allow any standard PCM wave data files to be played, provided it is sampled at the supported frequencies of the MMA.

A method of verifying GSS audio hardware is to write a signature value to the PCM data registers of Channel 1 and 2 of the MMA. If the value read back matches the value written, the audio hardware is GSS compatible.

Mixer and Set-up Function Implementation

The internal mixing register will have read/write capability with the exception of the supported features register. The supported features register will be read only.

Access Method

The mixer and set-up registers, when enabled, use two port addressing like the MMA and OPL3. The first address being an index into the register map with the next address for data.

A delay of 450 microseconds is recommended after writing to the output volume registers (04H – 08H).

A delay of 5 microseconds is recommended after writing to the mixing volume registers and channel/IRQ registers (09H – 15H).

In order to ensure these delays, the mixer access status register should be polled.

While writing the mixer registers to memory the mixer must not be accessed. This is achieved by polling the mixer register write status bit, checking for a "0".

Status Register

The index address register of the mixer is used as a status register. Reading the status register returns information as defined in the following figure.

Status Register								
D7	D6	D5	D4	D3	D2	D1	D0	Function
							X	Indicates FM Interrupt
						X		Indicates Sampler Interrupt
		X	X	X	X			Reserved
	X							Mixer Register Access Status
X								Mixer Register Write Status

D0. This bit provides interrupt information for the FM portion. When bit D0 is set to 0, it indicates the FM portion of the hardware has generated an interrupt.

D1. This bit provides interrupt information for the sampling portion. When bit D1 is set to 0, it indicates that the sampling portion of the hardware has generated the interrupt.

D2–D4 These bits are reserved.

D6. This bit indicates the mixer register write status. If bit D6 is set the card is currently writing to a mixer register.

D7. This bit indicates the card is currently writing its registers to memory. This is useful for notebook and portable devices utilizing power saving features.

Index Register Map

The following figure defines the mixer index and data register map. The index value is written to the address register of the mixer to access the desired register. The data is then written to the data register of the mixer.

Mixer and Set-up Index Register Map		
Index	Read/Write	Description
00	R	ID/Feature Register
02	R/W	Left Channel Sampling Gain
03	R/W	Right Channel Sampling Gain
04	R/W	Left Channel Output Volume
05	R/W	Right Channel Output Volume
06	R/W	Bass Output
07	R/W	Treble Output
08	R/W	Output Mode
09	R/W	Left Channel FM Volume
0A	R/W	Right Channel FM Volume
0B	R/W	Left Sampling Volume
0C	R/W	Right Sampling Volume
0D	R/W	Left Auxiliary Volume
0E	R/W	Right Auxiliary Volume
0F	R/W	Microphone Volume
11	R/W	Audio Selection
13	R/W	Audio IRQ/DMA Select—Channel 0
14	R/W	DMA Select Channel 1
15	R/W	Audio Relocation

The register map is a complete set of registers required to be compatible with the GSS. These are the minimum features required for mixer implementation on a GSS compatible audio card.

Register Reference

0H: ID/Feature Register

This read-only register provides information on supported features of the board. The bit functions are identified in the following figure.

0H: ID/Feature Register								
D7	D6	D5	D4	D3	D2	D1	D0	Function
			X	X	X	X	X	Reserved
		X						Surround Sound Option
	X							SCSI Option
X								Reserved = 1

02H: Left Channel Sampling Gain

The left channel sampling gain is controlled by values written to this register. There are 256 possible values. The amount of gain and step is dependent on the mixer implementation. The recommended gain implementation is computed by the following equation:

$$\text{Gain} = (\text{Register Value} * 10) / 256$$

The bit functions of this register are identified in the following figure.

02H: Left Channel Sampling Gain								
D7	D6	D5	D4	D3	D2	D1	D0	Function
X	X	X	X	X	X	X	X	Left Channel Output Gain

03H: Right Channel Sampling Gain

The right channel sampling gain is controlled by values written to this register. There are 256 possible values. The amount of gain and step is dependent on the mixer implementation. The recommended gain implementation is computed by the following equation:

$$\text{Gain} = (\text{Register Value} * 10) / 256$$

The bit functions of this register are identified in the following figure.

03H: Right Channel Sampling Gain								
D7	D6	D5	D4	D3	D2	D1	D0	Function
X	X	X	X	X	X	X	X	Right Channel Output Gain

04H: Left Channel Output Volume

This read/write register controls the overall left channel output volume. The bit functions of this register are identified in the following figure.

04H: Left Channel Output Volume								
D7	D6	D5	D4	D3	D2	D1	D0	Function
		X	X	X	X	X	X	Left Channel Output Volume
X	X							Reserved = 1

The left channel volume may range from 0 to 64 dB. The recommended volume range is from +6 dB to -64 dB, in two dB steps. The decibel values are listed in the following figure.

Decibels	D5–D0
6	3F
-62	1D
-80	0

05H: Right Channel Output Volume

This read/write register controls the overall right channel output volume. The bit functions of this register are identified in the following figure.

05H: Right Channel Output Volume								
D7	D6	D5	D4	D3	D2	D1	D0	Function
		X	X	X	X	X	X	Right Channel Output Volume
X	X							Reserved = 1

The right channel volume may range from 0 to 64 dB. The recommended volume range is from +6 dB to -64 dB, in two dB steps. The decibel values are listed in the following figure.

Decibels	D5-D0
6	3F
-62	1D
-80	0

06H: Bass Output

This read/write register controls the bass output with a range of values from 0 to 16. The bit functions of this register are identified in the following figure.

06H: Bass Output								
D7	D6	D5	D4	D3	D2	D1	D0	Function
				X	X	X	X	Bass Output
X	X	X	X					Reserved = 1

The recommended decibel range is from +15 dB to -12 dB, in 3 dB steps. The decibel values are listed in the following figure.

Decibels	D3-D0
15	F
15	B
0	6
-12	2
-12	0

07H: Treble Output

This read/write register controls the treble output with a range of values from 0 to 16. The bit functions of this register are identified in the following figure.

07H: Treble Output								
D7	D6	D5	D4	D3	D2	D1	D0	Function
				X	X	X	X	Treble Output
X	X	X	X					Reserved = 1

The recommended range is from +12 dB to -12 dB, in 3 dB steps. The decibel values are listed in the following figure.

Decibels	D3-D0
12	F
12	A
0	6
-12	2
-12	0

08H: Output Mode

This read/write register controls the final output. The final output uses the input and output of the mixer. The bit functions of this register are identified in the following figure and defined below.

08H: Output Mode								
D7	D6	D5	D4	D3	D2	D1	D0	Function
					X	X	X	Source of Final Output
			X	X				Type of Effect
		X						Mute
X	X							Reserved = 1

D2–D0. These bits determine the channels to be selected for the final output. If only one output channel is selected, it will be directed out to both channels. The following figure defines the signal configurations.

D2	D1	D0	Channels
1	1	0	Left and Right
1	0	0	Right Only
0	1	0	Left Only

D4–D3. These bits determine the output effect. The following figure defines the signal configurations.

D4	D3	Type of Effect
1	1	Spatial Stereo
1	0	Pseudo Stereo
0	1	Linear Stereo
0	0	Forced Stereo

D5. This bit enables or disables mute.

D7-D6. These bits are reserved and set to 1.

09H – 0FH

Registers 09H through 0FH are the individual mixing controls, and comprise the mixer section of the audio card. The following figure provides descriptions for these registers.

09H — 0FH	
Register	Description
09H	Left Channel FM Volume
0AH	Right Channel FM Volume
0BH	Left Sampling Volume
0CH	Right Sampling Volume
0DH	Left Auxiliary Volume
0EH	Right Auxiliary Volume
0FH	Microphone Volume

There are 128 possible linear volume levels, ranging from silent (80H) up to a maximum gain (0FFH). If values less than 80H are written to this register, a negative voltage signal (negative polarity) would result. This may cancel out another signal and should be avoided. The following figure specifies the volume range.

Value	Volume Range
FFH	Maximum Volume
80H	Minimum Volume
00H	Negative Maximum Volume

11H: Audio Selection

This read/write register controls the antialiasing filters (input/output) and the auxiliary input. The same antialiasing filter is used for sampling and playback. The bit functions of this register are identified in the following figure and defined below.

11H: Audio Selection								
D7	D6	D5	D4	D3	D2	D1	D0	Function
							X	Right Channel Filter
						X		Left Channel Filter
					X			Auxiliary Input Control
		X						Internal Speaker Mixer
X	X		X	X				Reserved

D0. This bit is used to set the filter for Right Channel. When this bit is set to 1, the filter is set for recording. When set to 0, the filter is set for playback.

D1. This bit is used to set the filter for Left Channel. When this bit is set to 1, the filter is set for recording. When set to 0, the filter is set for playback.

D2. This bit controls the auxiliary input. When this bit is set to 1 forces the stereo input to monophonic to be sampled on Left Channel. When set to 0, the auxiliary input to stereo is restored.

D3–D4. These bits are reserved.

D5. This bit enables or disables the internal speaker of the PC to be mixed with the final audio output.

D7–D6. These bits are available.

13H: Audio IRQ/DMA Select—Left Channel

This read/write register controls the interrupt and DMA functionality of the FM and sampling features. The bit functions of this register are identified in the following figure and defined below.

13H: Audio IRQ/DMA Select –Channel 0								
D7	D6	D5	D4	D3	D2	D1	D0	Function
					X	X	X	Select Interrupt
				X				Enables Audio Interrupt
	X	X	X					Selects DMA
X								Enables Left Channel DMA

D2–D0. These bits control the IRQ selection, as defined in the following figure.

Interrupt Select	IRQ
0	3
1	4
2	5
3	7
4	10
5	11
6	12
7	15

D3. When this bit is set to 1, audio interrupts are enabled.

D6–D4. These bits select the DMA line for Left Channel, as defined in the following figure.

DMA Select	DMA Line
0	0
1	1
2	2
3	3

D7. When this bit is set to 1, the DMA for Left Channel is enabled.

14H: DMA Select Right Channel

The DMA select Right Channel register controls the DMA for Right Channel and is identical to the Left Channel register except for the IRQ information. The bit functions of this register are identified in the following figure and defined below.

14H: DMA Select Channel 1								
D7	D6	D5	D4	D3	D2	D1	D0	Function
			X	X	X	X	X	Reserved
	X	X						Selects DMA
X								Enables Right Channel DMA

D4–D0. These bits are reserved.

D6–D5. These bits select the DMA line for Right Channel, as shown in the following figure.

DMA Select	DMA Line
0	0
1	1
2	2
3	3

D7. When this bit is set to 1, the DMA for Right Channel is enabled.

15H: Audio Relocation

The audio relocation register provides the flexibility of relocating the I/O map of the FM banks and the sampling channels. The value written to this register is the port address divided by eight, which will force the location to be on an even byte boundary. The OPL3 and MMA use eight I/O ports, the desired base address divided by eight is the value written to this register. The value written will immediately relocate the audio functions. The bit functions of this register are identified below.

15H: Audio Relocation								
D7	D6	D5	D4	D3	D2	D1	D0	Function
	X	X	X	X	X	X	X	Audio Relocation Address
X								Reserved

The following figure provides the recommended default addresses.

Address	Section
388H, 389H	FM Bank 0
38AH, 38BH	FM Bank 1
38CH, 38DH	Sampling Left Channel
38EH, 38FH	Sampling Right Channel

Conclusion

The Gold Sound Standard completely defines the requirements of hardware compatibility on the register level. This low level of compatibility provides the software developer, who writes directly to the hardware, with a large variety of implementations based on a common audio platform. The Gold Sound Standard is a minimum implementation standard, offering a safe migration path for today's hardware and software designs.

For more information on the "Magic" chip set and implementing the Gold Sound Standard, call your local YAMAHA representative or contact YAMAHA at:

981 Ridder Park Drive
San Jose, CA 95131

(408) 437-3133

FAX (408) 437-8791

Appendix B: Surround Sound

Introduction

This section briefly describes how to program the Yamaha YM7128 Surround Processor (SP2) on the Gold Card.

A first section describes the method used to access the SP2 chip through the Control Chip on the Ad Lib Gold card.

The second part is a hardware description of the SP2 chip.

Sample source code is also available in the Developer Toolkit disk, in the <SURROUND> directory. This sample source code demonstrates the procedure used to download a surround preset to the SP2.

Communicating with the SP2

Register 18H of the Control Chip is used to interface with the SP2 Surround Processor.

Communication with the SP2 is done using a bit-serial protocol.

Modifying a register value to the SP2 involves sending a "register address - register value" pair to the SP2 using a special bit-serial protocol through register 18H.

SP2 bit-serial protocol

Bit 0 of register 18H is the Data Bit (DATA).

Bit 1 of register 18H is the Clock Bit (CLK).

Bit 2 of register 18H is the Address Latch Bit (ADR).

Each bit of a message is sent to the SP2 by first sending a byte with the CLK bit low.

The message bit is sent in a byte with CLK low and the DATA bit containing the desired bit value.

By sending a third byte with CLK high, and DATA set to the correct value, the bit is "latched" into the SP2.

The ADR bit is used to differentiate the register-address- register value parts of the message.

When the bytes related to the register address part of the message are sent, ADR should be low. When all 8 bits of the address have been sent, a bit should be sent with ADR high, to latch the register address to the SP2.

ADR should then be high while the bytes related to the register value part of the message is sent.

Finally a last byte with ADR low should be sent, to latch the register value part of the message.

Sample code on how this procedure is accomplished is supplied on the Developer Toolkit diskette (in directory SURROUND).

While communicating with the SP2, we recommend that interrupts be disabled, in order to avoid access conflicts with background applications that could access the OPL3 chip or the Control Chip.

YAMAHA® LSI

YM7128

Surround Processor (SP2)

■ OUTLINE

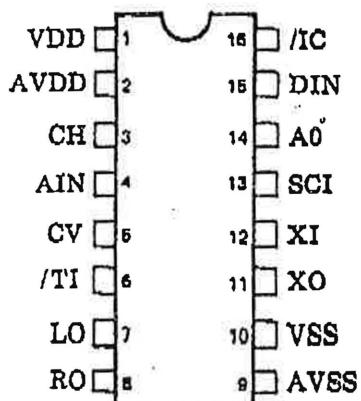
This is an LSI which has quality digital surround sound capabilities realized by Yamaha's digital audio technology. The LSI has built-in A/D and D/A converters which enable digital surround sound processing for analog input/output. Its eight digital delay lines may provide delay time of up to 100 msec. for each, and digital adding up of delay line signals for two-channel output assures a wide range of application.

■ FEATURES

- The built-in RAM realizes digital delay time of 100 msec.* at the maximum.
- Feedback loop can be constructed for reverberation.
- Various surround effect can be obtained by controlling this LSI with serial data from microprocessor.
- Digital attenuator is built in for surround sound volume control.
- Sampling frequency is 23.6 kHz*, and 14 bit floating A/D converter is built in.
- Two-times oversampling digital filter and 14 bit floating D/A converter are built in.
- 16 pin DIP package, silicone gate CMOS 5V power supply.

Note) When XI clock frequency is 7.16 MHz (304 fs is required for XI clock).

■ PIN CONFIGURATIONS



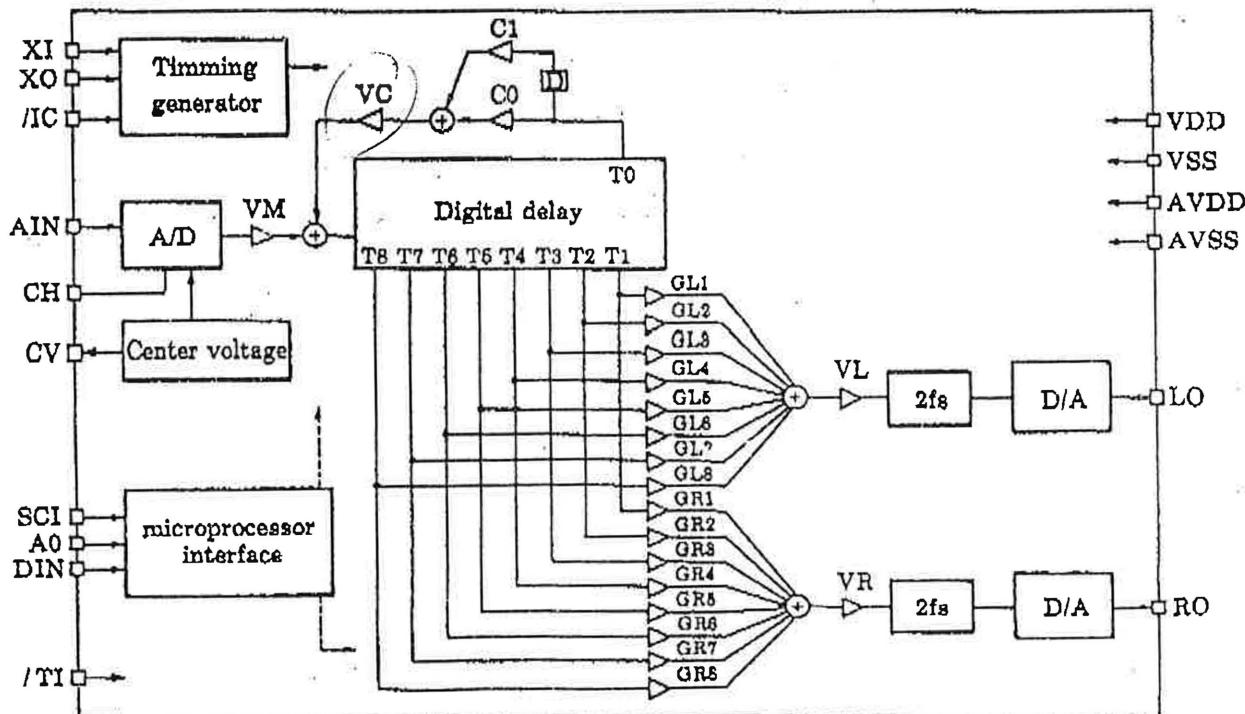
TOP VIEW

■ PIN DESCRIPTIONS

Pin No.	Name	I/O	Function
1	VDD	-	Digital +5V power supply
2	AVDD	-	Analog +5V power supply
3	CH	O	Sample/hold capacitor terminal
4	AIN	I	Analog signal input
5	CV	O	Center voltage of A/D
6	/TI	I+	Test terminal (without connection)
7	LO	O	L channel, analog out
8	RO	O	R channel, analog out
9	AVSS	--	Analog ground
10	VSS	-	Digital ground
11	XO	O	X'tal oscillator terminal (7.16 MHz typ.)
12	XI	I	
13	SCI	I	Bit clock for microprocessor interface
14	A0	I	Word clock for microprocessor interface
15	DIN	I	Serial data for microprocessor interface
16	/IC	I+	Initial clear terminal

+; pulled up

■ BLOCK DIAGRAM



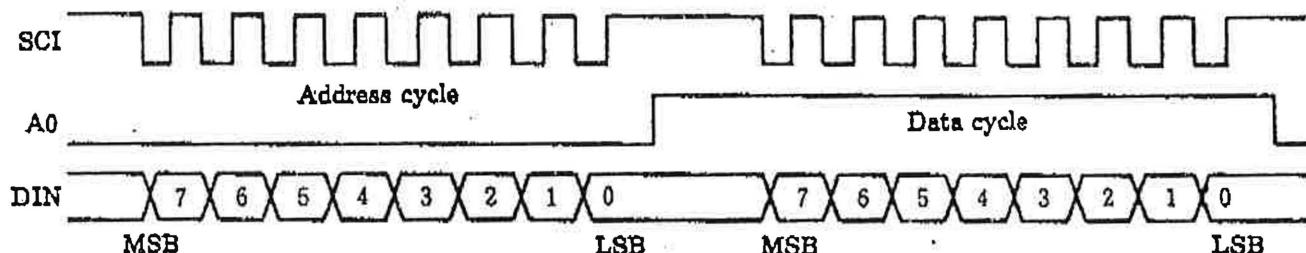
■ FUNCTION DESCRIPTION

As shown in the block diagram, analog signal input at AIN terminal are converted to 14 bit digital signal with the sampling frequency of 23.6 kHz using 14 bit floating type A/D converter, and then attenuated by the digital attenuator VM. Tap T0 output of digital delay passes through first order FIR type low pass filter and attenuated by VC. These signals are added before they are input to digital delay. Digital delay has nine output taps and tap positions can be switched by the registers T0 to T8. Outputs of eight taps from T1 to T8 are attenuated and added for each channel with the digital attenuator from GL1 to GL8 and GR1 to GR8 respectively, and attenuated by digital attenuator VL or VR to be input to two-times oversampling digital filter. Since this filter attenuates aliasing noise, it reduces the burden on external analog low pass filter. Digital input to D/A converter shall be with doubled value, which is 47.1 kHz sampling rate.

■ MICROPROCESSOR INTERFACE

Digital attenuation value, delay time and FIR type low pass filter coefficients are all set by writing data into registers.

With A0 = "L", 8 bit address data are sent synchronizing with SCI. At the rising edge of A0, register address is taken in. With A0 = "H", 8 bit data are sent synchronizing with SCI, then register data are changed at the falling edge of A0.



- At the time of initial clear, VM, VC, VL and VR registers are reset to 0. Other register values are not fixed.

■ REGISTER MAP

Address (HEX)	Data						Function	
	7	6	5	4	3	2	1	0
00	x	x						GL1
01	x	x						GL2
02	x	x						GL3
03	x	x						GL4
04	x	x						GL5
05	x	x						GL6
06	x	x						GL7
07	x	x						GL8
08	x	x						GR1
09	x	x						GR2
0A	x	x						GR3
0B	x	x						GR4
0C	x	x						GR5
0D	x	x						GR6
0E	x	x						GR7
0F	x	x						GR8

Address (HEX)	Data						Function	
	7	6	5	4	3	2	1	0
10	x	x						VM
11	x	x						VC
12	x	x						VL
13	x	x						VR
14	x	x						C0
15	x	x						C1
16	x	x	x					T0
17	x	x	x					T1
18	x	x	x					T2
19	x	x	x					T3
1A	x	x	x					T4
1B	x	x	x					T5
1C	x	x	x					T6
1D	x	x	x					T7
1E	x	x	x					T8

Note 1) x; Don't Care

Note 2) Don't write to the other address

■ REGISTER DATA DESCRIPTION

(1) Attenuation value setting (GL1 to GL8, GR1 to GR8, VM, VC, VL, VR)

• Output polarity (bit 5)

When bit 5 = "1": Output signal is in phase with input signal.

When bit 5 = "0": Output signal is reversed phase with input signal.

• Attenuation value (bit 4-0)

Level (dB)	Data					
	4	3	2	1	0	(HEX)
0	1	1	1	1	1	1F
-2	1	1	1	1	0	1E
-4	1	1	1	0	1	1D
-6	1	1	1	0	0	1C
-8	1	1	0	1	1	1B
-10	1	1	0	1	0	1A
-12	1	1	0	0	1	19
-14	1	1	0	0	0	18
-16	1	0	1	1	1	17
-18	1	0	1	1	0	16
-20	1	0	1	0	1	15
-22	1	0	1	0	0	14
-24	1	0	0	1	1	13
-26	1	0	0	1	0	12
-28	1	0	0	0	1	11
-30	1	0	0	0	0	10

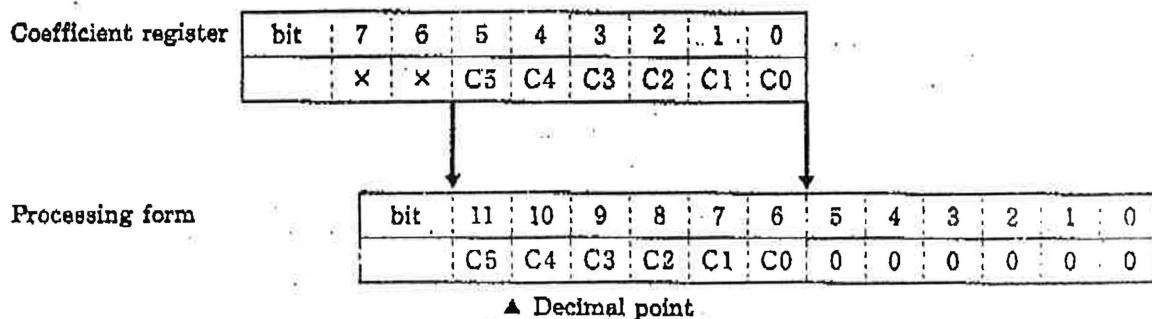
Level (dB)	Data					
	4	3	2	1	0	(HEX)
-82	0	1	1	1	1	0F
-84	0	1	1	1	0	0E
-86	0	1	1	0	1	0D
-88	0	1	1	0	0	0C
-40	0	1	0	1	1	0B
-42	0	1	0	1	0	0A
-44	0	1	0	0	1	09
-46	0	1	0	0	0	08
-48	0	0	1	1	1	07
-50	0	0	1	1	0	06
-52	0	0	1	0	1	05
-54	0	0	1	0	0	04
-56	0	0	0	1	1	03
-58	0	0	0	1	0	02
-60	0	0	0	0	1	01
-∞	0	0	0	0	0	00

(2) Delay time setting (T0 to T8) (XI = 7.16 MHz)

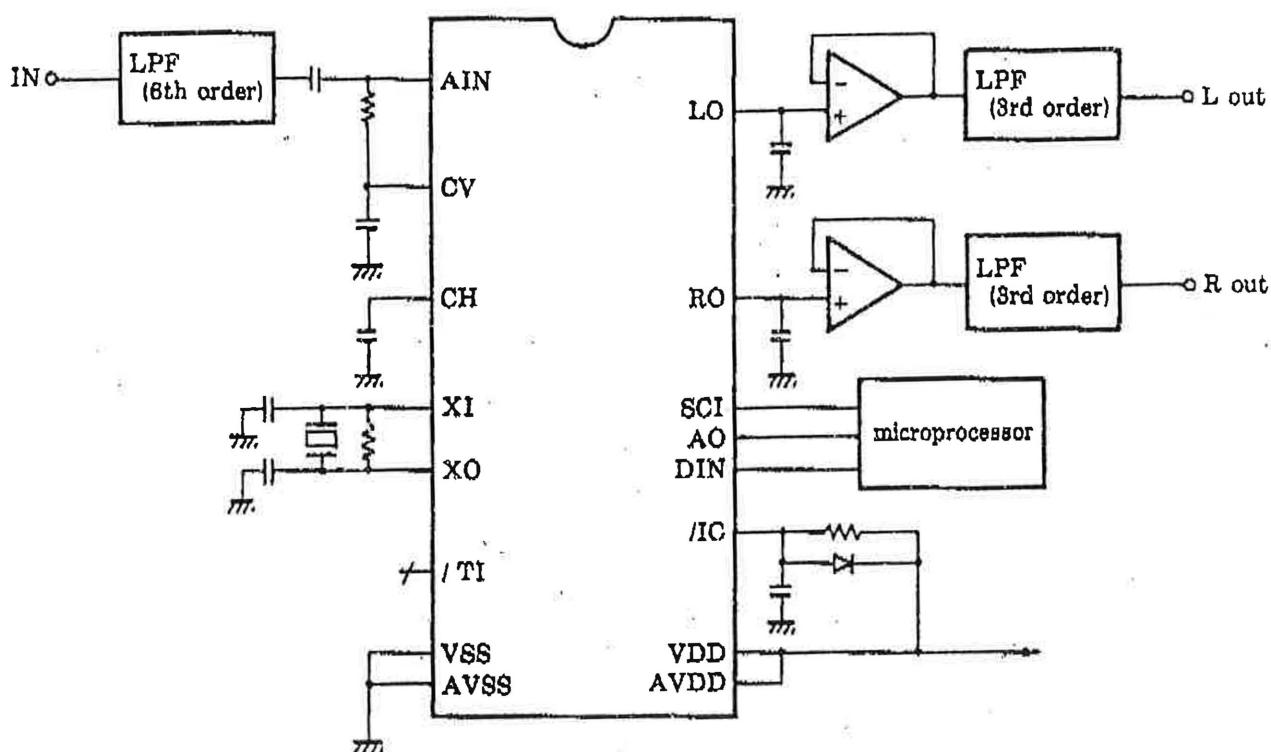
Delay time (ms)	Data		Delay time (ms)	Data		
	4	3 2 1 0	(HEX)	4	3 2 1 0	(HEX)
0.0	0	0 0 0 0	00	51.6	1 0 0 0 0	10
8.2	0	0 0 0 1	01	54.9	1 0 0 0 1	11
6.5	0	0 0 1 0	02	58.1	1 0 0 1 0	12
9.7	0	0 0 1 1	03	61.3	1 0 0 1 1	13
12.9	0	0 1 0 0	04	64.5	1 0 1 0 0	14
16.1	0	0 1 0 1	05	67.8	1 0 1 0 1	15
19.3	0	0 1 1 0	06	71.0	1 0 1 1 0	16
22.6	0	0 1 1 1	07	74.2	1 0 1 1 1	17
25.8	0	1 0 0 0	08	77.4	1 1 0 0 0	18
29.0	0	1 0 0 1	09	80.7	1 1 0 0 1	19
82.3	0	1 0 1 0	0A	83.9	1 1 0 1 0	1A
35.5	0	1 0 1 1	0B	87.1	1 1 0 1 1	1B
38.7	0	1 1 0 0	0C	90.4	1 1 1 0 0	1C
41.9	0	1 1 0 1	0D	93.6	1 1 1 0 1	1D
45.2	0	1 1 1 0	0E	96.8	1 1 1 1 0	1E
48.4	0	1 1 1 1	0F	100.0	1 1 1 1 1	1F

(3) FIR Low Pass Filter coefficient setting (C0, C1).

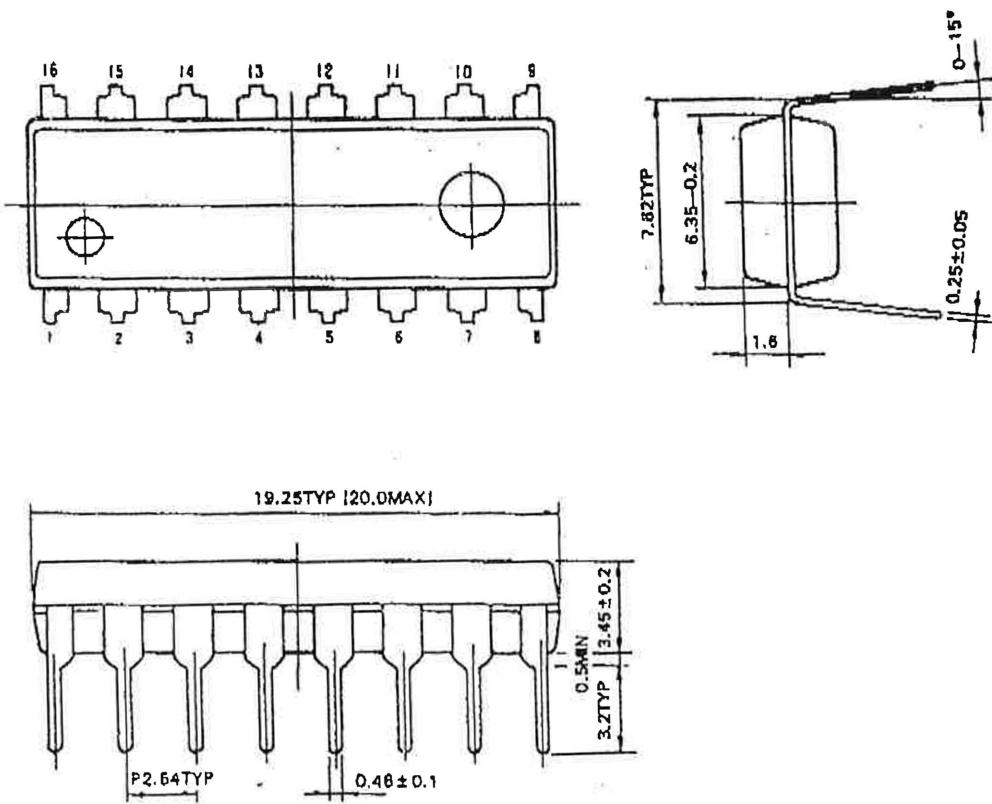
The lower 6 bits of coefficient register are used as the upper 6 bits of 12 bit 2's compliment data actually processed inside.



■ SYSTEM BLOCK DIAGRAM



■ EXTERNAL DIMENSIONS



ELECTRICAL CHARACTERISTICS

- Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 ~ +7.0	V
Operating temperature	Top	-20 ~ +85	°C
Storage temperature	Tstg	-60 ~ +125	°C

- Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	4.75	5.0	5.25	V
Operating temperature	Top	0	25	70	°C

- DC characteristics (Conditions: Ta = 25°C, VDD = 5.0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	IDD				50	mA
High-level input voltage (1)	VIH1		2.0			V *1
Low-level input voltage (1)	VIL1				0.8	V *1
High-level input voltage (2)	VIH2		4.0			V *2
Low-level input voltage (2)	VIL2				0.8	V *2
High-level output voltage	VOH	IOH = -0.4mA	4.0			V
Low-level output voltage	VOL	IOL = 0.2mA			0.4	V
Input leakage current	IIL	VI = 0 ~ 5V	-10		10	μA
Input capacitance	C _I			5.0	12.0	pF
Output capacitance	C _O				10.0	pF

Note 1: Applicable to the input terminals except XI

Note 2: Applicable to XI terminal

- AC characteristics (Conditions: Ta = 25°C, VDD = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XI Input frequency	fc	8.6	7.16	8.6	MHz
Duty		40	50	60	%
Rise time	TCR			50	ns
Fall time	TCF			50	ns
SCI Input frequency	fs			fc/8	MHz
On-off time	ts	600			ns
Rise time	TSR			200	ns
Fall time	TSF			200	ns

• ANALOG characteristics (Conditions: $T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog input voltage	V _{IA}	AIN terminal			4.5	V _{p-p}
Analog output voltage	V _{OA}	LO, RO terminal			4.5	V _{p-p}
DC offset voltage	C _V			2.5		V
Total harmonic distortion	THD	output voltage 0dB		0.3	0.4	%
		-10dB		0.4	0.5	%
		-20dB		0.4	0.5	%
		-30dB		0.6	0.8	%
S/N	S/N	S=0dB	75	80		dB

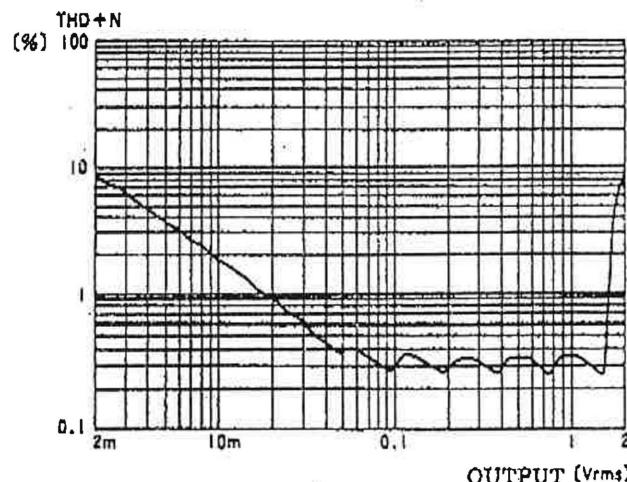
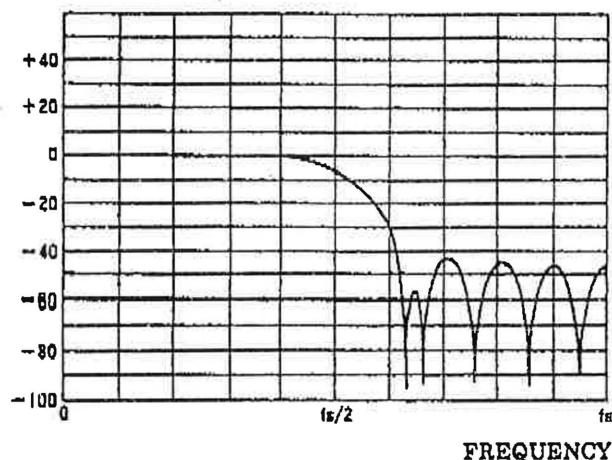
Note) 0dB = 1.5VRms

■ REFERENCE CHARACTERISTICS

2 times oversampling filter

Output vs THD + NOISE

(dB) OUTPUT



The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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The following source code demonstrates how to program a Surround preset.

Function Write_Srnd_Reg writes the specified value to the YM7128 through the control chip register 18H. The sample code assumes that the control chip is located at address 38AH.

Function Write_Surround sends the 32 bytes of a surround preset to the YM7128 using the bit-serial protocol. For each byte of the Surround preset, the register number (variable *addr*) is sent first , followed by the register value (variable *data*).

```
/*
   SURR.C
   Write a preset to the surround chip.
   Copyright 1992, Ad Lib Inc.
*/
unsigned control_io = 0x38a;      /* address of control chip section */

/* Write 'val' to the surround register in the control chip. */
static void __fastcall Write_Srnd_Reg (unsigned val)
{
    _asm {
        mov     dx, control_io
l10:
        in     al, dx
        test   al, 0c0h      ;status bits indicating chip is busy
        jnz    l10
        mov     ax, 18h        ;surround register number
        out    dx, al
        mov     ax, val
        inc    dx
        out    dx, al
    }
}
```

Appendix B: Surround Sound

Sample Source Code

```
/* NOTE: When writing a byte to the control chip, it is very important
   that the transfer not be interrupted. Therefore, interrupts are
   disabled while the preset is being sent. */
void Write_Surround (unsigned char *preset)
{
    unsigned addr, data, cmd;
    int i, k;

    __asm {
        pushf          ;preserve the current interrupt state
        push    dx
        cli             ;disable interrupts
        mov    dx, control_io
        mov    al, 0ffh      ;disable OPL3, enable control bank
        out    dx, al
    }

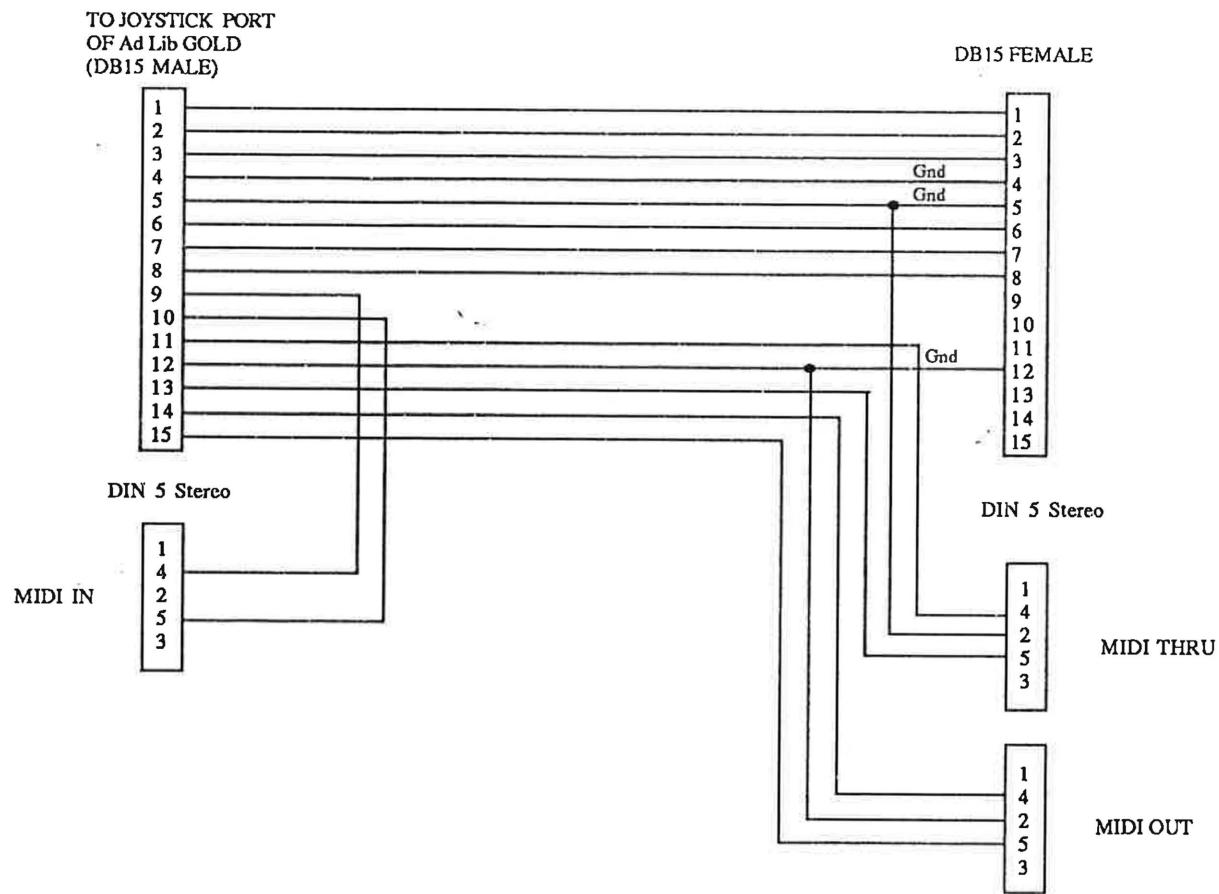
    /* Send the 31 array elements: */
    for (i = 0; i < 31; i++) {
        cmd = 0;           /* clock LOW, A0 LOW */
        addr = i;
        for (k = 7; k >= 0; k--) {
            cmd &= ~2;       /* clock LOW */
            Write_Srnd_Reg (cmd);
            cmd = (cmd & ~1) | ((addr >> k) & 1);
            Write_Srnd_Reg (cmd);
            cmd |= 2;         /* clock HIGH */
            Write_Srnd_Reg (cmd);
        }
        cmd |= 4;           /* Set A0 to 1 */
        Write_Srnd_Reg (cmd);

        data = preset [i];
        for (k = 7; k >= 0; k--) {
            cmd &= ~2;       /* clock LOW */
            Write_Srnd_Reg (cmd);
            cmd = (cmd & ~1) | ((data >> k) & 1);
            Write_Srnd_Reg (cmd);
            cmd |= 2;         /* clock HIGH */
            Write_Srnd_Reg (cmd);
        }
        cmd &= ~4;           /* Set A0 to 0 */
        Write_Srnd_Reg (cmd);
    }

    __asm {
        mov    dx, control_io
l20:
        in     al, dx
        test   al, 0c0h      ;status bits indicating chip is busy
        jnz    l20
        mov    al, 0feh      ;enable OPL3, disable control bank
        out    dx, al
        pop    dx
        popf
    }
}
```

Appendix C: Pin Out for Joystick-MIDI Connector

PIN OUT FOR JOYSTICK-MIDI CONNECTOR OF THE Ad Lib GOLD CARD



Appendix D: List of Installed Files

The Ad Lib Gold Developer Toolkit software included in the diskettes contains, when decompressed and installed, several files related to the utilization of the Gold card: drivers, application programs, music, sounds, and other various files. These files are:

- **README.TXT**
This file is not compressed on the diskette. It contains information on the latest program updates, if there are any, and any other pertinent information.
- **CTRLDRV.EXE**
This file is not compressed on the diskette. It contains the Ad Lib Gold Control chip driver. This low level driver is used by other programs, such as the Setup program, to implement: DMA channel & interrupt number select; sampling source select; sampling gain and input filter; microphone input gain; sampling output filtering and volume & tone control; mixing control; card localization setup and ID code reading; saving registers in non volatile memory.
- **SETUP.EXE**
This file is not compressed on the diskette. It contains the Installation and Configuration program. This program enables you to install the drivers and all associated programs, and to configure your Ad Lib Gold card.

Drivers and TSRs

Are located in the "DRIVERS" subdirectory.

- **FMDRV.EXE**
This file contains the FM driver. This low level driver implements: preset change; note on; note off; pitch bend; volume and stereo positioning.
- **WAVEDRV.EXE**
This file contains the Sampling driver. This low level driver implements: recording and playback of samples by DMA and interrupt.
- **TIMERDRV.EXE**
This file contains the Timer driver. This low level driver implements: the five timers of the Yamaha Magic Chip Set.
- **MIDIDRV.EXE**
This file contains the MIDI driver. This low level driver implements: MIDI In and Out serial port control.
- **RL2DRV.EXE**
This file contains the ROL2 driver. This low level TSR driver implements: playback of the .RL2 music files and user control commands .

Appendix D

List of Installed Files

- **MIXER.EXE**

This file contains the Mixer Panel TSR. This memory resident application allows for the control of the programmable volume and tone control, mixer settings, surround features, and setting of activation and volume keys.

- **PLAYRL2.EXE**

This file contains the executable code of ROL2 Playback utility.

- **PLAYDIGI.EXE**

This file contains the executable code of Digitized Sound Playback utility.

Application Programs (Executables)

- **TESTGOLD.EXE**

This file contains the Ad Lib Gold Test Program. This program enables you to verify that the Gold card is functioning properly in all of its different components.

- **JUKEG.EXE**

This file contains the executable code of Juke Box Gold Music Playback Program.

- **ED.EXE**

This file contains the executable code of Instrument Maker Gold.

- **SAMPL.EXE**

This file contains the executable code of Sample Maker Program.

- **SURR.EXE**

This file contains the executable code of Juke Box Gold with the Surround Sound Editor.

Batch Files

- **TEST.BAT**

This file contains the DOS command sequence which loads the necessary drivers and calls the Ad Lib Gold Test Program.

- **JUKEGOLD.BAT**

This file contains the DOS command sequence which loads the necessary drivers and calls the Juke Box Gold Music Playback Program.

- **INSGOLD.BAT**

This file contains the DOS command sequence which loads Instrument Maker Gold.

- **SURROUND.BAT**

This file contains the DOS command sequence which loads the necessary drivers and calls the Juke Box Gold Music Playback Program with the Surround Sound Editor.

- **DRIVERS.BAT**

This file contains the DOS command sequence which loads all Ad Lib Gold drivers.

Other Files

- ***.RL2**

The ".RL2" files contain the pieces of music that will be played with the Juke Box Gold.

- ***.SMP**

The ".SMP" files contain the PCM digitized sounds. TESTGLD1.SMP is the sound file that will be used by the Test Program.

- **SAMPLBNK.EQU**

This file contains a translation table of digitized instrument sound names, which is used by the ROL2 Playback driver.

- **OPL3.BNK**

This file contains the FM synthesized instrument sounds compatible with the OPL3 FM synthesis chip.

- **ED.RSR**

This file contains the resources required by Instrument Maker Gold.

- **SAMPL.RSR**

This file contains the resources required by Sample Maker Program.

Files Created by Programs

- **JUKEGOLD.DAT**

This file is created the first time you make a selection of songs in the Juke Box Gold program, permitting not to lose your selection even after rebooting the computer.

- **TESTGLD1.SMP**

This file is created by the Test Program when you test Sampling and Playback.

- **SAMPLES.BNK**

This bank file is created by the Sample Maker Program the first time you save a digitized sound in the ADPCM format.