SSD1306

Advance Information

128 x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

Appendix: IC Revision history of SSD1306 Specification

Version	Change	Items Effective	Date
1.0	1	1st release	3-Oct-07
1.1	1.	Revise typo 2. Revise command table	29-Apr-08
1.2	1.	Add Charge pump section 2. Add Advance graphic commands : 23h, D6h	07-Jul-09
1.3	1.	Revise Section 8.10 Charge Pump Regulator 2. Revise Section 12 DC Characteristics 3. Revise min. t_{AS} Address Setup Time in Table 13-2 to 5ns 4. Add Figure 10-7 Oscillator frequency setting 5. Update declaimer	07-May-10
1.4	1.	Replace SSD1306Z by SSD1306Z2 and add SSD1306Z2 into ordering information (P.7) 2. Add Power ON and OFF sequence with Charge Pump Application in section 8.9 (p.29)	13-Jul-10
1.5		1. Update Power on/off sequence with charge pump application in section 8.9 (p.29)	27-Aug-10

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TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1306 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1306 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface, I^2C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and calculator, etc.

2 FEATURES

- Resolution: 128 x 64 dot matrix panel
- Power supply
  - V_{DD} = 1.65V to 3.3V, < V_{BAT} for IC logic
  - V_{BAT} = 3.3V to 4.2V for charge pump regulator circuit
  - V_{CC} = 7V to 15V for Panel driving
- For matrix display
  - Segment maximum source current: 100uA
  - Common maximum sink current: 15mA
  - 256 step contrast brightness current control
- Embedded 128 x 64 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8-bit 6800/8080-series parallel interface
  - 3 /4 wire Serial Peripheral Interface
  - I^2C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Internal charge pump regulator
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG & COF
- Wide range of operating temperature: -40 ℃ to 85 ℃

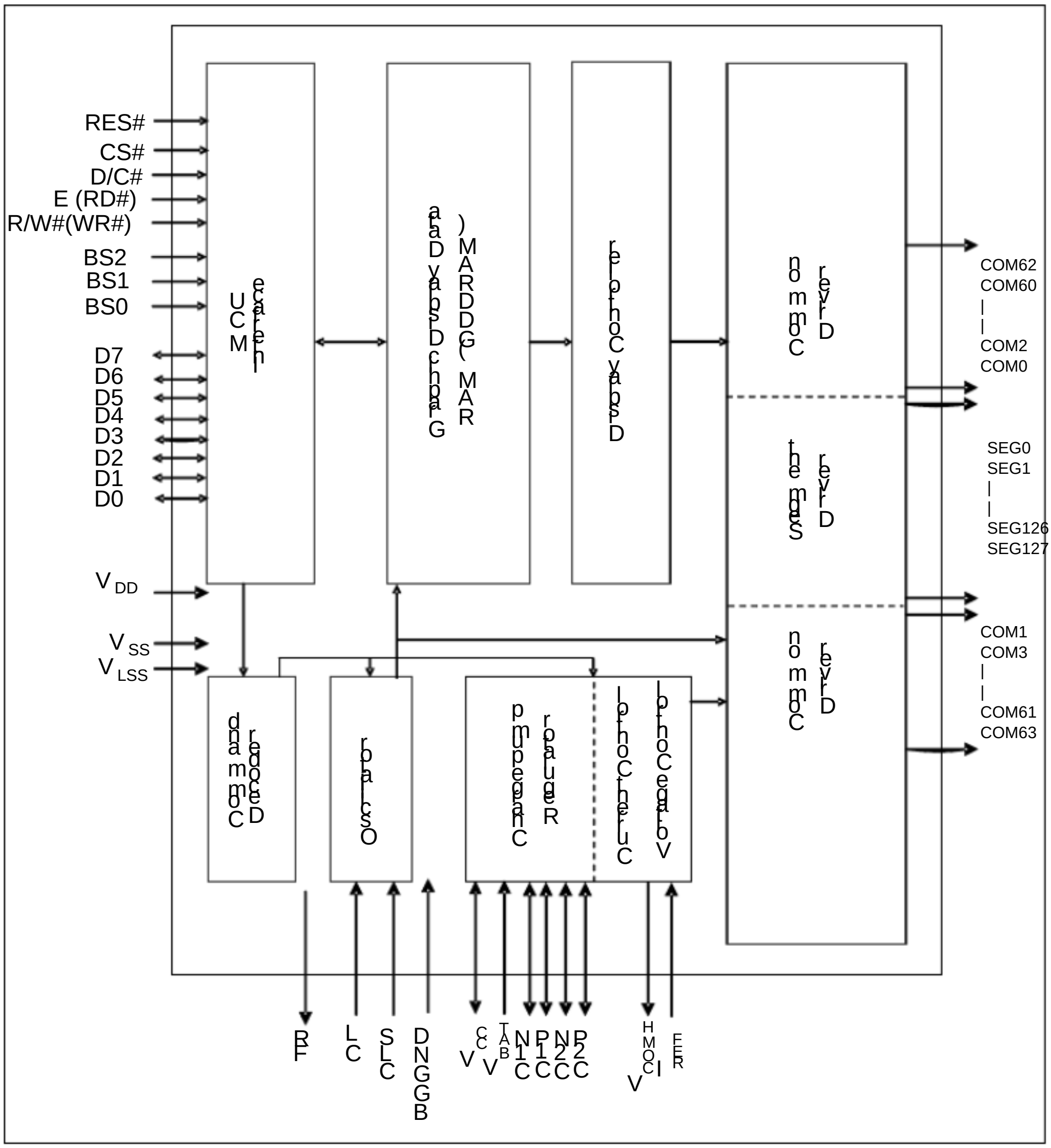
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1306Z2 128		64	COG	9	o Min SEG pad pitch : 47um o Min COM pad pitch : 40um o Die thickness: 300 +/- 25um
SSD1306TR1 104		48	TAB	12, 61	o 35mm film, 4 sprocket hole, Folding TAB o 8-bit 80 / 8-bit 68 / SPI / I^2C interface o SEG, COM lead pitch 0.1mm x 0.997 =0.0997mm o Die thickness: 457 +/- 25um

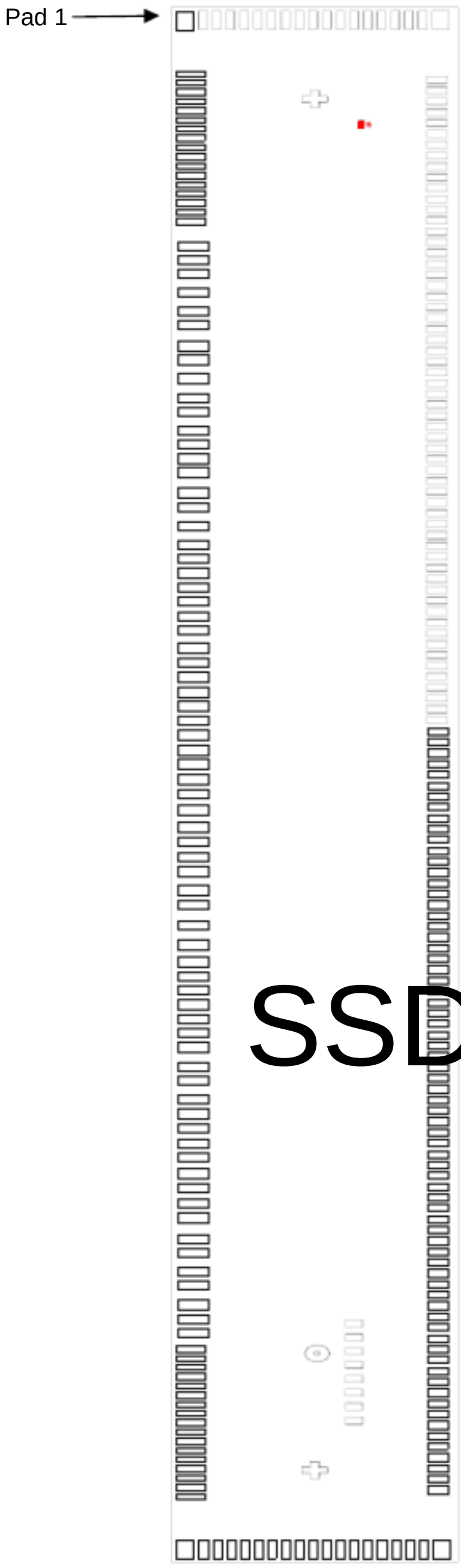
4 BLOCK DIAGRAM

Figure 4-1 SSD1306 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1306Z2 Die Drawing



Die Size (after sawing)	6.76mm +/- 0.05mm x 0.86mm +/- 0.05mm
Die thickness	300 +/- 15um
Min I/O pad pitch	60um
Min SEG pad pitch	47um
Min COM pad pitch	40um
Bump height	Nominal 12um

Bump size	
Pad 1, 106, 124, 256	80um x 50um
Pad 2-18, 89-105, 107-123, 257-273	25um x 80um
Pad 19-88	40um x 89um
Pad 125-255	31um x 59um
Pad 274-281 (TR pads)	30um x 50um

Alignment mark	Position Size	
+ shape	(-2973, 0)	75um x 75um
+ shape	(2973, 0)	75um x 75um
Circle	(2466.665, 7.575)	R37.5um, inner 18um
SSL Logo	(-2862.35, 144.82)	-

(For details dimension please see p.9)

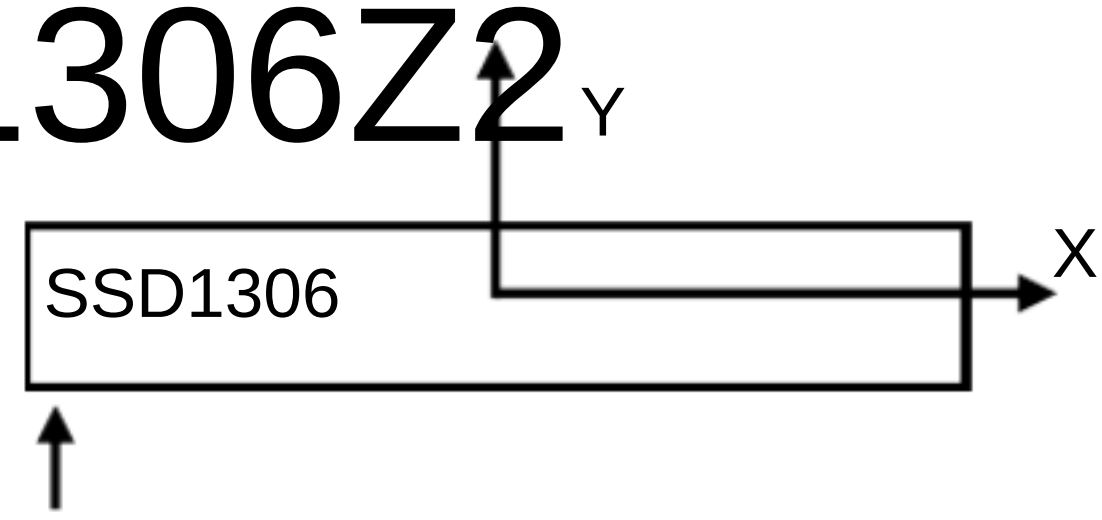
Note

(1) Diagram showing the Gold bumps face up.

(2) Coordinates are referenced to center of the chip.

(3) Coordinate units and size of all alignment marks are in um.

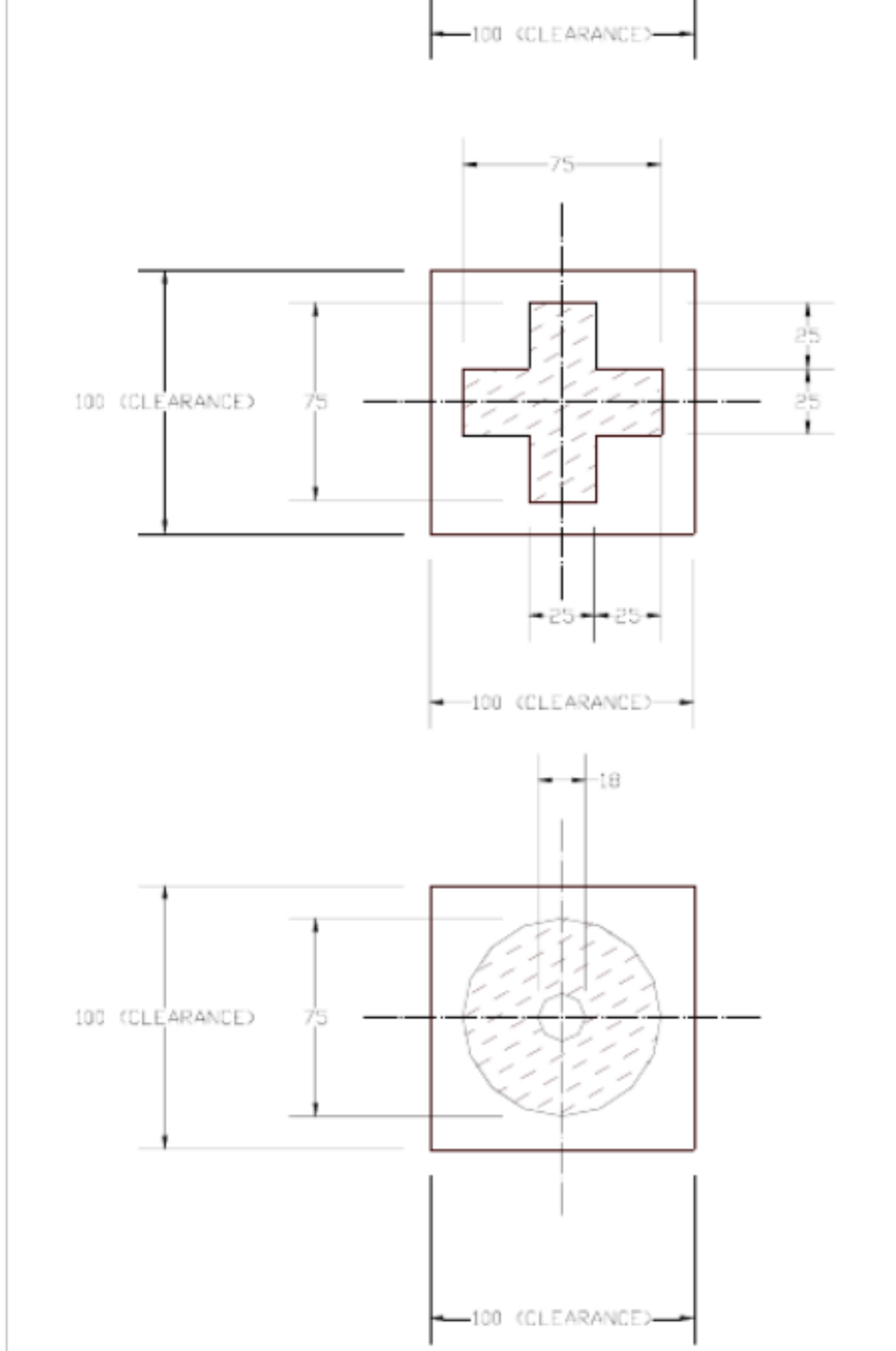
(4) All alignment keys do not contain gold



Pad 1,2,3, ⋯ ->281

Gold Bumps face up

Figure 5-2 : SSD1306Z2 alignment mark dimensions



T shape

+ shape

Circle

*All units are in um

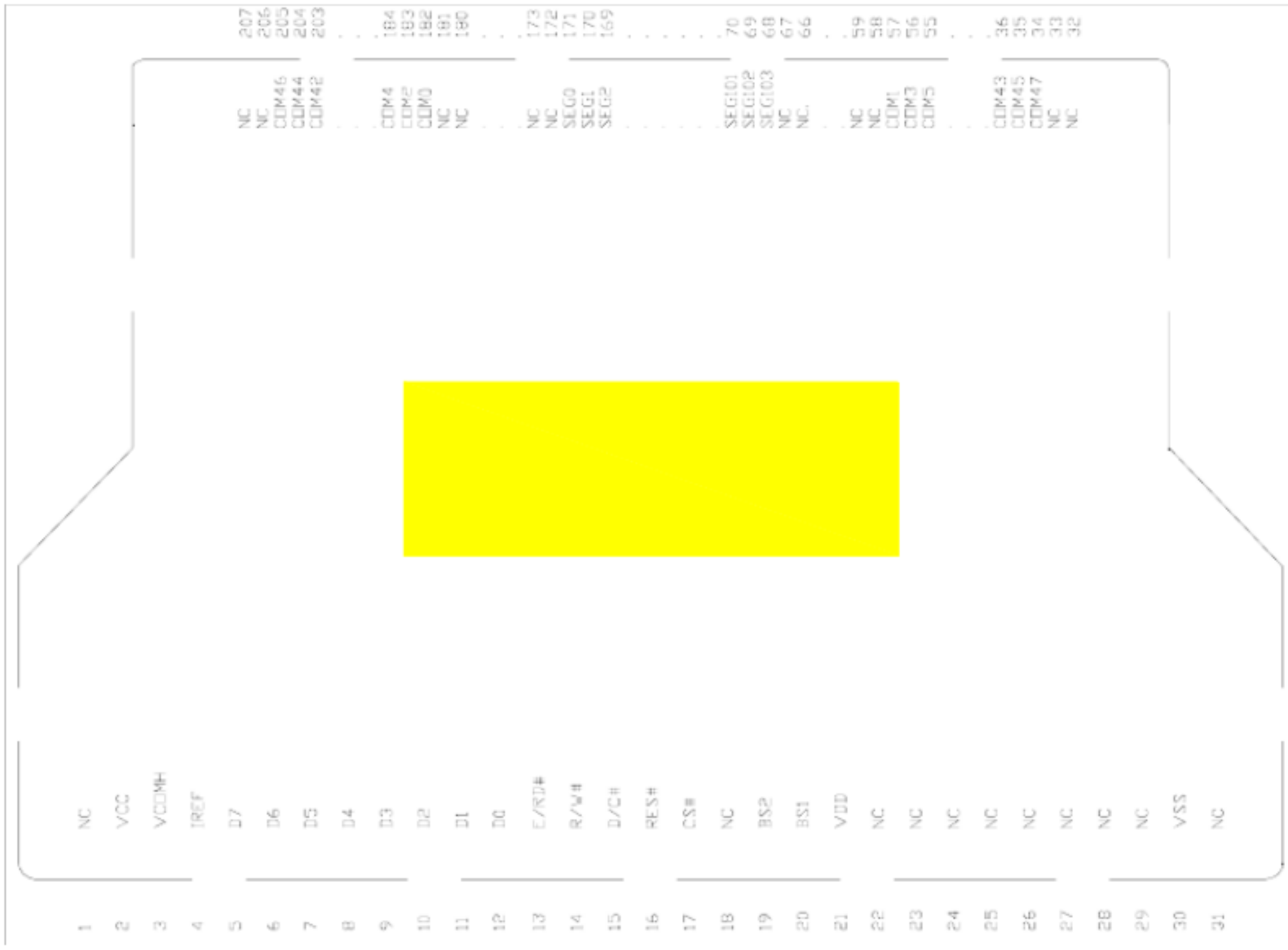
Table 5-1 : SSD1306Z2 Bump Die Pad Coordinates

Pad no.	Pad Name	X-pos	Y-pos	Pad no.	Pad Name	X-pos	Y-pos	Pad no.	Pad Name	X-pos	Y-pos	Pad no.	Pad Name	X-pos	Y-pos
1	NC	-3315	-377.5	81	VCOMH	1875.585	-352.83	161	SEG35	1364.5	356	241	SEG114	-2398.5	356
2	VSS	-3084.77	-362.5	82	VCC	1967.185	-352.83	162	SEG36	1317.5	356	242	SEG115	-2445.5	356
3	COM49	-3044.77	-362.5	83	VCC	2027.185	-352.83	163	SEG37	1270.5	356	243	SEG116	-2492.5	356
4	COM50	-3004.77	-362.5	84	VLSS	2109.185	-352.83	164	SEG38	1223.5	356	244	SEG117	-2539.5	356
5	COM51	-2964.77	-362.5	85	VLSS	2169.185	-352.83	165	SEG39	1176.5	356	245	SEG118	-2586.5	356
6	COM52	-2924.77	-362.5	86	VLSS	2254.185	-352.83	166	SEG40	1129.5	356	246	SEG119	-2633.5	356
7	COM53	-2884.77	-362.5	87	NC	2314.185	-352.83	167	SEG41	1082.5	356	247	SEG120	-2680.5	356
8	COM54	-2844.77	-362.5	88	NC	2374.185	-352.83	168	SEG42	1035.5	356	248	SEG121	-2727.5	356
9	COM55	-2804.77	-362.5	89	VSS	2444.77	-362.5	169	SEG43	988.5	356	249	SEG122	-2774.5	356
10	COM56	-2764.77	-362.5	90	COM31	2484.77	-362.5	170	SEG44	941.5	356	250	SEG123	-2821.5	356
11	COM57	-2724.77	-362.5	91	COM30	2524.77	-362.5	171	SEG45	894.5	356	251	SEG124	-2868.5	356
12	COM58	-2684.77	-362.5	92	COM29	2564.77	-362.5	172	SEG46	847.5	356	252	SEG125	-2915.5	356
13	COM59	-2644.77	-362.5	93	COM28	2604.77	-362.5	173	SEG47	800.5	356	253	SEG126	-2962.5	356
14	COM60	-2604.77	-362.5	94	COM27	2644.77	-362.5	174	SEG48	753.5	356	254	SEG127	-3009.5	356
15	COM61	-2564.77	-362.5	95	COM26	2684.77	-362.5	175	SEG49	706.5	356	255	NC	-3056.5	356
16	COM62	-2524.77	-362.5	96	COM25	2724.77	-362.5	176	SEG50	659.5	356	256	NC	-3315	367.5
17	COM63	-2484.77	-362.5	97	COM24	2764.77	-362.5	177	SEG51	612.5	356	257	COM32	-3315	315
18	VCOMH	-2444.77	-362.5	98	COM23	2804.77	-362.5	178	SEG52	565.5	356	258	COM33	-3315	275
19	NC	-2334.965	-352.83	99	COM22	2844.77	-362.5	179	SEG53	518.5	356	259	COM34	-3315	235
20	C2P	-2278.265	-352.83	100	COM21	2884.77	-362.5	180	SEG54	471.5	356	260	COM35	-3315	195
21	C2P	-2218.265	-352.83	101	COM20	2924.77	-362.5	181	SEG55	424.5	356	261	COM36	-3315	155
22	C2N	-2136.715	-352.83	102	COM19	2964.77	-362.5	182	SEG56	377.5	356	262	COM37	-3315	115
23	C2N	-2055.465	-352.83	103	COM18	3004.77	-362.5	183	SEG57	330.5	356	263	COM38	-3315	75
24	C1P	-1995.465	-352.83	104	COM17	3044.77	-362.5	184	SEG58	283.5	356	264	COM39	-3315	35
25	C1P	-1904.115	-352.83	105	VSS	3084.77	-362.5	185	SEG59	236.5	356	265	COM40	-3315	-5
26	C1N	-1844.115	-352.83	106	NC	3315	-377.5	186	SEG60	189.5	356	266	COM41	-3315	-45
27	C1N	-1762.865	-352.83	107	COM16	3315	-325	187	SEG61	142.5	356	267	COM42	-3315	-85
28	VBAT	-1679.31	-352.83	108	COM15	3315	-285	188	SEG62	95.5	356	268	COM43	-3315	-125
29	VBAT	-1619.31	-352.83	109	COM14	3315	-245	189	SEG63	48.5	356	269	COM44	-3315	-165
30	VBREF	-1537.51	-352.83	110	COM13	3315	-205	190	SEG64	1.5	356	270	COM45	-3315	-205
31	BGGND	-1477.51	-352.83	111	COM12	3315	-165	191	SEG65	-45.5	356	271	COM46	-3315	-245
32	VCC	-1416.01	-352.83	112	COM11	3315	-125	192	SEG66	-92.5	356	272	COM47	-3315	-285
33	VCC	-1356.01	-352.83	113	COM10	3315	-85	193	SEG67	-139.5	356	273	COM48	-3315	-325
34	VCOMH	-1266.955	-352.83	114	COM9	3315	-45	194	SEG68	-186.5	356				
35	VCOMH	-1206.955	-352.83	115	COM8	3315	-5	195	SEG69	-233.5	356	Pad no.	Pad Name	X-pos	Y-pos
36	VLSS	-1125.155	-352.83	116	COM7	3315	35	196	SEG70	-280.5	356	Pin#	Pin name	X-dir	Y-dir
37	VLSS	-1043.355	-352.83	117	COM6	3315	75	197	SEG71	-327.5	356	274	TR0	2757.05	114.8
38	VLSS	-983.355	-352.83	118	COM5	3315	115	198	SEG72	-374.5	356	275	TR1	2697.05	114.8
39	VSS	-920	-352.83	119	COM4	3315	155	199	SEG73	-421.5	356	276	TR2	2637.05	114.8
40	VSS	-856	-352.83	120	COM3	3315	195	200	SEG74	-468.5	356	277	TR3	2577.05	114.8
41	VSS	-796	-352.83	121	COM2	3315	235	201	SEG75	-515.5	356	278	VSS	2517.05	114.8
42	VDD	-732.645	-352.83	122	COM1	3315	275	202	SEG76	-562.5	356	279	TR4	2457.05	114.8
43	VDD	-672.645	-352.83	123	COM0	3315	315	203	SEG77	-609.5	356	280	TR5	2397.05	114.8
44	BS0	-595.655	-352.83	124	NC	3315	367.5	204	SEG78	-656.5	356	281	TR6	2337.05	114.8
45	VSS	-531.955	-352.83	125	NC	3055.5	356	205	SEG79	-703.5	356				
46	BS1	-467.655	-352.83	126	SEG0	3009.5	356	206	SEG80	-750.5	356				
47	VDD	-403.155	-352.83	127	SEG1	2962.5	356	207	SEG81	-797.5	356				
48	VDD	-342.555	-352.83	128	SEG2	2915.5	356	208	SEG82	-844.5	356				
49	BS2	-279.705	-352.83	129	SEG3	2868.5	356	209	SEG83	-891.5	356				
50	VSS	-215.705	-352.83	130	SEG4	2821.5	356	210	NC	-940	356				
51	FR	-151.955	-352.83	131	SEG5	2774.5	356	211	SEG84	-988.5	356				
52	CL	-89.815	-352.83	132	SEG6	2727.5	356	212	SEG85	-1035.5	356				
53	VSS	-25.665	-352.83	133	SEG7	2680.5	356	213	SEG86	-1082.5	356				
54	CS#	38.635	-352.83	134	SEG8	2633.5	356	214	SEG87	-1129.5	356				
55	RES#	109.835	-352.83	135	SEG9	2586.5	356	215	SEG88	-1176.5	356				
56	D/C#	182.425	-352.83	136	SEG10	2539.5	356	216	SEG89	-1223.5	356				
57	VSS	246.125	-352.83	137	SEG11	2492.5	356	217	SEG90	-1270.5	356				
58	R/W#	310.425	-352.83	138	SEG12	2445.5	356	218	SEG91	-1317.5	356				
59	E	373.125	-352.83	139	SEG13	2398.5	356	219	SEG92	-1364.5	356				
60	VDD	457.175	-352.83	140	SEG14	2351.5	356	220	SEG93	-1411.5	356				
61	VDD	517.175	-352.83	141	SEG15	2304.5	356	221	SEG94	-1458.5	356				
62	D0	609.275	-352.83	142	SEG16	2257.5	356	222	SEG95	-1505.5	356				
63	D1	692.475	-352.83	143	SEG17	2210.5	356	223	SEG96	-1552.5	356				
64	D2	765.675	-352.83	144	SEG18	2163.5	356	224	SEG97	-1599.5	356				
65	D3	828.875	-352.83	145	SEG19	2116.5	356	225	SEG98	-1646.5	356				
66	VSS	890.325	-352.83	146	SEG20	2069.5	356	226	SEG99	-1693.5	356				
67	D4	951.275	-352.83	147	SEG21	2022.5	356	227	SEG100	-1740.5	356				
68	D5	1013.315	-352.83	148	SEG22	1975.5	356	228	SEG101	-1787.5	356				
69	D6	1075.355	-352.83	149	SEG23	1928.5	356	229	SEG102	-1834.5	356				
70	D7	1137.395	-352.83	150	SEG24	1881.5	356	230	SEG103	-1881.5	356				
71	VSS	1220.735	-352.83	151	SEG25	1834.5	356	231	SEG104	-1928.5	356				
72	VSS	1280.735	-352.83	152	SEG26	1787.5	356	232	SEG105	-1975.5	356				
73	CLS	1362.585	-352.83	153	SEG27	1740.5	356	233	SEG106	-2022.5	356				
74	VDD	1425.285	-352.83	154	SEG28	1693.5	356	234	SEG107	-2069.5	356				
75	VDD	1485.885	-352.83	155	SEG29	1646.5	356	235	SEG108	-2116.5	356				
76	VDD	1553.185	-352.83	156	SEG30	1599.5	356	236	SEG109	-2163.5	356				
77	VDD	1613.185	-352.83	157	SEG31	1552.5	356	237	SEG110	-2210.5	356				
78	IREF	1684.585	-352.83	158	SEG32	1505.5	356	238	SEG111	-2257.5	356				
79	IREF	1744.585	-352.83	159	SEG33	1458.5	356	239	SEG112	-2304.5	356				
80	VCOMH	1815.585	-352.83	160	SEG34	1411.5	356	240	SEG113	-2351.5	356				

6 PIN ARRANGEMENT

6.1 SSD1306TR1 pin assignment

Figure 6-1 : SSD1306TR1 Pin Assignment



Note:
(1) COM sequence (Split) is under command setting: DAh, 12h

Table 6-1 : SSD1306TR1 Pin Assignment Table

Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name
1	NC	81	SEG90	161	SEG10
2	VCC	82	SEG89	162	SEG9
3	VCOMH	83	SEG88	163	SEG8
4	IREF	84	SEG87	164	SEG7
5	D7	85	SEG86	165	SEG6
6	D6	86	SEG85	166	SEG5
7	D5	87	SEG84	167	SEG4
8	D4	88	SEG83	168	SEG3
9	D3	89	SEG82	169	SEG2
10	D2	90	SEG81	170	SEG1
11	D1	91	SEG80	171	SEG0
12	D0	92	SEG79	172	NC
13	E/RD#	93	SEG78	173	NC
14	R/W#	94	SEG77	174	NC
15	D/C#	95	SEG76	175	NC
16	RES#	96	SEG75	176	NC
17	CS#	97	SEG74	177	NC
18	NC	98	SEG73	178	NC
19	BS2	99	SEG72	179	NC
20	BS1	100	SEG71	180	NC
21	VDD	101	SEG70	181	NC
22	NC	102	SEG69	182	COM0
23	NC	103	SEG68	183	COM2
24	NC	104	SEG67	184	COM4
25	NC	105	SEG66	185	COM6
26	NC	106	SEG65	186	COM8
27	NC	107	SEG64	187	COM10
28	NC	108	SEG63	188	COM12
29	NC	109	SEG62	189	COM14
30	VSS	110	SEG61	190	COM16
31	NC	111	SEG60	191	COM18
32	NC	112	SEG59	192	COM20
33	NC	113	SEG58	193	COM22
34	COM47	114	SEG57	194	COM24
35	COM45	115	SEG56	195	COM26
36	COM43	116	SEG55	196	COM28
37	COM41	117	SEG54	197	COM30
38	COM39	118	SEG53	198	COM32
39	COM37	119	SEG52	199	COM34
40	COM35	120	SEG51	200	COM36
41	COM33	121	SEG50	201	COM38
42	COM31	122	SEG49	202	COM40
43	COM29	123	SEG48	203	COM42
44	COM27	124	SEG47	204	COM44
45	COM25	125	SEG46	205	COM46
46	COM23	126	SEG45	206	NC
47	COM21	127	SEG44	207	NC
48	COM19	128	SEG43		
49	COM17	129	SEG42		
50	COM15	130	SEG41		
51	COM13	131	SEG40		
52	COM11	132	SEG39		
53	COM9	133	SEG38		
54	COM7	134	SEG37		
55	COM5	135	SEG36		
56	COM3	136	SEG35		
57	COM1	137	SEG34		
58	NC	138	SEG33		
59	NC	139	SEG32		
60	NC	140	SEG31		
61	NC	141	SEG30		
62	NC	142	SEG29		
63	NC	143	SEG28		
64	NC	144	SEG27		
65	NC	145	SEG26		
66	NC	146	SEG25		
67	NC	147	SEG24		
68	SEG103	148	SEG23		
69	SEG102	149	SEG22		
70	SEG101	150	SEG21		
71	SEG100	151	SEG20		
72	SEG99	152	SEG19		
73	SEG98	153	SEG18		
74	SEG97	154	SEG17		
75	SEG96	155	SEG16		
76	SEG95	156	SEG15		
77	SEG94	157	SEG14		
78	SEG93	158	SEG13		
79	SEG92	159	SEG12		
80	SEG91	160	SEG11		

7 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Figure 7-1 Pin Description

Pin Name	Type	Description
V_{DD}	P	Power supply pin for core logic operation.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. When charge pump is enabled, a capacitor should be connected between this pin and V_{SS}.
V_{SS}	P	This is a ground pin.
V_{LSS}	P	This is an analog ground pin. It should be connected to V_{SS} externally.
V_{COMH}	O	The pin for COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
V_{BAT}	P	Power supply for charge pump regulator circuit. Status V_{BAT}: Enable charge pump — Connect to external V_{BAT} source; V_{DD}: Connect to external V_{DD} source; V_{CC}: A capacitor should be connected between this pin and V_{SS} Disable charge pump — Keep float; Connect to external V_{DD} source; Connect to external V_{CC} source
BGGND	P	Reserved pin. It should be connected to ground.
C1P/C1N C2P/C2N	I	C1P/C1N – Pin for charge pump capacitor; Connect to each other with a capacitor. C2P/C2N – Pin for charge pump capacitor; Connect to each other with a capacitor.
V_{BREF}	P	Reserved pin. It should be kept NC.
BS[2:0]	I	MCU bus interface selection pins. Please refer to Table 7-1 for the details of setting.
I_{REF}	I	This is segment output current reference pin. A resistor should be connected between this pin and V_{SS} to maintain the I_{REF} current at 12.5 uA. Please refer to Figure 8-15 for the details of resistor value.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used. Please refer to Section 8.4 for details usage.
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.

Pin Name	Type	Description
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to V_{DD}) during normal operation.
CS#	I	This pin is the chip select input. (active LOW).
D/C#	I	This is Data/Command control pin. When it is pulled HIGH (i.e. connect to V_{DD}), the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS}. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams: Figure 13-1 to Figure 13-5.
E (RD#)	I	When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to V_{DD}) and the chip is selected. When connecting to an 8080-series microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
R/W#(WR#)	I	This is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to V_{DD}) and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	IO	These are 8-bit bi-directional data bus to be connected to the microprocessor ’s data l serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
TR0-TR6	-	Testing reserved pins. It should be kept NC.
SEG0 ~ SEG127	O	These pins provide Segment switch signals to OLED panel. These pins are V_{SS} state when display is OFF.
COM0 ~ COM63	O	These pins provide Common switch signals to OLED panel. They are in high impedance state when display is OFF.
NC	-	This is dummy pin. Do not group or short NC pins together.

Table 7-1 : MCU Bus Interface Pin Selection

SSD1306 Pin Name	I^2C Interface	6800-parallel interface (8 bit)	8080-parallel interface(8 bit)	4-wire Serial interface	3-wire Serial interface
BS0	0	0 0		0	1
BS1	1	0 1		0	0
BS2	0	1 1		0	0

Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface selection

SSD1306 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-1 for BS[2:0] setting).

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

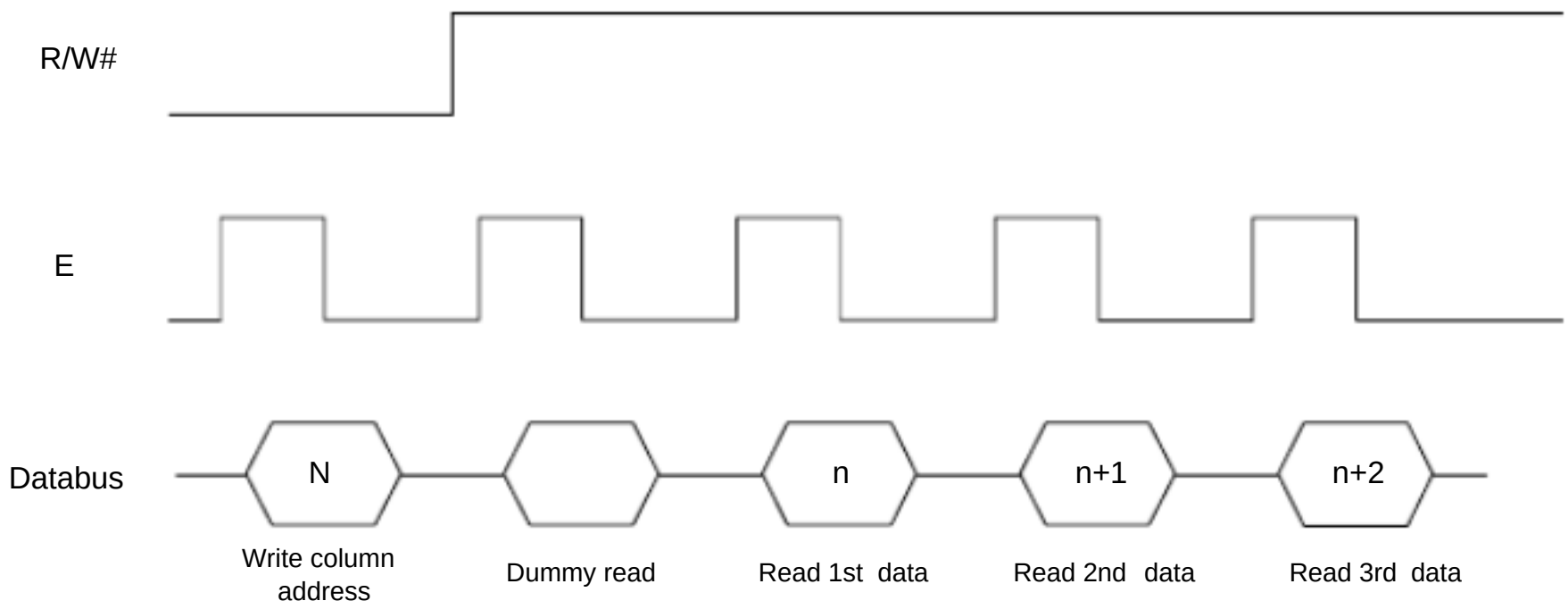
Table 8-2 : Control pins of 6800 interface

Function E		R/W#	CS#	D/C#
Write command	↓L L L			
Read status	↓H		L L	
Write data	↓L L H			
Read data	↓H		L H	

Note
(1) ↓stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

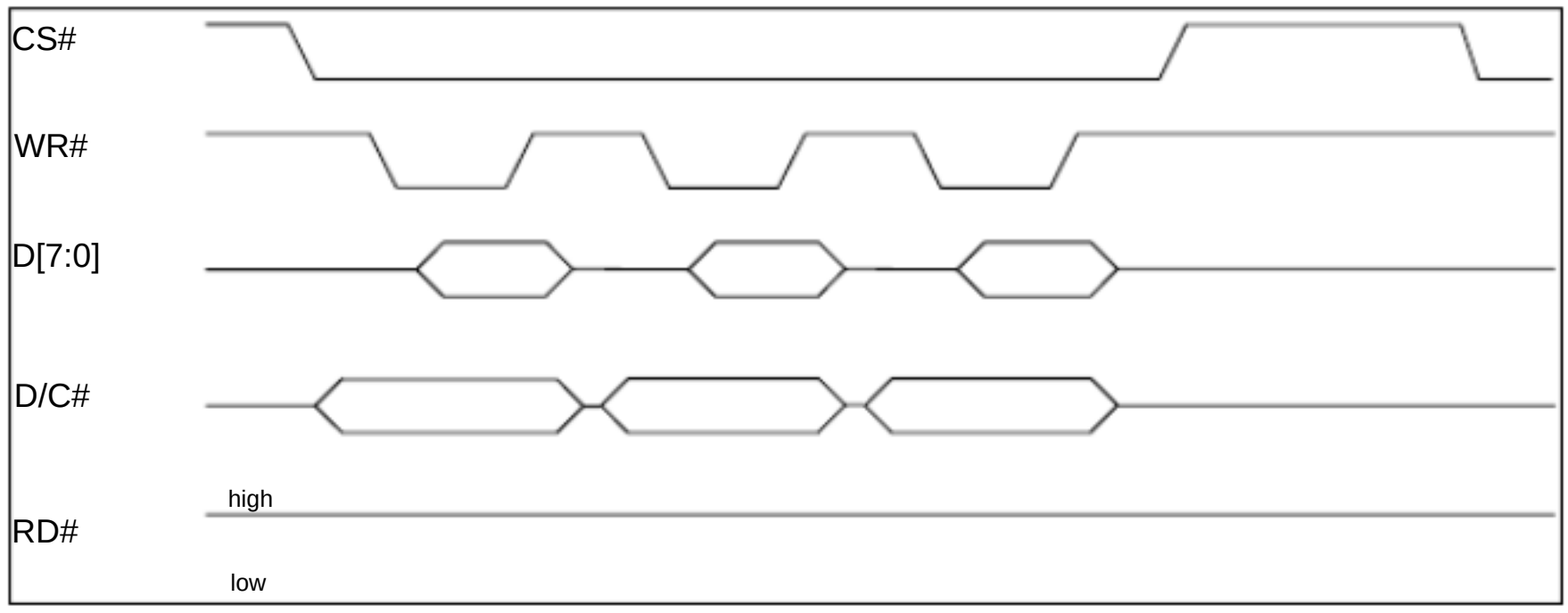


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

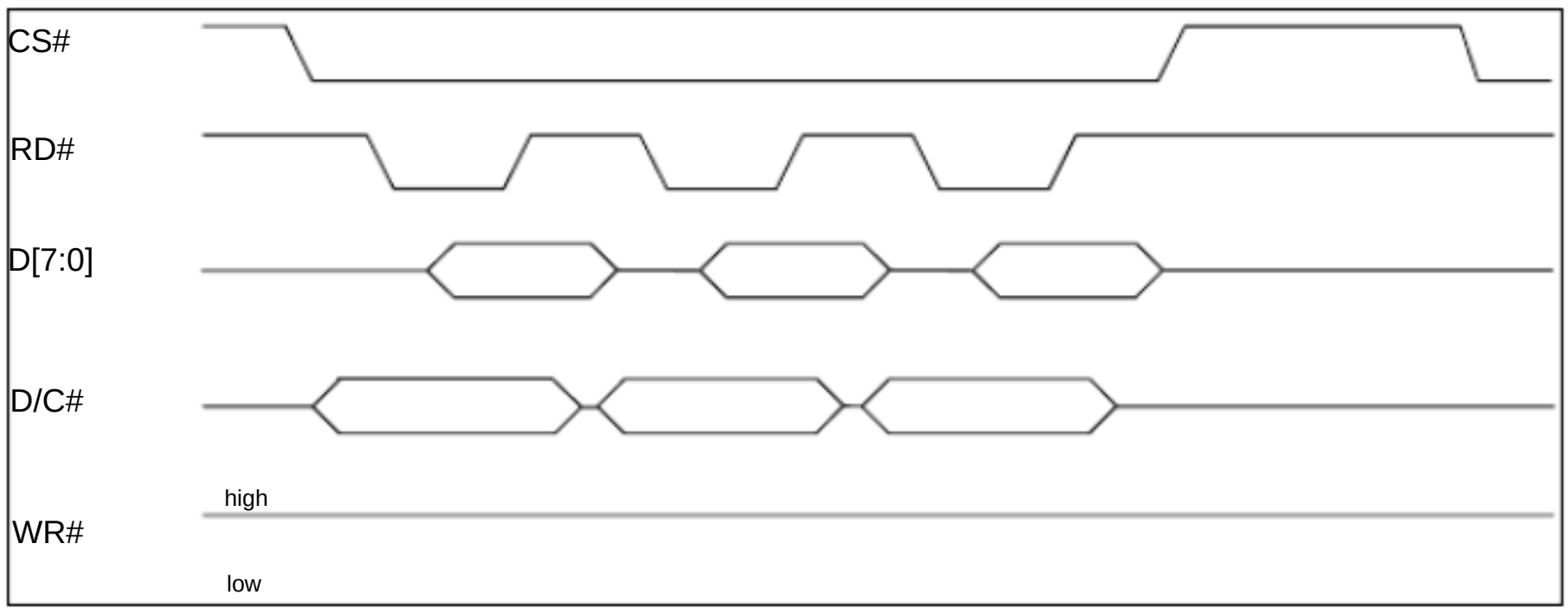


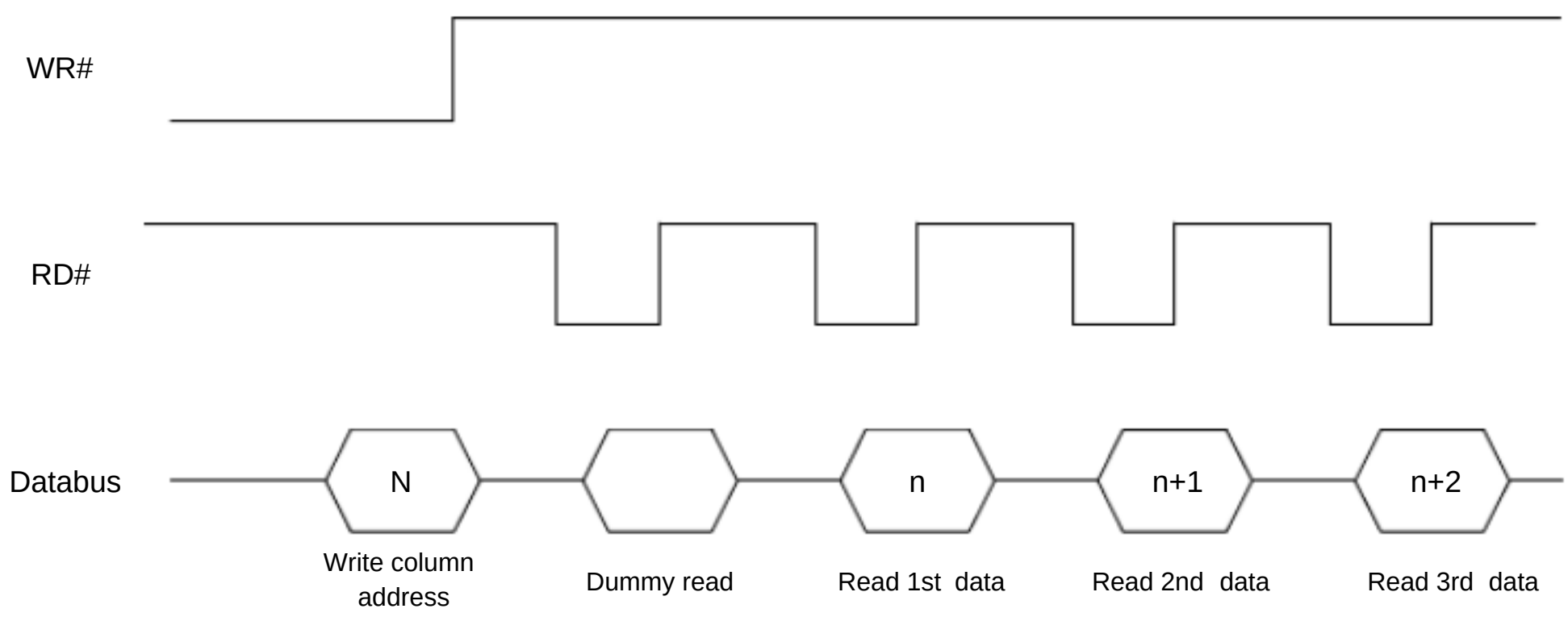
Table 8-3 : Control pins of 8080 interface

Function RD#		WR#	CS#	D/C#
Write command	H	↑	L L	
Read status	↑	H L L		
Write data	H	↑	L H	
Read data	↑	H L H		

Note
(1) ↑stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# (WR#)# can be connected to an external ground.

Table 8-4 : Control pins of 4-wire Serial interface

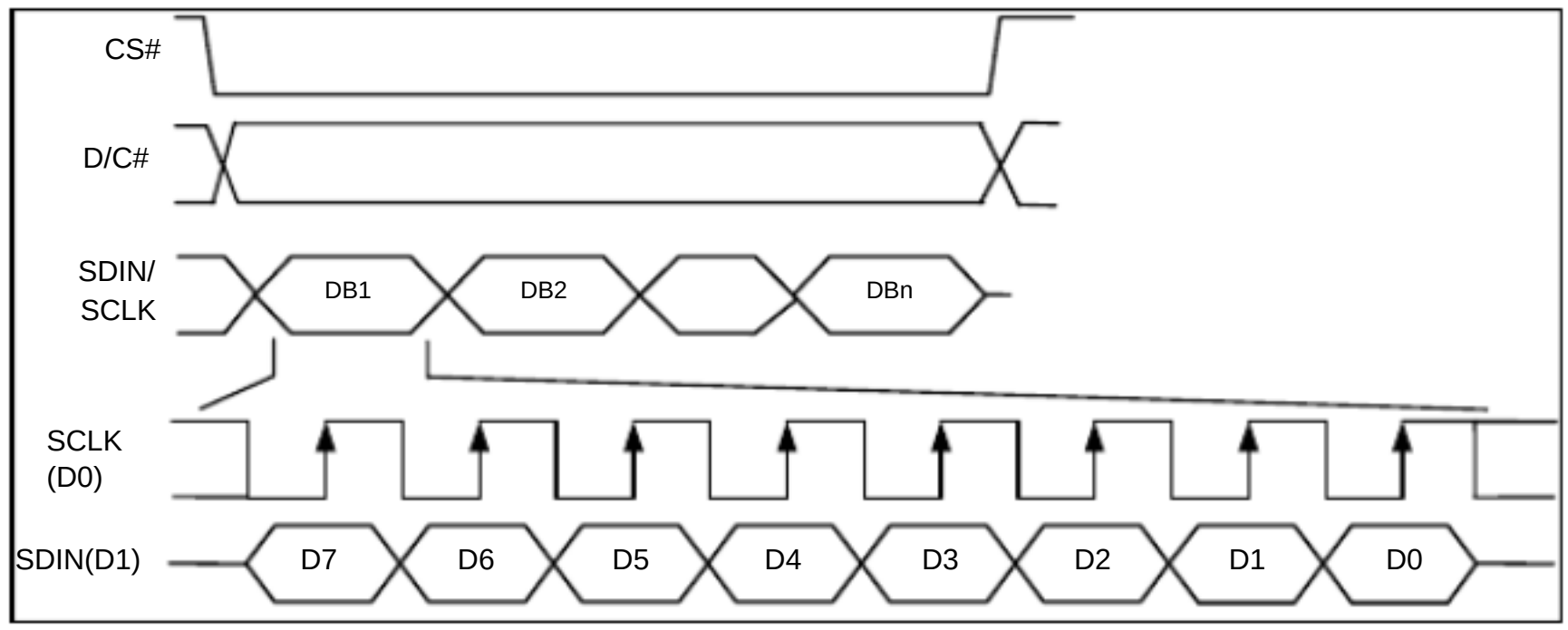
Function E(RD#)		R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

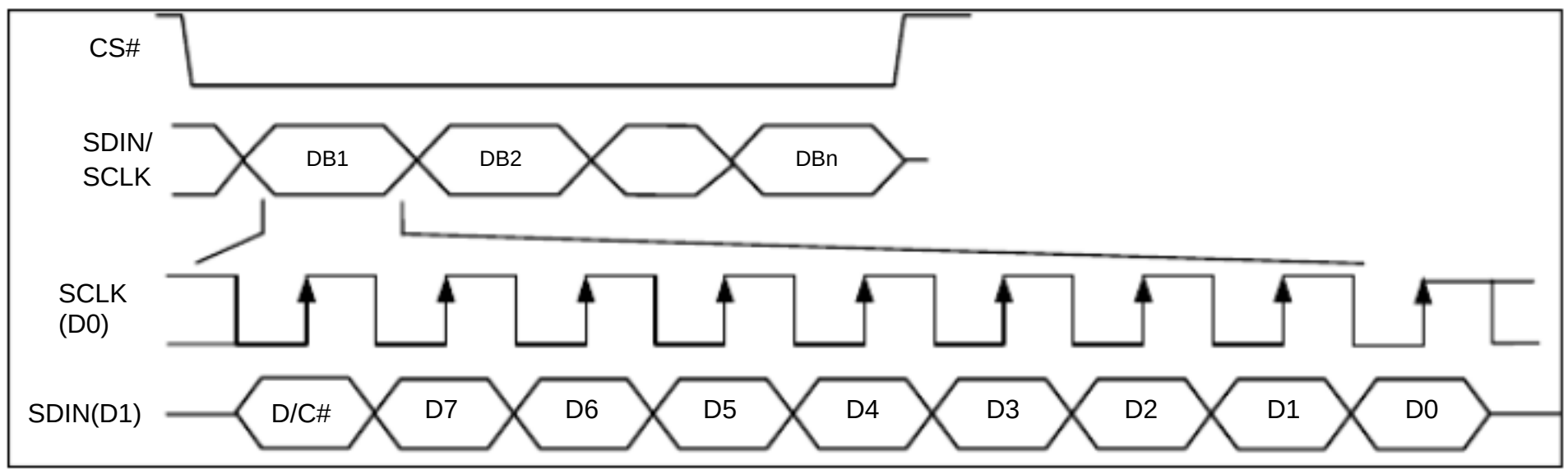
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 8-5 : Control pins of 3-wire Serial interface

Function E(RD#)		R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal

Figure 8-6 : Write procedure in 3-wire Serial interface mode



8.1.5 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA$_{OUT}$/D$_2$ for output and SDA$_{IN}$/D$_1$ for input) and I²C-bus clock signal SCL (D$_0$). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1306 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit (and the read/write select bit ("R/W#" bit) with the following byte format,

b7	b6	b5	b4	b3	b2	b1	b0
0	1	1	1	1	0	SA0	R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or " selected as the slave address of SSD1306. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.
It should be noticed that the ITO track resistance and the pulled-up resistance at " a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
"SDA$_{IN}$" and "SDA$_{OUT}$" are tied together and serve as SDA. The "SDA$_{IN}$" pin must be connected to act as SDA. The "SDA$_{OUT}$" pin may be disconnected. When "SDA$_{OUT}$" pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

8.1.5 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I²C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1306 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit (“SA0” bit) and the read/write select bit (“R/W#” bit) with the following byte format,

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	1	1	1	1	0	SA0	R/W#

“SA0” bit provides an extension bit for the slave address. Either “0111100” or “0111101”, selected as the slave address of SSD1306. D/C# pin acts as SA0 for slave address selection.
“R/W#” bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.
It should be noticed that the ITO track resistance and the pulled-up resistance at “SDA” pin be a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in “SDA”.
“SDA_{IN}” and “SDA_{OUT}” are tied together and serve as SDA. The “SDA_{IN}” pin must be connected to act as SDA. The “SDA_{OUT}” pin may be disconnected. When “SDA_{OUT}” pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

Figure 8-8 : Definition of the Start and Stop Condition

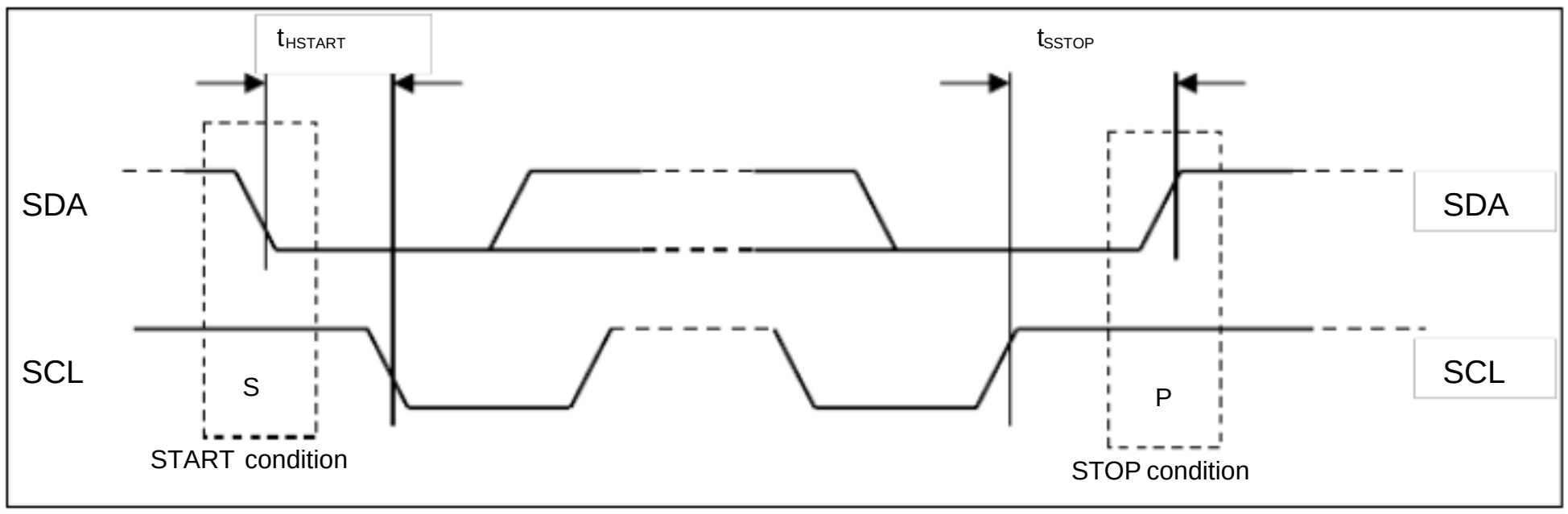
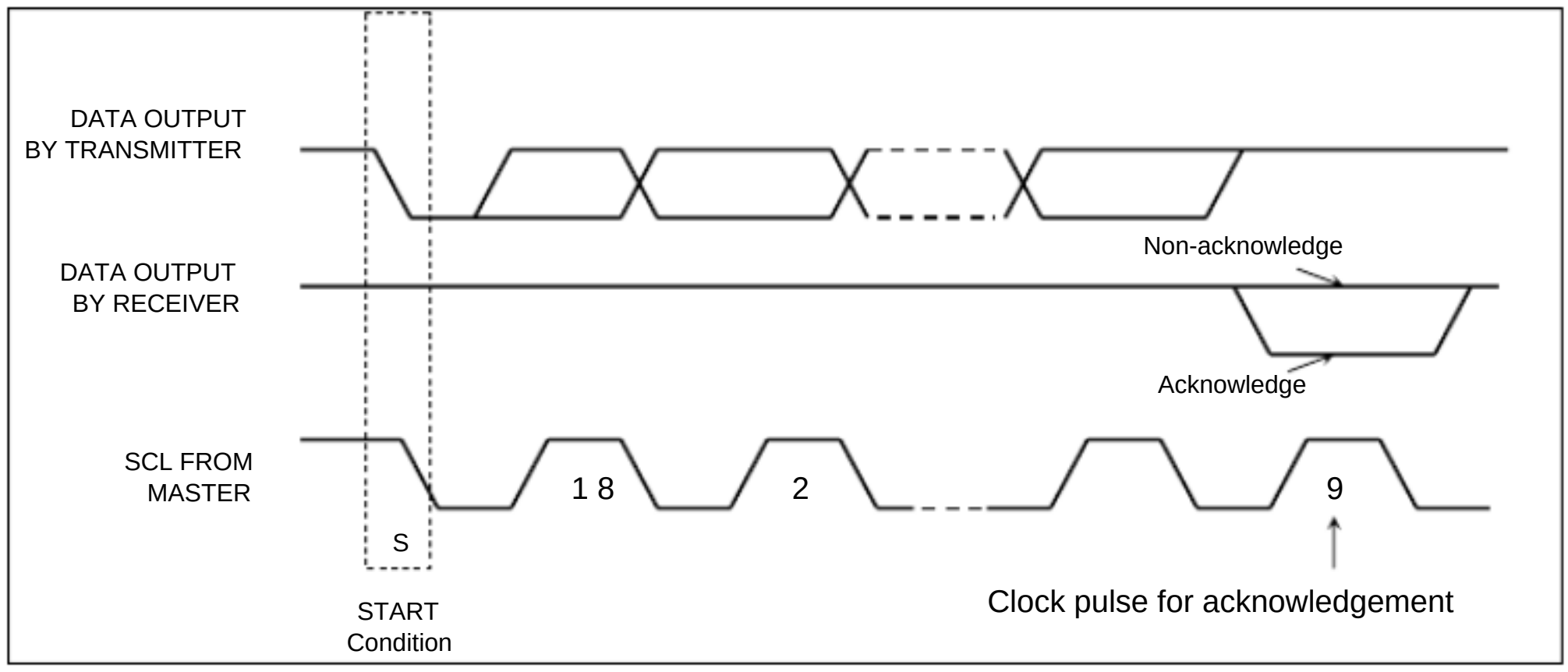


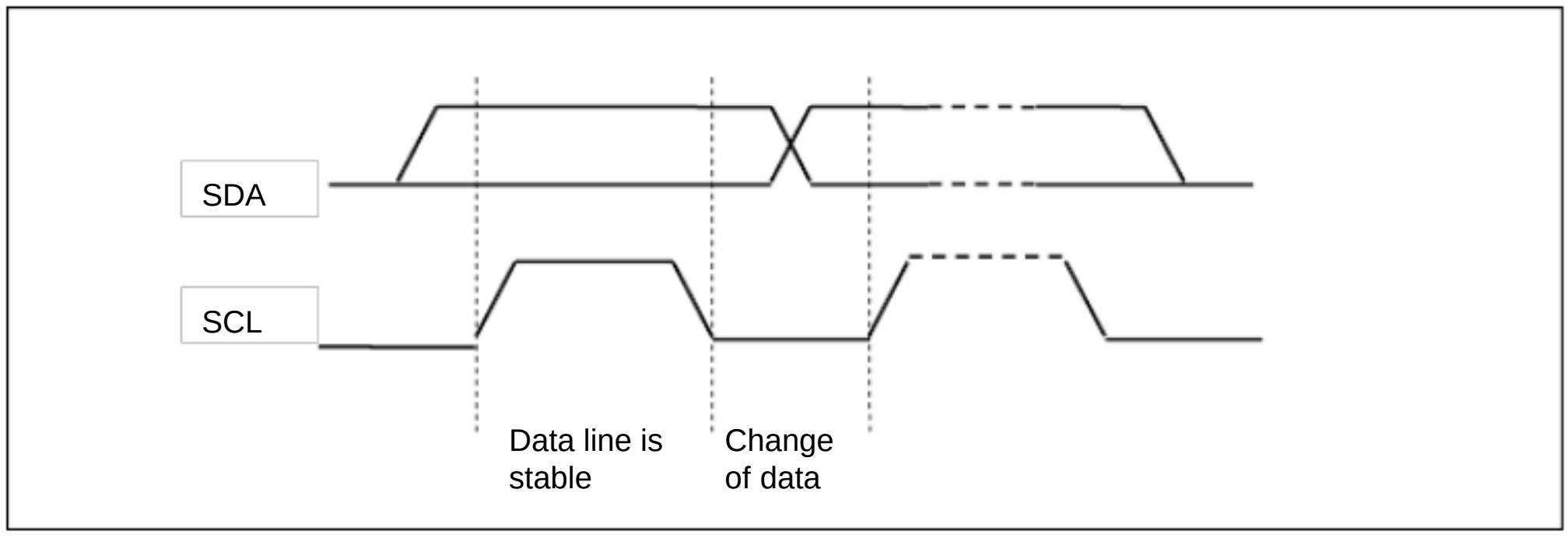
Figure 8-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the period of the clock pulse. Please refer to the Figure 8-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 8-10 : Definition of the data transfer condition



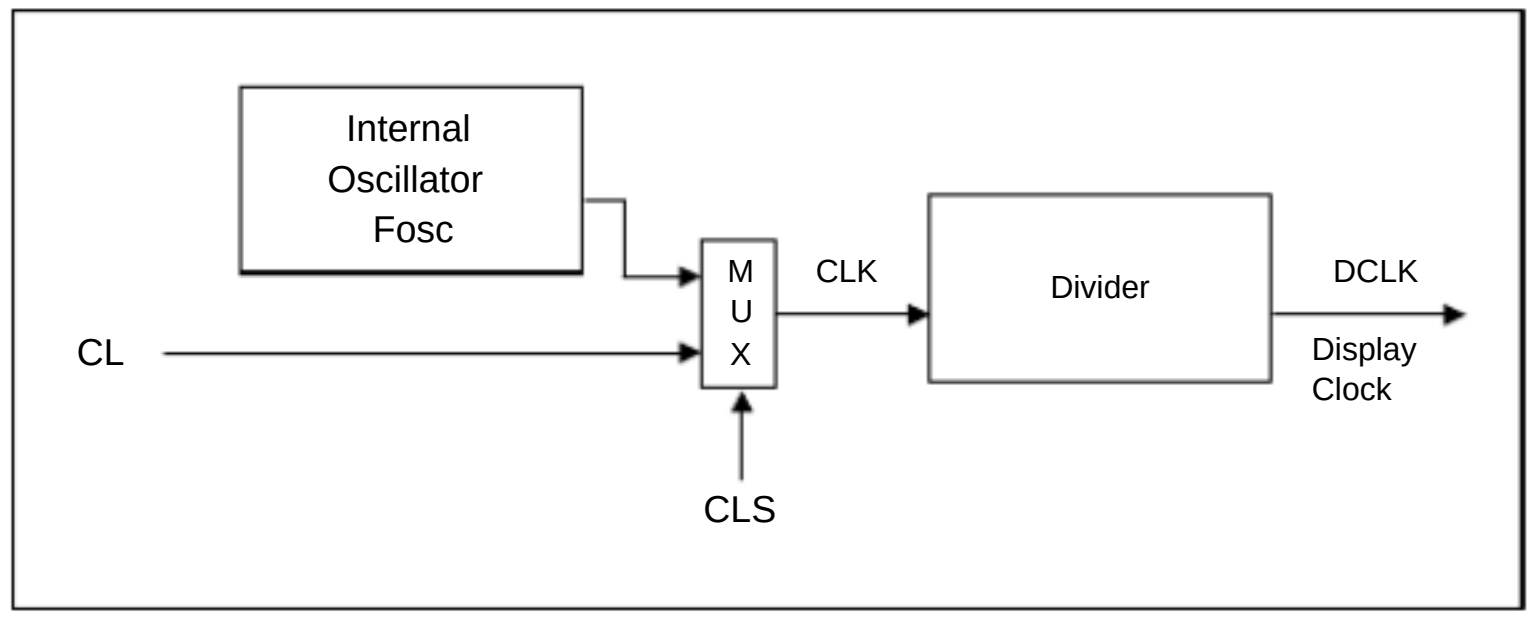
8.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM).
If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

8.3 Oscillator Circuit and Display Time Generator

Figure 8-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

? D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.

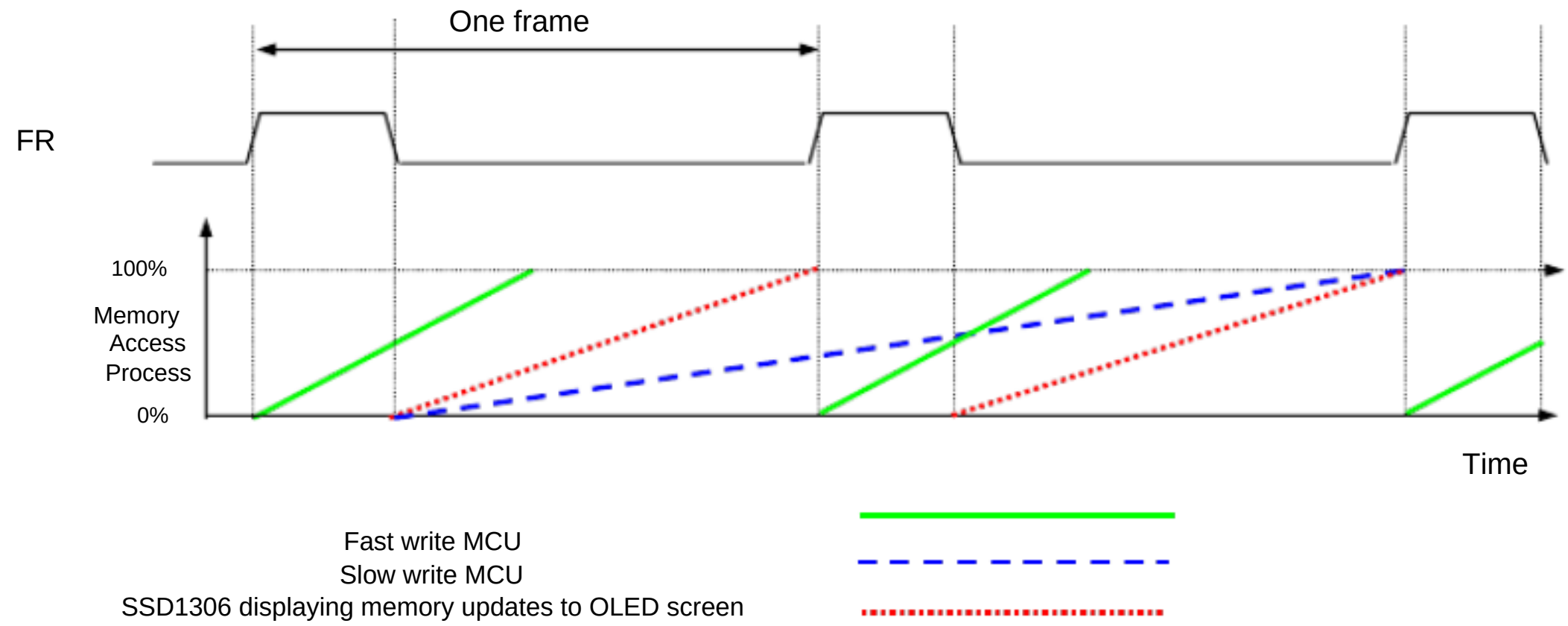
? K is the number of display clocks per row. The value is derived by
K = Phase 1 period + Phase 2 period + BANK0 pulse width
= 2 + 2 + 50 = 54 at power on reset
(Please refer to Section 8.6 “ Segment Drivers / Common Drivers ” for the details of the

? Number of multiplex ratio is set by command A8h. The power on reset value is 63 (i.e. 64MUX).

? F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

8.4 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU : MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

8.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

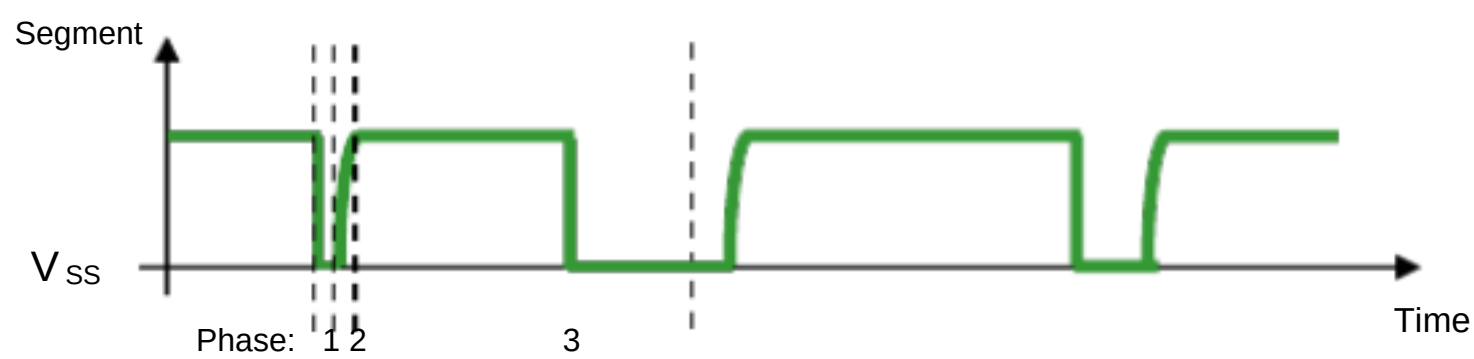
8.6 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 100uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 8-12 : Segment Output Waveform in three phases



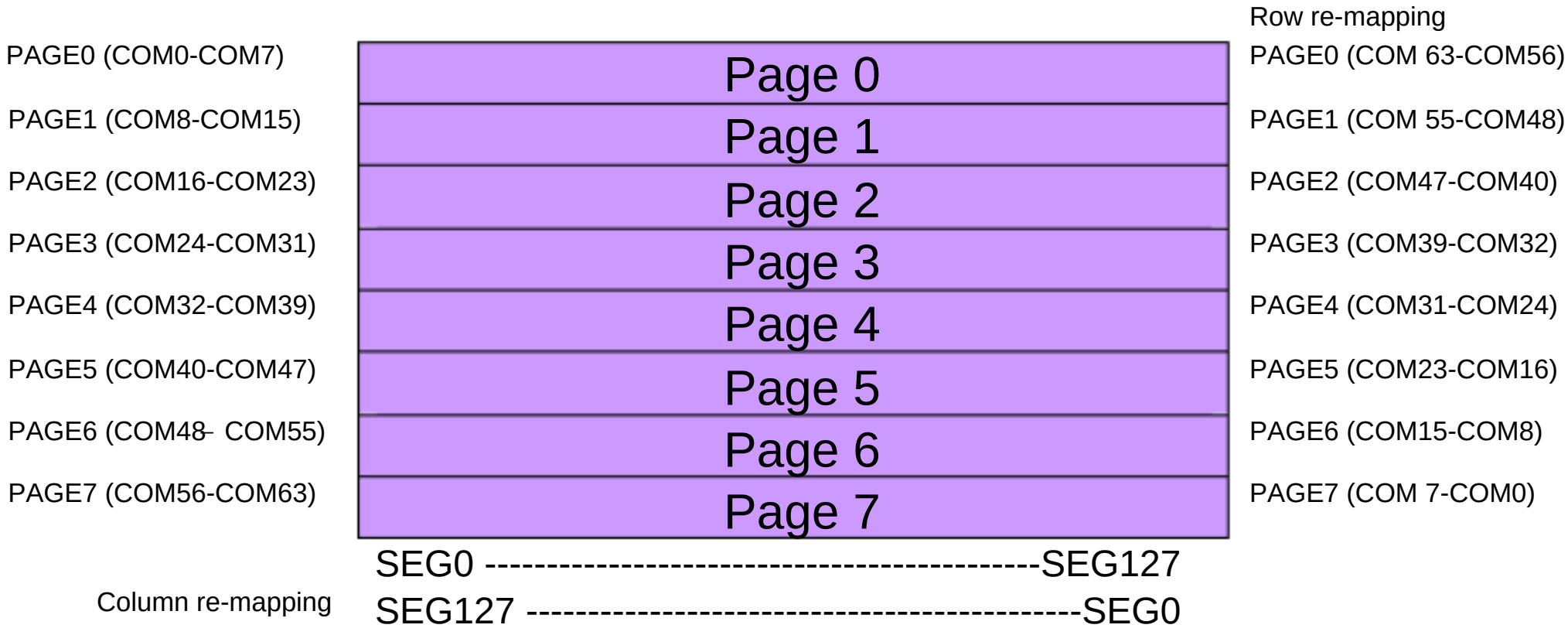
After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 50, after finishing 50 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

8.7 Graphic Display Data RAM (GDDRAM)

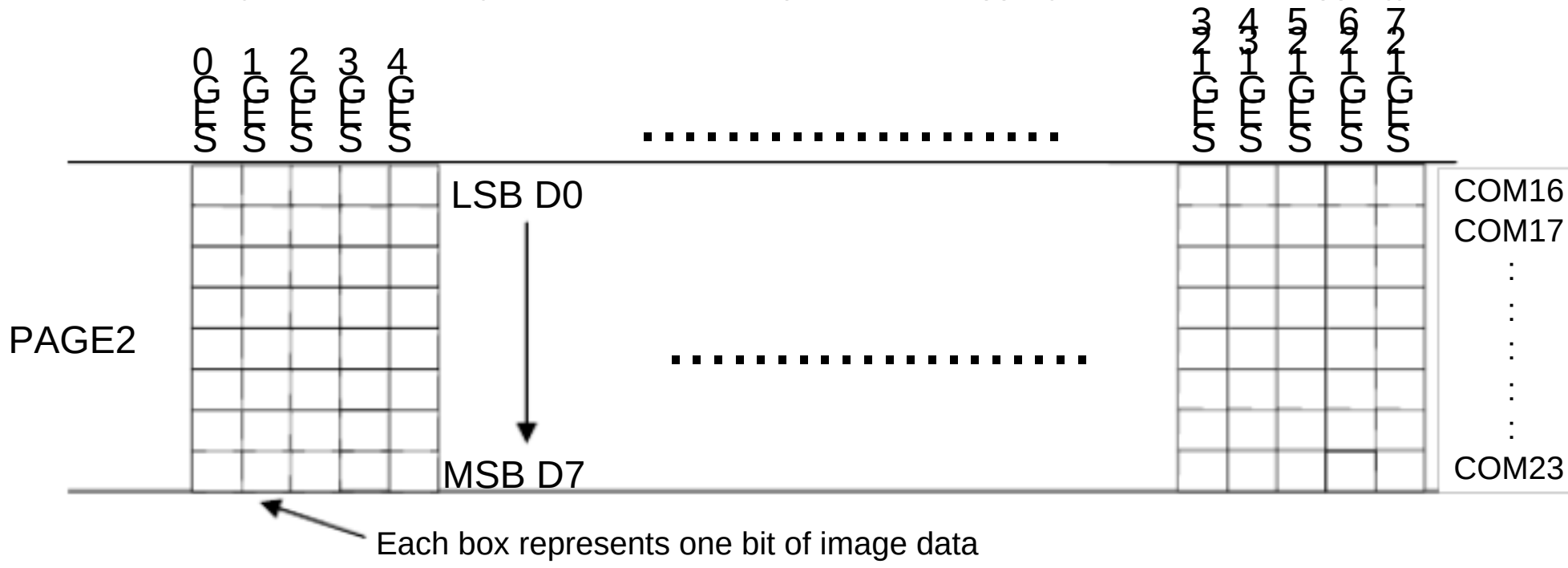
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in Figure 8-13.

Figure 8-13 : GDDRAM pages structure of SSD1306



When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 8-14.

Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 8-13.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

8.8 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- ? V_{CC} is the most positive voltage supply.
- ? V_{COMH} is the Common deselected level. It is internally regulated.
- ? V_{LSS} is the ground path of the analog and panel current.
- ? I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

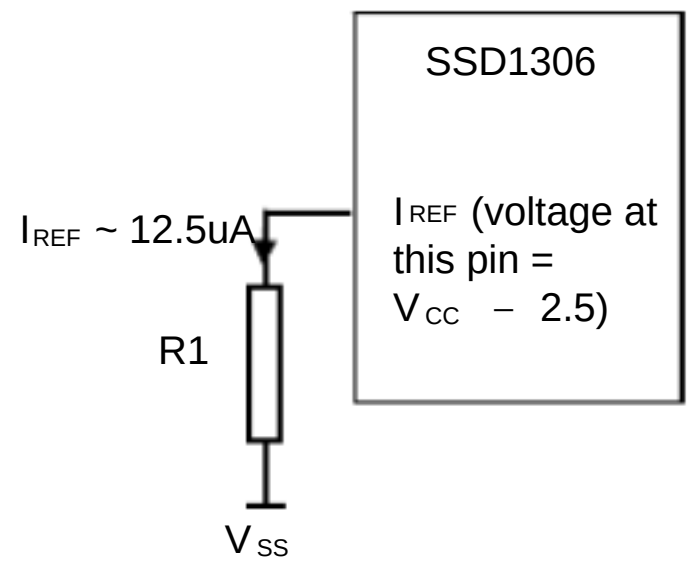
$$I_{SEG} = \text{Contrast} / 256 \times I_{REF} \times \text{scale factor}$$

in which

the contrast (0~255) is set by Set Contrast command 81h; and
the scale factor is 8 by default.

The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 8-15. It is recommended to set I_{REF} to 12.5 ± 2uA so as to achieve I_{SEG} = 100uA at maximum contrast 255.

Figure 8-15 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} − 2.5V, the value of resistor R1 can be found as below:

For I_{REF} = 12.5uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} − V_{SS}) / I_{REF}
= (12 − 2.5) / 12.5uA
= 760K Ω

8.9 Power ON and OFF sequence

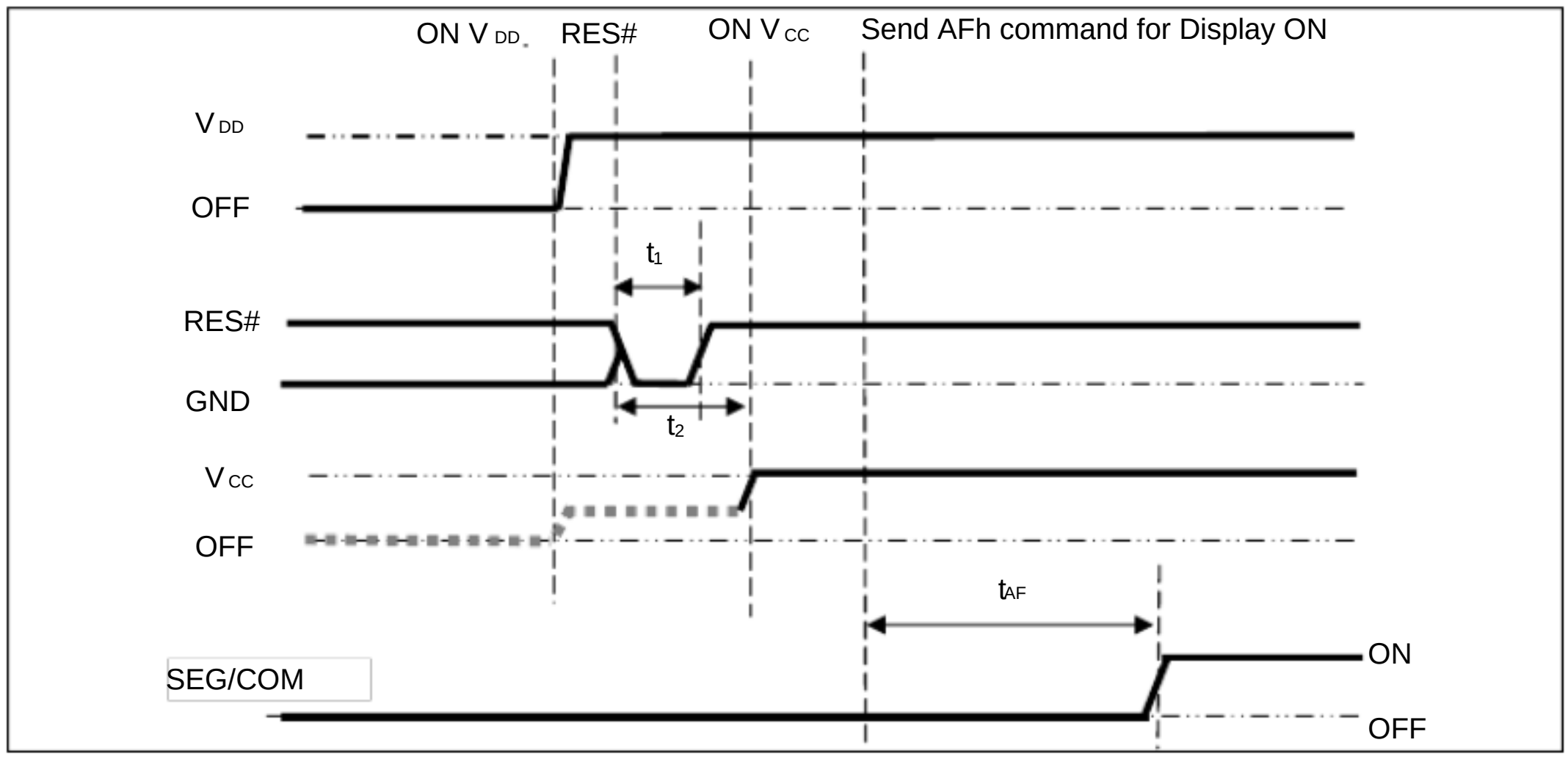
The following figures illustrate the recommended power ON and power OFF sequence of SSD1306 :

8.9.1 Power ON and OFF sequence with External V_{CC}

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. [1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

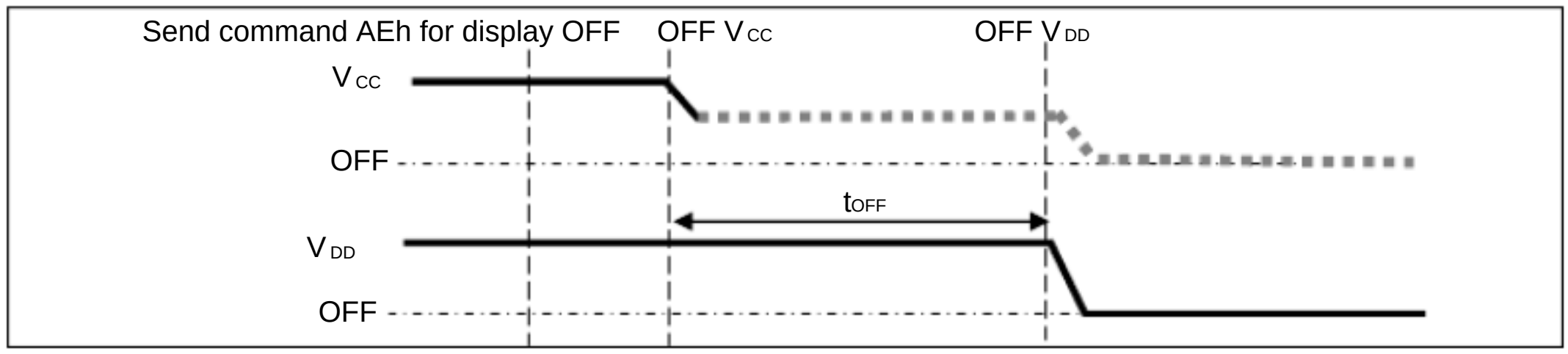
Figure 8-16 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. [1], [2], [3]
3. Power OFF V_{DD} after t_{OFF}. [5] (Typical t_{OFF}=100ms)

Figure 8-17 : The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-16 and Figure 8-17.

(2) V_{CC} should be kept float (i.e. disable) when it is OFF.

(3) Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

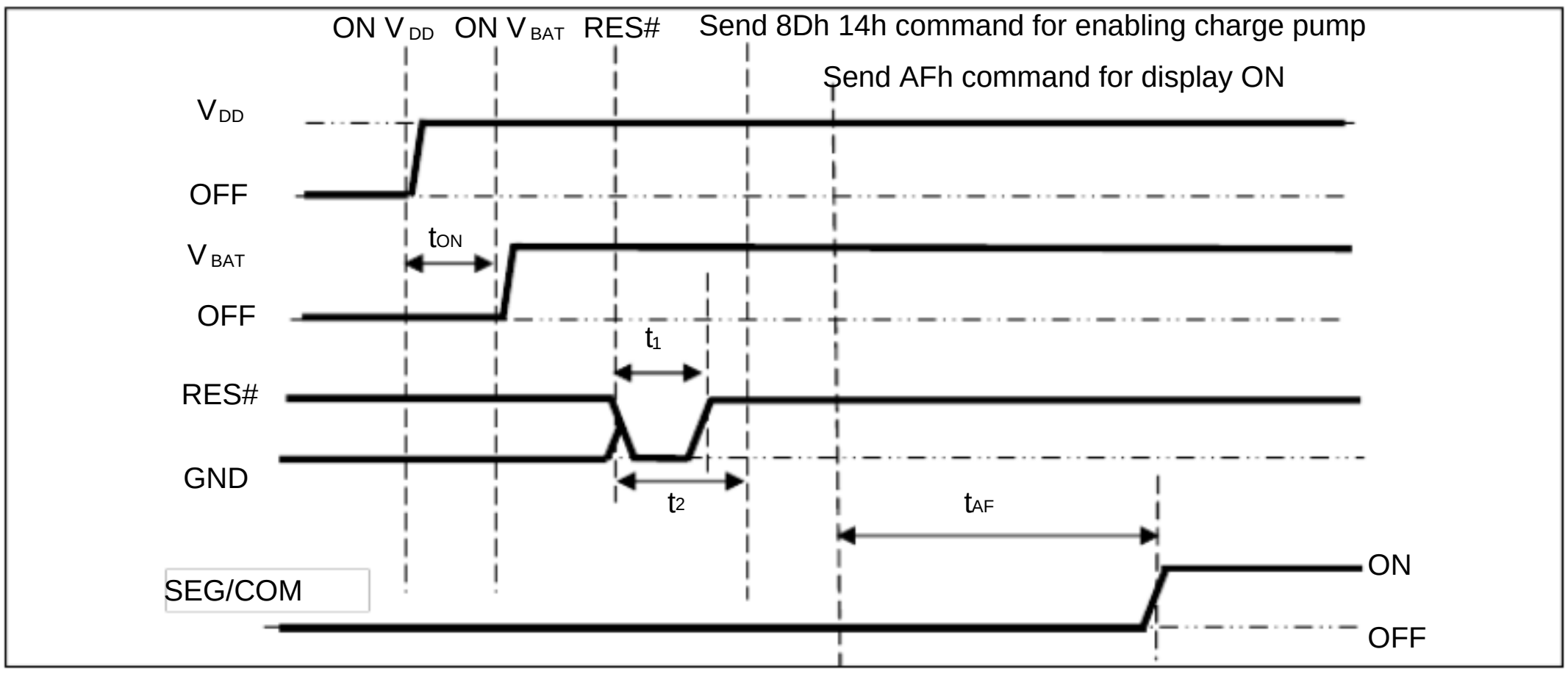
(5) V_{DD} should not be Power OFF before V_{CC} Power OFF.

8.9.2 Power ON and OFF sequence with Charge Pump Application

Power ON sequence:

1. Power ON V_{DD}
2. Wait for t_{ON}. Power ON V_{BAT}. [1], [2] (where Minimum t_{ON} = 0ms)
3. After V_{BAT} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [3] and then HIGH (logic high).
4. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then input commands with below sequence:
   a. 8Dh 14h for enabling charge pump
   b. AFh for display ON
5. SEG/COM will be ON after 100ms (t_{AF}).

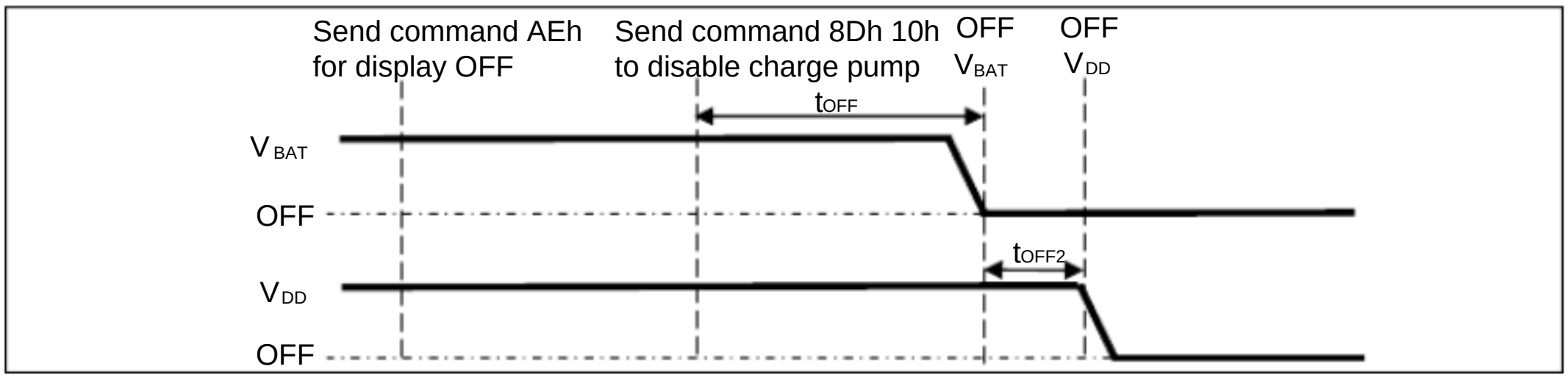
Figure 8-18 : The Power ON sequence with Charge Pump Application



Power OFF sequence:

1. Send command AEh for display OFF
2. Send command 8Dh 10h to disable charge pump
3. Power OFF V_{BAT} after t_{OFF}. . [1], [2] (Typical t_{OFF} =100ms)
4. Power OFF V_{DD} after t_{OFF2}. (where Minimum t_{OFF2} = 0ms [4] , Typical t_{OFF2}=5ms)

Figure 8-19 : The Power OFF sequence with Charge Pump Application



Note:

(1) V_{BAT} should be kept float (i.e. disable) when it is OFF.
(2) Power Pins (V_{DD} , V_{BAT}) can never be pulled to ground under any circumstance.
(3) The register values are reset after t_1.
(4) V_{DD} should not be Power OFF before V_{BAT} Power OFF

8.10 Charge Pump Regulator

The internal regulator circuit in SSD1306 accompanying only 2 external capacitors can generate a 7.5V voltage supply, V_{CC} and a maximum output loading of 6mA , from a low voltage supply input, V_{BAT} . The V_{CC} is the voltage supply to the OLED driver block. This regulator can be turned ON/OFF by software command 8Dh setting.

9 COMMAND TABLE

Table 9-1: Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

1. Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	81 A[7:0]	1	0	0	0	0	0	1	0	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0		0	1	1	X_0	Continuous Horizontal Scroll Setup 26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 011b – PAGE3 110b – PAGE6 001b – PAGE1 100b – PAGE4 111b – PAGE7 010b – PAGE2 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames 100b – 3 frames 001b – 64 frames 101b – 4 frames 010b – 128 frames 110b – 25 frame 011b – 256 frames 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 011b – PAGE3 110b – PAGE6 001b – PAGE1 100b – PAGE4 111b – PAGE7 010b – PAGE2 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0] E[7:0] : Dummy byte (Set as 00h) F[7:0] : Dummy byte (Set as FFh)
0	A[7:0]	0	0	0	0		0	0	0	0	
0	B[2:0]	*	*	*	*		*	B_2	B_1	B_0	
0	C[2:0]	*	*	*	*		*	C_2	C_1	C_0	
0	D[2:0]	*	*	*	*		*	D_2	D_1	D_0	
0	E[7:0]	0	0	0	0		0	0	0	0	
0	F[7:0]	1	1	1	1		1	1	1	1	
0	29/2A	0	0	1	0		1	0	X_1	X_0	Continuous Vertical and Horizontal Scroll Setup 29h, X_1X_0=01b : Vertical and Right Horizontal Scroll 2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte B[2:0] : Define start page address 000b – PAGE0 011b – PAGE3 110b – PAGE6 001b – PAGE1 100b – PAGE4 111b – PAGE7 010b – PAGE2 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames 100b – 3 frames 001b – 64 frames 101b – 4 frames 010b – 128 frames 110b – 25 frame 011b – 256 frames 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 011b – PAGE3 110b – PAGE6 001b – PAGE1 100b – PAGE4 111b – PAGE7 010b – PAGE2 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0] E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0] =3Fh refer to offset =63 rows Note (1) No continuous vertical scrolling is available.
0	A[2:0]	0	0	0	0		0	0	0	0	
0	B[2:0]	*	*	*	*		*	B_2	B_1	B_0	
0	C[2:0]	*	*	*	*		*	C_2	C_1	C_0	
0	D[2:0]	*	*	*	*		*	D_2	D_1	D_0	
0	E[5:0]		*	*	E_5	E_4	E_3	E_2	E_1	E_0	

2. Scrolling Command Table											
D/C#	Hex	D7	D6	D5	D4	D3 D2	D1 D0	Command			Description
0	2E	0 0	1 0			1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. Note (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0 0	1 0			1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if “26h; 2Ah; 2Fh.” commands a issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0 0 A[5:0] 0 B[6:0]	A3	1 0 * *	1 0 * B_6	A_5 B_5	A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). [RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] Note (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line ($X_5X_4X_3X_2X_1X_0$ of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls

3. Addressing Setting Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0 0	0 0			X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note (1) This command is only for page addressing mode

3. Addressing Setting Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	10~1F	0	0	0	1			X_3	X_2 X_1 X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *		A_1 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	1 A_2 B_2	A_1 B_1	A_0 B_0	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0]: Column end address, range : 0-127d, (RESET =127d) Note (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	1 A_2 B_2	0 A_1 B_1	A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) Note (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0			X_2 X_1 X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. Note (1) This command is only for page addressing mode

4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	40~7F	0	1		X_5	X_4	X_3	X_2	X_1 X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X 0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 0	A8 A[5:0]	1 *	0 *	1	0	1	0 A_5	0 A_4	0 A_3 A_2 A_1 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.

4. Hardware Configuration (Panel resolution & layout related) Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0				Command	Description
0	C0/C8	1	1	0	0			X_3	0		0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N − 1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0	D3	1	1	0	1	0	0	1				1	Set Display Offset	Set vertical shift by COM from 0d~63d
0	A[5:0]	*	*		A_5	A_4	A_3	A_2	A_1			A_0		The value is reset to 00h after RESET.
0	DA	1	1	0	1	1	0	1				0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap
0	A[5:4]	0	0		A_5	A_4	0	0	1			0		

5. Timing & Driving Scheme Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command			Description
0	D5	1	1	0	1	0	1	0	1				Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.
0	A[7:0]	A_7		A_6	A_5	A_4	A_3	A_2	A_1	A_0			
0	D9	1	1	0	1	1	0	0	1				Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0	A[7:0]	A_7		A_6	A_5	A_4	A_3	A_2	A_1	A_0			
0	DB	1	1	0	1	1	0	1	1				Set V_{COMH} Deselect Level	A[6:4] / Hex code / V_{COMH} deselect level
0	A[6:4]	0		A_6	A_5	A_4	0	0	0	0				000b 00h ~ 0.65 x V_{CC} 010b 20h ~ 0.77 x V_{CC} (RESET) 011b 30h ~ 0.83 x V_{CC}
0	E3	1	1	1	0	0	0	1	1				NOP	Command for no operation

6. Advance Graphic Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	23	0	1			0	0	1	1	Set Fade Out and Blinking	A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET] A[5:4] = 10b Enable Fade Out mode. Once Fade Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled. A[5:4] = 11b Enable Blinking mode. Once Blinking Mode is enabled, contrast decrease gradually to all pixels OFF and than contrast increase gradually to normal display. This process loop continuously until the Blinking mode is disabled. A[3:0] : Set time interval for each fade step A[3:0] = 0000b: 8 Frames; 0001b: 16 Frames; 0010b: 24 Frames; : ; 1111b: 128 Frames Note (1) Refer to section 10.3.1 for details.
0	A[6:0]	*	*	A5	A4	A3	A2	A1	A0		
0	D6	1	0			0	1	1	0	Set Zoom In	A[0] = 0b Disable Zoom in Mode[RESET] A[0] = 1b Enable Zoom in Mode Note (1) The panel must be in alternative COM pin configuration (command DAh A[4] =1) (2) Refer to section 10.3.2 for details.
0	A[0]	0	0			0	0	0	A0		

7. Charge Pump Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	8D	1	0	0			1	1	0	1	Charge Pump Setting	A[2] = 0b, Disable charge pump(RESET) A[2] = 1b, Enable charge pump during display on Note (1) The Charge Pump must be enabled by the following command sequence: 8Dh ; Charge Pump Setting 14h ; Enable Charge Pump AFh; Display ON
0	A[7:0]	*	*	0			0	A_2	0	0		

Note
(1) “ * ” stands for “ Don’t care ”.

Table 9-2 : Read Command Table

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : Reserved D[6] : “1” for display OFF / “0” for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

Note
(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

9.1 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.
In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.
Also, a dummy read is required before the first data read.
To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 9-3 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

10 COMMAND DESCRIPTIONS

10.1 Fundamental Command

10.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Section Table 9-1 and Section 10.1.3 for details.

10.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~1Fh)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Section Table 9-1 and Section 10.1.3 for details.

10.1.3 Set Memory Addressing Mode (20h)

There are 3 different memory addressing mode in SSD1306: page addressing mode, horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above three modes. In there, “COL” means the graphic display data RAM column.

Page addressing mode (A[1:0]=10xb)

In page addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 10-1.

Figure 10-1 : Address Pointer Movement of Page addressing mode

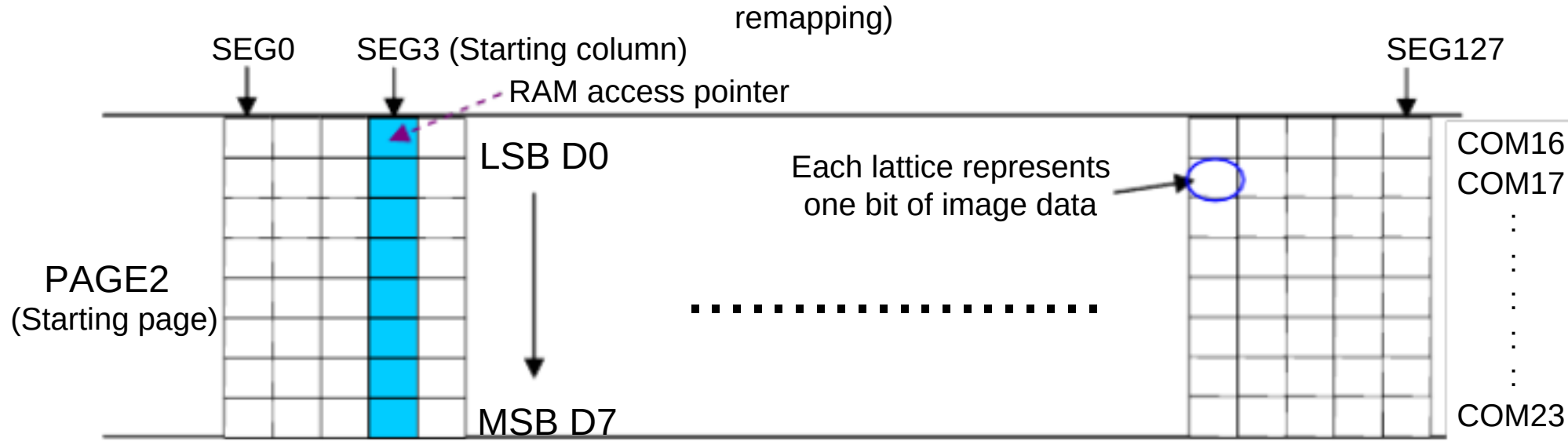
	COL0	COL 1	⋯..	COL 126	COL 127
PAGE0	→	→	→	→	→
PAGE1	→	→	→	→	→
:	: : : : :				
PAGE6	→	→	→	→	→
PAGE7	→	→	→	→	→

In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to B7h.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the upper start column address of pointer by command 10h~1Fh.

For example, if the page address is set to B2h, lower column address is 03h and upper column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 10-2. The input data byte will be written into RAM position of column 3.

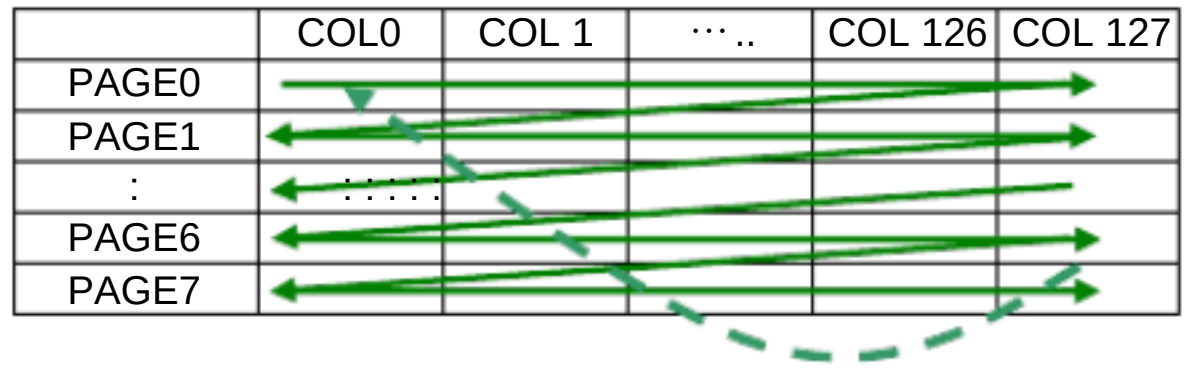
Figure 10-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



Horizontal addressing mode (A[1:0]=00b)

In horizontal addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 10-3. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-3.)

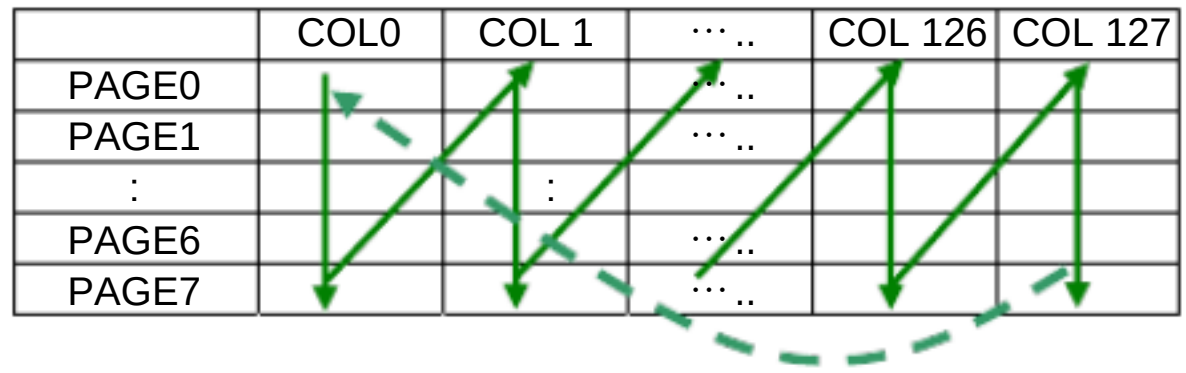
Figure 10-3 : Address Pointer Movement of Horizontal addressing mode



Vertical addressing mode: (A[1:0]=01b)

In vertical addressing mode, after the display RAM is read/written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 10-4. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-4.)

Figure 10-4 : Address Pointer Movement of Vertical addressing mode



In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

- Set the column start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 10-5.

10.1.4 Set Column Address (21h)

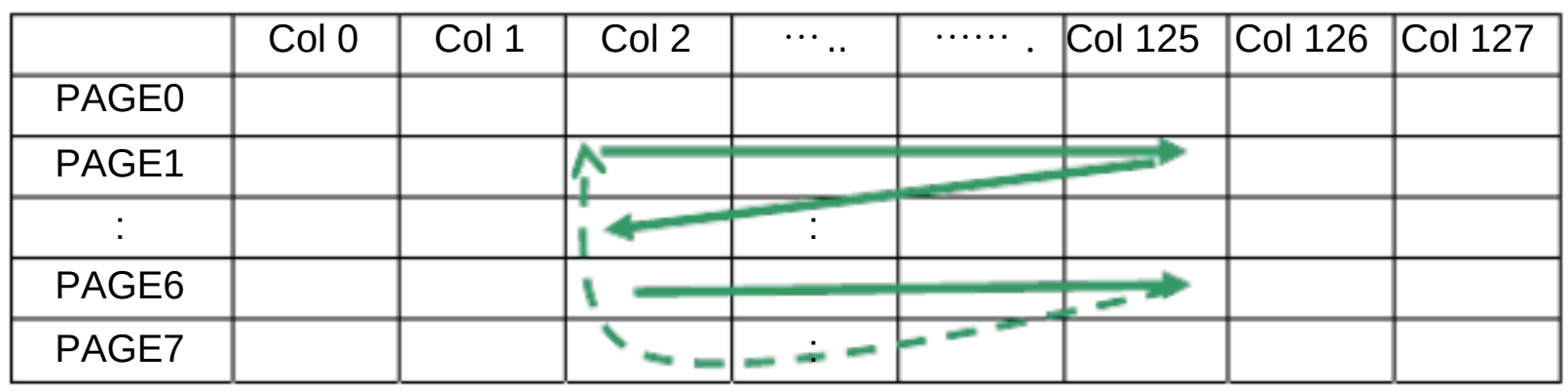
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command 20h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If vertical address increment mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of column and page address pointer movement through the example: column start address is set to 2 and column end address is set to 125, page start address is set to 1 and page end address is set to 6; Horizontal address increment mode is enabled by command 20h. In this case, the graphic display data RAM column accessible range is from column 2 to column 125 and from page 1 to page 6 only. In addition, the column address pointer is set to 2 and page address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (solid line in Figure 10-5). Whenever the column address pointer finishes accessing the end column 125, it is reset back to column 2 and page address is automatically increased by 1 (solid line in Figure 10-5). While the end page 6 and end column 125 RAM location is accessed, the page address is reset back to 1 and the column address is reset back to 2 (dotted line in Figure 10-5). .

Figure 10-5 : Example of Column and Row Address Pointer Movement



10.1.6 Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on.

Refer to Table 10-1 for more illustrations.

10.1.7 Set Contrast Control for BANK0 (81h)

This command sets the Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases as the contrast step value increases.

10.1.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 9-1.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

10.1.9 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.
If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents.
In other words, A4h command resumes the display from entire display "ON" stage.
A5h command forces the entire display to be "ON", regardless of the contents of the display data RAM.

10.1.10 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an "ON" pixel while in inverse display a RAM data of 0 indicates an "ON" pixel.

10.1.11 Set Multiplex Ratio (A8h)

This command switches the default 63 multiplex mode to any multiplex ratio, ranging from 16 to 63. The output pads COM0~COM63 will be switched to the corresponding COM signal.

10.1.12 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

Figure 10-6 :Transition between different modes

10.1.13 Set Page Start Address for Page Addressing Mode (B0h~B7h)

This command positions the page start address from 0 to 7 in GDDRAM under Page Addressing Mode. Please refer to Table 9-1 and Section 10.1.3 for details.

10.1.14 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately. Please refer to Table 10-3 for details.

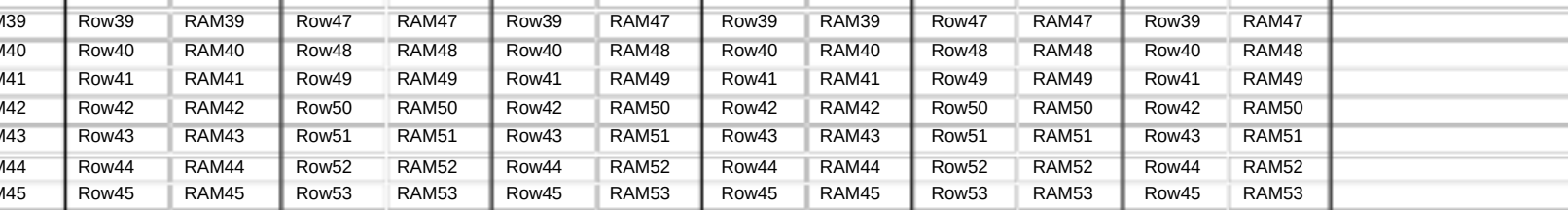
10.1.15 Set Display Offset (D3h)

This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM63 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM16 towards the COM0 direction by 16 lines the 6-bit data in the second byte should be given as 010000b. To move in the opposite direction by 16 lines the 6-bit data should be given by 64 − 16, so the second byte would be 100000b. The following two tables (Table 10-1, Table 10-2) show the example of setting the command C0h/C8h and D3h.

Table 10-1 : Example of Set Display Offset and Display Start Line with no Remap

	Output												
	64		64		64		56		56		56		Set MUX ratio(A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / Remapped (C0h / C8h)
Hardware	0		8		0		0		8		0		Display offset (D3h)
pin name	0		0		8		0		0		8		Display start line (40h - 7Fh)
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10	
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11	
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15	
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19	
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23	
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27	
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31	
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35	
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38	
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39	
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	Row40	RAM40	Row32	RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	Row41	RAM41	Row33	RAM41	
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	Row42	RAM42	Row34	RAM42	
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	Row43	RAM43	Row35	RAM43	
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	Row44	RAM44	Row36	RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	Row45	RAM45	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	Row46	RAM46	Row38	RAM46	
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	Row47	RAM47	Row39	RAM47	
COM40	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row40	RAM40	Row48	RAM48	Row40	RAM48	
COM41	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row41	RAM41	Row49	RAM49	Row41	RAM49	
COM42	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row42	RAM42	Row50	RAM50	Row42	RAM50	
COM43	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row43	RAM43	Row51	RAM51	Row43	RAM51	
COM44	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row44	RAM44	Row52	RAM52	Row44	RAM52	
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row45	RAM45	Row53	RAM53	Row45	RAM53	
COM46	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row46	RAM46	Row54	RAM54	Row46	RAM54	
COM47	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row47	RAM47	Row55	RAM55	Row47	RAM55	
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row48	RAM48	-	-	Row48	RAM56	
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row49	RAM49	-	-	Row49	RAM57	
COM50	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row50	RAM50	-	-	Row50	RAM58	
COM51	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row51	RAM51	-	-	Row51	RAM59	
COM52	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row52	RAM52	-	-	Row52	RAM60	
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row53	RAM53	-	-	Row53	RAM61	
COM54	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row54	RAM54	-	-	Row54	RAM62	
COM55	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row55	RAM55	-	-	Row55	RAM63	
COM56	Row56	RAM56	Row0	RAM0	Row56	RAM0	-	-	Row0	RAM0	-	-	
COM57	Row57	RAM57	Row1	RAM1	Row57	RAM1	-	-	Row1	RAM1	-	-	
COM58	Row58	RAM58	Row2	RAM2	Row58	RAM2	-	-	Row2	RAM2	-	-	
COM59	Row59	RAM59	Row3	RAM3	Row59	RAM3	-	-	Row3	RAM3	-	-	
COM60	Row60	RAM60	Row4	RAM4	Row60	RAM4	-	-	Row4	RAM4	-	-	
COM61	Row61	RAM61	Row5	RAM5	Row61	RAM5	-	-	Row5	RAM5	-	-	
COM62	Row62	RAM62	Row6	RAM6	Row62	RAM6	-	-	Row6	RAM6	-	-	
COM63	Row63	RAM63	Row7	RAM7	Row63	RAM7	-	-	Row7	RAM7	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		

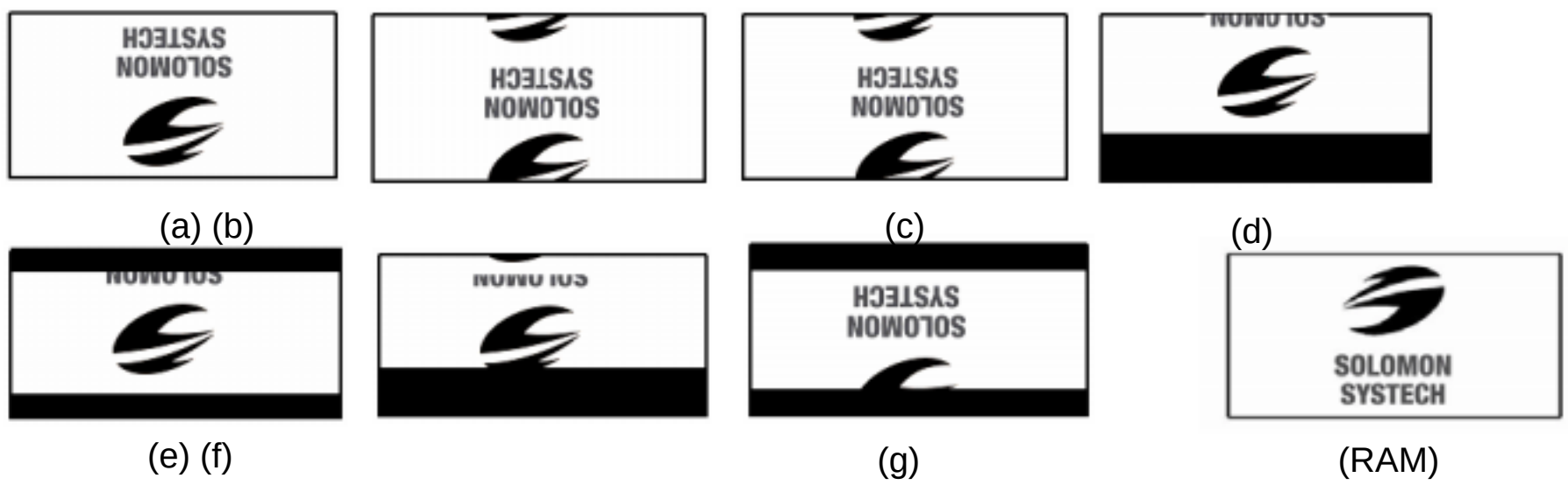


(a) (b) (c) (d)

(e) (f) (RAM)

Table 10-2 :Example of Set Display Offset and Display Start Line with Remap

Hardware pin name	Output														Set MUX ratio(A8h)
	64		64		64		48		48		48		48		Set MUX ratio(A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM Normal / Remapped (C0h / C8h)
	0		8		0		0		8		0		8		Display offset (D3h)
	0		0		8		0		0		8		16		Display start line (40h - 7Fh)
~~COM0~~	~~Row63~~	~~RAM63~~	~~Row7~~	~~RAM7~~	~~Row63~~	~~RAM7~~	~~Row47~~	~~RAM47~~			~~Row47~~	~~RAM55~~			
COM1	Row62	RAM62	Row6	RAM6	Row62	RAM6	Row46	RAM46	-	-	Row46	RAM54	-	-	
COM2	Row61	RAM61	Row5	RAM5	Row61	RAM5	Row45	RAM45	-	-	Row45	RAM53	-	-	
COM3	Row60	RAM60	Row4	RAM4	Row60	RAM4	Row44	RAM44	-	-	Row44	RAM52	-	-	
COM4	Row59	RAM59	Row3	RAM3	Row59	RAM3	Row43	RAM43	-	-	Row43	RAM51	-	-	
COM5	Row58	RAM58	Row2	RAM2	Row58	RAM2	Row42	RAM42	-	-	Row42	RAM50	-	-	
COM6	Row57	RAM57	Row1	RAM1	Row57	RAM1	Row41	RAM41	-	-	Row41	RAM49	-	-	
COM7	Row56	RAM56	Row0	RAM0	Row56	RAM0	Row40	RAM40	-	-	Row40	RAM48	-	-	
COM8	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row47	RAM63	
COM9	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row46	RAM62	
COM10	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row45	RAM61	
COM11	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row44	RAM60	
COM12	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row43	RAM59	
COM13	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row42	RAM58	
COM14	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row41	RAM57	
COM15	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row40	RAM56	
COM16	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row39	RAM55	
COM17	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row38	RAM54	
COM18	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row37	RAM53	
COM19	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row36	RAM52	
COM20	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row35	RAM51	
COM21	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row34	RAM50	
COM22	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row33	RAM49	
COM23	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row32	RAM48	
COM24	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row31	RAM47	
COM25	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row30	RAM46	
COM26	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row29	RAM45	
COM27	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row28	RAM44	
COM28	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row27	RAM43	
COM29	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row26	RAM42	
COM30	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row25	RAM41	
COM31	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row24	RAM40	
COM32	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row23	RAM39	
COM33	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row22	RAM38	
COM34	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row21	RAM37	
COM35	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row20	RAM36	
COM36	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row19	RAM35	
COM37	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row18	RAM34	
COM38	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row17	RAM33	
COM39	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row16	RAM32	
COM40	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row15	RAM31	
COM41	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row14	RAM30	
COM42	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row13	RAM29	
COM43	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row12	RAM28	
COM44	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row11	RAM27	
COM45	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row10	RAM26	
COM46	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row9	RAM25	
COM47	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row8	RAM24	
COM48	Row15	RAM15	Row23	RAM23	Row15	RAM23	-	-	Row7	RAM7	-	-	Row7	RAM23	
COM49	Row14	RAM14	Row22	RAM22	Row14	RAM22	-	-	Row6	RAM6	-	-	Row6	RAM22	
COM50	Row13	RAM13	Row21	RAM21	Row13	RAM21	-	-	Row5	RAM5	-	-	Row5	RAM21	
COM51	Row12	RAM12	Row20	RAM20	Row12	RAM20	-	-	Row4	RAM4	-	-	Row4	RAM20	
COM52	Row11	RAM11	Row19	RAM19	Row11	RAM19	-	-	Row3	RAM3	-	-	Row3	RAM19	
COM53	Row10	RAM10	Row18	RAM18	Row10	RAM18	-	-	Row2	RAM2	-	-	Row2	RAM18	
COM54	Row9	RAM9	Row17	RAM17	Row9	RAM17	-	-	Row1	RAM1	-	-	Row1	RAM17	
COM55	Row8	RAM8	Row16	RAM16	Row8	RAM16	-	-	Row0	RAM0	-	-	Row0	RAM16	
COM56	Row7	RAM7	Row15	RAM15	Row7	RAM15	-	-	-	-	-	-	-	-	
COM57	Row6	RAM6	Row14	RAM14	Row6	RAM14	-	-	-	-	-	-	-	-	
COM58	Row5	RAM5	Row13	RAM13	Row5	RAM13	-	-	-	-	-	-	-	-	
COM59	Row4	RAM4	Row12	RAM12	Row4	RAM12	-	-	-	-	-	-	-	-	
COM60	Row3	RAM3	Row11	RAM11	Row3	RAM11	-	-	-	-	-	-	-	-	
COM61	Row2	RAM2	Row10	RAM10	Row2	RAM10	-	-	-	-	-	-	-	-	
COM62	Row1	RAM1	Row9	RAM9	Row1	RAM9	-	-	-	-	-	-	-	-	
COM63	Row0	RAM0	Row8	RAM8	Row0	RAM8	-	-	-	-	-	-	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		(g)		



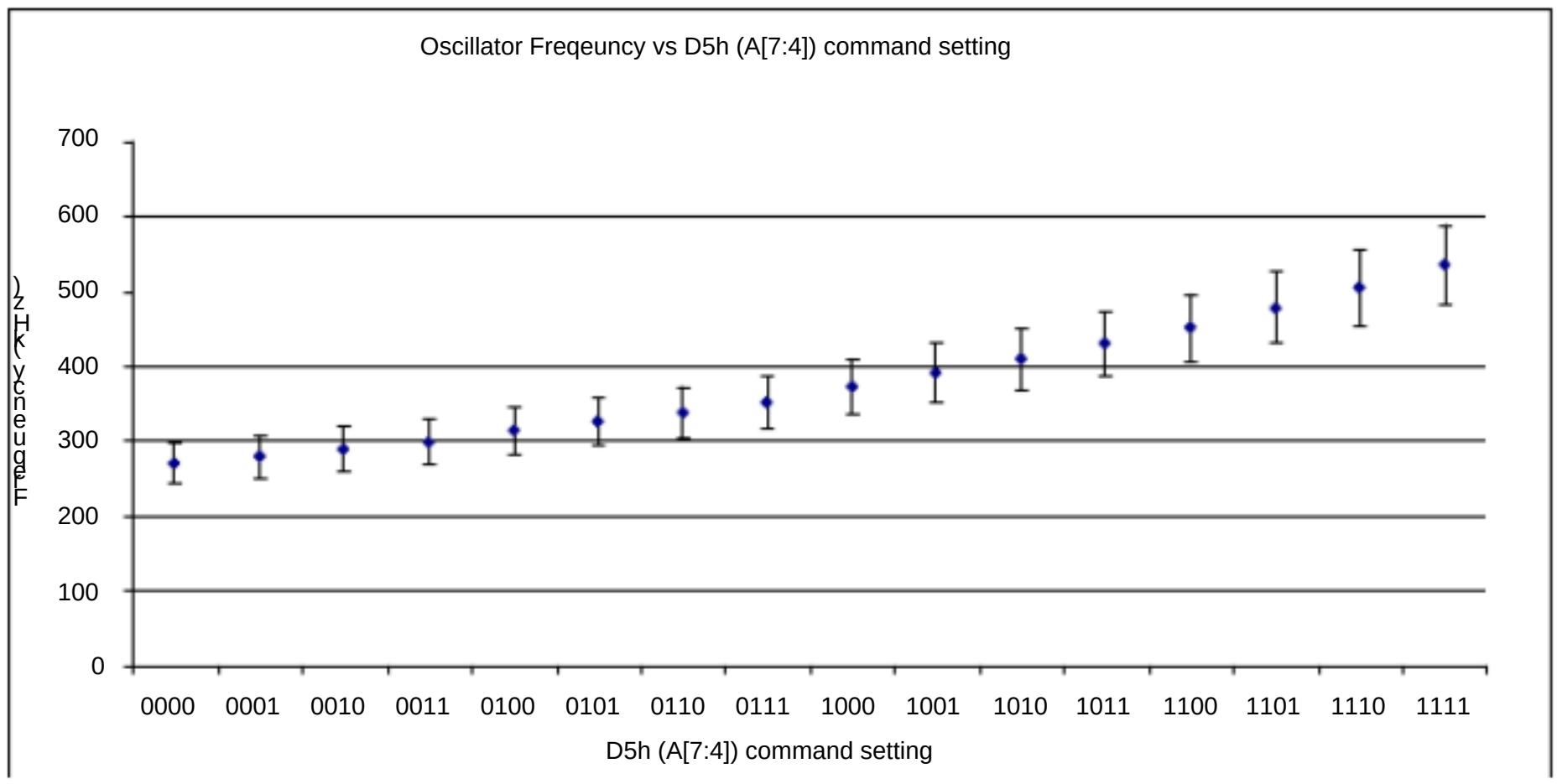
10.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D)(A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to section 8.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1000b.

Figure 10-7 : Oscillator frequency setting



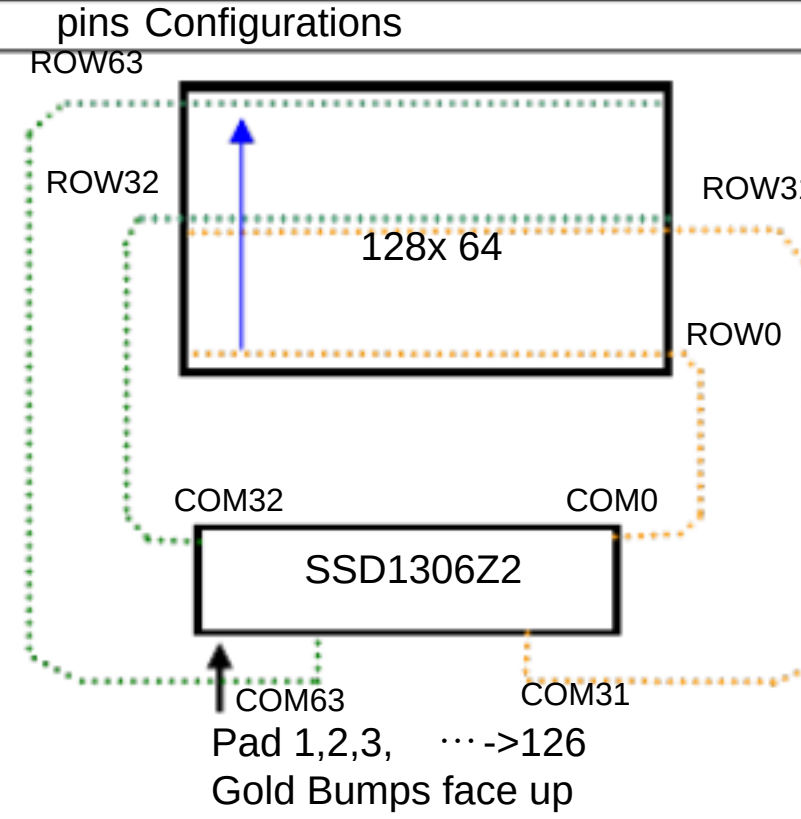
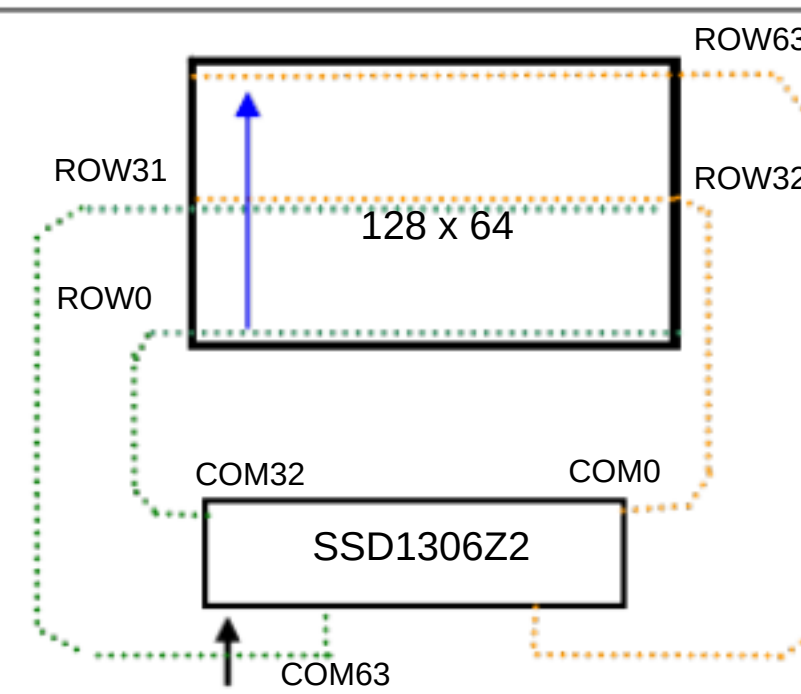
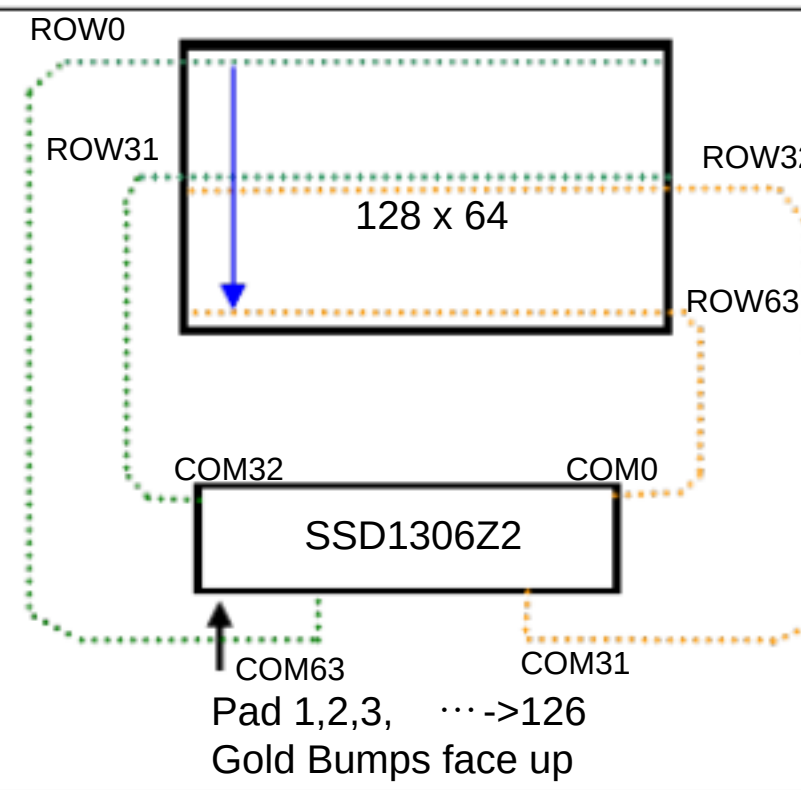
10.1.17 Set Pre-charge Period (D9h)

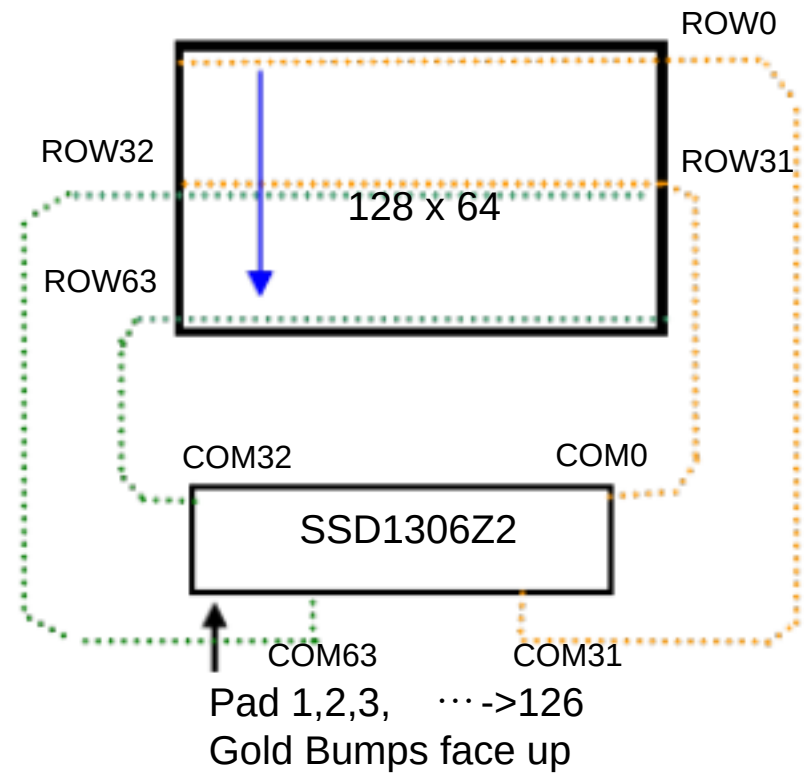
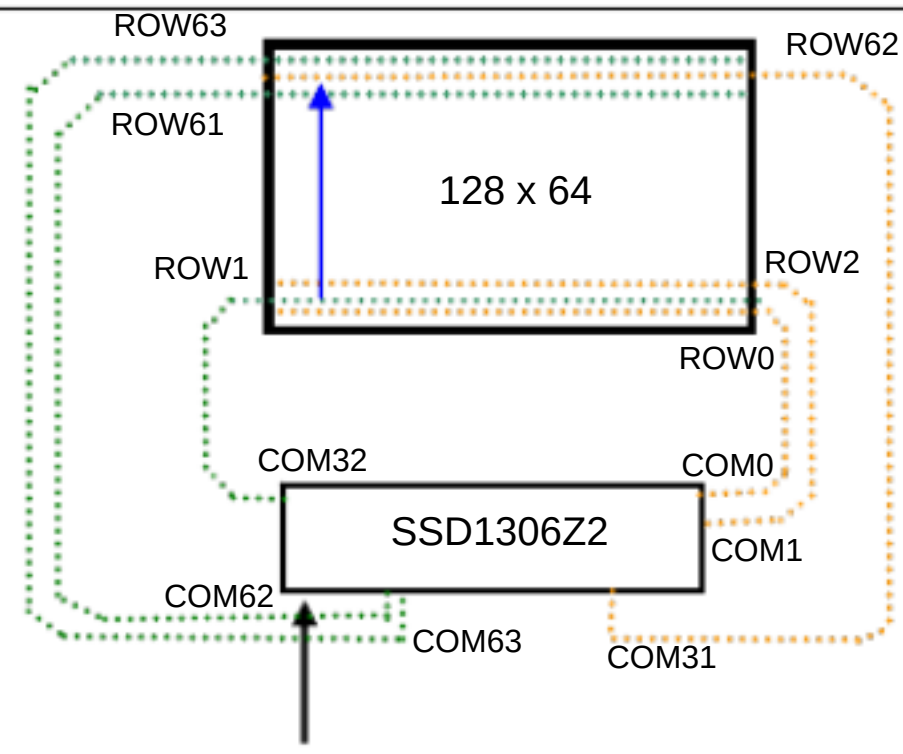
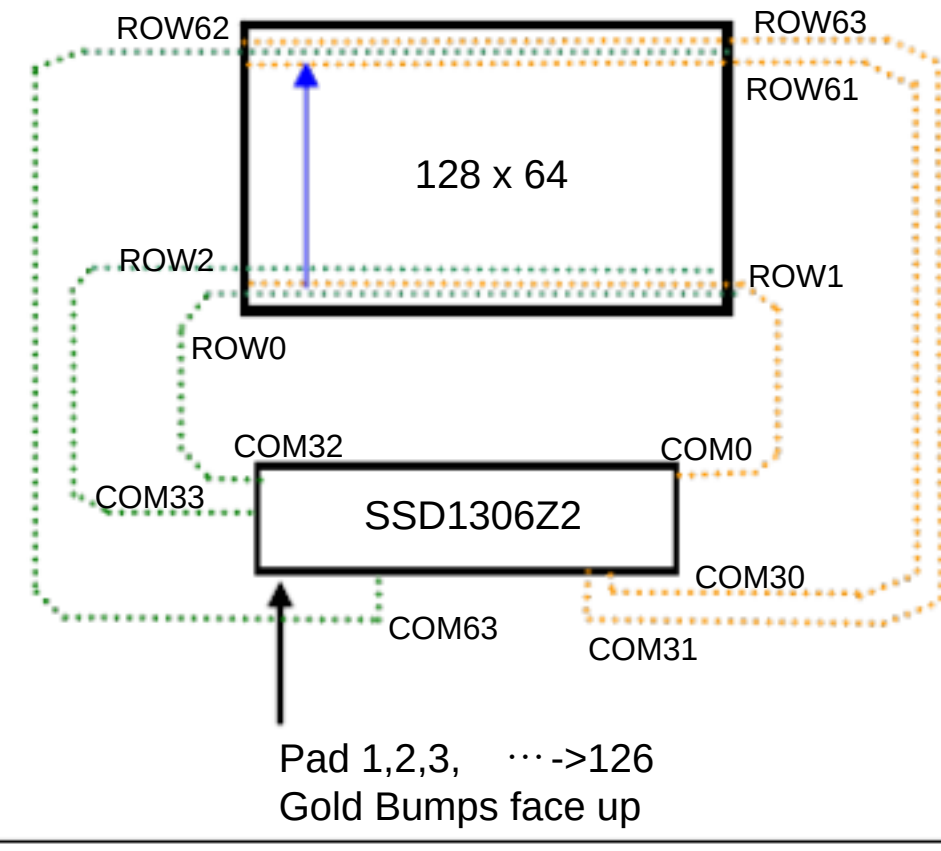
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals 2 DCLKs.

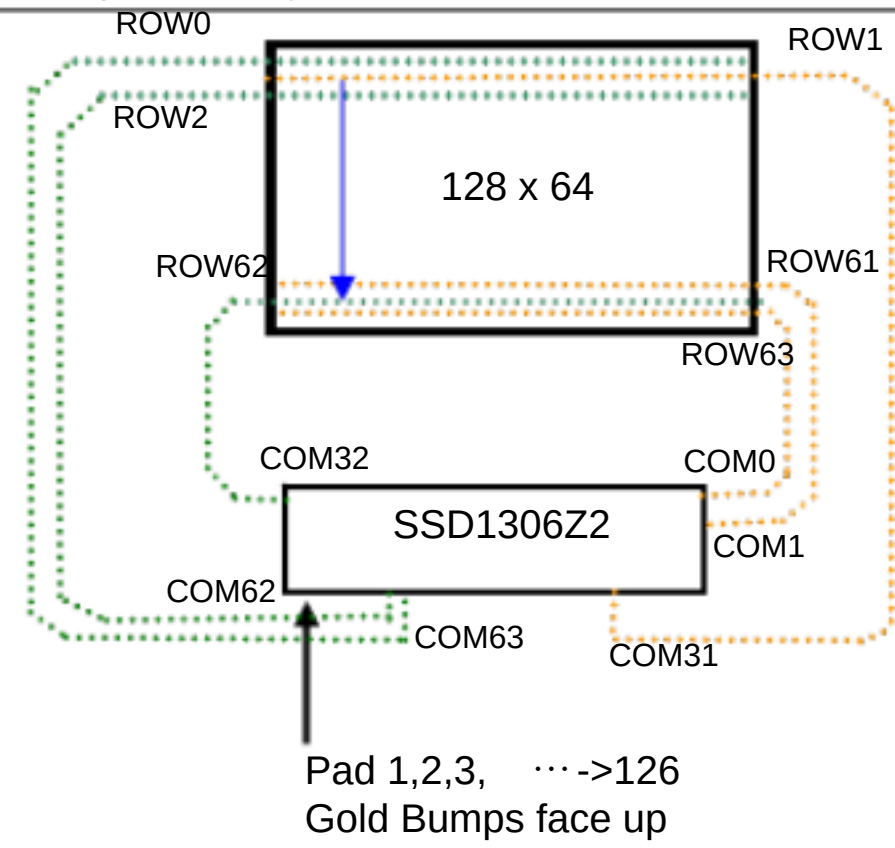
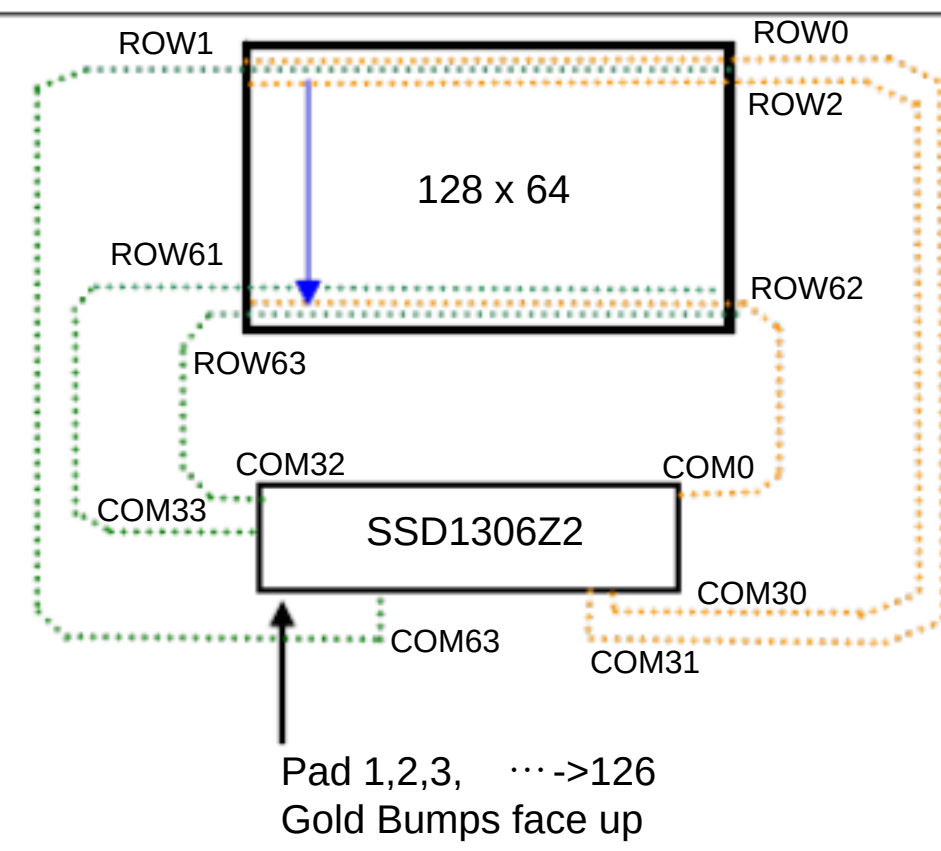
10.1.18 Set COM Pins Hardware Configuration (DAh)

This command sets the COM signals pin configuration to match the OLED panel hardware layout. The table below shows the COM pin configuration under different conditions (for MUX ratio =64):

Table 10-3 : COM Pins Hardware Configuration

Conditions COM	pins Configurations
1 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM0 to COM63 (C0h) Disable COM Left/Right remap (DAh A[5] =0)	
2 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM0 to COM63 (C0h) Enable COM Left/Right remap (DAh A[5] =1)	
3 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM63 to COM0 (C8h) Disable COM Left/Right remap (DAh A[5] =0)	

Conditions COM	pins Configurations
4 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM63 to COM0 (C8h) Enable COM Left/Right remap (DAh A[5] =1)	
5 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM0 to COM63 (C0h) Disable COM Left/Right remap (DAh A[5] =0)	
6 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM0 to COM63 (C0h) Enable COM Left/Right remap (DAh A[5] =1)	

Conditions COM	pins Configurations
7 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM63 to COM0(C8h) Disable COM Left/Right remap (DAh A[5] =0)	
8 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM63 to COM0(C8h) Enable COM Left/Right remap (DAh A[5] =1)	

10.1.19 Set V_{COMH} Deselect Level (DBh)

This command adjusts the V_{COMH} regulator output.

10.1.20 NOP (E3h)

No Operation Command

10.1.21 Status register Read

This command is issued by setting D/C# ON LOW during a data read (See Figure 13-1 to Figure 13-2 for parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

10.1.22 Charge Pump Setting (8Dh)

This command controls the ON/OFF of the Charge Pump. The Charge Pump must be enabled by the following command sequence:

8Dh ; Charge Pump Setting
14h ; Enable Charge Pump
AFh; Display ON

10.2 Graphic Acceleration Command

10.2.1 Horizontal Scroll Setup (26h/27h)

This command consists of consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page and scrolling speed.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

The SSD1306 horizontal scroll is designed for 128 columns scrolling. The following two figures (Figure 10-8, Figure 10-9, Figure 10-10) show the examples of using the horizontal scroll:

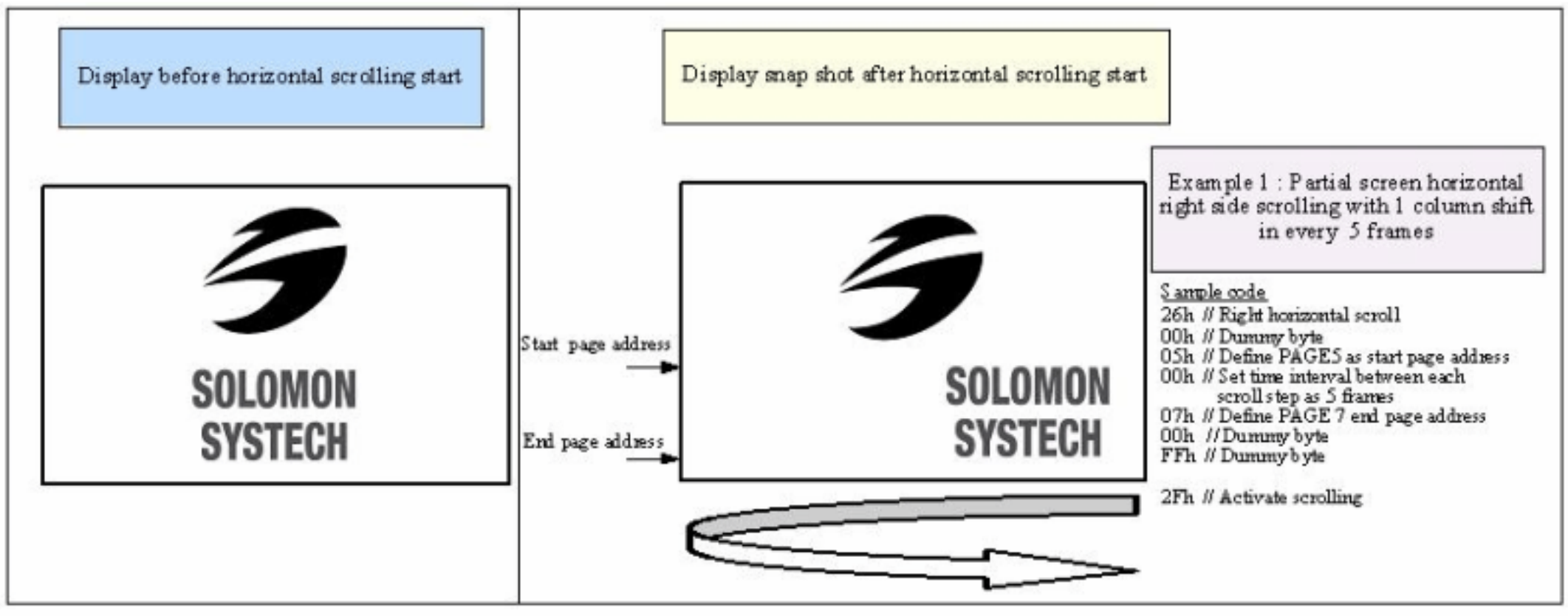
Figure 10-8 : Horizontal scroll example: Scroll RIGHT by 1 column

Original Setting	0 PAGES	1 PAGES	2 PAGES	3 PAGES	4 PAGES	5 PAGES	…	…	…	253 PAGES	254 PAGES	255 PAGES	256 PAGES	257 PAGES	258 PAGES
After one scroll step	258 PAGES	0 PAGES	1 PAGES	2 PAGES	3 PAGES	4 PAGES	…	…	…	254 PAGES	255 PAGES	256 PAGES	257 PAGES	258 PAGES	259 PAGES

Figure 10-9 : Horizontal scroll example: Scroll LEFT by 1 column

Original Setting	0 PAGES	1 PAGES	2 PAGES	3 PAGES	4 PAGES	5 PAGES	…	…	…	253 PAGES	254 PAGES	255 PAGES	256 PAGES	257 PAGES	258 PAGES
After one scroll step	1 PAGES	2 PAGES	3 PAGES	4 PAGES	5 PAGES	6 PAGES	…	…	…	254 PAGES	255 PAGES	256 PAGES	257 PAGES	258 PAGES	259 PAGES

Figure 10-10 : Horizontal scrolling setup example



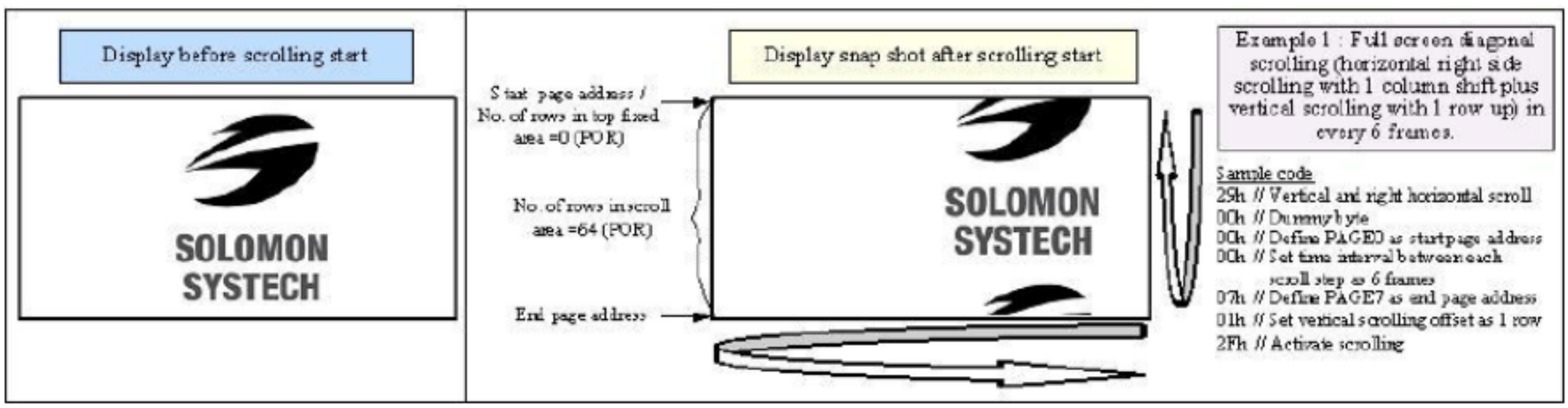
10.2.2 Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)

This command consists of 6 consecutive bytes to set up the continuous vertical scroll parameters and determines the scrolling start page, end page, scrolling speed and vertical scrolling offset.

The bytes B[2:0], C[2:0] and D[2:0] of command 29h/2Ah are for the setting of the continuous horizontal scrolling. The byte E[5:0] is for the setting of the continuous vertical scrolling offset. All these bytes together are for the setting of continuous diagonal (horizontal + vertical) scrolling. If the vertical scrolling offset byte E[5:0] is set to zero, then only horizontal scrolling is performed (like command 26/27h).

Before issuing this command the scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted. The following figure (Figure 10-11) show the example of using the continuous vertical and horizontal scroll:

Figure 10-11 : Continuous Vertical and Horizontal scrolling setup example



10.2.3 Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

10.2.4 Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands :26h/27h/29h/2Ah . The setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

The following actions are prohibited after the scrolling is activated

1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

10.2.5 Set Vertical Scroll Area(A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29/2Ah), the number of rows that in vertical scrolling can be set smaller or equal to the MUX ratio.

10.3 Advance Graphic Command

10.3.1 Set Fade Out and Blinking (23h)

This command allow to set the fade mode and adjust the time interval for each fade step. Below figures show the example of Fade Out mode and Blinking mode.

Figure 10-12 : Example of Fade Out mode

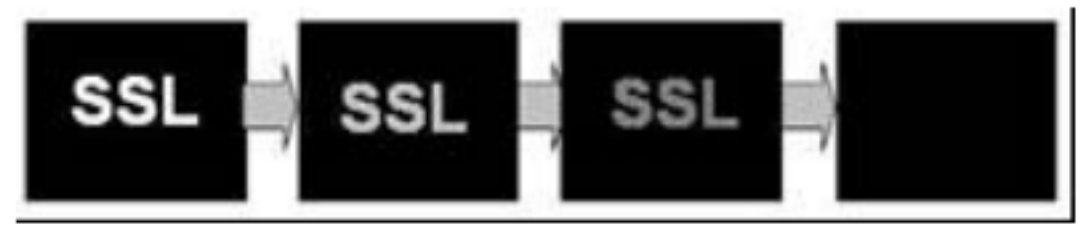
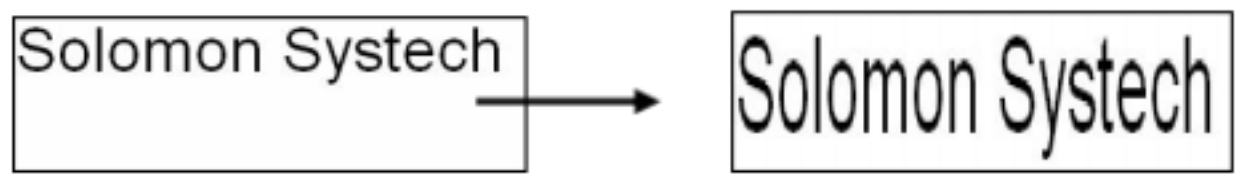


Figure 10-13 : Example of Blinking mode

10.3.2 Set Zoom In (D6h)

Under Zoom in mode, one row of display contents is expanded into two rows on the display. That is, contents of row0~31 fill the whole display panel of 64 rows. It should be notice that the panel must be in alternative COM pin configuration (command DAh A[4] =1) for zoom in function.

Figure 10-14 : Example of Zoom In



11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings (Voltage Referenced to VSS)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{BAT}		-0.3 to +5	V
V_{CC}		0 to 16	V
V_{SEG}	SEG output voltage	0 to V_{CC} V	
V_{COM}	COM output voltage	0 to 0.9*V_{CC} V	
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3 V	
T_A	Operating Temperature	-40 to +85	oC
T_{stg}	Storage Temperature Range	-65 to +150	oC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}

V_{DD} = 1.65 to 3.3V

T_A = 25 ℃

Table 12-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	7	-	15	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.3	V
V_{BAT}	Charge Pump Regulator Supply Voltage	- 3.3		-	4.2	V
Charge Pump V_{CC}	Charge Pump Output Voltage	V_{BAT} = 3.3V~4.2V, Output loading = 6mA	7 7.5		-	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1 x V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DD} -		-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2 x V_{DD}	V
$I_{CC, SLEEP}$	$I_{CC,}$ Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	- -		10	uA
$I_{DD, SLEEP}$	$I_{DD,}$ Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	- -		10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} = 12V, I_{REF} = 12.5uA No loading, Display ON, All ON	Contrast = FFh	- 430		780	uA
I_{DD}	V_{DD} Supply Current V_{DD} = 2.8V, V_{CC} = 12V, I_{REF} = 12.5uA No loading, Display ON, All ON		- 50		150	uA
I_{SEG}	Segment Output Current V_{DD}=2.8V, V_{CC}=12V, I_{REF}=12.5uA, Display ON.	Contrast FFh -		100	-	uA
		Contrast AFh -		69	-	
		Contrast 3Fh -		25	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:131] = Segment current at contrast = FFh	-3 -		+3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	+2	%

13 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD} =1.65 to3.3V
T_A = 25 ℃

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.8V	333	370	407	kHz
F_{FRM}	Frame Frequency for 64 MUX Mode	128x64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1/(DxKx64) (2)	-	Hz
RES#	Reset low pulse width		3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

(2) D: divide ratio (default value = 1)
K: number of display clocks (default value = 54)
Please refer to Table 9-1 (Set Display Clock Divide Ratio/Oscillator Frequency, D5h) for detailed description

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25 ° C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-1 : 6800-series MCU parallel interface characteristics

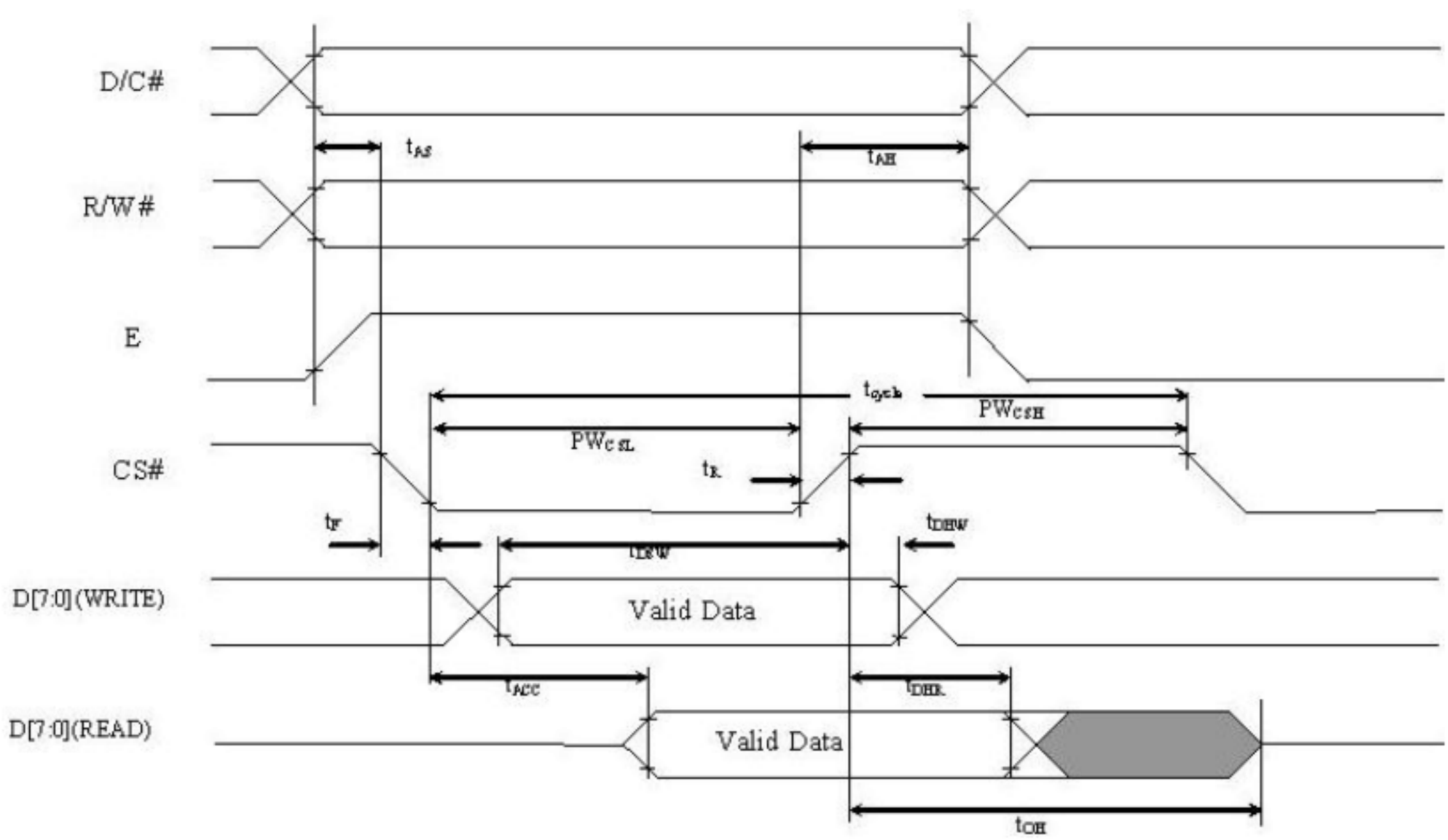


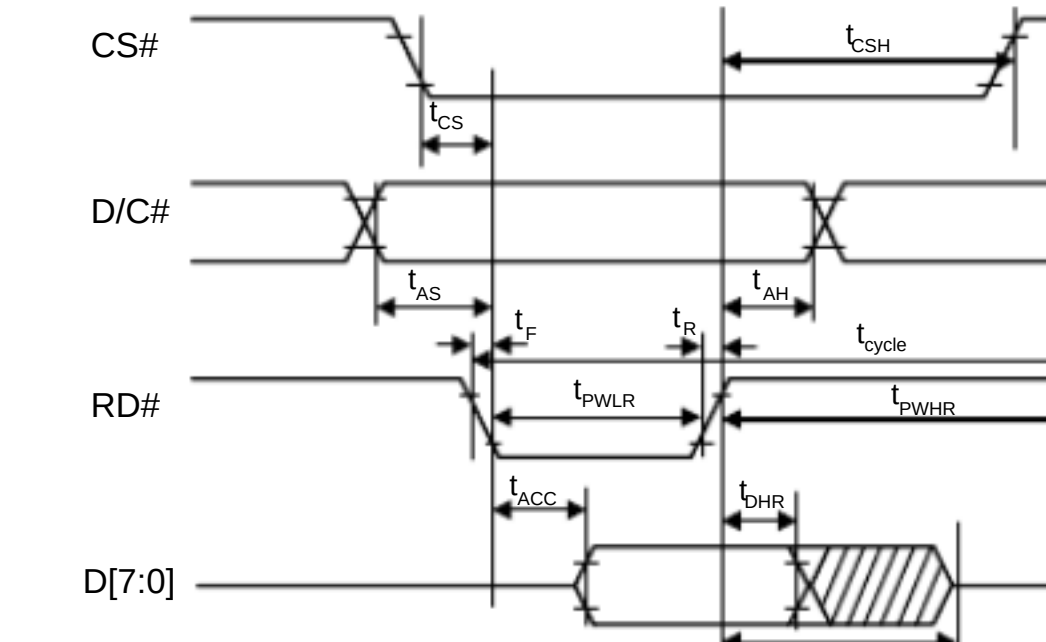
Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25 ° C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	- -		140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	- - 40			ns
t_F	Fall Time	- - 40			ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series parallel interface characteristics

Write Cycle



Read cycle

Table 13-4 : 4-wire Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25 ° C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-3 : 4-wire Serial interface characteristics

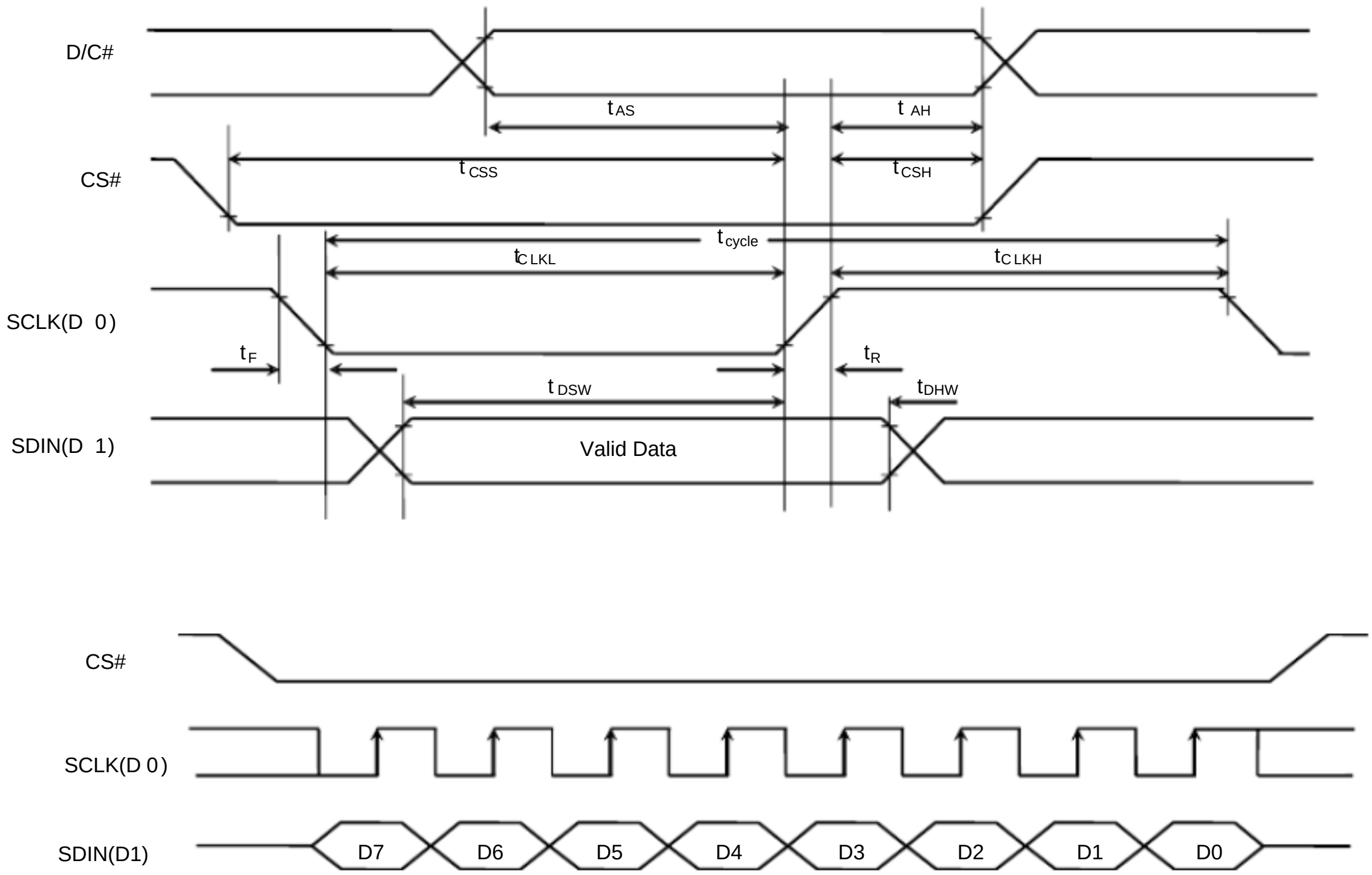
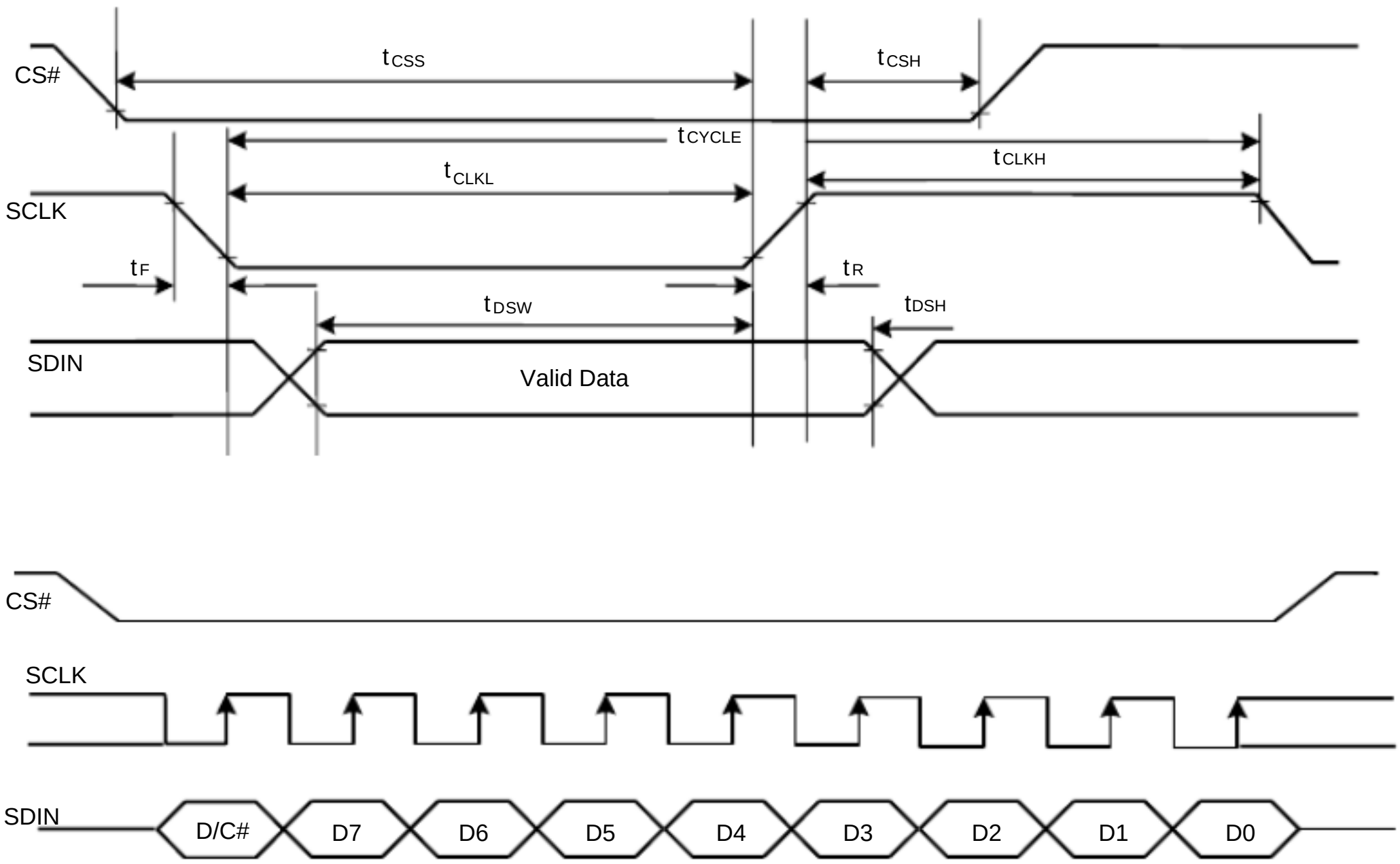


Table 13-5 : 3-wire Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25 ° C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-4 : 3-wire Serial interface characteristics



Conditions:

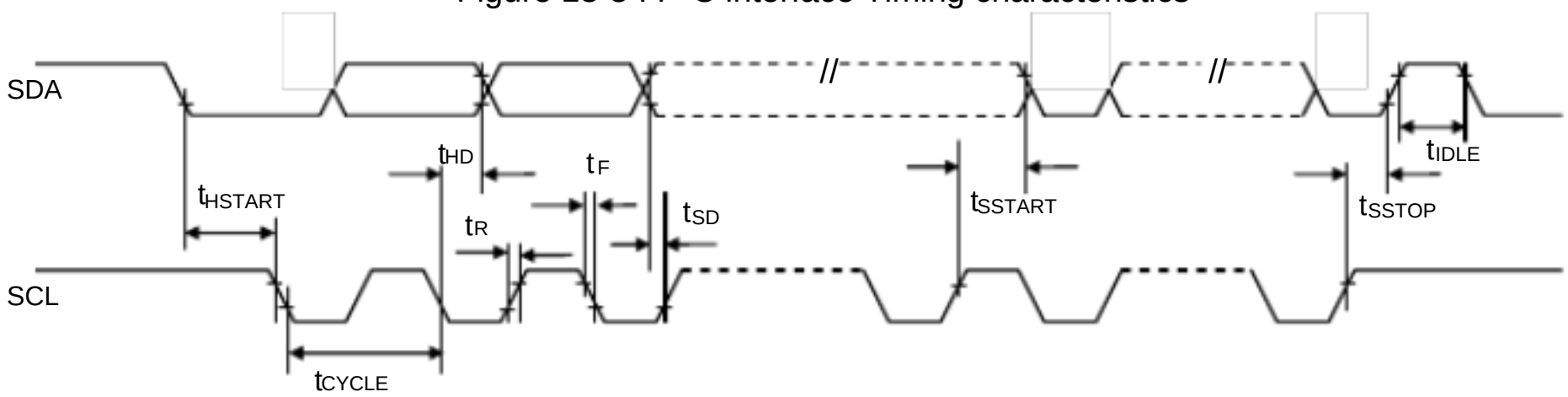
V_{DD} - V_{SS} = V_{DD} - V_{SS} = 1.65V to 3.3V

T_A = 25 ℃

Table 13-6 :I ^{2}C Interface Timing Characteristics

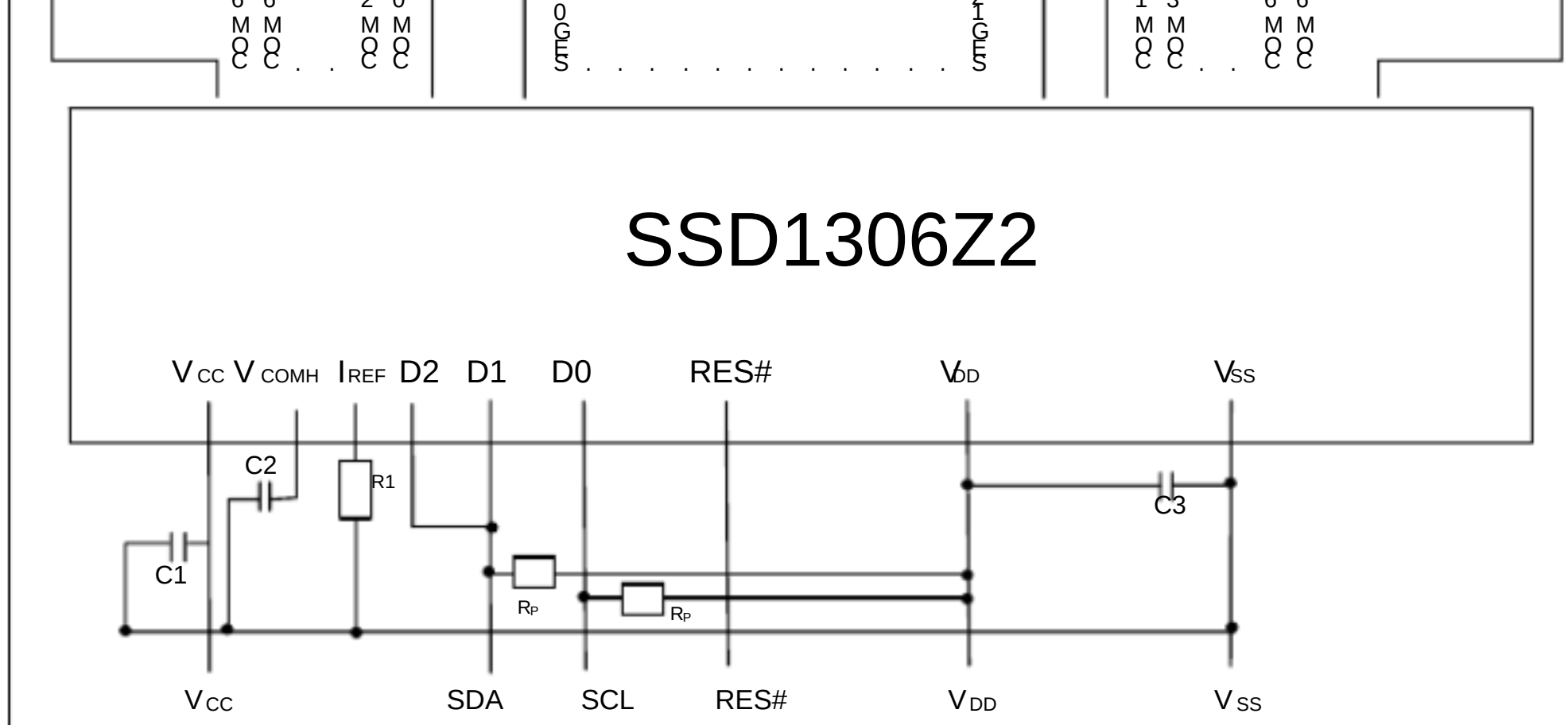
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "OUT" SDA pin)	0	-	-	ns
	Data Hold Time (for "IN" SDA pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6 -		-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Figure 13-5 : I ^{2}C interface Timing characteristics



14 Application Example

Figure 14-1 : Application Example of SSD1306Z2 with External V_{CC} and I^2C interface



The configuration for I^2C interface mode is shown in the following diagram:
(V_{DD} = 1.65V ~ 3.3V, V_{CC} =7V~15V, I_{REF}=12.5uA)

Pin connected to MCU interface: RES#, SDA, SCL
Pin internally connected to V_{SS}: BS0, BS2, CL, D[7:3], E, R/W#, CS#, D/C#, BGGND
Pin internally connected to V_{DD}: BS1, CLS
V_{BAT}, C1P, C1N, C2P, C2N, V_{BREF}, FR should be left open.

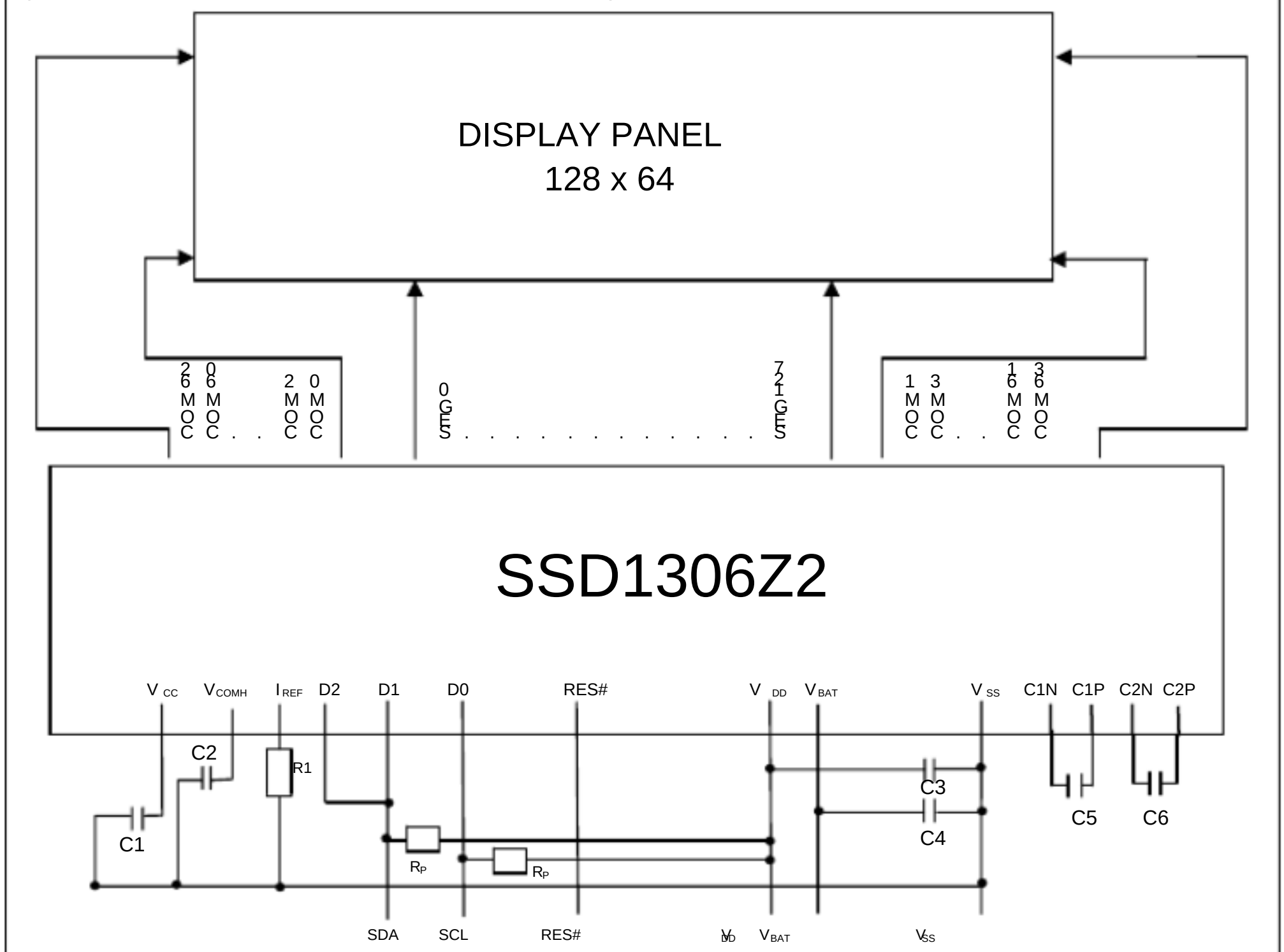
C1, C2: 2.2uF (1)
C3: 1.0uF (1)
R_P : Pull up resistor

Voltage at I_{REF} = V_{CC} – 2.5V. For V_{CC} = 7.5V, I_{REF} = 12.5uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (7.5-2.5) / 12.5u
=400K Ω

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.

Figure 14-2 Application Example of SSD1306Z2 with Internal Charge Pump and I 2C interface

The configuration for I 2C interface mode is shown in the following diagram:
(V_{DD} = 1.65V ~ 3.3V, V_{BAT} =3.3V~4.2V, I_{REF}=12.5uA)



Pin connected to MCU interface: RES#, D[2:0]
Pin internally connected to V_{SS}: BS0, BS2, CL, D[7:3], E, R/W#, CS#, D/C#, BGGND
Pin internally connected to V_{DD} : BS1, CLS
V_{BREF} , FR should be left open.

C1, C2: 2.2uF (1)
C3, C4 : 1.0uF (1)
C5, C6: 1.0uF/10V (1)
R_P : Pull up resistor

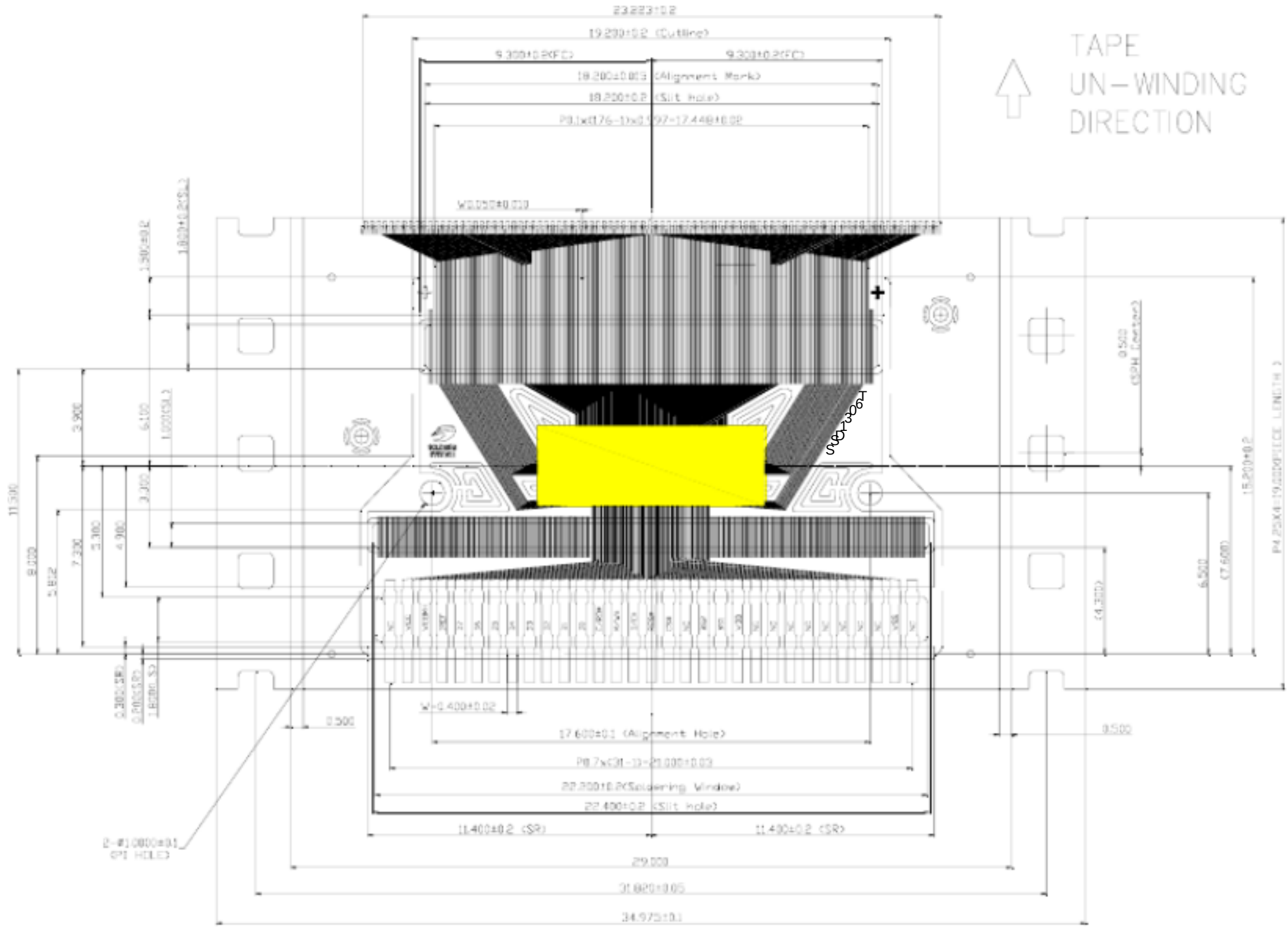
Voltage at I_{REF} = V_{CC} − 2.5V. For V_{CC} = 7.5V, I_{REF} = 12.5uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (7.5-2.5) / 12.5u
=400KΩ

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.

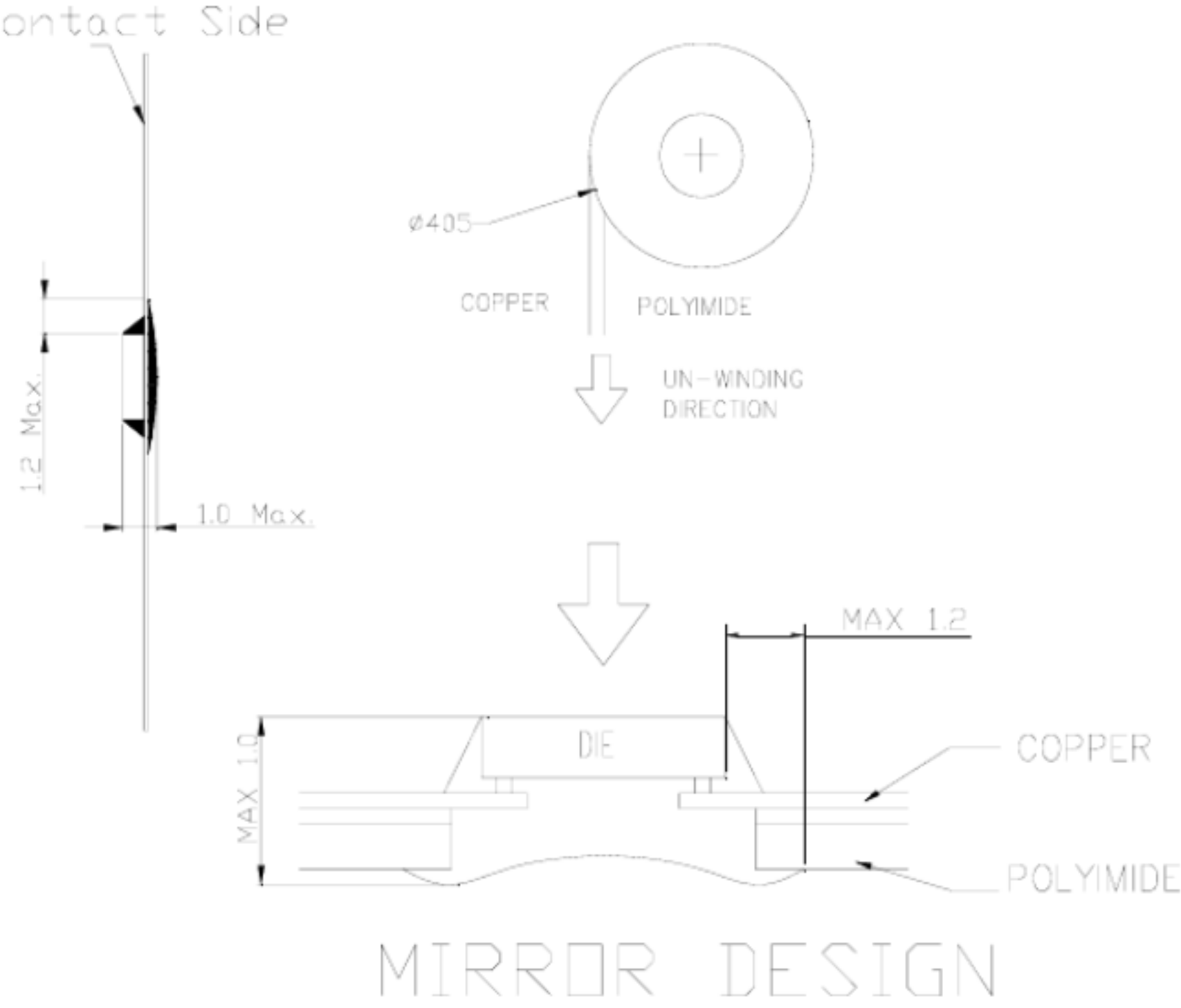
15 PACKAGE INFORMATION

15.1 SSD1306TR1 Detail Dimension

Figure 15-1 SSD1306TR1 Detail Dimension

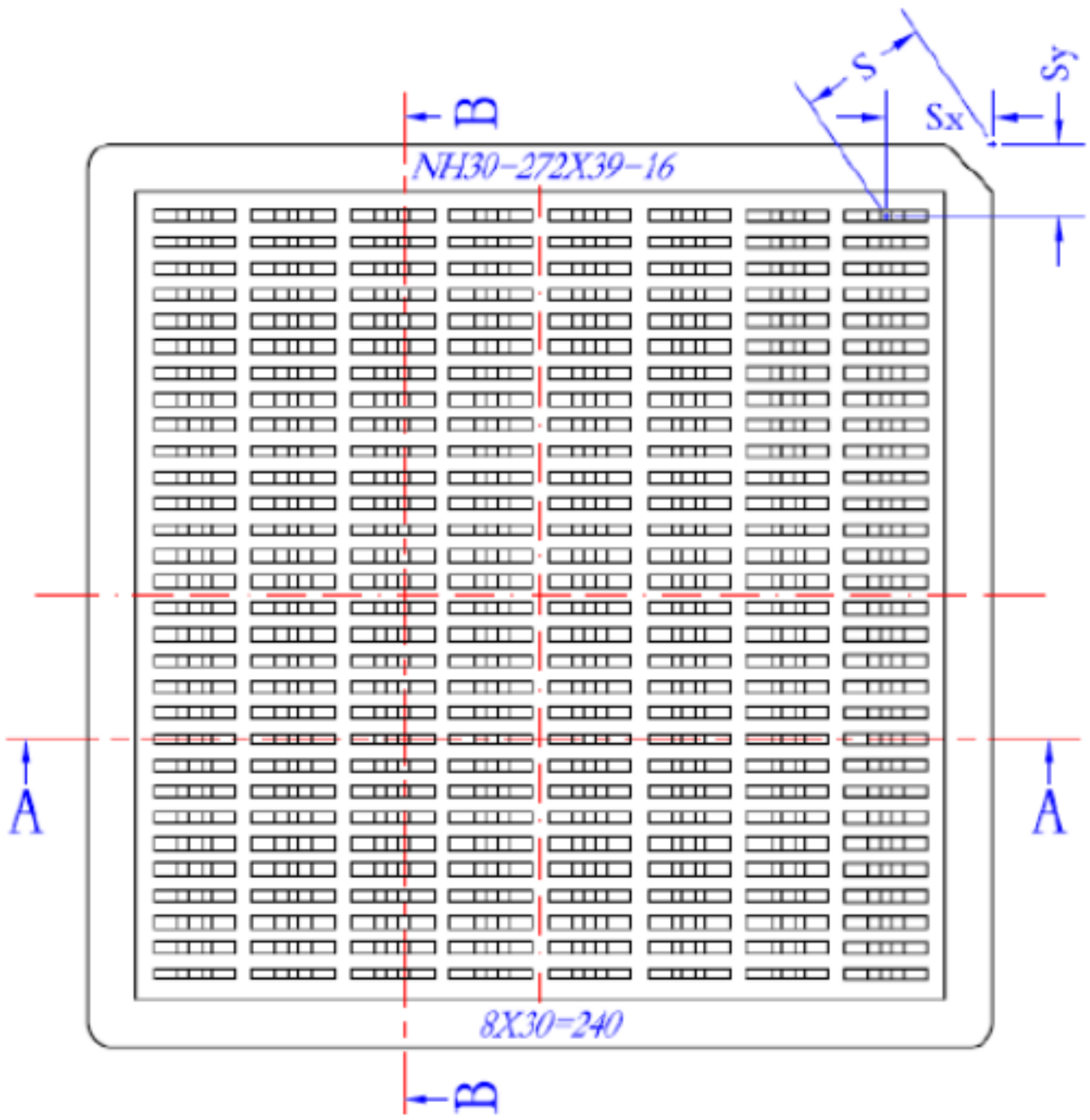


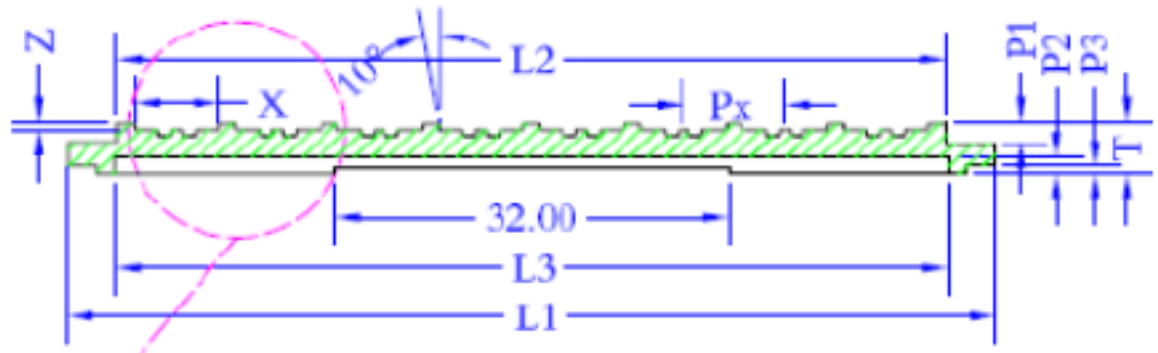
Specification:
1. GENERAL TOLERANCE: ±0.05 mm
2.MATERIAL
PI: 75 ± 8 um
CU: 15 ± 3 um
ADHESIVE: 12 ± 3um
SR: 26 ± 14 um
TOLERANCE ± 0.200 mm
FLEX COATING: Min 10 um
3.Plating : Sn 0.20 ±0.05 um
4. TAPESITE: 4 SPH, 19 mm



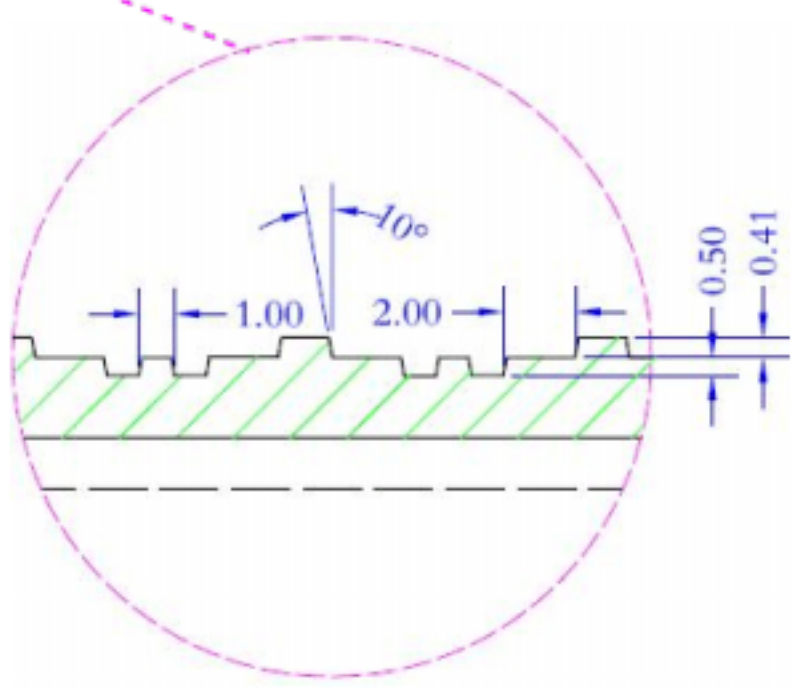
15.2 SSD1306Z2 Die Tray Information

Figure 15-2 : SSD1306Z2 die tray information





SECTION A-A



SPEC	
	MM
(L1)	76.00±0.10
(L2)	68.10±0.10
(L3)	68.20±0.10
(T)	4.20±0.05
(SX)	8.95
(SY)	6.10
(S)	10.83
(X)	6.91±0.05
(Y)	1.00±0.05
(Z)	0.41±0.05
(Px)	8.30±0.05
(Py)	2.20±0.05
(Nx)	8
(Ny)	30
(N)	240
(P1)	1.60
(P2)	1.40
(P3)	0.65

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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