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Ceramic and Glass-Ceramic Packaging in the 1990s

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A broad overview of packaging involving interconnecting, powering, protecting, and cooling semiconductor chips to meet a variety of computer system needs is presented. The general requirements for ceramics in terms of their thermal, mechanical, electrical, and dimensional control requirements are presented, both for high-performance and low-performance applications. Glass-ceramics are identified as the best candidates for high-performance systems, and aluminum nitride, alumina, or mullite are identified for low-performance systems. Glass-ceramic/copper substrate technology is discussed as an example of high-performance ceramic packaging for use in 1990s. Lower-dielectric-constant ceramics such as composites of silica, borosilicate, and cordierite, with or without polymers and porosity, are projected as potential ceramic substrate materials by the year 2000. [Key words: packaging, semiconductors, ceramics, glass-ceramics, computers.]

I. Introduction

MICROELECTRONICS is a 500-billion-dollar industry worldwide. It spans from consumer products, such as compact disc players, to supercomputers. It involves a broad spectrum of technologies including semiconductors and packaging for processing information, magnetics and optics for storing information, cathode ray tubes and liquid crystals with thin-film transistors for displaying information, electrophotography for printing information, and optical fibers for transferring information. Some of the ceramic materials currently in use in these products are shown in Table I.[1]

Computers in the 1990s that do not look and act like computers and that provide full-motion video and high-quality audio through digital video interactive technology, as compared with the current simple and single-frame images, will be common. Workstations will progress to a level where they will provide facsimile capability, making it possible for users to compose and transmit full-color images accompanied by voice annotation. Machines will respond readily to spoken commands and provide intelligent conversations.[2] Supercomputers will perform at least four trillion complex calculations a second, about 1000 times more than current machines. Scientists will be able to calculate complex electronic interactions to a level where they will be able to synthesize microelectronic materials with properties that never existed before.[3]

Microelectronic packaging is one of the key technologies that will make all these advances possible. Packaging has been identified recently as one of the ten critical technologies for the advancement of mankind in the 1990s.[4] Ceramics and glass-ceramics are the basis of packaging. This paper reviews the functions of packaging, the semiconductor and system technology requirements for packaging, and the role of ceramics and glass-ceramics in meeting these requirements in the 1990s. Glass-ceramic/copper technol-

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feature

Table I. Application of Ceramics in Microelectronics

Information technology	Application	Ceramic material
Information processing		
Package	Substrate	Al_2O_3, glass+ceramics, AlN
Device	Dielectric	Si_3N_4, SiO_2, PSG*
	Mask	Borosilicate glasses
Information storage	Disc	Iron oxide, Ferrite
	Tape	Chromium oxide
	Head	Ferrites, glass, Al_2O_3+TiC substrate
Information display	Liquid crystal Thin-film Transistor	Sputtered SiO_2/Si_3N_4
Information printing	Ink-jet nozzle	ZrO_2-containing glass
	Electroerosion head	Ceramic–metal composites
Information transfer	Optical fiber	SiO_2, B_2O_3–SiO_2 glasses

*PSG is phosphosilicate glass.

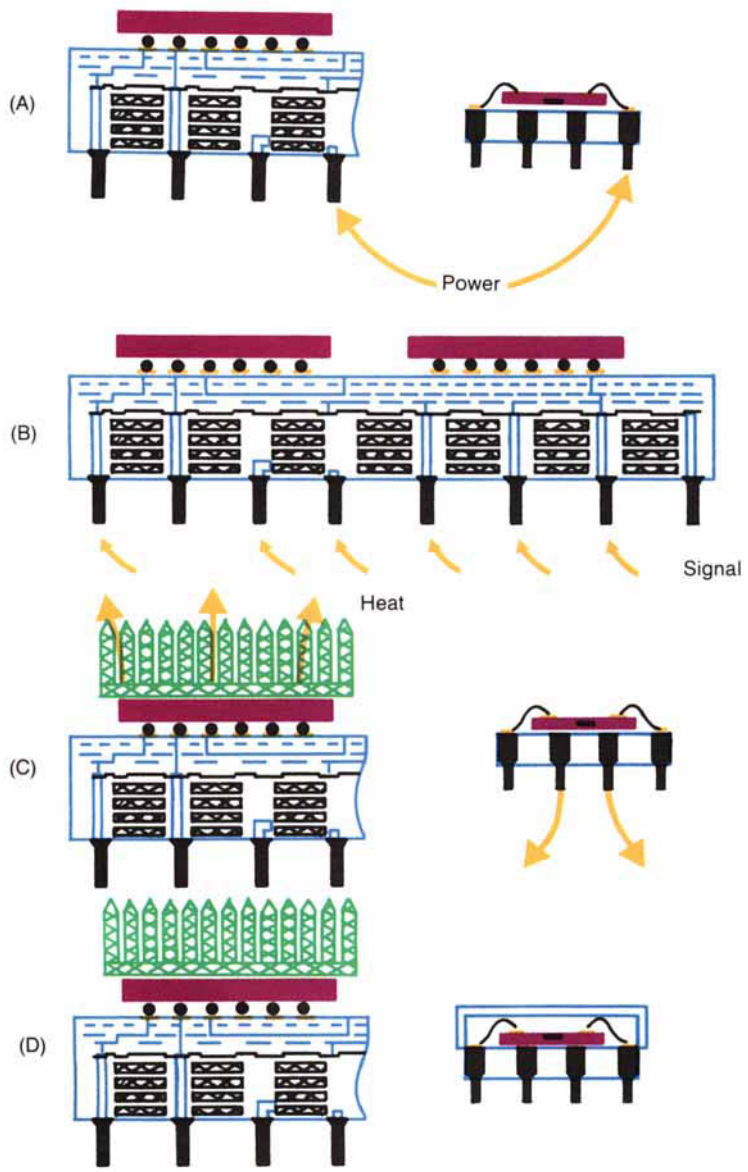

Fig. 1. Four major functions of the package: (A) power distribution, (B) signal distribution, (C) heat dissipation, and (D) package protection.

ogy developments that started at IBM in 1976 for top-of-the-line computers and that are currently in production are used as examples to discuss the state-of-the-art in ceramic packaging. Finally, this paper also projects the challenges in ceramic materials to the year 2000.

II. Packaging

Packaging involves interconnecting, powering, protecting, and cooling of semiconductor circuits to meet a variety of microelectronic applications.[5] These package functions are schematically illustrated in Fig. 1. The semiconductor chips (in red) are powered from a power supply through the metal wiring in the substrate (Fig. 1(A)), interconnected for signal distribution by means of interchip wiring (Fig. 1(B)), cooled by thermal conduction through the substrate or cooled from the back of the chip by means of a heatsink (Fig. 1(C)), and protected by hermetic packaging or encapsulation (Fig. 1(D)). The properties of the substrate, consistent with these four requirements, are as follows. The dielectric constant of the ceramic in which the metal is embedded defines the signal propagation speed as

$$T_d = \sqrt{\frac{E_r}{C}} \tag{1}$$

where T_d is the signal propagation delay, E_r the dielectric constant of the ceramic, and C the speed of light. Thus, low-dielectric-constant ceramics have high performance. Another requirement is for efficient power distribution from the power supply to the chip, with minimum voltage variations. Thus, high-conductive metal, such as copper, is most desirable. Heat removal from the chip is a very important property of the package to maintain the chip temperature below 100°C for efficient and reliable operation of the chip. The heat-removal characteristics of the substrate, however, depend on how the chip is bonded to the substrate. This particular requirement is, perhaps, most misunderstood by the ceramic community. The two most common methods of bonding the chip to the substrate are illustrated in Fig. 2: active side down to the substrate as in Fig. 2(A), or active side up or back bonded to the substrate as in Fig. 2(B). Whereas, in the latter method, heat from the chip is conducted through the substrate, thus requiring high thermal conductivity for the substrate, the former method does not depend on the high thermal conductivity of the substrate. The heat is conducted through a thin, high-conductance silicon chip to an aluminum, copper, aluminum nitride, or other high-conductance, but inexpensive, heatsink. The thermal conductivity of silicon is 150 W/(m·K), about 7 times higher than that of polycrys-

talline alumina; very efficient cooling (up to 100 W/cm^2) becomes possible with face-down, backside heatsink, air, and water cooling. Almost all superfast computers are currently in this technology. High-thermal-conduction ceramics such as aluminum nitride are useful in low-cost, back-bonded applications, as discussed later.

A typical packaging hierarchy is illustrated in Fig. 3. The hierarchy involves bonding of semiconductor chips to the substrate by either wirebonding, tape-automated bonding (TAB), or flip-chip solder bonding. All these methods are schematically illustrated in Fig. 4. Wirebonding requires that the chip be bonded active side up and, based on the previous discussion, that heat removal be accomplished through the substrate, thus requiring high thermal conductivity for the substrate. Contrary to wirebonding, TAB and flip-chip solder connections do not depend on the thermal properties of the substrate. Most high-performance applications in the 1990s that require more than 500 chip connections are expected to be solder or TAB connected. The substrate to which the chips are bonded can be single-chip or multichip carriers, which can be either ceramic or plastic. These carriers are interconnected to the next level assembly, usually an organic printed wiring card. A number of cards are plugged into a larger organic board, often referred to as a printed wiring board or a back panel. The connection between the ceramic or plastic carrier to the organic card is accomplished by either solder connection (referred to as surface mount technology (SMT)) or pin connection (referred to as pin-through-hole connection (PTH)). If the carrier is a ceramic substrate, an additional property of the ceramic substrate is that of high mechanical strength to withstand pin-joining and insertion stresses. All these technologies are discussed in great detail in a recent book.[5]

III. Semiconductors

A majority of the semiconductor circuits currently in use are silicon. However, a number of other device technologies—such as gallium arsenide, Josephson junction, and high electron mobility transistor (HEMT)—with better speed–power relations (Fig. 5) have been demonstrated. This popularity is due to the process experience with silicon, which is expected to reach giga-bit integration by the year 2000. The phenomenal growth in the number of circuits in the two most important silicon device families—field effect transistor (FET) and bipolar—during the last two and one-half decades is illustrated in Fig. 6. In contrast, the non-silicon technologies are about 10 times lower in circuit integration. Since the recently reported performance of silicon is below 50 ps, high performance and high integration of circuits in silicon simply require more and more power per chip, requiring enormous increases in cooling capabilities of ceramics. This is schematically illustrated in Fig. 7, wherein the number of circuits on a 1-cm chip is plotted as a function of power that the package needs to distribute and remove at various circuit-switching thresholds. The actual package power (in W/cm^2) is illustrated in Fig. 8 for various top-of-the-line computers since the days of the first transistor.[6] The experimental cooling capabilities, however, have been demonstrated to be about 50 times more than those currently in commercial use.[7]

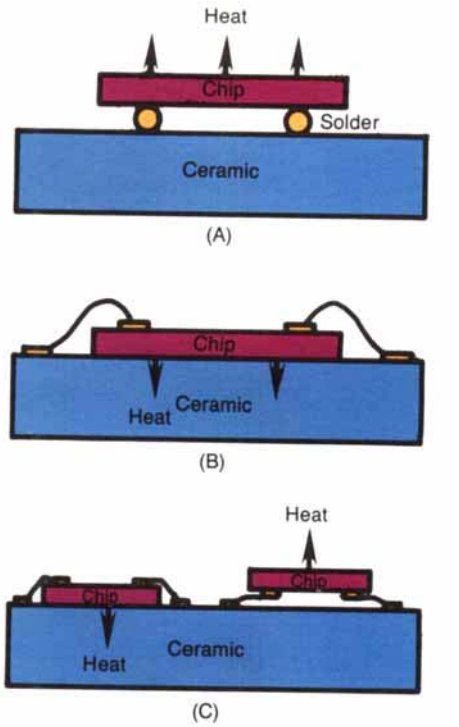

Fig. 2. Ideal properties of ceramic depend on chip connection: (A) heat removal with solder connection, (B) heat removal with wirebond, and (C) heat removal with tab.

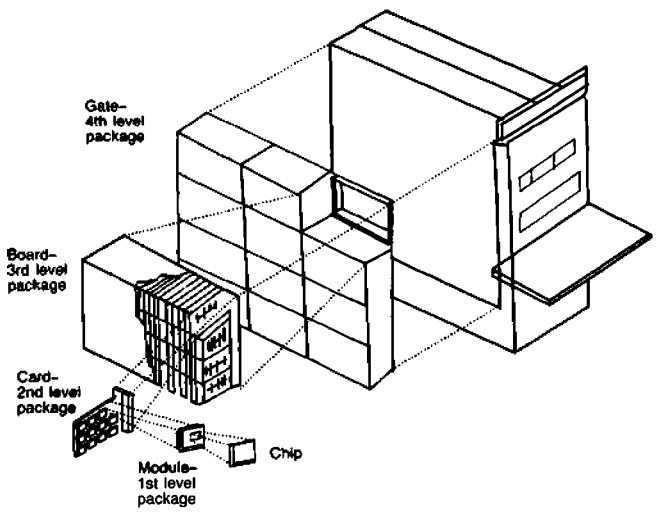

Fig. 3. Electronic package hierarchy in computers.

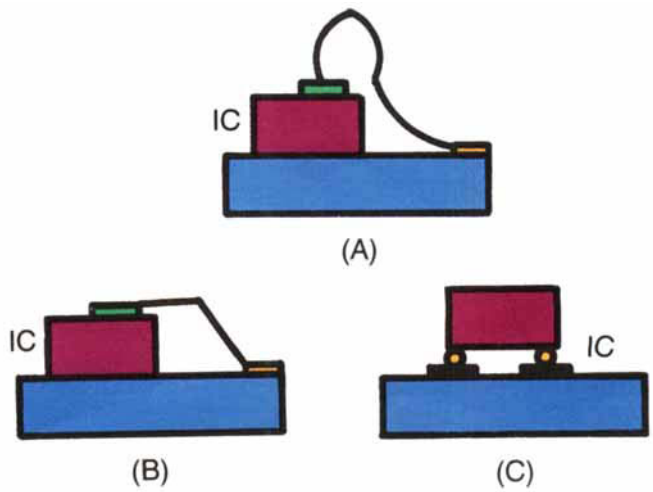

Fig. 4. Chip-joining technologies: (A) wirebond, (B) tab, and (C) flip chip.

The input/output (I/O) requirements for the ceramic substrate consistent with the silicon integrations shown in Fig. 6 can be calculated from Rent's rule:[8]

$$P = BN^S \quad (2)$$

where N is the number of logic gates, P is the number of signal connections, and B and S are constants.

These I/O requirements and the chip sizes required to accommodate the circuit integrations over the last two and one-half decades are illustrated in Fig. 9 as a function of the number of circuits on the chip.

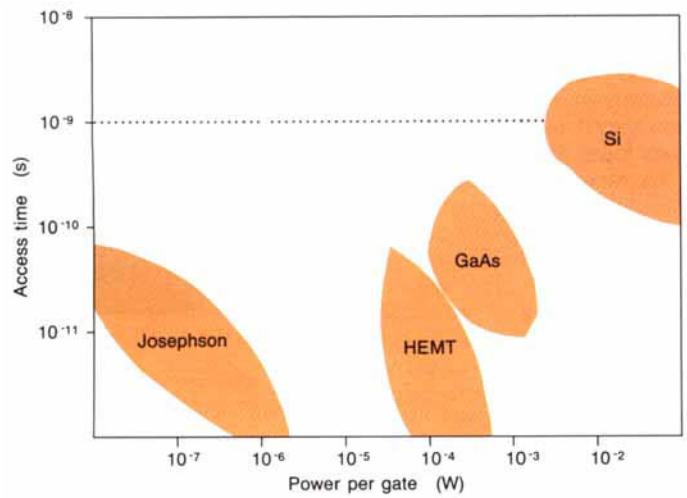

Fig. 5. Power per gate versus access time.

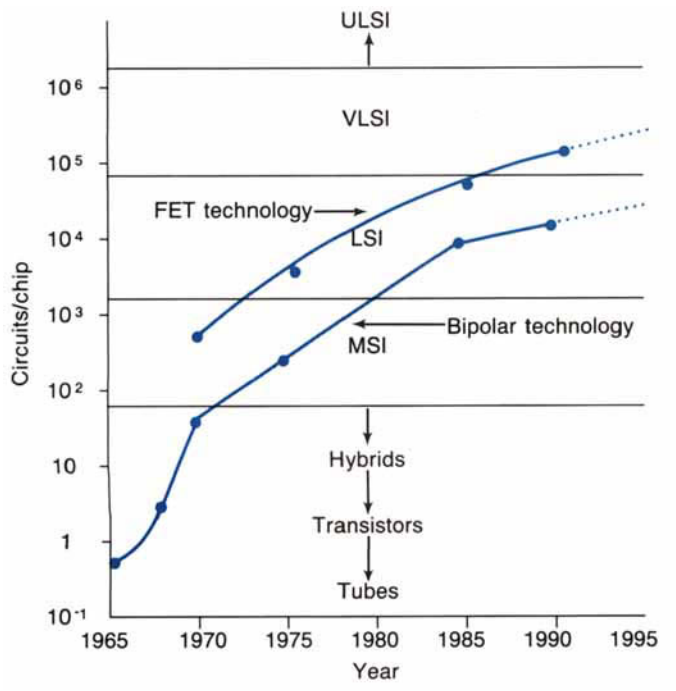

Fig. 6. Evolution and projected growth of chip circuit density.

IV. Computer System Requirements

Figure 10 illustrates, through the year 2000, the performance of the computer systems, measured in millions of instructions per second (Mips), as a function of time for large systems, minicomputers, and personal computers.[9] Figure 10 shows that the uniprocessor performance in Mips for large systems will double or triple from the current 40 to 50 Mips during the 1990s. This trend is also true for other computers. These performances can be converted into a very important parameter for packages and semiconductors called "cycle time," which refers to the total time required to execute an instruction set. Cycle time is related to computer performance by

$$\text{computer performance} = \frac{1000}{\left(\text{cycle time}\right) \times \left(\text{cycles/instruction}\right)} \quad (3)$$

where cycles/instruction refers to the number of system cycles required to process an instruction set. The cycle times, corresponding to Mips, are illustrated on the left-hand vertical axis in Fig. 10. Thus, to achieve a performance of 50 Mips requires a technology cycle time of about 8 ns. This technology cycle time is further broken into two major parts: silicon and packaging. A general equation describing these is as follows:

$$\text{computer cycle time} = (\text{logic} + \text{array} + \text{clock skew}) + (\text{driver} + \text{receiver} + \text{wiring} + \text{noise}) \quad (4)$$

where the four terms in the first set of parentheses are due to the semiconductor, and the four terms in the second set are due to the packaging. Thus, to support a 50-Mips processor requires about 8 ns of cycle time, which requires that the signal delay for all

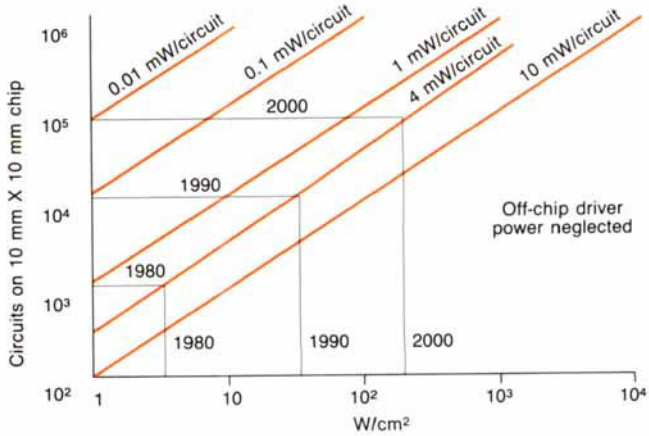

Fig. 7. Power density as a function of chip integration.

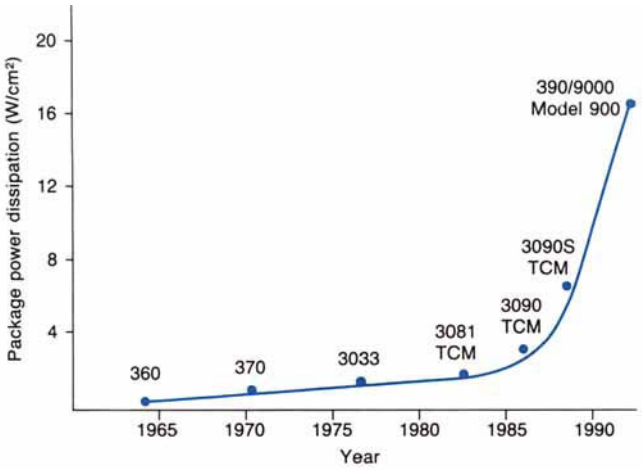

Fig. 8. Ceramic package power dissipation trends in IBM's mainframe systems.

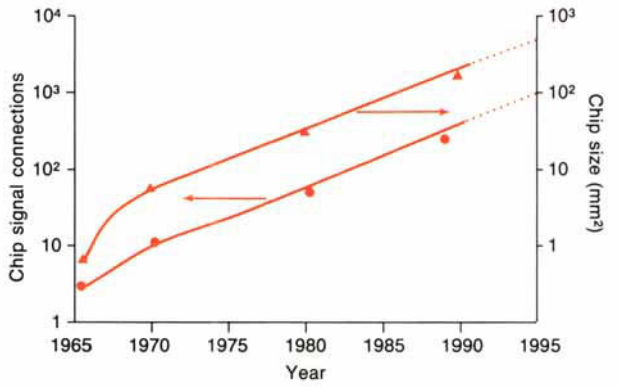

Fig. 9. Evolution and projected increase of chip signal connections and chip sizes.

critical paths in the ceramic package be no more than about 4 ns. Given that light travels 20 cm in 1 ns, only very-high-performance ceramic packages in which all the critical wiring is embedded in ceramics of very low dielectric constant are expected to meet the performance requirements for leading-edge computers. The package contribution to the total cycle time for a number of leading-edge computers is illustrated in Fig. 11 in terms of ceramics and their dielectric constants.

V. Ceramic Packaging Requirements in the 1990s

The general requirements for leading-edge ceramic packages in the 1990s are given in Table II for both high-performance and low-performance systems.

Very-low-performance systems such as consumer electronics will continue in plastic packages, primarily because of cost advantages of plastic packages over ceramic packages. In addition, plastic packages, based on their recent improvements in reliability without hermeticity, will continue to move into low- and mid-range computers.

VI. High-Performance Ceramic Packaging

The thermal conductivity of ceramics for high-performance packaging is assumed to be of little importance. The heat can be removed from the back of the chip without going through the ceramic substrate, as in previous and current ceramic substrate approaches used by leading mainframe manufacturers.[10,11]

The importance of the dielectric constant of the dielectric in providing fast signal propagation was discussed earlier and is illustrated in Fig. 12 for a number of currently available and projected ceramic materials.

The most important property after dielectric constant for high-performance multichip packages is the conductor wiring density. Figure 13 shows the general wiring requirements plotted as a function of gates/chip for a 100-chip module, both in cofired thick-film ceramic technology and polyimide–copper thin-film technology. Figure 13 shows that cofired ceramic wiring layers of the order of 50 to 60 are required for leading-edge semiconductor technologies currently available.[5]

Clearly, the desired substrate metallurgy for cofired metallization is copper because of its high conductivity, low cost, and good electromigration resistance. The need for high-conduction metallurgy such as copper is due to the high power requirements, which are expected to be in excess of 50 W/chip in the early 1990s. Although the power requirements could also be met by gold or silver, the respective cost and

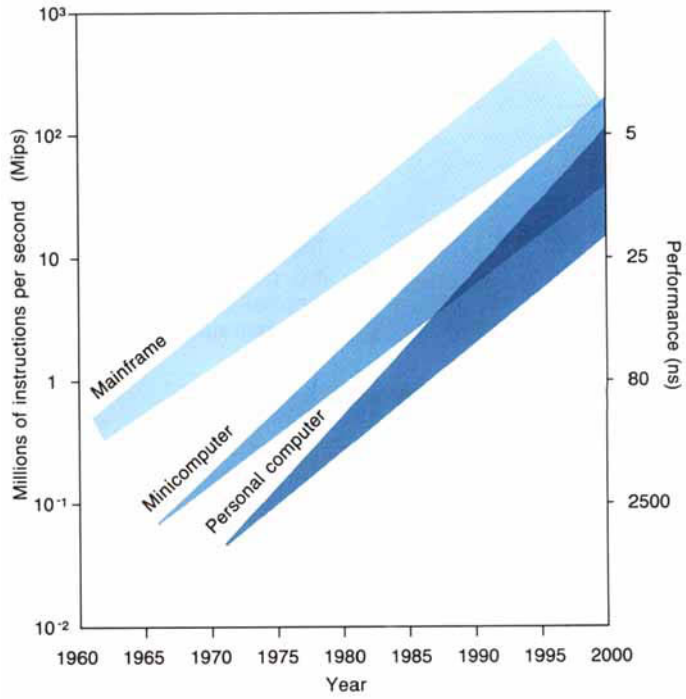

Fig. 10. Performance trends of computers.

reliability concerns favor copper. The requirement for cofired copper of 50 to 60 layers, however, poses the most demanding technology challenges, as discussed later in this paper.

The area solder connection, referred to as controlled collapse chip connection (C-4), between the chip and the substrate has clear advantages over wirebond and TAB, both in providing the number of connections and low inductance of each connection. Rent's rule,[8] which predicts the number of connections as a function of circuits on a chip, demonstrates the need for 500 to 1000 connections for signal alone, clearly favoring the area connection. This connection, however, requires good thermal-expansion match between silicon and the substrate for current substrate systems, and *exact* thermal-expansion match for future systems based on larger silicon chips. The need for expansion match is illustrated in Fig. 14, wherein the fatigue life of the solder connection is plotted as a function of thermal-expansion mismatch between the chip and the substrate for a 6-mm chip size; larger chips clearly require lower mismatch. The projected silicon chip sizes, requiring ceramic substrates with exact thermal-expansion match to silicon, are illustrated in Fig. 9.

The stringent mechanical requirements for cofired multichip ceramic substrates result from a number of different mechanical challenges imposed during substrate fabrication and subsequent use. These requirements range from built-in residual stresses due to mismatches in thermal expansion between copper and ceramic and polyimide and ceramic (deposited on top of the substrate), as well as from surface-attach pin and chip metallizations. IBM's original multilayer substrate, based on alumina, has a tensile strength in excess of 280 MPa (40 000 psi) and a toughness of 3.0 MPa·$m^{1/2}$. Considering the difficulties involved in achieving these levels of properties for a low-temperature ceramic, it is believed that mechanical properties of about 75% of alumina may allow substrate fabrication and use with proper design of material and process technologies.

Potential ceramic substrate materials and their electrical, thermal, and mechanical properties are listed in Table III. Referring to Table II, which indicates the importance by "weight factor" for each of the five properties discussed earlier, glass-ceramics with copper has the best combination of characteristics that meet most of the requirements set forth earlier for a

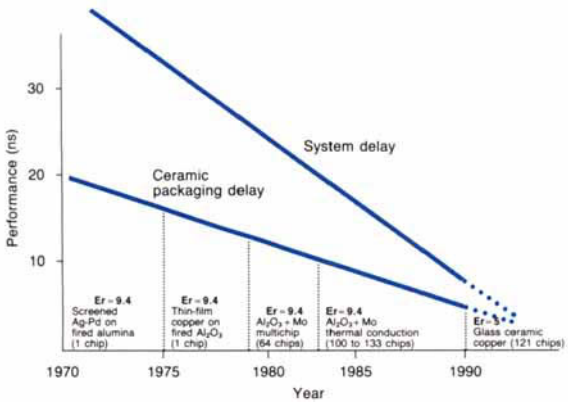

Fig. 11. Ceramic technology evolution and delay for IBM's large computer systems.

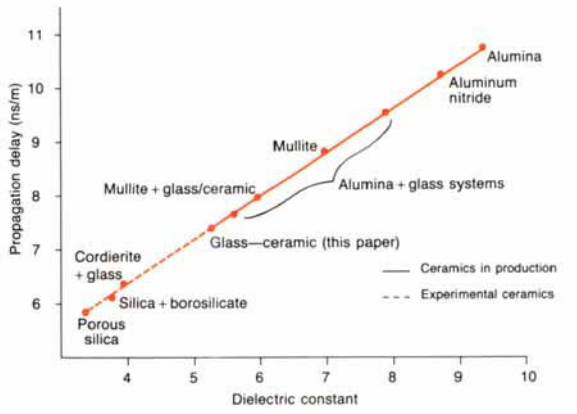

Fig. 12. Propagation delay as a function of dielectric constant of ceramic materials in production.

Table II. Important Characteristics of Ceramic Substrates

High-performance applications			Low-performance applications		
Property	Importance	Weight factor	Property	Importance	Weight factor
Dielectric constant	Highest	5	Low cost	Highest	5
Wiring density	Highest	5	Thermal conductivity	Highest	5
Metallization with copper	Highest	5	Thermal-expansion match to silicon	High	4
Thermal-expansion match to silicon	High	4	Wiring density	Medium	3
Dimensional control	High	4	Mechanical strength	Low	2
Mechanical strength	Medium	2			

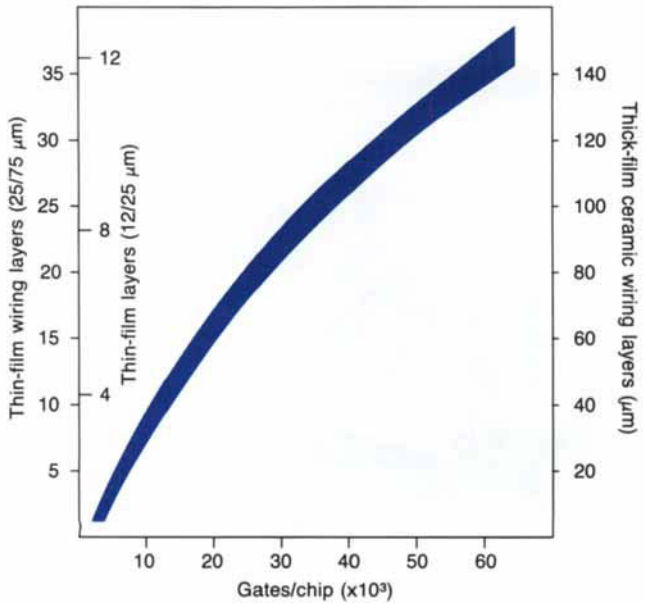

Fig. 13. Wiring needs for mainframe and supercomputers for a 100-chip module.

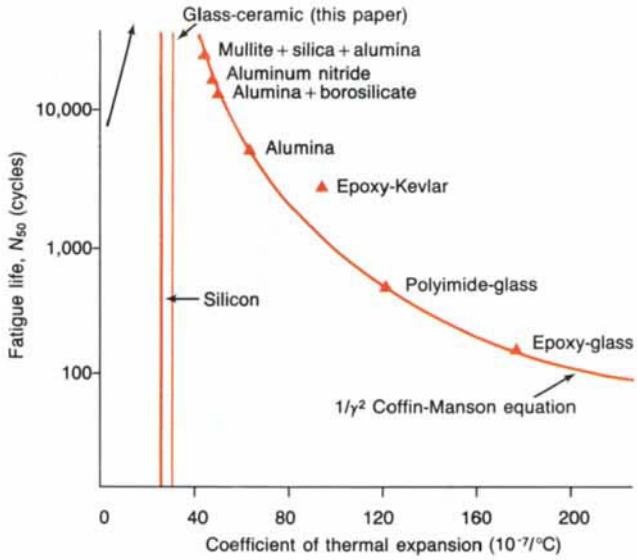

Fig. 14. Solder fatigue life improvement by glass-ceramic substrate.

Table III. Potential Substrate Materials and Their Properties

Ceramic material	Dielectric constant (at 1 MHz)	Strength (MPa)	Coefficient of thermal expansion (20° to 200°C) (10^{-7}/°C)	Thermal conductivity (W/m·K)	Process temperature (°C)
Alumina	9.4	280	65	25	1500
SiC (2% BeO)	42	420	37	270	2000
Si_3N_4	7.0	350	23	33	1600
AlN	8.8	350	42	230	1900
BeO	6.8	250	68	290	2000
Mullite	6.5	200	40	7	1400
Borosilicate glass	4.0	70	30	2	800
Glass-ceramic	5.0	210	30	5	950

leading-edge multichip module, as illustrated in Fig. 15. The figure of merit in Fig. 15 is assumed to be the sum of all the factors listed in Table II.

Borosilicate glass makes a good thin-film material[12] but falls short of the mechanical requirements for the substrate. Mullite can be cofired only with tungsten, nickel, or molybdenum. Beryllia, silicon carbide, and aluminum nitride have outstanding thermal properties and, therefore, make good candidates for low-end applications, if they can be fabricated at low cost. Since these have too high a dielectric constant and cannot be metallized with copper, they are not suitable for very-high-performance applications. A crystallizable glass that can be nucleated, sintered, and then completely crystallized to high mechanical strength seems to meet most of the requirements set forth in Table II for a high-performance ceramic. Low dielectric constant, thermal-expansion match to silicon, and a steep viscosity–temperature relation required for good greensheet binder burn-off has led to use of a glass-ceramic in the MgO–Al_2O_3–SiO_2 system, as discussed later. Glasses added to ceramics, referred to as glass + ceramics, can also be considered as good candidates for high-performance packaging, as reported by a number of Japanese companies, for example, Fujitsu.

VII. Low-Performance Ceramic Packaging

The cross-hatched bars in Fig. 15 represent the potential ceramic materials for low-cost applications, such as workstations. Alumina—because of its maturity and, hence, low cost—will continue to be used for all computer applications except for the very top and the very bottom ends of the product line, which require the highest performance and lowest cost, respectively. The alumina substrate cannot meet either extreme. The state-of-the-art in alumina multilayer substrate technology has recently been announced for use in high-performance, midrange computers. This substrate is 127 mm in size, and interconnects 121 complex logic and array chips by its 63 layers of molybdenum metallization (Fig. 16). Mullite multilayer ceramic technology, shown in Fig. 17, is being

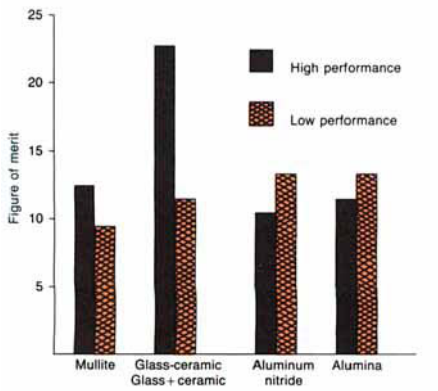

Fig. 15. Relative comparison of ceramic substrate materials.

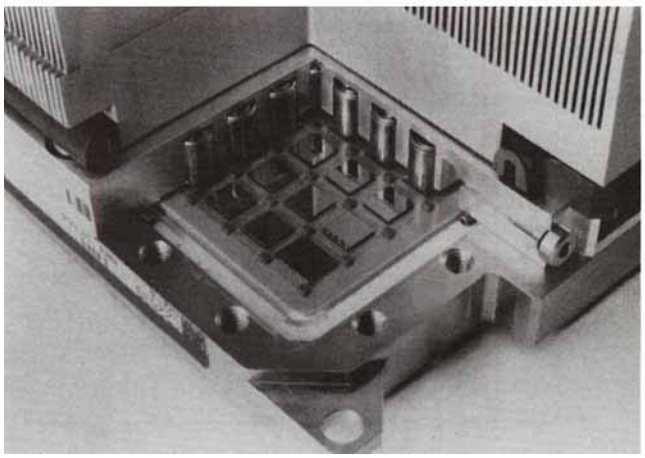

Fig. 16. State-of-the-art 63-layer alumina multilayer ceramic substrate (courtesy of IBM).

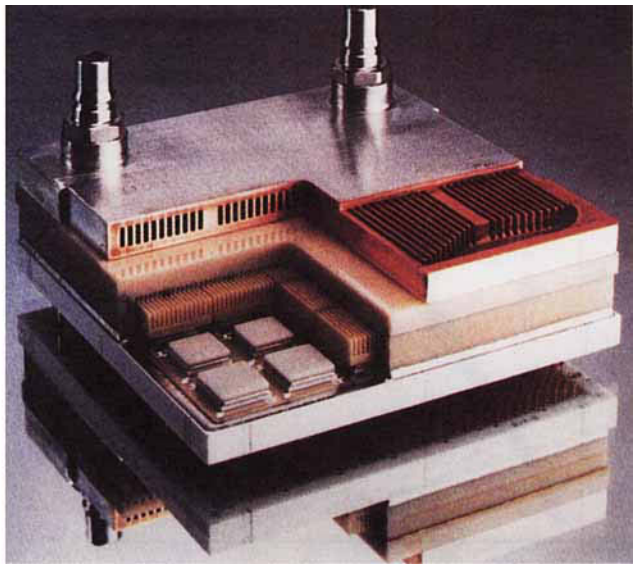

Fig. 17. State-of-the-art mullite multilayer ceramic package (courtesy of Hitachi).

increasingly used and is expected to be more widely used in the future.

Aluminum nitride technology is well documented in a number of recent publications and, therefore, will not be discussed in this paper. Aluminum nitride in Fig. 15 is comparable in its figure of merit to alumina, and will be preferable to alumina if its cost decreases significantly.

VIII. Status of Glass-Ceramic/Copper Technology

The material and process challenges in developing glass-ceramic/copper substrates relative to the goals discussed earlier for the final electrical, thermal, mechanical, and dimensional control properties were formidable. First, the glass-ceramic material with the required properties had to be developed and characterized (see Fig. 18, which shows the basic multilayer process). Second, powder, paste, and greensheet technologies had to be engineered to allow compatibility between greensheet and paste, resulting in the required dimensional stability in the prefired state. Third, shrinkage matching of glass—as it densifies and crystallizes, with copper, as it densifies—had to be developed, with interfacial integrity prior to sintering. Fourth, a process or materials technology had to be discovered that permitted dozens of layers of copper to be metallized with glass-ceramic, with complete greensheet and paste–organic removal without the oxidation of the copper. The process needed to result in bonding of the copper to the glass-ceramic, despite the large mismatch in their thermal expansions. Fifth, the dimensional control properties had to be achieved, to allow several dozens of layers, with as many as two million vias, each less than 100 μm, to be aligned through all the layers and yet provide a planar substrate base for polyimide–copper surface wiring. The best previous multilayer technology achieved a linear shrinkage control of about $\pm 0.15\%$, around a nominal value of 17.2%. The requirements for the next generation of substrates with polyimide–copper thin-film wiring are clearly tighter than with alumina.

	Alumina/Mo	Glass-Ceramic/Cu
Raw materials	Al_2O_3+10% glass	100% glass powder
↓		
Slurry	Acid–base	Acid–acid
↓		
Greensheet	Continuous cast	Continuous cast
↓		
Punching	Mechanical	Mechanical
↓		
Paste screening	Mo paste	Cu paste
↓		
Inspection	Vias+lines	Vias+lines
↓		
Stacking and lamination	Automated	Automated
↓		
Sintering	Controlled H_2	Controlled steam atmosphere
↓		
Substrate machining	Seal flange	Top and bottom surface finishing and seal flange
↓		
Final ceramic	Al_2O_3+glass	100% glass-ceramic

Fig. 18. Glass-ceramic/copper substrate process compared with alumina–molybdenum multilayer ceramic process.

(1) Glass-Ceramic Material

In developing glass-ceramic material with the required properties, a number of major crystalline systems have been considered, as shown in Table IV.[13] The stoichiometric compositions of none of these materials either sinter well or sinter at a temperature compatible with copper. The only materials that have the potential to meet the dielectric

constant and thermal-expansion requirements are cordierite, spodumene, and celsian. Of these three, cordierite has the lowest dielectric constant. However, pure cordierite neither sinters below 1000°C nor has the proper thermal-expansion coefficient. Original cordierite glass-ceramics from Corning, Inc. (Corning, NY),[14] have many useful applications but are unsuitable for substrates because the thermal-expansion coefficient is too low, the processing temperature too high, and they crystallize prematurely when formed into greensheets from powders and sintered. However, given the good dielectric properties of this material, it was believed that the composition in the system $MgO–Al_2O_3–SiO_2$ could be modified to overcome these problems.

The glass that has been developed to form this glass-ceramic (in 1977) has the composition SiO_2 (50 to 55 wt%), Al_2O_3 (18 to 23 wt%), MgO (18 to 25 wt%), and P_2O_5 and B_2O_3 (0 to 3 wt%).[15] In this composition range, the MgO content is greater, and Al_2O_3 lower, than in stoichiometric cordierite. Experiments have shown that the excess MgO content aids in sintering and increases the thermal-expansion coefficient from the undesirable lower value of pure cordierite. Analysis of the crystallized compositions by X-ray diffraction shows no residual glass, indicating that the excess MgO goes into solid solution in the cordierite. Even though B_2O_3 and P_2O_5 are used in small quantities, their effects are significant. The discovery of their role in densification and α-cordierite phase formation has been essential in achieving glass-ceramic substrate goals. B_2O_3 raises the crystallization temperature, thus allowing densification of glass prior to crystallization, while lowering the viscosity, allowing complete densification of the sintered powder. The P_2O_5, similar to the B_2O_3, encourages the formation of low-expansion α-cordierite. Through the formation of α-cordierite as the primary phase and small amounts of clinoenstatite, an exact thermal-expansion match to single-crystal silicon was achieved. In fact, a wide range of thermal-expansion coefficients is possible, as shown in Fig. 19, allowing the glass-ceramics to be tailored for silicon as well as GaAs.

Japanese computer manufacturers have generally chosen glass + ceramic systems for multilayered ceramic substrates. However, these systems typically consist of a glass added to crystalline ceramic rather than the glass-ceramic which crystallizes during the substrate firing cycle.[16–18] Some of these systems are shown in Table V. The most sophisticated of these types of glass + ceramic substrates in production is illustrated in Fig. 20. This substrate is made of 61 layers of borosilicate + alumina and copper conductor, 245 mm in size; it supports 144 high-performance bipolar chips.

In forming the desirable glass-ceramic substrate material, a unique sequence of events must occur in forming a useful substrate. As stated earlier, it is important that the sintering of glass does not occur below 800°C and that complete densification occurs first, followed by crystallization below the melting point of copper, preferably around 900° to 950°C, as shown in Fig. 21. Any densification of glass below 800°C is undesirable because of carbon removal, which takes place efficiently above about 800°C from greensheet and paste organics, as discussed later. The complete carbon removal and copper metallization processes are the two most important challenges imposed on the glass material selection, requiring certain viscosity–temperature relations for the glass, as illustrated in Fig. 22.

The reference line in Fig. 22 assumes no sintering of glass at 800°C, corresponding to a glass viscosity of 10^{12} P, and a glass with this viscosity–temperature relation can be considered, therefore, a desirable candidate for

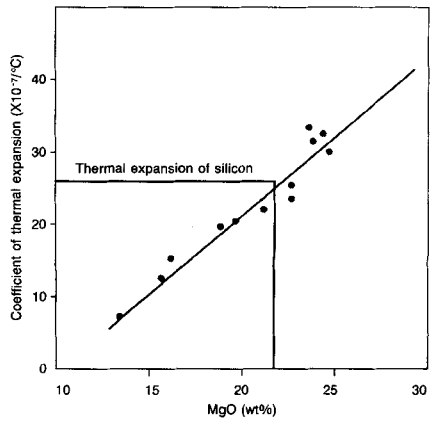

Fig. 19. Thermal-expansion tailorability in the $MgO–Al_2O_3–SiO_2$ glass-ceramic system.

Table IV. Crystalline Phases Considered for Glass-Ceramic*

Composition	Crystal phase	Coefficient of thermal expansion (20° to 200°C) (10^{-6}/°C)
$Li_2O·Al_2O_3·SiO_2$	β-Eucryptite	−10.0
$Al_2O_3·TiO_2$	Aluminum titanate	0.5
$2MgO·2Al_2O_3·5SiO_2$	Cordierite	1.0
$Li_2O·Al_2O_3·4SiO_2$	β-Spodumene	0.9
$BaO·Al_2O_3·2SiO_2$	Celsian	2.7
$CaO·Al_2O_3·2SiO_2$	Anorthite	4.5
$MgO·SiO_2$	Clinoenstatite	7.8
$MgO·TiO_2$	Magnesium titanate	7.9
$2MgO·SiO_2$	Forsterite	9.4
$CaO·SiO_2$	Wollastonite	9.4
$Li_2O·2SiO_2$	Lithium disilicate	11.0
SiO_2	Quartz	11.2
SiO_2	Cristobalite	12.5
SiO_2	Tridymite	17.5

*Reference 13.

Table V. Composition and Properties of Glass + Ceramic

Glass + ceramic	Dielectric constant	Coefficient of thermal expansion (10^{-7}/°C)	Conductor
$PbO+B_2O_3+SiO_2+CaO+(Al_2O_3)$	7.5	42	Au, Ag+Pd
$MgO+Al_2O_3+SiO_2+B_2O_3+(SiO_2)$	5.0	30–79	Au, Ag, Ag+Pd
$B_2O_3+SiO_2+(Al_2O_3)$	5.6	40	Cu
$CaO+Al_2O_3+SiO_2$	7.7	55	Ag, Ag+Pd
$B_2O_3+SiO_2+Al_2O_3+2MgO·SiO_2$	6.5	60	Ag+Pd
$Li_2O+SiO_2+MgO+Al_2O_3+SiO_2+(Al_2O_3)$	7.3	59	Au, Ni, Ag+Pd
$Glass+Al_2O_3+CaZrO_3$	8.0	79	Au, Ag

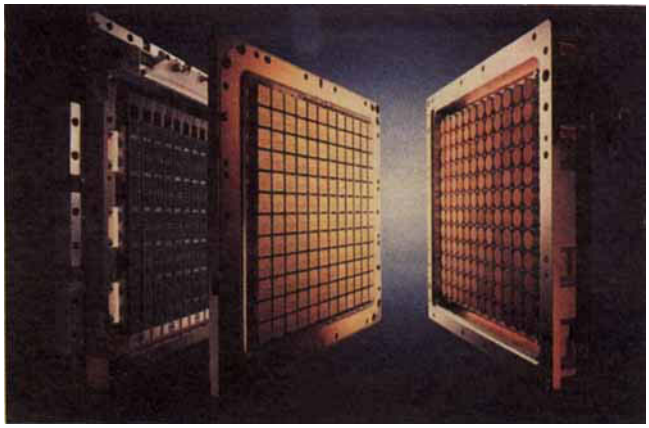

Fig. 20. State-of-the-art glass + ceramic substrate (courtesy of Fujitsu).

cofiring with copper. The glass in the $MgO–Al_2O_3–SiO_2$ system, falling to the right of the reference glass in Fig. 22, makes it an excellent candidate for binder burn-off. Contrary to this, borosilicate glasses, which have a shallow viscosity–temperature relation (annealing point of 500°C and softening point of 750°C), are less likely to achieve the required carbon removal.

(2) Copper Powder and Paste Technology

Cofired multilayer glass-ceramic substrates with copper offer unique challenges in thick-film technology. The challenges can be classified in four general categories.

(1) A copper powder with physical properties suitable for fabrication of fine-line, thick-film dimensions by screening and via fill must be developed.

(2) A copper thick-film system that is compatible with the organic system of the glass greensheet binder must be developed.

(3) A compatible copper powder and its sintering behavior with a glass-ceramic resulting in good shrinkage control and interfacial integrity between copper and ceramic must be developed.

(4) Good electrical conductivity of sintered copper must be achieved.

The sintering temperature of the glass-ceramic (see Fig. 23) is about 850°C while that of copper is about 600°C, indicating large shrinkage differences both in the total shrinkage s, and the temperature T. The total mismatch can result in undesirable topography of the features on the ceramic surface, as shown in Fig. 23(A). In addition, the mismatches may result in distortion of the substrate, which is undesirable for automated processing of the substrates, where repeatability of feature positions is very important. The mismatch in the onset of sintering temperature between glass-ceramic and copper, shown as ΔT in Fig. 23, can result in loss of adhesion between the conductor and the ceramic, as shown in Fig. 23(B), resulting in loss of mechanical integrity. If copper were to sinter at a higher temperature than the glass-ceramic, viscous tearing would be expected during the sintering. For these reasons, both glass-ceramic and copper materials must be tailored such that both the temperature and total shrinkage mismatches are modified to be approximately the same, to eliminate the problems described.

Extensive work was conducted to modify the shrinkage of the copper powders. The modification of the shrinkage had to be accomplished without any significant increase in the resistivity of the sintered copper conductor. Modifications explored included the following.

(1) Copper particles were coated with an organic barrier material that prevented diffusion between the particles, thus inhibiting the driving force

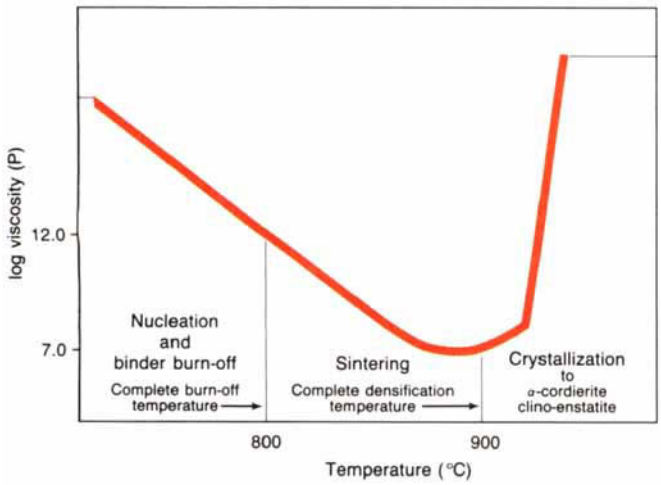

Fig. 21. Glass-ceramic process sequence in cordierite glass.

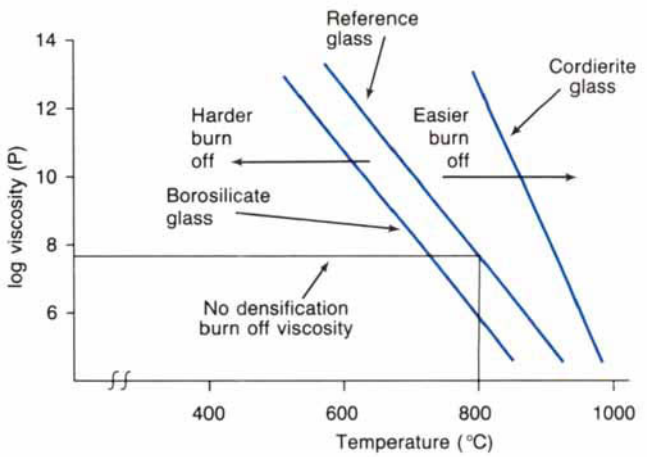

Fig. 22. Viscosity–temperature relation for borosilicate and cordierite glasses.

for sintering. This barrier was later removed at the desired temperature. Some examples of these materials are poly(vinyl formvar), poly(vinyl alcohol), poly(vinyl butyral), epoxies, urethanes, and siloxanes.

(2) Copper particles were interspersed with metals or their oxides, which acted as grain-boundary inhibitors and thus delayed the sintering to higher temperatures. Some examples of these materials are chromium, copper, molybdenum, aluminum, gold, nickel, and palladium.

(3) Binder Removal and Carbon Oxidation

One of the key challenges in sintering glass-ceramic/copper substrate is the need to completely remove all solvents, binders, and plasticizers. Any residual carbon that may form during binder decomposition, if left in the substrate, would adversely affect the dielectric constant of the ceramic. Figure 24 shows the dielectric constant of glass-ceramic as a function of residual carbon content. As the data indicate, it is necessary to reduce the residual carbon content to a very low level, well below 300 ppm. This requirement presented one of the most important obstacles in the early development of glass-ceramic/copper technology in 1978. The formation of residual carbon from greensheet organics adsorbed onto active glassy surfaces is illustrated in Fig. 25, wherein the degradation of pure polymer and the same polymer adsorbed onto the glassy surface is plotted as a function of temperature. The removal of the last traces of carbon from the greensheet extends to almost 800°C, requiring the glass to stay open without densification to this temperature.

Table VI shows the various approaches that were explored in the late 1970s to reduce the residual carbon content to the desired low levels and yet maintain copper in the unoxidized, high-conductance sintered state.

The only process that is successful in removing organics to below 300 ppm is based on the thermodynamics of oxidation of carbon and reduction of copper oxide. At 750°C, an oxygen partial pressure of 10^{-10} atm is slightly reducing to cuprous oxide and 10 orders of magnitude above the level needed for carbon oxidation, as illustrated in Fig. 26 in which the thermodynamics of Cu-O-C are presented. There are many ways to achieve an oxygen partial pressure of 10^{-10} atm at 750°C. Combinations of air, oxygen, nitrogen, hydrogen, carbon dioxide, and steam have been evaluated to meet this requirement. A patented pioneering process[19] requires a mixture of hydrogen in steam for the best carbon reaction rate.[10] With this atmosphere, the residual carbon of a 60-layer substrate was reduced to less than 300 ppm in a few hours. All other gas systems required days to weeks. Figure 26 shows the carbon oxidation and copper reduction window for the hydrogen/steam atmosphere as a function of temperature. The hydrogen/steam atmosphere not only results in a good reaction rate for carbon oxidation but also provides a wide processing window over a large temperature range for the particular glass-ceramic/copper system chosen.

The final glass-ceramic/copper substrate properties achieved as a result of all the technology developments discussed to this point are summarized and compared with an existing alumina/molybdenum substrate in Table VII. This technology will be used for top-of-the-line computers. The top surface of the substrate, illustrating 121 high-performance chips and discrete decoupling capacitors around each corner of each silicon chip, is shown in Fig. 27.

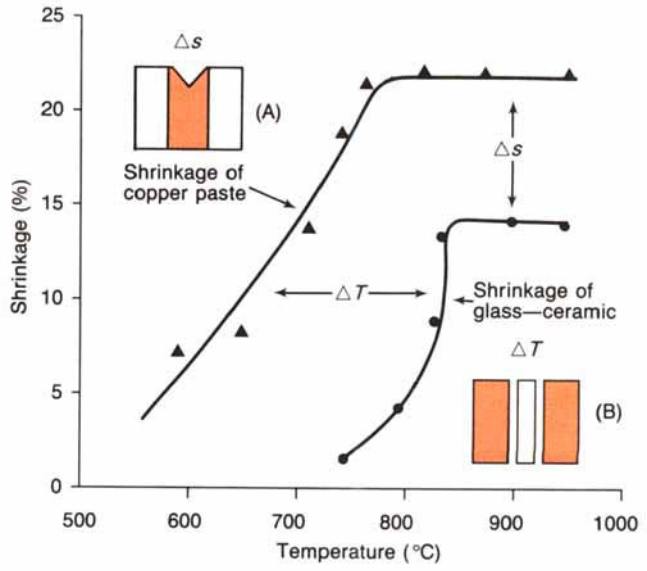

Fig. 23. Typical shrinkage mismatch between glass (glass-ceramic) and copper.

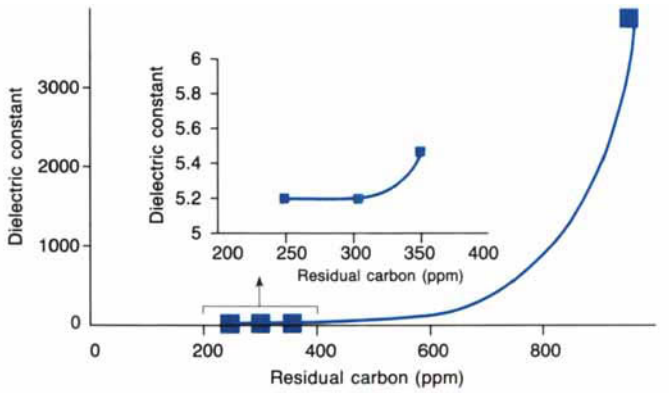

Fig. 24. Dielectric constant as a function of residual carbon in glass-ceramic.

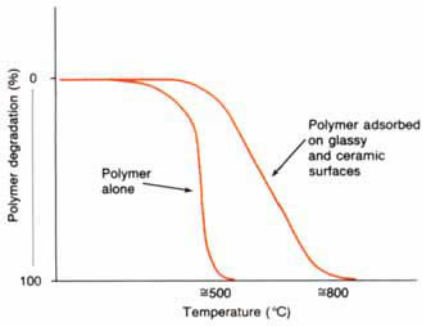

Fig. 25. Polymer degradation in neutral atmosphere.

Table VI. Methods Evaluated for Organics Removal

Unzippable polymers in greensheets
Alternating cycles for oxidation/ reduction of copper
Oxygen/nitrogen atmospheres
CO/CO_2 atmospheres
H_2/CO_2 atmospheres
Dry and wet H_2 atmospheres
Dry and wet forming gas atmospheres
Pure steam atmospheres
Catalysts
Plasma treatment of glass powders

IX. Future Ceramic Packaging

Alumina has been the workhorse of the microelectronics industry since the days of the first transistor. It has been and will continue to be used in a number of substrate forms, from dual-in-line packages with 64 I/Os to very sophisticated multilayer packages with thousands of connections. However, this material system poses limitations for high-performance applications in the 1990s because of its (1) high dielectric constant (9.4), (2) high thermal expansion coefficient (60×10^{-7}/°C), (3) metallizability only with high-resistance metals such as molybdenum and tungsten, and (4) good but inadequate dimensional control, limiting the number of layers. These limitations are largely overcome with glass-ceramics and glass + ceramics which are currently in production and expected to be used in almost all large general-purpose computers and supercomputers in the early 1990s. It is also evident that glass + ceramics will be enhanced by a competitive technology that is referred to as thin-film technology based on the use of thin polymers of dielectric constant 3.0, thickness of 10 to 20 μm, metallized with 25-μm-wide pure thin-film copper of intrinsic electrical conductivity. Thus, it appears that signal distribution in the critical paths of the system will be carried in thin film, whereas the noncritical signal distribution and power distribution will be performed in cofired ceramics. In addition, the cofired ceramic will act as a base for thermal-expansion control of the substrate and will provide thousands of I/O connections. An alternative technology path is the continued use of ceramics with very low dielectric constant and with fine-line copper wiring.

Figure 28 illustrates the use of composites to achieve a dielectric constant below 5.0.[5] There are very few ways in which low dielectric constant (less than 5.0) can be accomplished. Composites of borosilicate, silica, or cordierite, with or without porosity or polymer, can yield low-dielectric-constant ceramics. A number of materials summarized in Table VIII have been reported.[20–23]

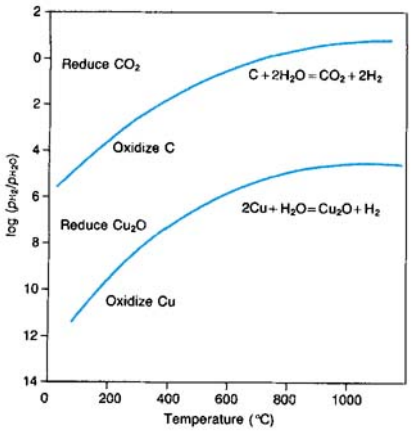

Fig. 26. Thermodynamics of Cu-O-C system.

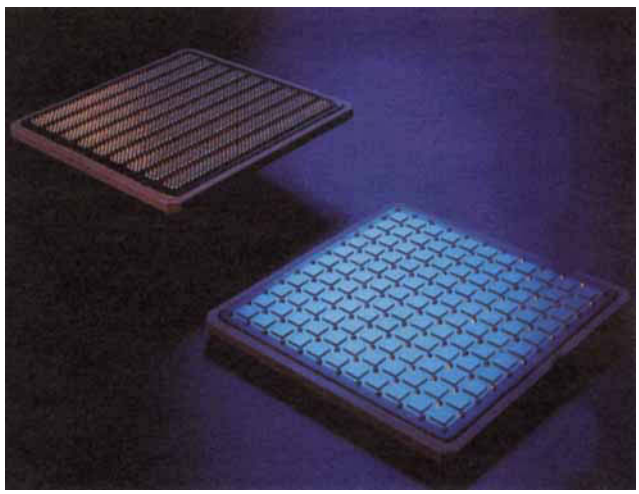

Fig. 27. State-of-the-art glass-ceramic substrate (courtesy of IBM).

Table VII. Glass-Ceramic/Copper Substrate Characteristics

Substrate characteristic	IBM System 3090 with alumina–molybdenum	IBM System 390/ES9000 with glass-ceramic/copper
Size (mm)	110.5×117.5	127.5×127.5
Layers	45	63
Number of vias (total)	4.7×10^5	2×10^6
Wiring density (cm/cm^2)	450	844
Line width (mm)	100	75
Via diameter (mm)	125	90 and 100
Dielectric constant	9.4	5.0
Resistivity ($\mu\Omega\cdot$cm)	11	3.5
Coefficient of thermal expansion (RT to 200°C) (10^{-7}/°C)	60	30
Shrinkage control (%)	±0.15	±0.1

X. Summary

Figure 29 depicts the evolution and projection of ceramic packaging described in this article. Although the future for high-performance ceramic packaging seems clear with current glass-ceramic and glass + ceramic technologies and projected low-dielectric-constant composite ceramics, it is not obvious how ceramics will be used beyond aluminum nitride, alumina, and mullite for low-performance applications where low cost is the primary requirement, and a cost improvement of about 20% is required from year to year.

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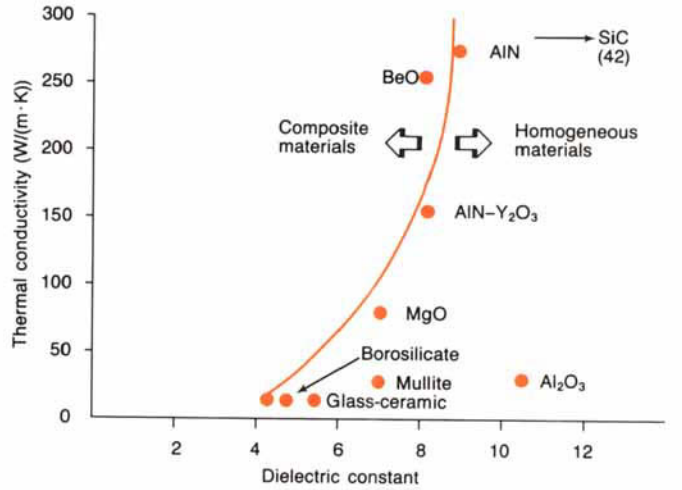

Fig. 28. Thermal conductivity versus dielectric constant for ceramics.

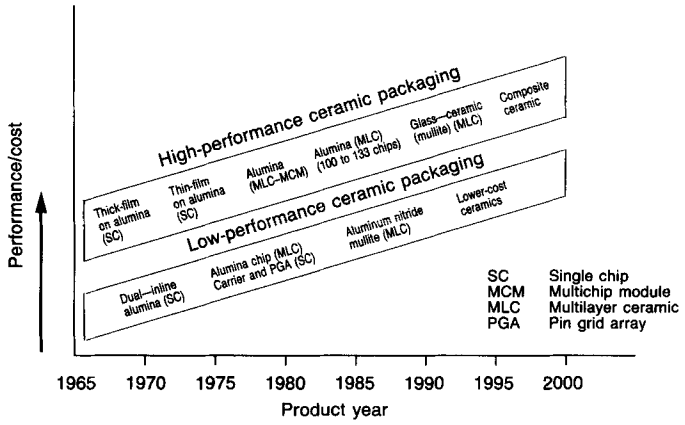

Fig. 29. Ceramic packaging evolution.

Table VIII. Very-Low-Dielectric-Constant Ceramic Substrate Materials

Ceramic composite	Dielectric constant	Coefficient of thermal expansion (10^{-7}/°C)	Strength (kg/cm^2)
Quartz+borosilicate glass +cordierite+porosity	3.4	32	850
Quartz+borosilicate glass +cordierite	4.4	32	1600
Silica+borosilicate	3.9	19	1400
Cordierite+borosilicate	5.0	79	1500

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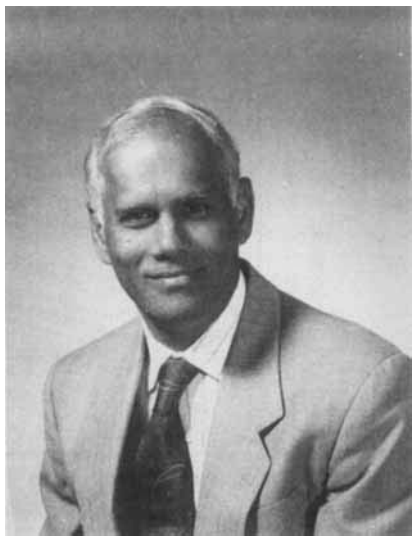

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