Generalized Steady-State VSC MTDC Model for Sequential AC/DC Power Flow Algorithms

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***Abstract*—In this paper, a steady-state multi-terminal voltage source converter high voltage direct current (VSC MTDC) model is introduced. The proposed approach is extended to include multiple AC and DC grids with arbitrary topologies. The DC grids can thereby interconnect arbitrary buses in one or more non-synchronized AC systems. The converter equations are derived in their most general format and correctly define all set-points with respect to the system bus instead of the converter or filter bus, which is often done to simplify calculations. The paper introduces a mathematical model to include the converter limits and discusses how the equations change when a transformerless operation is considered or when the converter filter is omitted. An AC/VSC MTDC power flow is implemented using MATPOWER to show the validity of the generalized power flow model.**

***Index Terms*—HVDC converters, HVDC transmission, load flow analysis, VSC HVDC.**

I. Introduction

THE ever growing need for transmission capacity in current day power systems has led to an increased interest in transmission based on voltage source converter high voltage direct current (VSC HVDC) technology. One of the advantages of the VSC technology over conventional current source commutated (CSC) HVDC is the relatively straightforward extension to multi-terminal (MTDC) configurations. The VSC HVDC offers significant advantages over traditional AC grid reinforcements and an operation in an MTDC grid could facilitate the integration of renewable energy sources in the future. Recently, plans have even been suggested to build offshore grids based on DC technology or a DC supergrid to connect the growing share of renewable energy sources [1], [2].

One of the outstanding research issues is the steady-state behavior of these integrated AC/DC systems. In the past, numerous efforts have been spent on the joint solution of integrated AC/DC systems based on the traditional CSC technology [3]–[7]. Generally, the solution methods presented for CSC HVDC systems can be subdivided in unified and sequential methods. In unified methods, the AC and DC system equations are solved together [6], whereas in the sequential method, the AC and DC system equations are solved sequentially [7]. The biggest advantage of the sequential methods over their unified counterparts is that the sequential methods can be implemented relatively easily as an extension to existing AC power flow programs, whereas a unified implementation requires an alteration of existing AC power flow algorithms.

A lot of research has been conducted on the operation of CSC HVDC in a multi-terminal set-up, but the inherent technical specifics of the CSC technology make a multi-terminal operation impractical if more than three converters are involved, thus impeding an application of the CSC technology in large scale, meshed DC grids. In a parallel operation, a power reversal is complex as it requires mechanical switching. A different voltage to ground at the different converters results in a complex insulation and grounding scheme in a series operation, hampering an extension of the scheme. VSC HVDC has much better prospects for an operation in a MTDC system than CSC HVDC technology: The DC side of the converter behaves as a current source, which makes a power reversal at any terminal a straightforward control set-point change.

The general distinction between unified and sequential methods is also applicable to integrated AC/VSC MTDC power flow algorithms, but due to the technical specifics of the VSC, the power flow models of CSC and VSC MTDC systems differ. Whereas the past research has been focussing on the power-flow solutions for CSC MTDC systems, a general approach for VSC HVDC systems is missing. Most VSC HVDC power flow models available in literature or embedded in commercial software are limited to two-terminal VSC HVDC systems or are not general enough, which can impede their extension to a general VSC MTDC model [8]. In [9] and [10], the analysis is limited to a two-terminal VSC HVDC system. In [11], converter losses are neglected, DC variables are not accessible and the power flow set-points are defined at the converter bus instead of the system bus. This simplifies the calculations, but is not in accordance with current practice. In [12], losses are included but the VSC is only modeled to a limited extent while converter limits are not included.

The main contribution of this paper is the development of a detailed, general steady-state VSC MTDC model for a sequential AC/DC power flow algorithm. The method elaborates further on the general algorithm presented in [13], now including a representation of converter transformers, filters and operation limits as a part of the converter model. Additionally, the model can represent multiple DC grids interconnecting different buses within one AC system or connecting buses from

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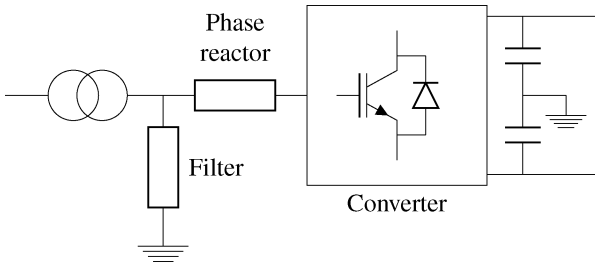

Fig. 1. VSC HVDC converter station.

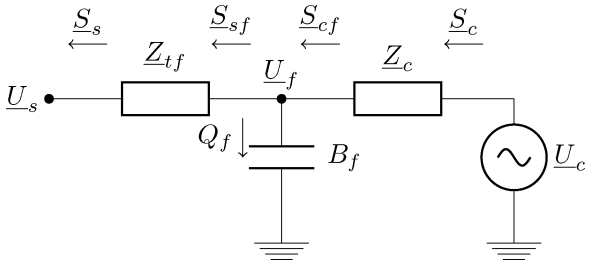

Fig. 2. Equivalent single phase power flow model of a converter station connected to the AC grid.

various AC systems. The paper also discusses the modifications to be made when a transformer- or filterless operation is considered. Section II discusses the power flow model of the converter and that of the DC grid. The sequential AC/DC power flow implementation is discussed in Section III. Finally, Section IV discusses simulation results by combining the proposed methodology with the open source Matlab toolbox, MATPOWER [14].

II. Power Flow Modeling

A. Converter Model

In its most general format, a VSC HVDC converter (Fig. 1) can be represented by a controllable voltage source $\underline{U}_c = U_c \angle \delta_c$ behind the phase reactor with a complex impedance $\underline{Z}_c = R_c + \jmath X_c$. As shown in Fig. 2, the phase reactor is connected to the susceptance B_f which forms a part of the low pass filter. The filter bus is connected to the AC grid through a transformer, represented by its impedance $\underline{Z}_{tf} = R_{tf} + \jmath X_{tf}$. The equations for the power flowing to the AC network can thus be written as

$$P_s = -U_s^2 G_{tf} + U_s U_f [G_{tf} \cos(\delta_s - \delta_f) + B_{tf} \sin(\delta_s - \delta_f)] \quad (1)$$

$$Q_s = U_s^2 B_{tf} + U_s U_f [G_{tf} \sin(\delta_s - \delta_f) - B_{tf} \cos(\delta_s - \delta_f)] \quad (2)$$

with $\underline{U}_s = U_s \angle \delta_s$ and $\underline{U}_f = U_f \angle \delta_f$, respectively, the complex grid side and filter bus voltage. The equations at the converter side can be written as

$$P_c = U_c^2 G_c - U_f U_c [G_c \cos(\delta_f - \delta_c) - B_c \sin(\delta_f - \delta_c)] \quad (3)$$

$$Q_c = -U_c^2 B_c + U_f U_c [G_c \sin(\delta_f - \delta_c) + B_c \cos(\delta_f - \delta_c)]. \quad (4)$$

Assuming the AC filters to be lossless, the filter power reduces to its reactive part

$$Q_f = -U_f^2 B_f \quad (5)$$

while the expressions for the filter side complex power flowing through the transformer are written as

$$P_{sf} = U_f^2 G_{tf} - U_f U_s [G_{tf} \cos(\delta_s - \delta_f) - B_{tf} \sin(\delta_s - \delta_f)] \quad (6)$$

$$Q_{sf} = -U_f^2 B_{tf} + U_f U_s [G_{tf} \sin(\delta_s - \delta_f) + B_{tf} \cos(\delta_s - \delta_f)] \quad (7)$$

and those flowing through the phase reactor side are

$$P_{cf} = -U_f^2 G_c + U_f U_c [G_c \cos(\delta_f - \delta_c) + B_c \sin(\delta_f - \delta_c)] \quad (8)$$

$$Q_{cf} = U_f^2 B_c + U_f U_c [G_c \sin(\delta_f - \delta_c) - B_c \cos(\delta_f - \delta_c)]. \quad (9)$$

In the absence of low pass filters or with the filters omitted, the phase reactor and the converter transformer can be lumped together [13], eliminating the dependence on the complex filter bus voltage in (1)–(4). Similarly, if transformerless designs are considered, the filter bus and the AC grid bus coincide, hence simplifying the equations.

A VSC HVDC converter can independently control the active and reactive power injection with respect to the AC system. In the power flow algorithm presented in this paper, the active power injection is modeled in two different ways:

1) *Constant P*: The converter has a constant active power injection P_s into the AC grid.
2) *Constant U_{dc}*: The algorithm adapts the active power injection P_s to obtain a constant DC bus voltage U_{dc}.

The actual steady-state behavior of a two-terminal VSC HVDC link can be modeled in a power flow algorithm by one constant P converter and one constant U_{dc} converter. The active power injection of the latter is unknown prior to the power flow and depend on the losses in the VSC HVDC system. This constant U_{dc} converter is referred to as the DC slack converter, due to its similarity to the slack bus in AC power flow algorithms.

This two-terminal representation can be extended to model x different MTDC systems with a total of y DC converters. With one DC slack bus per MTDC system , this results in $y - x$ converters controlling their active power output (constant P). The x remaining DC slack converters, one per MTDC system, adjust their power to account for the DC system losses and to keep up the voltage of the DC grids. Alternatively, a voltage droop can be implemented to study the effect of distributing the DC voltage control function on the power flows [15].

The ability of the converter to independently control the reactive power results in two different representations in the power flow algorithm:

1) *Constant Q*: The converter has a constant reactive power injection Q_s into the AC grid.
2) *Constant U*: The converter adapts the reactive power injection to obtain a constant AC bus voltage magnitude U_s.

As discussed in [8], commercial software models include the converter up to the filter bus while the filter and transformer have to be added separately. The power and voltage set-points are then defined with respect to the filter bus or the converter bus [11] instead of the system bus. Although these alternative methods are easier to implement, they do not comply with current day practices in VSC HVDC systems.

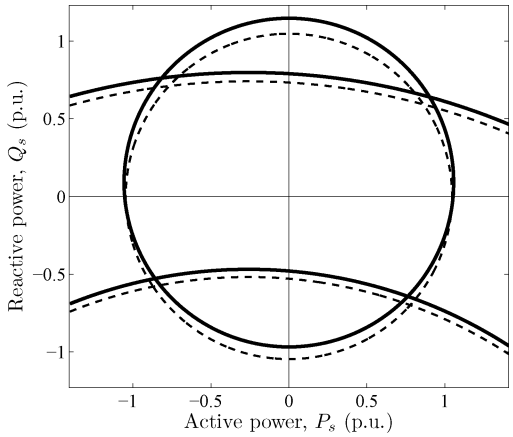

Fig. 3. PQ-capability chart—Converter station current and voltage limits (with $I_{c_{\max}} = 1.05$ p.u., $U_{c_{\min}} = 0.85$ p.u., and $U_{c_{\max}} = 1.2$ p.u.).

The model developed in this paper also includes the converter station losses using a generalized loss formula with the converter losses quadratically dependent on the converter current I_c [16]:

$$P_{loss} = a + b \cdot I_c + c \cdot I_c^2 \tag{10}$$

with the per unit converter current magnitude I_c given by

$$I_c = \frac{\sqrt{P_c^2 + Q_c^2}}{\sqrt{3} U_c}. \tag{11}$$

This aggregated loss model has been derived for the Södra Länken project, a VSC HVDC link with a rating of 600 *MW* and a DC voltage of ± 300 kV. The model includes the losses in the different components of a VSC HVDC converter substation. The loss components are further discussed in [16]. The loss data in this paper has been scaled down to the appropriate MVA base.

B. VSC HVDC Converter Limits

To ensure an overall safe operation of the converter station, the steady state working point must be situated within the PQ-capability chart of the converter, depicted in Fig. 3. The full lines include the effect of the filters, the dotted lines neglect the filters. The full circle forms the converter current limit. The arcs depict the upper and lower converter voltage limits.

With the apparent power injection written as

$$\underline{S}_s = \underline{U}_s \underline{I}_s^* \tag{12}$$

the system bus voltage equation, which is equal to

$$\underline{U}_s = \underline{U}_f - \underline{Z}_{tf} \underline{I}_s \tag{13}$$

can be reformulated and substituted in the equation for the current at the filter bus, yielding

$$\underline{I}_s = \underline{I}_c - \frac{\underline{U}_s + \underline{Z}_{tf} \underline{I}_s}{\underline{Z}_f}. \tag{14}$$

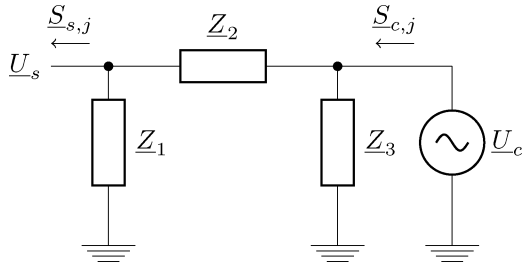

Fig. 4. Pi-equivalent scheme of a VSC HVDC converter.

Rewriting this equation in terms of the current $\underline{I}_s$ and substituting it in (12) results in a closed expression of the converter current limit

$$\underline{S}_s = -U_s^2 \left(\frac{1}{\underline{Z}_f^* + \underline{Z}_{tf}^*} \right) + \underline{U}_s \underline{I}_{cm}^* \left(\frac{\underline{Z}_f^*}{\underline{Z}_f^* + \underline{Z}_{tf}^*} \right) \tag{15}$$

with $\underline{I}_{cm}$ the phasor of the maximum current

$$\underline{I}_{cm} = I_{c_{\max}} \angle \delta_{I_c}. \tag{16}$$

With the filters omitted, (15) simplifies to

$$\underline{S}_s = \underline{U}_s \underline{I}_{cm}^*. \tag{17}$$

As shown in Fig. 3, the circular current limit from (17) slightly scales and shifts to a new center point as a result of the filter inclusion. The filter capacitance thus leads to a small bias in Q-axis direction [17].

In VSC systems that use pulse width modulation (PWM), the modulation factor has an upper and lower limit, respectively, to avoid overmodulation and the reappearance of harmonics. In [18], the lower reactive power limit is a constant at -0.5 p.u. With the modular multilevel converter (MMC) technology, the reactive power is limited by the current in the lagging region [19]. The lower voltage limit can thus be omitted in this case.

These limits are implemented as limits on the converter voltage. The voltage limits can be obtained by applying a $Y - \Delta$ transformation to the equivalent model from Fig. 2. This is shown in Fig. 4, with the equivalent impedances $\underline{Z}_1$, $\underline{Z}_2$, and $\underline{Z}_3$, respectively

$$\underline{Z}_1 = \frac{\underline{Z}_{tf}\underline{Z}_c + \underline{Z}_c\underline{Z}_f + \underline{Z}_f\underline{Z}_{tf}}{\underline{Z}_c} \tag{18}$$

$$\underline{Z}_2 = \frac{\underline{Z}_{tf}\underline{Z}_c + \underline{Z}_c\underline{Z}_f + \underline{Z}_f\underline{Z}_{tf}}{\underline{Z}_f} \tag{19}$$

$$\underline{Z}_3 = \frac{\underline{Z}_{tf}\underline{Z}_c + \underline{Z}_c\underline{Z}_f + \underline{Z}_f\underline{Z}_{tf}}{\underline{Z}_{tf}}. \tag{20}$$

Rewriting $\underline{I}_s^*$ in (12) in terms of the currents $\underline{I}_1$ and $\underline{I}_2$, through $\underline{Z}_1$ and $\underline{Z}_2$ results in

$$\underline{S}_s = \underline{U}_s \left(\underline{I}_2^* - \underline{I}_1^* \right) \tag{21}$$

$$= \underline{U}_s \left(\frac{\underline{U}_c^* - \underline{U}_s^*}{\underline{Z}_2^*} - \frac{\underline{U}_s^*}{\underline{Z}_1^*} \right). \tag{22}$$

Rewriting this equation in terms of admittances results in the expression for $\underline{S}_s$ in terms of a converter voltage limit

$$\underline{S}_s = -U_s^2\,(\underline{Y}_1^* + \underline{Y}_2^*) + \underline{U}_s\,\underline{U}_{cm}^*\,\underline{Y}_2^* \tag{23}$$

with $\underline{U}_{cm}$ the phasor of the minimum or maximum converter voltage $U_{c_{\min}}$ or $U_{c_{\max}}$. $U_{c_{\max}}$ is the maximum voltage that can be generated by the converter while avoiding overmodulation. The lower voltage limit $U_{c_{\min}}$ in Fig. 3 has been chosen to comply with the minimum reactive power limit from [18]. This limit can be omitted in an MMC or when no minimum reactive power limit is imposed on the converter.

Similar expressions can be found by applying l'Hôpital's rule to (18)–(20) for $\underline{Z}_f \to \infty$ or $\underline{Z}_{tf} \to 0$ when the filter or transformer are not included. The expression without the filter hence simplifies to

$$\underline{S}_s = -U_s^2\left(\frac{1}{\underline{Z}_{tf}^* + \underline{Z}_c^*}\right) + \frac{\underline{U}_s\underline{U}_{cm}^*}{\underline{Z}_{tf}^* + \underline{Z}_c^*}. \tag{24}$$

Similar to the current limit, the inclusion of the filter shifts the voltage limit circles from (17) to a new center point, while their radii slightly change.

C. DC Grid Model

The power flows in the DC grid can be obtained in a way similar to a conventional AC power flow. The current injected at a DC node i can be written as the current flowing to the other $n-1$ nodes in the network:

$$I_{dc_i} = \sum_{\substack{j=1\\ j\neq i}}^{n} Y_{dc_{ij}} \cdot (U_{dc_i} - U_{dc_j}) \tag{25}$$

with $Y_{dc_{ij}}$ equal to $1/R_{dc_{ij}}$. Combining all currents injected in an n bus DC network results in

$$\boldsymbol{I_{dc}} = \mathsf{Y}_{\mathsf{dc}}\boldsymbol{U_{dc}} \tag{26}$$

with $\boldsymbol{I_{dc}} = [I_{dc_1}, I_{dc_2} \ldots I_{dc_k}, 0 \ldots 0]^T$ the DC current vector with $n-k$ zero elements due to DC buses without a power injection and converter outages, $\boldsymbol{U_{dc}} = [U_{dc_1}, U_{dc_2} \ldots U_{dc_n}]^T$ the DC voltage vector, and Y_{dc} the DC bus matrix. When line outages are taken into account, the DC bus matrix needs to be updated accordingly. When x DC grids are considered, all DC bus matrices $\mathsf{Y}_{\mathsf{dc}j}$ of the different DC grids are combined in one single sparse band matrix Y_{dc}:

$$\mathsf{Y}_{\mathsf{dc}} = \begin{bmatrix} \mathsf{Y}_{\mathsf{dc}1} & & \\ & \ddots & \\ & & \mathsf{Y}_{\mathsf{dc}x} \end{bmatrix}. \tag{27}$$

For a monopolar DC grid, the active power injected in node i can be written as

$$P_{dc_i} = U_{dc_i} I_{dc_i}, \forall i \leq k \tag{28}$$

whereas for a monopolar, symmetrically grounded DC grid, the power injections become

$$P_{dc_i} = 2U_{dc_i} I_{dc_i}, \forall i \leq k. \tag{29}$$

A similar expressions holds for a bipolar configuration. The current injections $\boldsymbol{I_{dc}}$ are not known prior to the power flow solution for the DC grid, whereas the active power injections $\boldsymbol{P_{dc}}$ are known for all buses except for the DC slack buses as a results of the AC power flow. Combining (26) and (29) and assuming a monopolar, symmetrically grounded DC grid

$$P_{dc_i} = 2\,U_{dc_i} \sum_{\substack{j=1\\ j\neq i}}^{n} Y_{dc_{ij}} \cdot (U_{dc_i} - U_{dc_j}). \tag{30}$$

This system of nonlinear equations can either be solved with a Newton-Raphson (NR) method, as derived in the next section, or rewritten to include the unknown DC slack buses power equations directly [20].

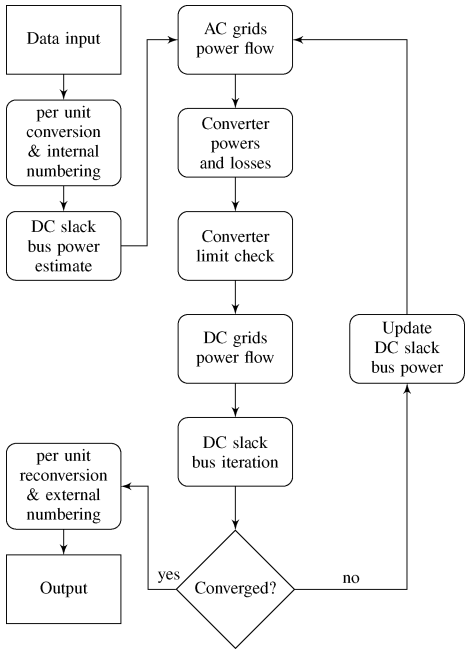

Fig. 5. Flow chart of the sequential VSC AC/DC power flow algorithm.

III. AC/DC Power Flow

Fig. 5 shows the flow chart of the sequential power flow algorithm. The algorithm starts with a per unit conversion and an internal bus renumbering from [8] which facilitates the inclusion of multiple DC grids, line and converter outages, as well as DC buses without an AC grid connection. In order to simplify notation, it is assumed in the remainder of the paper that interconnected AC and DC buses have the same bus number. For convenience, the analysis will be confined to one AC grid and one DC grid with n buses of which k have a connection to the AC grids. The method can easily be extended to include multiple AC and DC grids.

A. AC Network Power Flow

The power flow equations for bus i in the AC grid can be written as

$$P_i(\boldsymbol{U},\boldsymbol{\delta}) = U_i \sum_{j=1}^{p} U_j \left[G_{ij}\cos(\delta_i - \delta_j) + B_{ij}\sin(\delta_i - \delta_j)\right] \tag{31}$$

$$Q_i(\boldsymbol{U},\boldsymbol{\delta}) = U_i \sum_{j=1}^{p} U_j \left[G_{ij}\sin(\delta_i - \delta_j) - B_{ij}\cos(\delta_i - \delta_j)\right]. \tag{32}$$

The nonlinear set of power flow equations for all AC buses can be solved using a NR power flow, with the converter power injections $\boldsymbol{P_s}$ and $\boldsymbol{Q_s}$ included in the power mismatch vectors $\boldsymbol{\Delta P}^{(k)}$ and $\boldsymbol{\Delta Q}^{(k)}$ as negative loads. The power mismatch vectors can be rewritten as

$$\Delta P_i^{(j)} = P_i^{gen} - (P_i^{dem} - P_{s_i}) - P_i(\boldsymbol{U}^{(j)}, \boldsymbol{\delta}^{(j)}) \quad (33)$$

$$\Delta Q_i^{(j)} = Q_i^{gen} - (Q_i^{dem} - Q_{s_i}) - Q_i(\boldsymbol{U}^{(j)}, \boldsymbol{\delta}^{(j)}). \quad (34)$$

Converters in V-control are represented as dummy AC generators and their AC buses are changed from PQ-nodes to PV-nodes. The active power injections of the slack buses are changed in order to control the DC grid voltages. Without lack of generality, the first converter of the DC grid is assumed to operate as DC slack bus to simplify notation. As a first estimate to initiate the iteration, the DC system is assumed to be lossless, hence

$$P_{s_1}^{(0)} = -\sum_{j=2}^{k} P_{s_j}. \quad (35)$$

For subsequent iterations, the solution from the previous iteration is used for $P_{s_1}^{(k)}$.

B. Converter Calculations

With the AC grid voltages $\underline{\boldsymbol{U_s}}$ and power injection at the AC grid side $\underline{\boldsymbol{S_s}}$ known, the converter side voltage and currents can be calculated. With (12)–(13), the filter bus voltage $\underline{U}_f$ can be written as

$$\underline{U}_{f_i} = \underline{U}_{s_i} + \underline{Z}_{tf_i} \cdot \left(\frac{\underline{S}_{s_i}^*}{\underline{U}_{s_i}^*}\right) \quad \forall i < k. \quad (36)$$

The converter current $\underline{I}_c$ can be extracted from (14), with $\underline{I}_s$ rewritten using (12)

$$\underline{I}_{c_i} = \frac{\underline{U}_{s_i}}{\underline{Z}_{f_i}} + \left(\frac{\underline{S}_{s_i}^*}{\underline{U}_{s_i}^*}\right) \cdot \frac{\underline{Z}_{f_i} + \underline{Z}_{tf_i}}{\underline{Z}_{f_i}} \quad \forall i < k \quad (37)$$

which can be substituted in (10) to calculate the converter losses. The converter voltage $\underline{U}_c$ can be calculated as

$$\underline{U}_{c_i} = \underline{U}_{f_i} + \underline{Z}_{c_i}\underline{I}_{c_i}, \quad \forall i < k. \quad (38)$$

With all quantities on the AC side known, the DC grid's injected power becomes

$$P_{dc_i} = -P_{c,i} - P_{loss_i}, \quad \forall i < k. \quad (39)$$

C. Converter Limit Check

If the converter is operating outside its limits, the power injections are adapted to ensure a safe operation. In general, a weighting factor can be used to give a higher priority to active or reactive power. In this paper, priority is given to active power. The grid injected power P_s can remain unaltered if intersections with the capability chart can be found. If, on the contrary, P_s is too large, the active power is limited to its maximum value and the reactive power is adapted accordingly.

The current and voltage limits in (15) and (23) are circles in the PQ-plane. Hence, with P_s known, the two reactive power limits imposed by the current limit can be calculated as

$$Q_s = Q_0 \pm \sqrt{r^2 - (P_s - P_0)^2} \quad (40)$$

with the circle's center $\underline{S}_0 = P_0 + \jmath Q_0$ and a radius r. The center point and radius of the current limit are given by

$$\underline{S}_0 = -U_s^2 \left(\frac{1}{\underline{Z}_f^* + \underline{Z}_{tf}^*}\right) \quad (41)$$

$$r = U_s I_{c_{\max}} \left|\frac{\underline{Z}_f^*}{\underline{Z}_f^* + \underline{Z}_{tf}^*}\right|. \quad (42)$$

The two solutions refer to the upper and lower reactive power limit imposed by the current limit.

Similarly, the voltage limits center point and radius are given by

$$\underline{S}_0 = -U_s^2 (\underline{Y}_1^* + \underline{Y}_2^*) \quad (43)$$

$$r = U_s U_{cm} Y_2. \quad (44)$$

Replacing U_{cm} in (44) with $U_{c_{\min}}$ or $U_{c_{\max}}$ and substituting (43)–(44) in (40) gives an analytical expression for the lower and upper voltage limit reactive power. Only the solution with the positive sign is of interest, as the other solution refers to the lower crossing point with voltage limit circle.

The limit checks can be implemented similarly to those of generator limits: If a converter is operating outside its active power limits, the set-points must be reduced to their maximum values. Additionally, it must be ascertained that the DC slack buses are working within their bounds. Apart from the active power violations, the converter's reactive power must stay within limits. When a Q-limit is hit, the most stringent reactive power limit imposes the new converter operation point. If the converter is operating in V-control, the voltage controlled bus also has to be changed to a PQ-bus. If one or more converters hit their limits, the most stringent one is enforced and the convergence flag is reset.

Contrary to generator limits, which are often approximated by constant values, the Q-limits of the converters are updated every iteration due to changing grid conditions. As a consequence, it was found that simply enforcing the limits during each iteration proved unsatisfactory. Therefore, the set-points are only updated when the incremental change in apparent power exceeds a minimum value of $1\mathrm{e}-2\,\mathrm{p.u.}$ Alternatively, it was also found that checking the limits after every iteration and only updating their value every three iterations led to convergence as well. The algorithm should be properly tuned to achieve good convergence.

D. DC Network Power Flow

Alternatively to the approach proposed in [20], the non-linear DC network equations from (30) can be solved with an NR method

$$\left(\boldsymbol{U_{dc}}\frac{\partial \boldsymbol{P_{dc}}}{\partial \boldsymbol{U_{dc}}}\right)^{(j)} \cdot \frac{\boldsymbol{\Delta U_{dc}}^{(j)}}{\boldsymbol{U_{dc}}} = \boldsymbol{\Delta P_{dc}}^{(j)}. \quad (45)$$

The power mismatch vector $\boldsymbol{\Delta P_{dc}}^{(j)}$ is given by

$$\Delta P_{dc_i}^{(j)} = \begin{cases} P_{dc_i}^{(k)} - P_{dc_i}(\boldsymbol{U_{dc}}^{(j)}) & \forall i \le k \\ -P_{dc_i}(\boldsymbol{U_{dc}}^{(j)}) & \forall k \le i \le n \end{cases} \quad (46)$$

with superscripts (j) and (k), respectively, referring to the inner NR iteration and the outer AC/DC power flow iteration. The terms of the Jacobian are

$$\left(U_{dc_j}\frac{\partial P_{dc_i}}{\partial U_{dc_j}}\right)^{(j)} = -2U_{dc_i}^{(j)}Y_{dc_{ij}}U_{dc_j}^{(j)} \tag{47}$$

$$\left(U_{dc_i}\frac{\partial P_{dc_i}}{\partial U_{dc_i}}\right)^{(j)} = P_{dc_i}^{(j)} + 2\,{U_{dc_i}^{(j)}}^2\sum_{\substack{j=1\\ j\neq i}}^{n} Y_{dc_{ij}}. \tag{48}$$

The equations and terms corresponding to the slack bus are removed since its voltage is known prior to the DC network power flow. After convergence, the voltages on all DC buses are known, while the slack bus power injection can be found using (30). The DC line currents can be obtained by premultiplying the DC bus voltage vector $\boldsymbol{U_{dc}}$ by the system branch admittance matrices $\mathsf{Y_{dcf}}$ and $\mathsf{Y_{dct}}$, which are obtained as a byproduct of the construction of the DC bus matrix $\mathsf{Y_{dc}}$.

E. DC Slack Bus Iteration

The AC bus active power injection P_{s_1} of the DC slack bus is calculated from its DC power P_{dc_1} by accounting for the converter losses. As the converter losses from (10) depend on the yet unknown converter current, an additional iteration is needed to calculate the active power injection P_{s_1}. During this iteration, the grid side voltage $\underline{U}_{s_1}$ and reactive power injection Q_{s_1} are kept constant. Omitting the subscript 1 to simplify notations, the value of P_c is iteratively updated according to

$$P_c^{(i)} = -P_{dc}^{(k)} - P_{loss}^{(i)} \tag{49}$$

with the superscripts (i) and (k), respectively, referring to the DC slack bus iteration and the outer AC/DC power flow iteration. The converter losses P_{loss} are calculated from (10)–(11). The previous AC network power flow results are used to provide an initial estimate for the converter losses $P_{loss}^{(0)}$.

An NR iteration based on $\underline{U}_c$ and $\underline{U}_f$ as variables is internally used to update the converter state in order to obtain a new value for $P_{loss}^{(i)}$

$$\begin{bmatrix} \left(\frac{\partial P_c}{\partial \delta_c}\right)^{(j)} & \left(\frac{\partial P_c}{\partial \delta_f}\right)^{(j)} & \left(U_c\frac{\partial P_c}{\partial U_c}\right)^{(j)} & \left(U_f\frac{\partial P_c}{\partial U_f}\right)^{(j)} \\ 0 & \left(\frac{\partial Q_s}{\partial \delta_f}\right)^{(j)} & 0 & \left(U_f\frac{\partial Q_s}{\partial U_f}\right)^{(j)} \\ \left(\frac{\partial F_1}{\partial \delta_c}\right)^{(j)} & \left(\frac{\partial F_1}{\partial \delta_f}\right)^{(j)} & \left(U_c\frac{\partial F_1}{\partial U_c}\right)^{(j)} & \left(U_f\frac{\partial F_1}{\partial U_f}\right)^{(j)} \\ \left(\frac{\partial F_2}{\partial \delta_c}\right)^{(j)} & \left(\frac{\partial F_2}{\partial \delta_f}\right)^{(j)} & \left(U_c\frac{\partial F_2}{\partial U_c}\right)^{(j)} & \left(U_f\frac{\partial F_2}{\partial U_f}\right)^{(j)} \end{bmatrix} \cdot \begin{bmatrix} \Delta\delta_c^{(j)} \\ \Delta\delta_f^{(j)} \\ \frac{\Delta U_c}{U_c}(j) \\ \frac{\Delta U_f}{U_f}(j) \end{bmatrix} = \begin{bmatrix} \Delta P_c^{(j)} \\ \Delta Q_s^{(j)} \\ -F_1^{(j)} \\ -F_2^{(j)} \end{bmatrix} \tag{50}$$

with the functions F_1 and F_2 given by

$$F_1(\underline{U}_s, \underline{U}_c, \underline{U}_f) = P_{cf} - P_{sf} \tag{51}$$

$$F_2(\underline{U}_s, \underline{U}_c, \underline{U}_f) = Q_{cf} - Q_{sf} - Q_f. \tag{52}$$

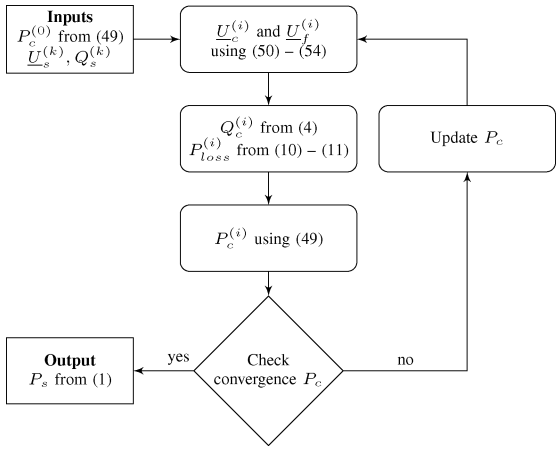

Fig. 6. DC slack bus iteration flow chart.

The power mismatches $\Delta P_c^{(j)}$ and $\Delta Q_s^{(j)}$ can be calculated by, respectively, using (3) and (2) and are given by

$$\Delta P_c^{(j)} = P_c^{(i)} - P_c(\underline{U}_f^{(j)}, \underline{U}_c^{(j)}) \tag{53}$$

$$\Delta Q_s^{(j)} = Q_s^{(k)} - Q_s(\underline{U}_s^{(k)}, \underline{U}_f^{(j)}), \tag{54}$$

The superscript (j) refers to the inner NR iteration. The elements of the Jacobian matrix can be analytically derived from (1)–(9) directly and by substitution in the expressions for F_1 and F_2. The results are given in the Appendix. Fig. 6 shows the flow chart of the DC slack bus iteration.

In absence of the transformer, the active and reactive power injections can be rewritten in terms of $\underline{U}_s$ and $\underline{U}_c$ as

$$P_s = -U_s^2 G_c + U_s U_c[G_c\cos(\delta_s - \delta_c) + B_c\sin(\delta_s - \delta_c)] \tag{55}$$

$$Q_s = U_s^2 B_{cf} + U_s U_c[G_c\sin(\delta_s - \delta_c) - B_c\cos(\delta_s - \delta_c)] \tag{56}$$

with $B_c + B_f$ abbreviated as B_{cf}. By rewriting Q_s, the Jacobian matrix simplifies to a 2×2 structure retaining $\Delta\delta_c$ and $\Delta U_c/U_c$ as unknowns and the derivates related to the P_c and Q_s equations as Jacobian elements

$$\begin{bmatrix} \left(\frac{\partial P_c}{\partial \delta_c}\right)^{(j)} & \left(U_c\frac{\partial P_c}{\partial U_c}\right)^{(j)} \\ \left(\frac{\partial Q_s}{\partial \delta_c}\right)^{(j)} & \left(U_c\frac{\partial Q_s}{\partial U_c}\right)^{(j)} \end{bmatrix} \cdot \begin{bmatrix} \Delta\delta_c^{(j)} \\ \frac{\Delta U_c}{U_c}(j) \end{bmatrix} = \begin{bmatrix} \Delta P_c^{(j)} \\ \Delta Q_s^{(j)} \end{bmatrix} \tag{57}$$

with $(\partial P_c/\partial\delta_c)^{(j)}$ and $(U_c(\partial P_c/\partial U_c))^{(j)}$ given by the expressions in the Appendix and the other elements of the reduced Jacobian matrix given by

$$\left(\frac{\partial Q_s}{\partial \delta_c}\right)^{(j)} = -P_s^{(j)} - {U_s^{(k)}}^2 G_c \tag{58}$$

$$\left(U_c\frac{\partial Q_s}{\partial U_c}\right)^{(j)} = Q_s^{(j)} - {U_s^{(k)}}^2 B_{cf} \tag{59}$$

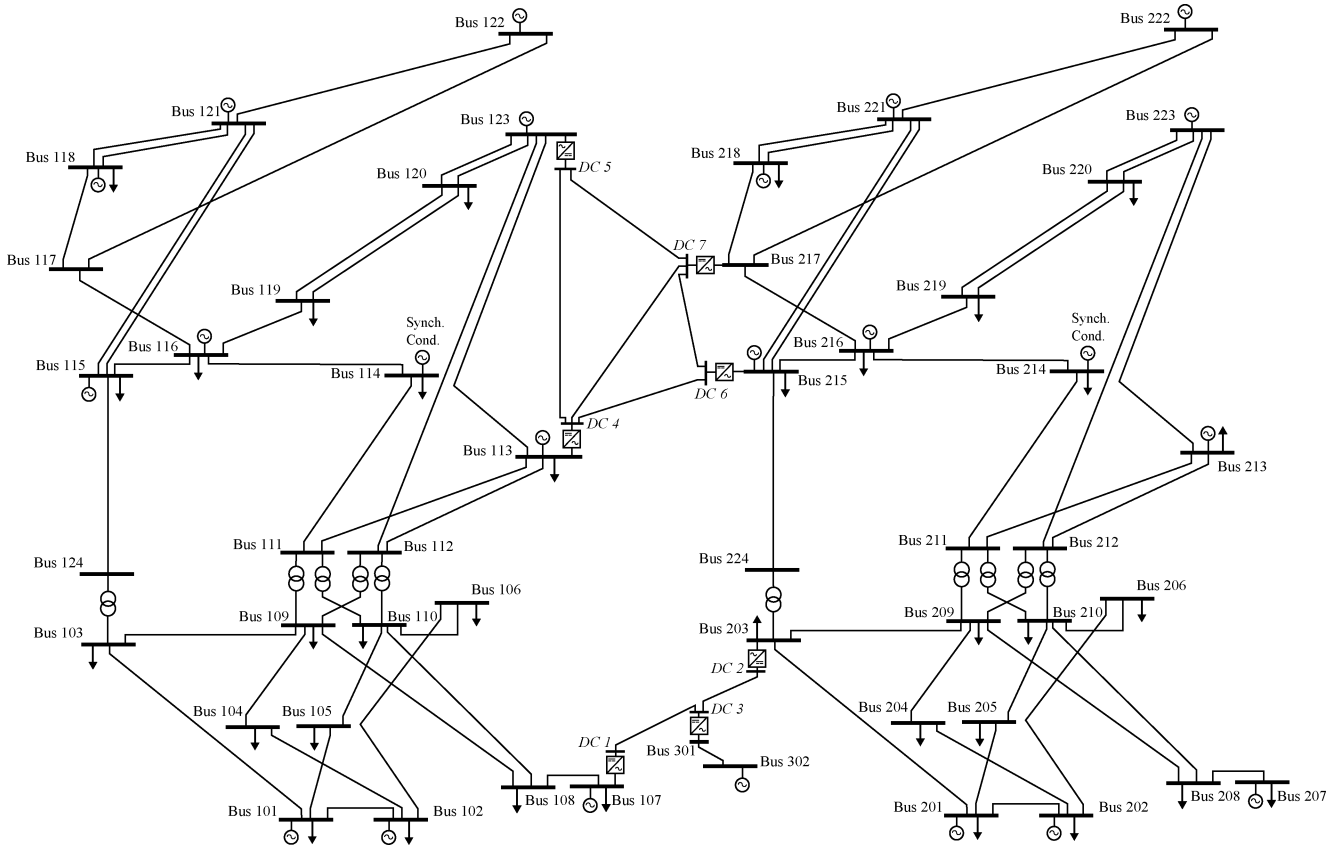

Fig. 7. Modified two-area RTS-96 system with 2 MTDC systems.

with P_s, Q_s from (55)–(56) and P_c, Q_c from (3)–(4) with $\underline{U}_f$ replaced by $\underline{U}_s$. In absence of the converter filters, the equations can be reduced to the forms derived in [13].

When multiple DC grids and slack buses are present, all Jacobian matrices are combined and solved simultaneously.

IV. Simulation Results

This section presents simulation results of the proposed AC/DC power flow algorithm implemented in the open-source Matlab toolbox, MATPOWER [14]. In the case of commercial closed-source AC power flow software, the model has to be integrated with the coding level and not at the end-user level, hence making the implementation less evident.

In this implementation, a tolerance of $1\mathrm{e}-8$ p.u. was used for the AC and DC networks power flow, DC slack bus iteration and the overall iteration loop. Results are presented on a modified version of the IEEE Two Area RTS-96 (MRTS) network [21]. A single-line diagram of the MRTS network is shown in Fig. 7. In this MRTS network, the three interconnections between the two areas have been replaced by MTDC systems: In the 138-kV system, line 107-203 has been replaced by a 3-terminal 150-kV MTDC system connecting the two asynchronous systems with a 150-MW offshore wind farm (buses 301 and 302). In the 345-kV system, lines 113-215 and 123-217 have been replaced by a 4-terminal 300-kV MTDC system. The parameters of the DC systems can be found in Table I. The 3-terminal DC system between buses 107 and 203 represents a filterless MMC VSC MTDC system, the 4-terminal MTDC scheme includes low-pass filters and represents a 2-level PWM VSC MTDC system. The three sequentially solved AC networks operate asynchronously, with reference (slack) buses at 113, 213, and 302. A generator (U100), producing 80 MW, at bus 107 and a generator (U76), producing 76 MW, at bus 201 have been disabled and replaced by the production of 150 MW in bus 302. The active power injections of the 4-terminal MTDC grid converters closely resemble the line flows between the different zones in the original two-area MRTS network. All but one converters are set to reactive power control, working at unity power factor. Tables II and III summarize the AC and DC powers and voltages of the VSC converters connected to the 2 MTDC grids.

TABLE I
VSC Converter Data

Converter parameters		Rating & Converter loss data				
		No.	1, 2	3	4, 6	5, 7
X_{tr} *(p.u.)*	0.1121	P_{dc} *(MW)*	100	200	200	100
R_{tr} *(p.u.)*	0.0015	$\pm V_{dc}$ *(kV)*	150	150	300	300
B_f *(p.u.)*	0.0887[a]	a *(MW)*	1.103	2.206	1.103	2.206
X_c *(p.u.)*	0.16428	b *(kV)*	0.887	0.887	1.800	1.800
R_c *(p.u.)*	0.0001	c_{rec} *(Ω)*	2.885	1.442	5.94	11.88
		c_{inv} *(Ω)*	4.371	2.185	9	18

[a] Only included for converters 4 – 7.

TABLE II
POWER FLOW SOLUTION—MTDC GRID 1

Converter	1	2	3
Control	Slack - Q	P - V	P - Q
P_s *(MW)*	66.84	75.00	-150.00
Q_s *(MVAr)*	0.00	5.86	0.00
U_s *(p.u.)*	1.025	1.000	1.050
δ_s *(deg)*	-8.93	-4.88	-0.08
P_c *(MW)*	66.91	75.09	-149.67
Q_c *(MVAr)*	11.75	21.50	56.40
U_c *(p.u.)*	1.042	1.038	1.120
δ_c *(deg)*	1.04	6.63	-20.73
P_{loss} *(MW)*	1.56	1.67	3.52
P_{dc} *(MW)*	-68.47	-76.76	146.16
U_{dc} *(p.u.)*	1.000	0.999	1.006

TABLE III
POWER FLOW SOLUTION—MTDC GRID 2

Converter	4	5	6	7
Control	Slack - Q	P - Q	P - Q	P - Q
P_s *(MW)*	124.43	-50.00	-135.00	50.00
Q_s *(MVAr)*	0.00	0.00	0.00	0.00
U_s *(p.u.)*	1.020	1.050	1.014	1.039
δ_s *(deg)*	0.00	10.11	10.25	14.60
P_c *(MW)*	124.67	-49.96	-134.72	50.04
Q_c *(MVAr)*	31.36	-3.46	39.26	-3.14
U_c *(p.u.)*	1.061	1.042	1.062	1.033
δ_c *(deg)*	18.41	2.90	-9.89	21.96
P_{loss} *(MW)*	2.81	1.36	3.04	1.33
P_{dc} *(MW)*	-127.49	48.60	131.67	-51.37
U_{dc} *(p.u.)*	1.000	1.008	1.010	1.006

The power flow converges in 2 overall iterations with a flat start. In the first overall iteration cycle, all grids need 4 internal iteration steps. In the second overall cycle, the AC grid connected to the DC slack buses is the only grid that needs 3 steps to converge, the other grids are already converged after the first cycle. Compared to the situation without MTDC systems, the calculation time increases with a factor 2.4, with the largest contributions resulting from the repeated AC power flow (75%) and the DC slack iteration (21%). The DC power flow is only responsible for 1.7% of the overall calculation time due to the limited size of the DC grids compared to the AC grids. Since no converter limits are encountered, enabling the limits does not increase the overall number of iterations. However, the overall calculation time increases by a factor 1.3.

V. CONCLUSION

In this paper, a steady-state VSC MTDC model for power flow programs has been developed. The model allows simulating multiple AC grids interconnected by multiple DC grids. The approach demonstrated in this paper is general and allows to include converter limits as well as different converter topologies by either including converter transformers and/or low-pass filters. Simulation results show the ability of the proposed model to fully represent MTDC systems in power flow software and demonstrate how the model can be incorporated with an open-source AC power flow analysis code.

APPENDIX

The slack bus iteration Jacobian elements from (50) are

$$\left(\frac{\partial P_c}{\partial \delta_c}\right)^{(j)} = -Q_c^{(j)} - {U_c^{(j)}}^2 B_c$$

$$\left(\frac{\partial P_c}{\partial \delta_f}\right)^{(j)} = Q_c^{(j)} + {U_c^{(j)}}^2 B_c$$

$$\left(U_c \frac{\partial P_c}{\partial U_c}\right)^{(j)} = P_c^{(j)} + {U_c^{(j)}}^2 G_c$$

$$\left(U_f \frac{\partial P_c}{\partial U_f}\right)^{(j)} = P_c^{(j)} - {U_c^{(j)}}^2 G_c$$

$$\left(\frac{\partial Q_s}{\partial \delta_f}\right)^{(j)} = -P_s^{(j)} - {U_s^{(k)}}^2 G_{tf}$$

$$\left(U_f \frac{\partial Q_s}{\partial U_f}\right)^{(j)} = Q_s^{(j)} - {U_s^{(k)}}^2 B_{tf}$$

$$\left(\frac{\partial F_1}{\partial \delta_c}\right)^{(j)} = Q_{cf}^{(j)} - {U_f^{(j)}}^2 B_c$$

$$\left(\frac{\partial F_1}{\partial \delta_f}\right)^{(j)} = -Q_{cf}^{(j)} + Q_{sf}^{(j)} + {U_f^{(j)}}^2 (B_c + B_{tf})$$

$$\left(U_c \frac{\partial F_1}{\partial U_c}\right)^{(j)} = P_{cf}^{(j)} + {U_f^{(j)}}^2 G_c$$

$$\left(U_f \frac{\partial F_1}{\partial U_f}\right)^{(j)} = P_{cf}^{(j)} - P_{sf}^{(j)} - {U_f^{(j)}}^2 (G_c + G_{tf})$$

$$\left(\frac{\partial F_2}{\partial \delta_c}\right)^{(j)} = -P_{cf}^{(j)} - U_f^{(j)} G_c$$

$$\left(\frac{\partial F_2}{\partial \delta_f}\right)^{(j)} = P_{cf}^{(j)} - P_{sf}^{(j)} + {U_f^{(j)}}^2 (G_c + G_{tf})$$

$$\left(U_c \frac{\partial F_2}{\partial U_c}\right)^{(j)} = Q_{cf}^{(j)} - {U_f^{(j)}}^2 B_c$$

$$\left(U_f \frac{\partial F_2}{\partial U_f}\right)^{(j)} = Q_{cf}^{(j)} - Q_{sf}^{(j)} + {U_f^{(j)}}^2 (B_c + B_{tf} + 2B_f)$$

with the converter powers from (1)–(9).

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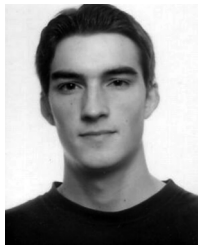

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