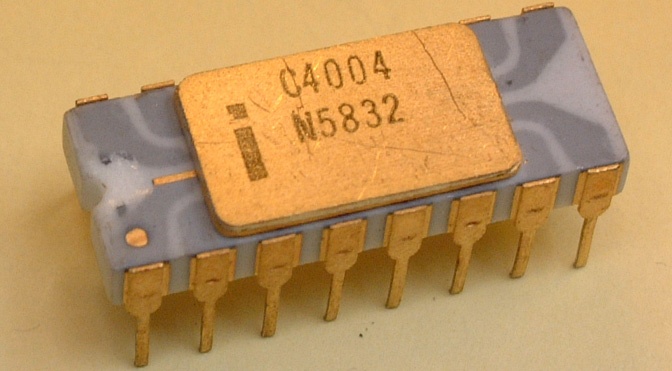
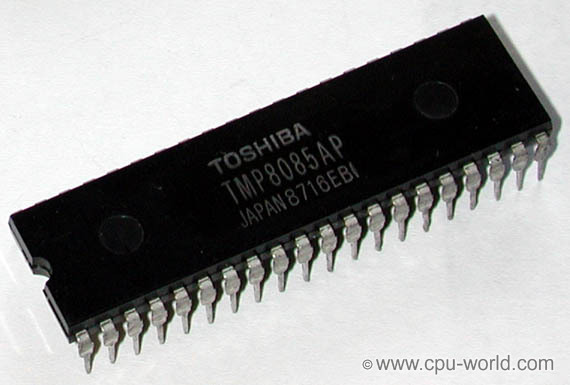
**Aim: Case study on intel processors.**

**1.4004**

* The Intel 4004 is a [4-bit](http://en.wikipedia.org/wiki/4-bit) [central processing unit](http://en.wikipedia.org/wiki/Central_processing_unit) (CPU) released by [Intel Corporation](http://en.wikipedia.org/wiki/Intel) in 1971. .
* The 4004 microprocessor was one of 4 chips constituting the MCS-4 chip-set, which included the 4001 ROM, 4002 RAM, and 4003 Shift Register.
* Maximum [clock speed](http://en.wikipedia.org/wiki/Clock_speed) was 740 [kHz](http://en.wikipedia.org/wiki/Kilohertz).
* [Instruction set](http://en.wikipedia.org/wiki/Instruction_set) contained 46 instructions
* Register set contained 16 registers of 4 bits each
* Instruction cycle time: 10.8 µs.
* Instruction execution time 1 or 2 instruction cycles (10.8 or 21.6 µs), 46300 to 92600 instructions per second
* Its is commonly manufactured by Intel
* Min. feature size is 10[μm](http://en.wikipedia.org/wiki/%CE%9Cm)(10^-6)
* [Instruction set](http://en.wikipedia.org/wiki/Instruction_set) is 4-bit [BCD](http://en.wikipedia.org/wiki/Binary-coded_decimal)-oriented
* Application : Busicom calculator, arithmetic manipulation
* Package(s) : 16-pin [DIP](http://en.wikipedia.org/wiki/Dual_in-line_package)(Dual in-line package)

**2.8085**

* Intel 8085 microprocessor is the next generation of [Intel 8080 CPU](http://www.cpu-world.com/CPUs/8080/index.html) family
* Intel 8085 had single 5 Volt power supply.
* Clock oscillator and system controller were integrated on the chip.
* The CPU included serial I/O port.
* Two new instructions were added to 8085 instruction set..

**Application** - The microprocessor is provided with an instruction set which consists of various instructions such as MOV, ADD, SUB, JMP, etc. These instructions are written in the form of a program which is used to perform various operations such as branching, addition, subtraction, [bitwise logical](http://en.wikipedia.org/wiki/Bitwise_operation) and [bit shift](http://en.wikipedia.org/wiki/Bit_shifting) operations.

**Features**

It consists of 74 instruction sets

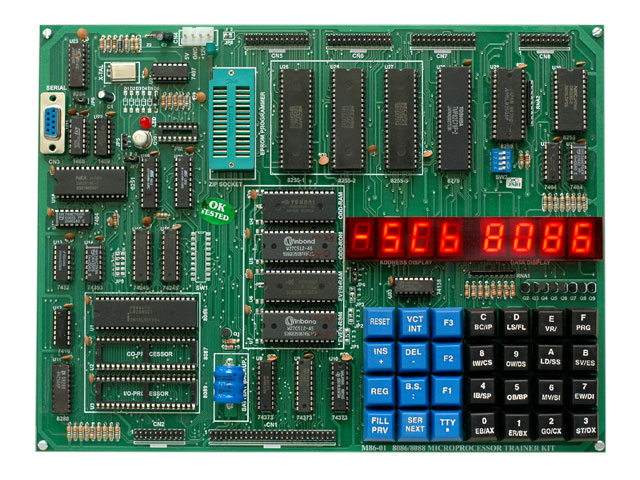
A 16 bit program counters (PC).

A 16 bit stack pointer (SP).

It is an 8 bit microprocessor

1.3 micro sec instruction cycles.

It performs arithmetic and logical operations.

**3.8086**

1.It is 16 bit processor. So that it has 16 bit ALU, 16 bit registers and internal data bus and 16 bit external data bus. It make s faster processing.

2.It has three version based on the frequency of operation:

a)8086 -> 5MHz

b)8086-2 ->8MHz

c) 8086-1 ->10 MHz

3.8086 have 20 bit address lines to access memory. Hence it can access

                  2^20 = 1 MB memory location.

4.8086 has 16-bit address lines to access I/O devices, hence it can access

                  2^16 = 64K I/O location

5. **Pipelining:-**8086 uses two stage of pipelining. First is Fetch Stage and the second is Execute Stage.

Fetch stage that prefetch upto 6 bytes of instructions store them in the queue.

Execute stage that executes these instructions.

Pipelining improves the performance of the processor so that operation is faster.

**6. Operates in two modes:-**8086 operates in two modes:

A) Minimum Mode: A system with only one microprocessor.

B) Maximum Mode:-A system with multiprocessor.

**7.8086 uses memory banks:-**The 8086 uses a memory banking system. It means entire data is not stored sequentially in a single memory of 1 MB but memory is divided into two banks of 512KB

**8. Interrupts:-**8086 has 256 vectored interrupts.

**9. Multiplication and Division:-**8086 has a powerful instruction set. So that it supports multiply and divide operation.

**4.8386 DX**

* It supports 8/16/32 bit data operands
* It has 32-bit internal registers
* It supports 32-bit data bus and 32-bit non-multiplexed address bus
* It supports
  + Physical Address of 4GB
  + Virtual Address of 64TB
  + Maximum Segment size of 4GB
* It operates in 3 different modes
  + Real
  + Protected
  + Virtual 8086
* MMU provides virtual memory, paging and 4 levels of protection
* Clock Frequency : 20,25 and 33MHz
* It has 132 pin package

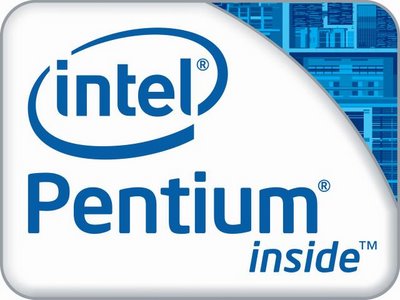
**5.80486**



**Features:**

* The 80486 microprocessor is an improved version of the 80386 microprocessor that contains an 8K-byte cache and an 80387arithmetic co processor; it executes many instructions in one clocking period.
* The 80486 microprocessor executes a few new instructions that control the internal cache memory.
* A new feature found in the 80486 in the BIST (built-in self-test) that tests the microprocessor, coprocessor, and cache at reset time.
* If the 80486 passes the test, EAX contains a zero.
* Additional test registers are added to the 80486 to allow the cache memory to be tested.
* These new test registers are TR3 (cache data), TR4 (cache status), and TR5 (cache control).

**6. Pentium**



* The Pentium microprocessor is almost identical to the earlier 80386 and 80486 microprocessors.
* The main difference is that the Pentium has been modified internally to contain a dual cache (instruction and data) and a dual integer unit. The Pentium also operates at a higher clock speed of 66 MHz
* The data bus on the Pentium is 64 – bits wide and contains eight byte-wide memory banks selected with bank enable signals.
* Memory access time, without wait states, is only about 18 ns in the 66 MHz Pentium.
* The superscalar structure of the Pentium contains three independent processing units: a floating point processor and two integer processing units.
* A new mode of operation called the System Memory Management (SMM) mode has been added to the Pentium.
* It is intended for high-level system functions such as power management and security.
* The Built-in Self-test (BIST) allows the Pentium to be tested when power is first applied to the system.
* Allows 4MByte memory pages instead of the 4KByte.

**7. Pentium п**

Available at 350 MHz, 400 MHz, and 450 MHz frequencies

• System bus frequency at 100 MHz

• Binary compatible with applications running on previous members of the Intel microprocessor line

• Dynamic execution micro architecture

• Dual Independent Bus architecture: Separate dedicated external System Bus and dedicated internal high-speed cache bus

• Power Management capabilities

—System Management mode

—Multiple low-power states

Optimized for 32-bit applications running on advanced 32-bit operating systems.

• Single Edge Contact Cartridge (S.E.C.C.) and S.E.C.C.2 packaging technology; the S.E.C. cartridges deliver high performance with improved handling protection and socketability.

• Integrated high performance 16 KB instruction and 16 KB data, nonblocking, level one cache.

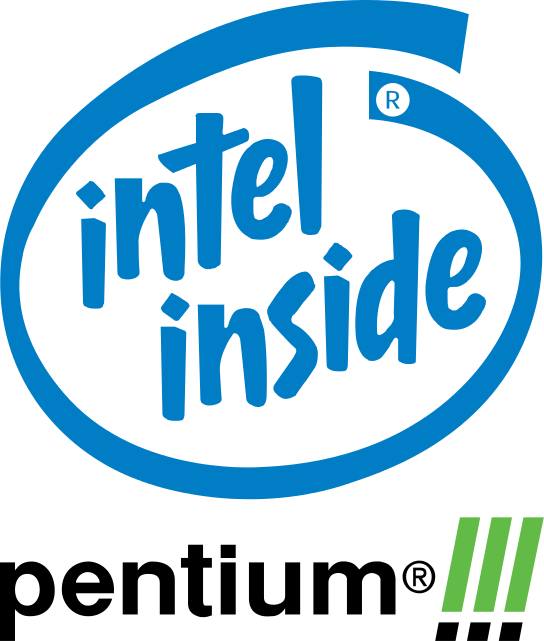
• Available with integrated 512 KB unified, nonblocking, level two cache.

• Enables systems which are scaleable up to two processors.

• Error-correcting code for System Bus data.

**8. Pentium Pro**

* The Pentium Pro is an enhanced version of the Pentium microprocessor that contains not only the level 1 caches found inside the Pentium, but the level 2 cache of 256 K or 512K found on most main boards.
* The Pentium Pro operates using the same 66 MHz bus speed as the Pentium and the 80486.
* It uses an internal clock generator to multiply the bus speed by various factors to obtain higher internal execution speeds.
* The only significant software difference between the Pentium Pro and earlier microprocessors is the addition of FCMOV and CMOV instructions.
* The only hardware difference between the Pentium Pro and earlier microprocessors is the addition of 2M paging and four extra address lines that allow access to a memory address space of 64G Bytes

**9.Pentium III**

Pentium III microprocessor family was an evolutionary upgrade from [Pentium II](http://www.cpu-world.com/CPUs/Pentium-II/index.html).

The first Pentium III core, Katmai, featured SSE instruction set, which allowed SSE-enabled applications to process up to four single-precision floating point numbers at once.

Other Pentium 3 cores added other features, like 256 and 512 KB on-die L2 cache memory and smaller package size.

During its lifetime, the core of Pentium III microprocessors was shrunk twice - from 0.25 micron to 0.18 micron, and then to 0.13 micron.

Like the previous generation of x86 processors, the Pentium III family consists of a few sub-families targeting different segments of computer market:

* Pentium III Xeon - high performance version.
* Pentium III desktop processors - desktop computers.
* [Desktop Celeron](http://www.cpu-world.com/CPUs/Celeron/index.html) - low-cost version.
* Mobile Pentium III and mobile Pentium III-M - mobile versions of the Pentium III processor.
* Mobile Celeron - mobile version of Intel Celeron processor.

**10.Pentium IV**

* Speeds range from 1.3GHz to 3.8GHz.
* 42 million transistors, 0.18-micron process, 217 sq. mm die (Willamette).
* 55 million transistors, 0.13-micron process, 131 sq. mm die (Northwood).
* 125 million transistors, 0.09-micron process, 112 sq. mm die (Prescott).
* Software compatible with previous Intel 32-bit processors.
* Some Prescott versions support EM64T (64-bit extensions) and Execute Disable Bit (buffer overflow protection).
* Processor (front-side) bus runs at 400MHz, 533MHz, 800MHz, or 1066MHz.
* Arithmetic logic units (ALUs) run at twice the processor core frequency.
* Hyper-pipelined (20-stage or 31-stage) technology.
* Hyper-threading technology support in all 2.4GHz and faster processors running an 800MHz bus and all 3.06GHz and faster processors running a 533MHz bus.
* Very deep out-of-order instruction execution.
* Enhanced branch prediction.
* 8KB or 16KB L1 cache plus 12K micro-op execution trace cache.
* 256KB, 512KB, or 1MB of on-die, full-core speed 256-bit-wide L2 cache with eight-way associativity.
* L2 cache can handle up to 4GB RAM and supports ECC.
* 2MB of on-die, full-speed L3 cache (Extreme Edition).
* SSE2—SSE plus 144 new instructions for graphics and sound processing (Willamette and Northwood).
* SSE3—SSE2 plus 13 new instructions for graphics and sound processing (Prescott).
* Enhanced floating-point unit.
* Multiple low-power states.



**11.Dual Core**

It has combined two processors and their [caches](http://www.webopedia.com/TERM/C/cache.html) and cache [controllers](http://www.webopedia.com/TERM/C/controller.html) onto a single [integrated circuit](http://www.webopedia.com/TERM/I/integrated_circuit_IC.html) ([silicon](http://www.webopedia.com/TERM/S/silicon.html) chip).

Dual-core processors are well-suited for[multitasking](http://www.webopedia.com/TERM/M/multitasking.html) environments because there are two complete execution [cores](http://www.webopedia.com/TERM/C/core_logic.html) instead of one, each with an independent interface to the [frontside bus](http://www.webopedia.com/TERM/F/frontside_bus.html).

Since each core has its own cache, the[operating system](http://www.webopedia.com/TERM/O/operating_system.html) has sufficient resources to handle most compute intensive tasks in parallel.