2015 EE214A Design Project

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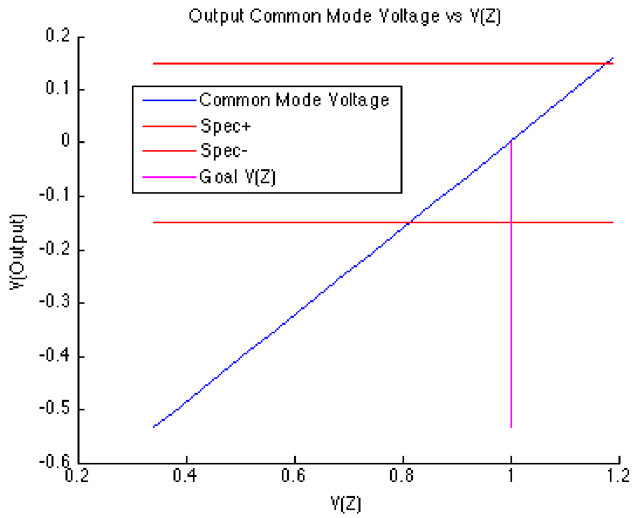
December 4, 2015

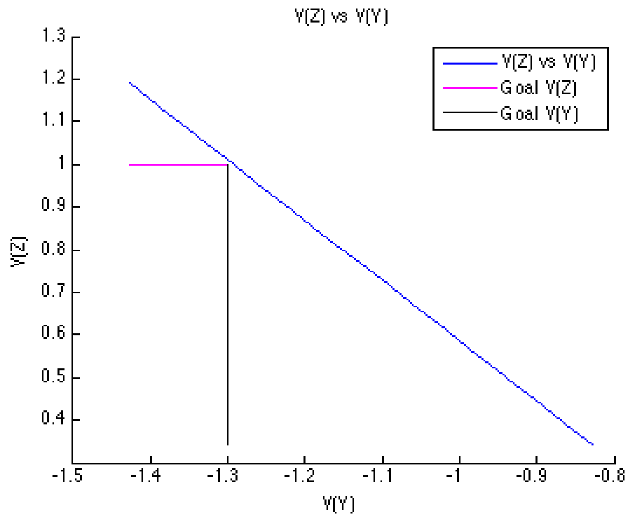
Specfications	Given Spec	Achieved Spec
Gain	30kΩ	34.7kΩ
Bandwidth	90MHz	93MHz
Power	2.0mW	1.0mW
FOM	1350	3043

Area Breakdown	% Core Area	Area (um)
Core Area	100%	112μm^2
VNMOS-bias	19.6%	22μm^2
VPMOS-bias	10.7%	12μm^2
Bias Generator	73.1%	82μm^2

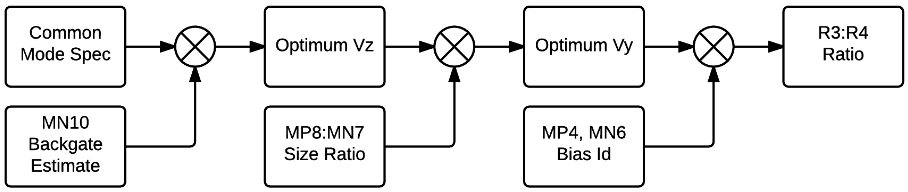
1 Design Outline

Our approach to this design was to first develop sizing ratios of the transistors and their DC relationships to Vx, Vy, Vz and Vo. We developed the equations necessary to 'program' those voltages and to develop what their reasonable ranges are. Here are some graphs that show the relationships between the output common mode voltage and Vz, and then Vz to Vy given our sizing decisions. We developed a MATLAB program to quickly estimate critical parameters for a given design, to allow easy investigation of parametric variation.

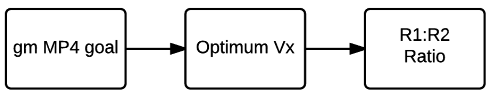




These graphs give rise to a process to choose exactly the value of those voltages based on the size of the transistors. Here, given the common mode output spec, choosing a size for MN10, and estimating the MN10 backgate gives the needed value of Vz. Given a size ratio for MN7 to MP8 gives the needed value of Vy, knowing Vz. Given the size ratio for MP4 to MN6 and knowing the value of Vy gives the gives the necessary ratio of R3 to R4 to program the value of Vy.



Similarly for Vx, given a goal for MP4 gm (from our chosen distribution of stage gain) we can solve for the ratio of R1 to R2 to program the value of Vx. Since we have set the K value of MN1 and MP3 equal, the voltage at Vx is selected purely by the ratio of R1 and R2.

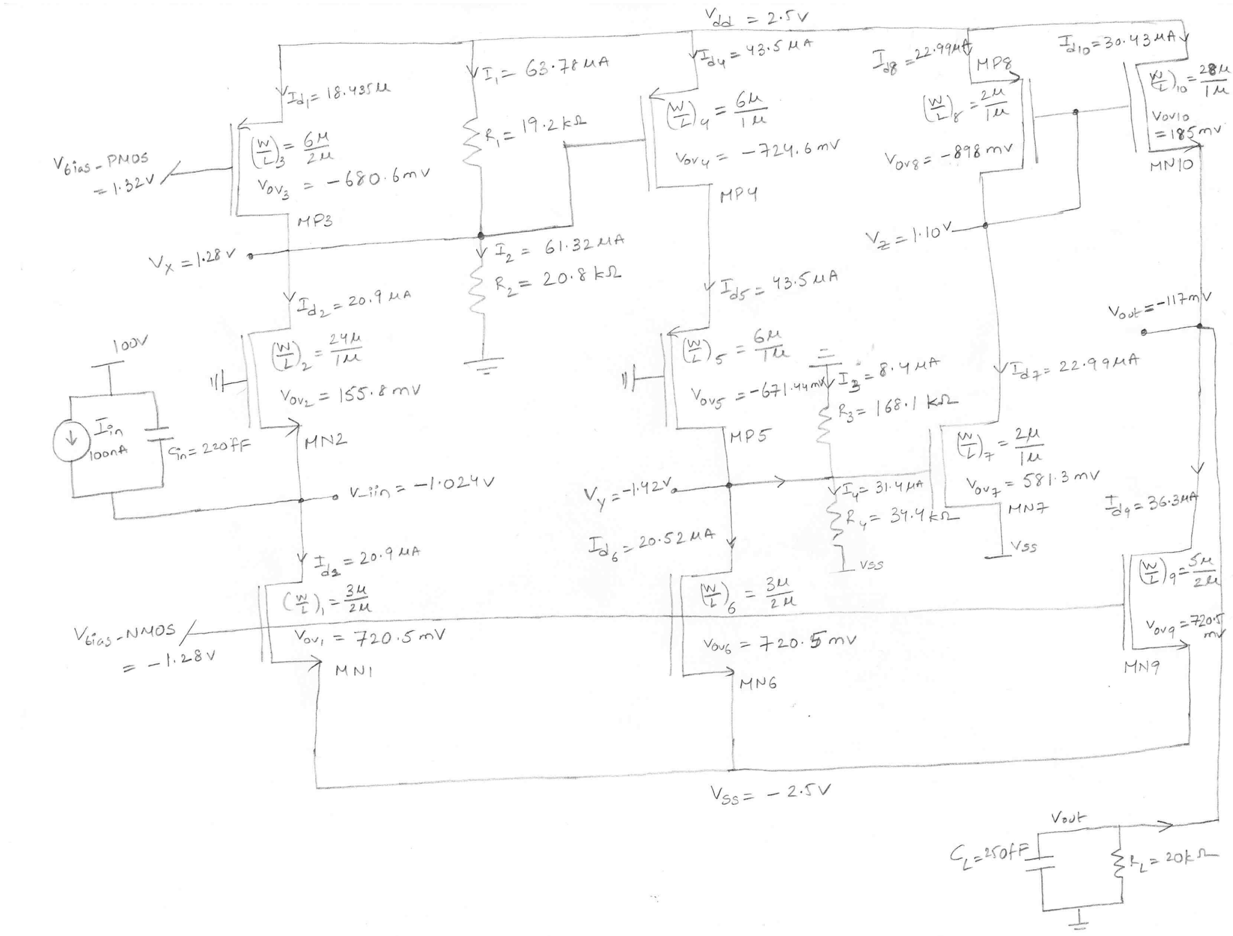


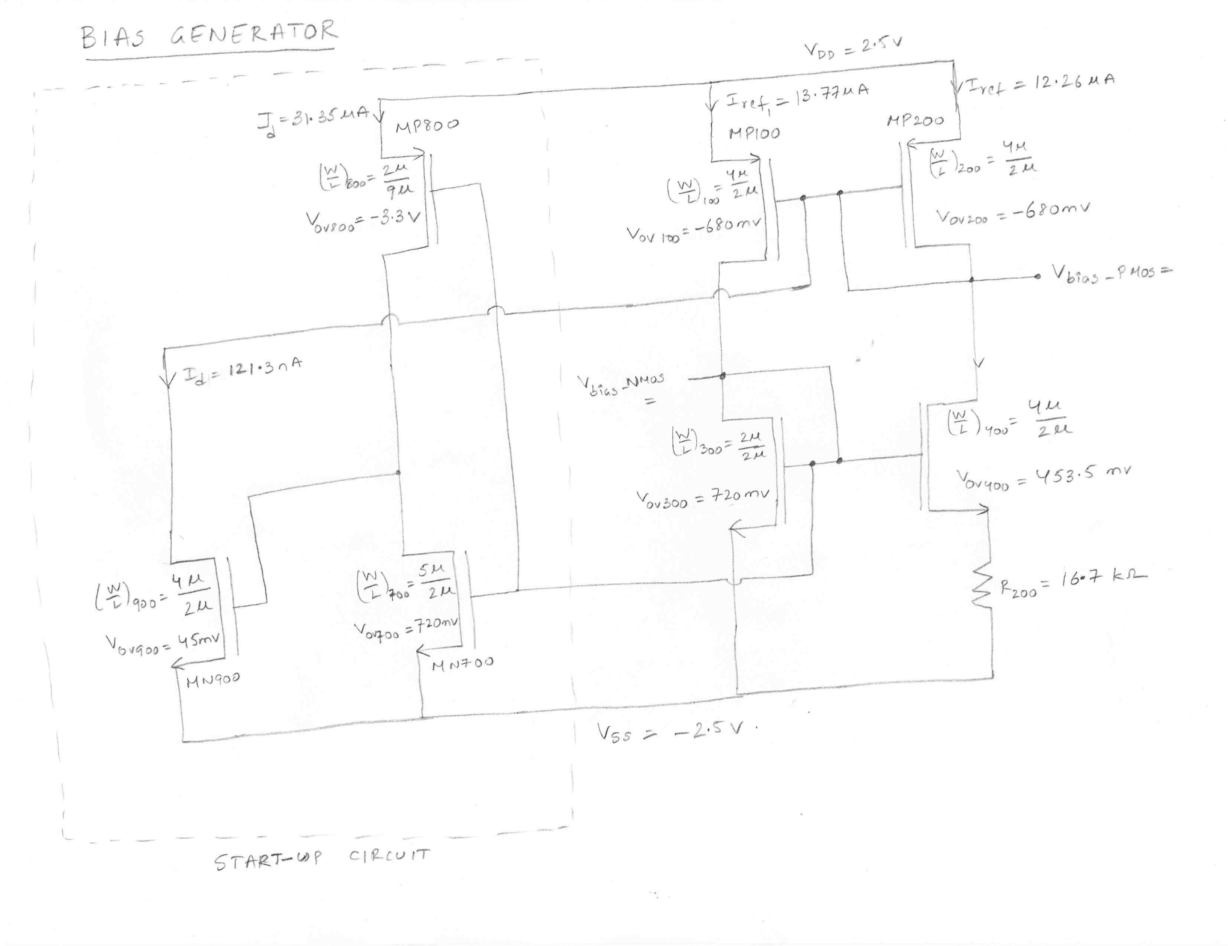
Once the math was developed to decouple the selection of stage gain to the DC biasing selection, the focus was on gain/speed. First we distributed the desired gain for each stage, then choose the vov level to drive the transistors based on the gm/Id plots, and then sized the transistors to minimize tau for adjacent stages.

The gain budget was based on the X stage having the most gain, since it's easy to get there, getting the balance of gain from the Y stage and then setting the Z stage to cancel out the gain loss of the output CD stage. Thus total gain simplifies to X * Y = 30k.

By making plots of the sum of tau for adjacent stages vs critical transistor sizing we were able to minimize total tau for the design, with the given gain budget.

2 Design Schematic





[1] Drawings also attached to end of appendix in full size

3 Calculation of Key Design Parameters

Choice of L

- All devices used in current source have a minimum length of 2μm.
- All other devices in the amplifier have minimum length of 1μm. Minimum length is used as f_t is inversely proportional to L.
- All devices in bias generator circuit have length >=2μm.

Bias Generator circuit

- Constant gm reference based design is used as bias circuit to reduce mismatch errors.
- Transconductance of bias device (mn300) depends only on R2 and m (m is the ratio of MN300/MN400). Therefore gm can be set precisely.
- Start-up circuit is used to force the circuit to the desired operating point.

Approximations for hand calculations
For simpler hand calculations, following approximations are used.

1. $Cdb = Csb = 0.35Cgs$
2. $Cgs = (\frac{2}{3})WLCox + Cov'W$
3. $Cgd = Cov'W$
4. $gmb = 0.2gm$

Stage4

- As per the spec, common mode output voltage (vout) has to be within -0.15v to 0.15v. Since the body is connected to vss, MN10 experiences back gate effect and the threshold voltage is given by:

$$\begin{aligned} Vt = Vt_0 + \gamma(\sqrt{2\phi f + V_{sb}} - \sqrt{2}\phi f \\ Vt_0 = 0.5V, \gamma = 0.6, 2\phi f = 0.8 \end{aligned} \tag{1}$$

- Stage 4 is a source follower which has a gain given by

$$A4 = \frac{gm_{10}}{gm_{10} + gmb_{10} + (\frac{1}{R_L})} \tag{2}$$

- Gain of stage4 (A4) <1 due to back gate effect and the output load.
- To achieve gain closer to 1 (0.6 - 0.7), it is important to size and bias MN10 such that $(gm_{10} + gmb_{10}) >> (1/R_L)$.
- Transconductance of and drain current of MN_{10} is given by

$$gm_{10} = \mu nCox(\frac{W}{L})vov_{10} \tag{3}$$

$$Id_{10} = 0.5\mu nCox(\frac{W_{10}}{L_{10}})vov_{10}^2(1 + \lambda(Vdd - Vout)) \tag{4}$$

- MN_9 (bias device for source follower) is sized such that $Id_{10} + I_{R_L} = Id_9$ and the common mode output voltage does not fall out of range. This device is chosen to be of smaller size to reduce loading on Vout node.

$$\tau_{OUTPUT} = (R_L || \frac{1}{1.2gm_{10}})(C_L + Csb_{10} + Cgd_9 + Cdb_9) \tag{5}$$

- Cgs10 is assumed to be very small due to boot-strapping.

Stage 3

- Loading at node Vy increases with the increase in gain of stage 3 due to the miller effect. Hence gain of stage3 is kept low and is fixed at sqrt(2) to compensate for the gain lost in stage 4. Gain of stage3 (CS amplifier with diode connected load):

$$|A3| = \frac{gm7}{gm8} = \frac{Vov8}{Vov7} = \frac{Vdd - Vz - abs(Vtp)}{Vy - Vss - Vtn} = \sqrt{2} \tag{6}$$

- Choice of Vz from above (stage4) determines Vy.
- Minimum device sizes (W=2μm, L=1μm) are used for both MN7 and MP8 to reduce loading on Vy and Vz.

$$Id_7 = Id_8 = 0.5\mu nCox(\frac{W_7}{L_7})vov_7^2(1 + \lambda(Vz - Vss)) \tag{7}$$

$$\tau_Z = (\frac{1}{gm_8})(Cgs_8 + Cdb_8 + Cgd_{10} + Cgd_7(1 + \frac{1}{|A3|}) + Cdb_7) \tag{8}$$

Stage 2

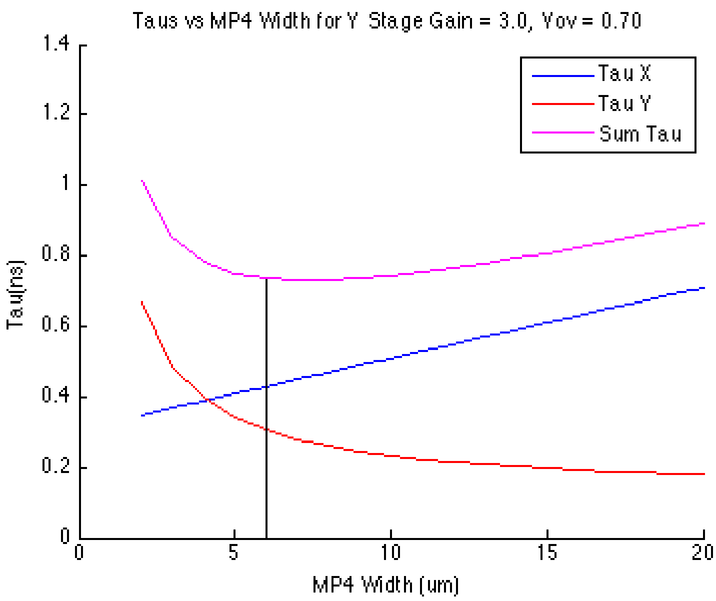
- Vy from stage Z above determines the required ratio of R3 and R4.

$$(\frac{R4}{R3}) = \frac{Vss}{Vy} - 1 \tag{9}$$

- Gain of stage Y (Cascode amplifier) is set to 3.

$$|A2| = gm4(R3||R4) \tag{10}$$

- Vov_4 and W_4 are optimized to reduce τ_X.



- MN6 is sized such that current through MN6 is same as the current through MP4 and MP5.

$$Id4 = Id5 = Id6 = 0.5\mu pCox(\frac{W4}{L4})(Vdd - Vx - abs(Vtp))^2(1 + \lambda(Vdd - Vw) \tag{11}$$

- Current through R3 and R4

$$I_{R3} + I_{R4} = Vss/(R3 + R4) \tag{12}$$

$$\tau_Y = (R3||R4)(Cgs_7 + Cgd_7(1 + |A3|) + Cgd_6 + Cdb_6 + Cgd_5 + Cdb_5) \tag{13}$$

Stage 1

- Vov_4 from stage 2 sets V_X which in turn sets the ratio of R1 and R2.

$$Vov_4 = Vdd - Vx - |Vtp| \tag{14}$$

$$(\frac{R1}{R2}) = \frac{Vdd}{Vx} - 1 \tag{15}$$

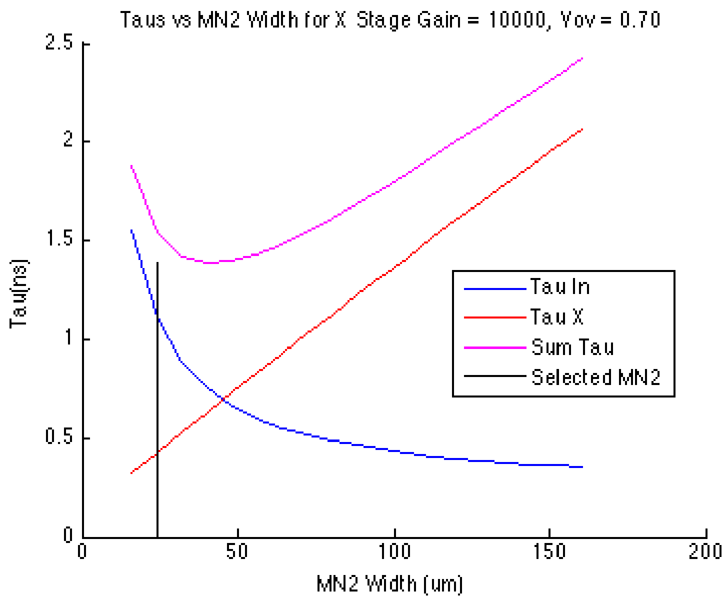
- Gain of stage 1 (Common gate amplifier) is set to 10000.

$$|A1| = (R1||R2) \tag{16}$$

- MN1 and MP3 are sized such that Id1 = Id3.
- MN2 is sized to reduce τ_{IIN} node. τ_{IIN} is inversely proportional to gm_2.

$$\tau_{IIN} = (\frac{1}{gm2})(Cin + Cgd_1 + Cdb_1 + Cgs_2 + Csb_2) \tag{17}$$

$$\tau_X = (R1||R2)(Cgd_2 + Cdb_2 + Cgd_3 + Cdb_3 + Cgs_4 + Cgd_4) \tag{18}$$



- Current through MN1, MN2 and MP3

$$Id_{1,2,3} = 0.5\mu pCox(\frac{W_3}{L_3})(Vdd - VbiasP - |Vtp|)^2(1 + \lambda(Vdd - Vx)) \tag{19}$$

- Current through R1 and R2

$$I_{R1} + I_{R2} = Vdd/(R1 + R2) \tag{20}$$

Vovn, Vovp

- Vovn and Vovp are chosen to achieve a reasonable balance between gain, Tau total and Power, and our choice was educated by the gm/Id technology plots.

Total Design Performance

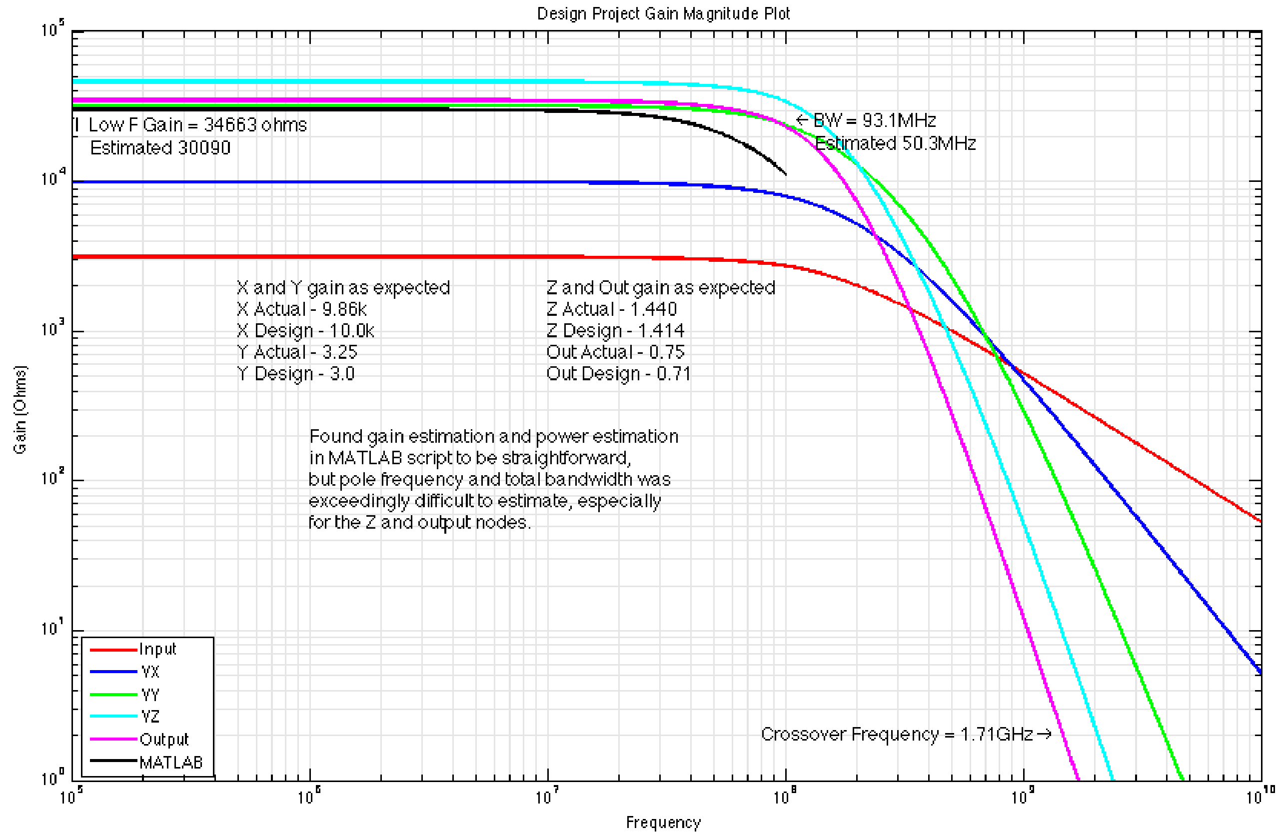
$$|A_{TOTAL}| = A1 * A2 * A3 * A4 \quad (21)$$

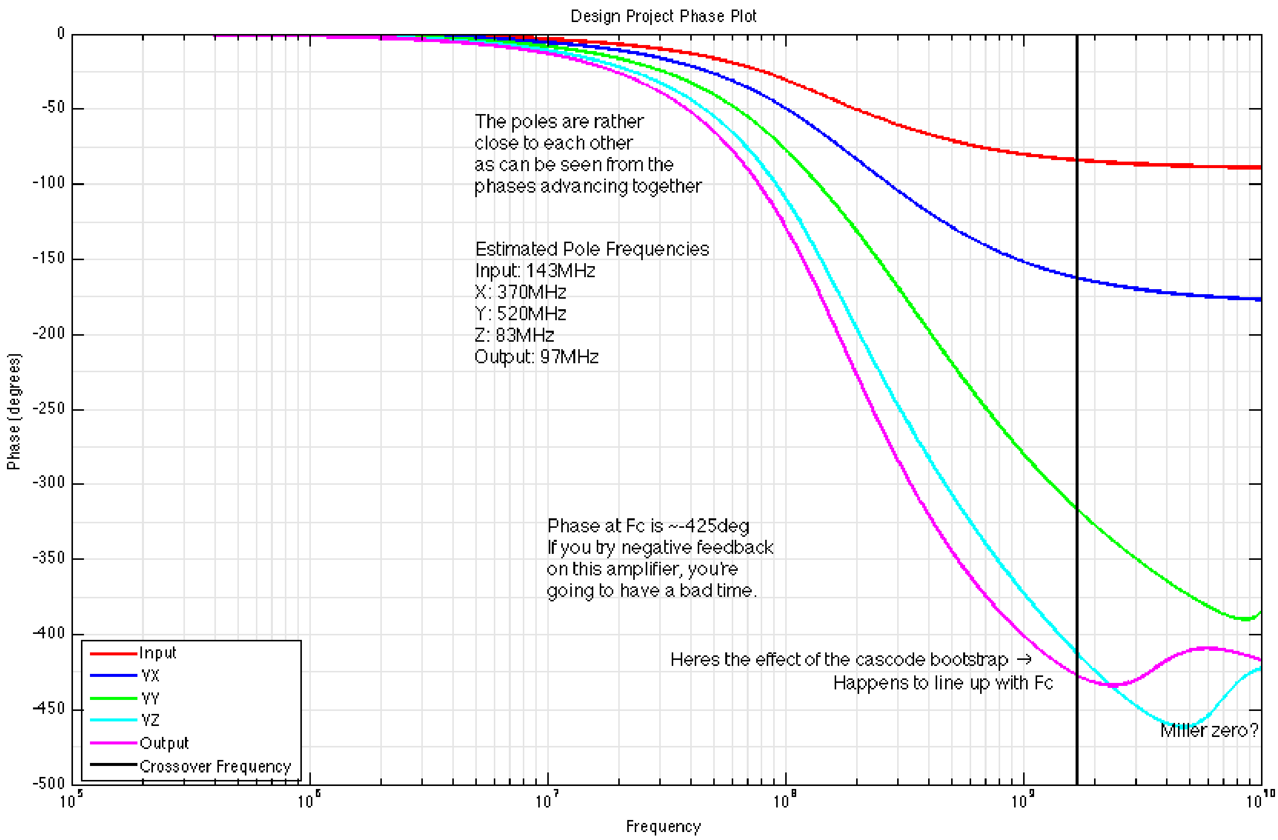
$$\tau_{TOTAL} = \tau_{IIN} + \tau_X + \tau_Y + \tau_Z + \tau_{OUTPUT} \quad (22)$$

$$Power = (Vdd - Vss)(Id_1 + Id_4 + Id_7 + Id_{10}) + (\frac{Vdd^2}{R1 + R2}) + (\frac{Vss^2}{R3 + R4}) \quad (23)$$

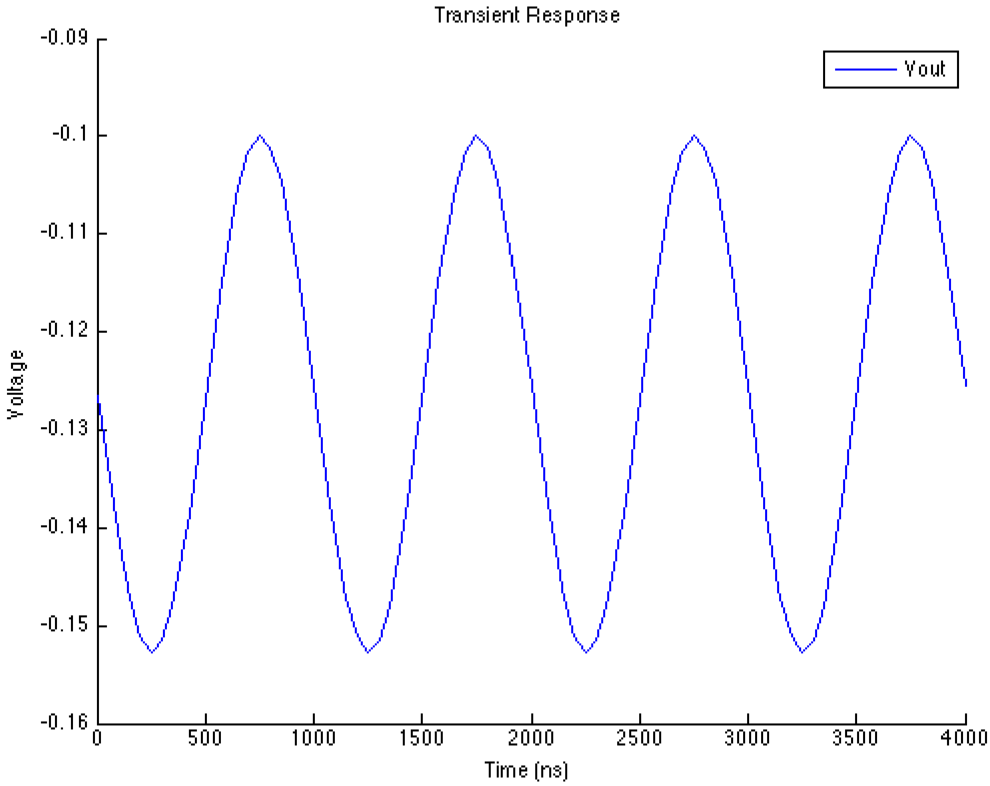
Bias Generator	Hand calc	Spice	%Error	Reason for error
V_{BiasN}	-1.300V	-1.279V	-1.6%	Startup circuit bias
V_{BiasP}	1.300V	1.319V	1.5%	Startup circuit bias
Stage1	Hand calc	Spice	%Error	Reason for error
Id_1	18.3μA	20.9μA	14.2%	Bias generator error
Vx	1.300V	1.275V	-1.9%	
A_X	10kΩ	9.86kΩ	-1.4%	Finite MN_1 and MP_3 output resistance
gm_2	210μS	268μS	27.6%	Bias generator error
τ_{IN}	1.11ns			
τ_X	420ps			
Stage2	Hand calc	Spice	%Error	Reason for error
Id_4	36.75μA	43.5μA	18.4%	
V_W	1.496V	1.450V	-3.2%	
V_Y	-1.550V	-1.418V	-8.5%	Imbalance between MP_4 and MN_6 current
gm_4	105μS	120μS	14.3%	Error in V_Y
A_Y	-3.0	-3.25	8.3%	Error estimating gm_4
τ_Y	306ps			
Stage3	Hand calc	Spice	%Error	Reason for error
Id_7	10.25μA	22.9μA	123%	Error in V_Y plus finite output resistance
V_Z	1.364	1.102V	-19.2%	Error in V_Y
gm_7	45μS	79μS	75.5%	Error in Id_7
gm_8	31.2μS	51μS	63.5%	Error in Id_7
A_Z	1.414	1.440	1.8%	The benefit of ratiometric design
τ_Z	1.92ns			Error in estimating gm_8
Stage4	Hand calc	Spice	%Error	Reason for error
Id_{10}	2.96μA	30.43μA	928%	MN_{10}'s large width is a big error amplifier
V_{OUT}	0.299	-0.117V	-139%	
Vt_{10}	0.999	1.034V	3.5%	
gm_{10}	91.1μS	327μS	258%	
gmb_{10}	13.0μS	55.1μS	323%	
A_{OUT}	0.71	0.75	5.6%	
τ_{OUT}	1.63ns			Error in estimating gm_{10}
Total Power	578μW	1.065mW	84%	Not accounting for bias gen
Total Gain	30.04kΩ	34.66kΩ	15.5%	Error in estimating gm

4 Simulated Bode Plots





5 Simulated Transient Response



6 Comments and Conclusion

6.1 Notes about Design

- Resistors contribute to a large part of the overall gain. From manufacturability perspective, passive components are not friendly and also occupy more area on the chip. We feel that while the large value resistors helped us achieve a high gain and low power that they result in a possibly overly acedemic design thats not suitable for actual production.

- The output source follower stage is very sensitive to biasing due to back gate effect. Small variations on V_Z can drive the output to fall out of desired common mode voltage or drive MN_10 into cutoff region and lose all the gain from previous stages.

- Any variations in supply voltage causes variation in Vov of MN7 directly (as the device is biased through R3 & R4) causing V_Z to vary and thereby impacting the biasing of MN10 and gain. This is a great node to lose any and all PSRR.

- Common source stage with diode connected load attributes to miller cap loading effect on cascade stage. This is limiting the gain of common source stage to smaller values.

- Since the output is single ended, it is susceptible to noise, a differential configuration will be better.

6.2 Notes on Project

- We found it very difficult to balance the many simultaneous requirements, and I felt that this was a very useful exercise that's directly applicable to industry, and not only to chip design. Many times I have found myself trying to explore design spaces that have myrid of opposing non-orthogonal requirements. I feel like I have learned interesting ways to approach these problems both mathematically and strategically.

7 Appendix I

7.1 SPICE Netlist

```
* Design Problem, ee114/214A-2015
* Team Member 1 Name: Usha Kankanala
* Team Member 2 Name: Samuel Lenius
* Please fill in the specification achieved by your circuit
* before you submit the netlist
**************************************************************
* sunetids of team members:
*   ukankana@stanford.edu:  06091239
*   lenius@stanford.edu:    06091240
* The specification that this script achieves are:
* Power         1.06mW    <= 2.00 mW      Meets Spec
* Gain          34.6kOhm  >=  30.0 kOhm   Meets Spec
* BandWidth     93.0MHz   >= 90.0 MHz     Meets Spec
* FOM           3043      >= 1350         Meets Spec
**************************************************************

* Including the model file
.include /usr/class/ee114/hspice/ee114_hspice.sp

* Defining Top level circuit parameters
.param p_Cin = 220f
.param p_CL  = 250f
.param p_RL  = 20k

* Defining the supply voltages
vdd     n_vdd   0       2.5
vss     n_vss   0       -2.5

*Defining the input current source
** For ac simulation uncomment the following 2 lines**
Iin     n_iin   0       ac      100n
*Iin     n_iin   0       ac      1

** For transient simulation uncomment the following 2 lines**
*Iin    n_iin    0    sin(0 0.5u 1e6)

* Defining Input capacitance
Cin    n_iin    0    'p_Cin'

* Defining the load
RL      n_vout  0       'p_RL'
CL      n_vout  0       'p_CL'

*** Your Trans-impedance Amplifier here ***
***     d       g       s       b       n/pmos114       w       l

*** Vx/Iin = V(n_x) / Iin, use "n_x" as the node label for Vx ***
MN1     n_iin   n_bias_n  n_vss   n_vss nmos114  w=3.0u l=2.0u

* Increasing the size of MN2 here is a power-free trick to improve the input
* pole performance.
MN2     n_x     0         n_iin  n_vss  nmos114  w=28.0u l=1.0u
MP3     n_x     n_bias_p  n_vdd  n_vdd  pmos114  w=6.0u l=2.0u

* The parallel combination of these resistors provide the first stage gain.
R1      n_vdd   n_x       19200
R2      n_x     0         20800

*** Vy/Vx = V(n_y) / V(n_x), use "n_y" as the node label for Vy ***
```

```
* MP4 both provides gain to the second stage and provides most of the node
* capacitance to the first stage, hence it's sizing is a delicate balance.
MP4     n_w     n_x       n_vdd  n_vdd  pmos114 w=6.0u l=1.0u
MP5     n_y     0         n_w    n_vdd  pmos114 w=6.0u l=1.0u
MN6     n_y     n_bias_n  n_vss  n_vss  nmos114 w=3.0u l=2.0u
* We used asymmetry on MN6 in order to make Vy faster, and allow a higher Vov on
* MN6 however it made selecting the resistor values a lot tougher.

* These resistors provide the second stage gain, when combined with gm4.
* Asymmetry in MN6:MP4 sizing leads to a bit of a wonky ratio as they need to
* accoutn for the imbalanced current.
R3      n_y     0         168100
R4      n_y     n_vss     34400

*** Vz/Vy = V(n_z) / V(n_y), use "n_z" as the node label for Vz ***
* The size of these transistors sets up the gain of the third stage. Here it's
* approximately sqrt(2)
MN7     n_z     n_y       n_vss  n_vss  nmos114 w=2.0u l=1.0u
MP8     n_z     n_z       n_vdd  n_vdd  pmos114 w=2.0u l=1.0u

*** Vout/Vz = V(n_vout) / V(n_z), use "n_vout" as the node label for Vout ***
* MN10 is very tricky to bias right. You need to account for it's large Vt due
* to backgate and you tend to have a lot of error stacked up by the time that Vz
* is biased. Hence it required a small amount of monkeying to get it just right
* after we hand calculated the values.
MN9     n_vout  n_bias_n  n_vss  n_vss  nmos114 w=5.0u l=2.0u
MN10    n_vdd   n_z       n_vout n_vss  nmos114 w=28.0u l=1.0u

*** Your Bias Circuitry goes here ***

* This design is a self-biasing delta-Vgs / constant gm reference with startup
* circuit. The design was taken from lecture notes 14.

* These transistors provide the PMOS bias
MP100   n_bias_n n_bias_p n_vdd n_vdd  pmos114 w=4u  l=2u
MP200   n_bias_p n_bias_p n_vdd n_vdd  pmos114 w=4u  l=2u

* These transistors provide the NMOS bias and are the source of the delta
* Vgs reference. The ratio between the widths of these transistors defines m.
MN300   n_bias_n n_bias_n n_vss n_vss  nmos114 w=2u  l=2u
MN400   n_bias_p n_bias_n n_biasr2   n_vss  nmos114 w=4u l=2u

* This resistor is the denominator of the reference vov equation.
R200    n_biasr2 n_vss  16.7k

* These transistors are the startup circuit that enforces that it stay at
* the upper stable point, as the system is bistable.
MP800   n_biasn9 n_bias_n n_vdd n_vdd pmos114 w=2u  l=9u
MN700   n_biasn9 n_bias_n n_vss n_vss nmos114 w=5u  l=2u
MN900   n_bias_p n_biasn9 n_vss n_vss nmos114 w=4u  l=2u

*** defining the analysis ***
.op
.option post brief nomod

** For ac simulation uncomment the following line**
.ac dec 1k 100 1g

.measure ac gainmax_vout max vdb(n_vout)
.measure ac f3db_vout when vdb(n_vout)='gainmax_vout-3'

.measure ac gainmax_vx max vdb(n_x)
.measure ac f3db_vx when vdb(n_x)='gainmax_vx-3'
```

```
.measure ac gainmax_vy max vdb(n_y)
.measure ac f3db_vy when vdb(n_y)='gainmax_vy-3'

.measure ac gainmax_vz max vdb(n_z)
.measure ac f3db_vz when vdb(n_z)='gainmax_vz-3'

** For transient simulation uncomment the following line **
*.tran 0.01u 4u

.end
```

7.2 SPICE .op Output

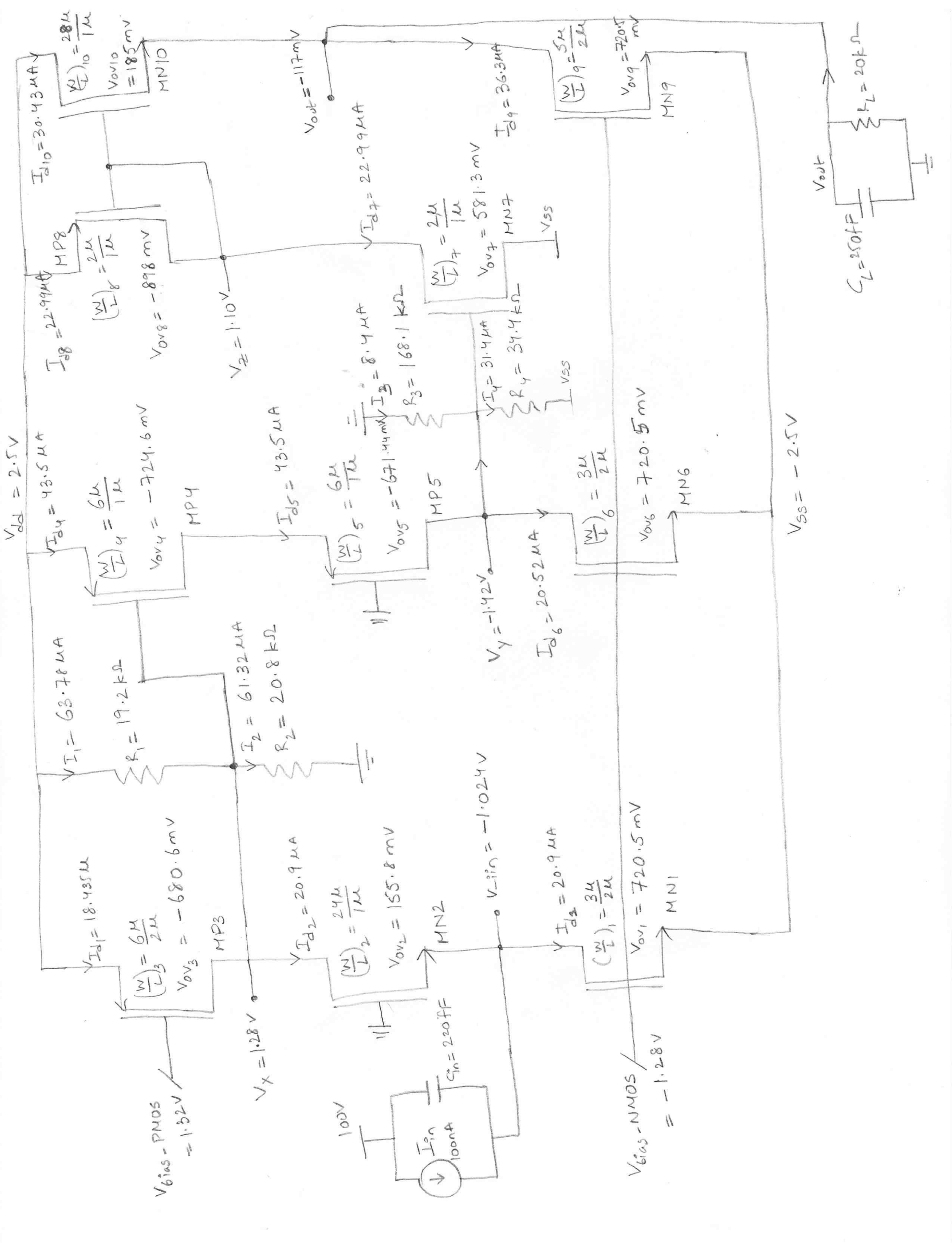
```
 ****** HSPICE -- I-2013.12-SP2 64-BIT (May 27 2014) RHEL64 ******
  Copyright (C) 2014 Synopsys, Inc. All Rights Reserved.
  Unpublished-rights reserved under US copyright laws.
  This program is protected by law and is subject to the
  terms and conditions of the license agreement from Synopsys.
  Use of this program is your acceptance to be bound by the
  license agreement. HSPICE is the trademark of Synopsys, Inc.
  Input File: Final_Samuel_Lenius_Usha_Kankanala_1p0_34p6_93p0_3043.sp
  Command line options: Final_Samuel_Lenius_Usha_Kankanala_1p0_34p6_93p0_3043.sp
 lic:
 lic: FLEXlm: v10.9.8
 lic: USER:   lenius               HOSTNAME: corn27.stanford.edu
 lic: HOSTID: 001b213a6bad         PID:      9885
 lic: Using FLEXlm license file:
 lic: 27000@cadlic0
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 09-jan-2016/2015.06
 lic: 2(in_use)/200(total) FLOATING license(s) on SERVER 27000@cadlic0
 lic:


 ******************************************************************************
 ******  option summary
 ******
 runlvl  = 3         bypass  = 2
 **info** dc convergence successful at Newton-Raphson method
 ****** HSPICE -- I-2013.12-SP2 64-BIT (May 27 2014) RHEL64 ******
 ******
 * design problem, ee114/214a-2015

 ****** operating point information tnom=  25.000 temp=  25.000 ******
 ****** operating point status is all       simulation time is     0.
    node    =voltage       node    =voltage       node    =voltage

 +0:n_bias_n=  -1.2795  0:n_bias_p=   1.3194  0:n_biasn9=  -1.9549
 +0:n_biasr2=  -2.2972  0:n_iin   =  -1.0243  0:n_vdd   =   2.5000
 +0:n_vout  =-117.4867m 0:n_vss   =  -2.5000  0:n_w     =   1.4507
 +0:n_x     =   1.2754  0:n_y     =  -1.4186  0:n_z     =   1.1019


 **** voltage sources

 subckt
 element  0:vdd      0:vss
  volts      2.5000    -2.5000
  current -236.5422u  189.5402u
  power    591.3555u  473.8505u

     total voltage source power dissipation=    1.0652m       watts


```

```

**** current sources

subckt
element  0:iin
 volts      -1.0243
 current     0.
 power       0.


    total current source power dissipation=   0.            watts

**** resistors

subckt
element  0:rl        0:r1        0:r2        0:r3        0:r4        0:r200
 r value   20.0000k   19.2000k   20.8000k  168.1000k   34.4000k   16.7000k
 v drop  -117.4867m    1.2246     1.2754    -1.4186     1.0814   202.7945m
 current   -5.8743u   63.7831u   61.3156u   -8.4393u   31.4349u   12.1434u
 power    690.1559n   78.1111u   78.1997u   11.9723u   33.9924u    2.4626u



**** mosfets


subckt
element  0:mn1       0:mn2       0:mp3       0:mp4       0:mp5       0:mn6
model    0:nmos114. 0:nmos114. 0:pmos114. 0:pmos114. 0:pmos114. 0:nmos114.
region     Saturati   Saturati   Saturati   Saturati   Saturati   Saturati
 id        20.9028u   20.9028u  -18.4353u  -43.5146u  -43.5146u   20.5190u
 ibs        0.       -14.7571f    0.         0.        10.4928f    0.
 ibd      -14.7571f  -37.7536f   12.2464f   10.4928f   39.1864f  -10.8136f
 vgs        1.2205     1.0243    -1.1806    -1.2246    -1.4507     1.2205
 vds        1.4757     2.2997    -1.2246    -1.0493    -2.8694     1.0814
 vbs        0.        -1.4757     0.         0.         1.0493     0.
 vth      500.0000m  868.4718m -500.0000m -500.0000m -779.2740m  500.0000m
 vdsat    720.4904m  155.8143m -680.6195m -724.6359m -671.4420m  720.4904m
 vod      720.4904m  155.8143m -680.6195m -724.6359m -671.4420m  720.4904m
 beta      80.5339u    1.7220m   79.5924u  165.7393u  193.0403u   79.0551u
 gam eff  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m
 gm        58.0239u  268.3046u   54.1721u  120.1006u  129.6154u   56.9584u
 gds      973.3246n    1.6995u  868.5804n    3.9382u    3.3813u  973.3246n
 gmb       19.4618u   53.3569u   18.1699u   40.2830u   28.5941u   19.1044u
 cdtot      5.3930f   27.9761f    9.8099f   10.0272f    7.8875f    5.6372f
 cgtot     12.3208f   72.3462f   24.6430f   15.3124f   15.3250f   12.3136f
 cstot     16.1000f   74.6671f   31.0001f   21.8000f   19.2080f   16.1000f
 cbtot      9.3595f   32.7274f   16.5627f   16.7010f   11.9148f    9.6109f
 cgs       10.7000f   56.9335f   21.4001f   12.2000f   12.2000f   10.7000f
 cgd        1.5272f   14.1975f    3.0451f    3.0193f    3.0528f    1.5199f



subckt
element  0:mn7       0:mp8       0:mn9       0:mn10      0:mp100     0:mp200
model    0:nmos114. 0:pmos114. 0:nmos114. 0:nmos114. 0:pmos114. 0:pmos114.
region     Saturati   Saturati   Saturati   Saturati   Saturati   Saturati
 id        22.9857u  -22.9857u   36.3091u   30.4348u  -13.7696u  -12.2647u
 ibs        0.         0.         0.       -23.8251f    0.         0.
 ibd      -36.0186f   13.9814f  -23.8251f  -50.0000f   37.7951f   11.8062f
 vgs        1.0814    -1.3981     1.2205     1.2194    -1.1806    -1.1806
 vds        3.6019    -1.3981     2.3825     2.6175    -3.7795    -1.1806
 vbs        0.         0.         0.        -2.3825     0.         0.
 vth      500.0000m -500.0000m  500.0000m    1.0337  -500.0000m -500.0000m
```

```
 vdsat     581.3598m -898.1364m  720.4904m  185.6306m -680.6195m -680.6195m
 vod       581.3598m -898.1364m  720.4904m  185.6306m -680.6195m -680.6195m
 beta      136.0186u   56.9907u  139.8907u    1.7664m   59.4488u   52.9515u
 gam eff   600.0000m  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m
 gm         79.0758u   51.1854u  100.7899u  327.9067u   40.4620u   36.0399u
 gds         1.6899u    2.0166u    1.6222u    2.4121u  579.0536n  579.0536n
 gmb        26.5228u   17.1681u   33.8060u   55.1425u   13.5714u   12.0881u
 cdtot       3.6813f    4.2306f    7.0089f   26.8604f    5.7669f    7.1139f
 cgtot       5.1272f    5.1004f   20.5625f   72.0600f   16.4914f   16.4276f
 cstot       8.6667f    8.6667f   24.8334f   72.6537f   21.3667f   21.3667f
 cbtot       7.2976f    7.8472f   11.5918f   29.2575f   10.9061f   12.3169f
 cgs         4.0667f    4.0667f   17.8334f   56.9335f   14.2667f   14.2667f
 cgd         1.0221f    1.0086f    2.5731f   14.2248f    2.0927f    2.0290f



subckt
element  0:mn300    0:mn400    0:mp800    0:mn700    0:mn900
model    0:nmos114. 0:nmos114. 0:pmos114. 0:nmos114. 0:nmos114.
region      Saturati   Saturati   Saturati     Linear   Saturati
 id         13.7696u   12.1434u  -31.3543u   31.3543u  121.3242n
 ibs         0.         -2.0279f    0.          0.          0.
 ibd       -12.2049f  -38.1938f   44.5486f   -5.4514f  -38.1938f
 vgs         1.2205     1.0177    -3.7795     1.2205   545.1376m
 vds         1.2205     3.6166    -4.4549   545.1376m    3.8194
 vbs         0.      -202.7945m    0.          0.          0.
 vth       500.0000m  564.1814m -500.0000m  500.0000m  500.0000m
 vdsat     720.4904m  453.5145m   -3.2795   545.1376m   45.1376m
 vod       720.4904m  453.5145m   -3.2795   720.4904m   45.1376m
 beta       53.0512u  118.0829u    5.8305u  128.4071u  119.0969u
 gam eff   600.0000m  600.0000m  600.0000m  600.0000m  600.0000m
 gm         38.2229u   53.5523u   19.1213u   69.9995u    5.3757u
 gds       648.8830n  514.1885n  331.9501n   24.0427u    5.0935n
 gmb        12.8204u   16.0433u    6.4135u   23.4786u    1.8031u
 cdtot       4.4573f    5.5601f    3.5781f   13.8464f    5.5651f
 cgtot       8.2107f   16.5346f   29.9091f   25.3172f   17.7794f
 cstot      11.7334f   20.0468f   33.2001f   24.2459f   20.4667f
 cbtot       8.1048f    9.4306f    6.9952f   13.0872f   11.0903f
 cgs         7.1334f   14.2667f   28.6001f   17.2459f   14.2667f
 cgd         1.0150f    2.0887f    1.2459f    7.9152f    2.0937f



******
* design problem, ee114/214a-2015

****** ac analysis tnom=  25.000 temp=  25.000 ******
gainmax_vout= -49.2028     at=   5.3333k
            from= 100.0000     to=   1.0000g
f3db_vout=  92.9703x
gainmax_vx= -60.1155     at=  36.1410k
            from= 100.0000     to=   1.0000g
f3db_vx= 131.9439x
gainmax_vy= -49.8772     at=  21.4289k
            from= 100.0000     to=   1.0000g
f3db_vy= 108.3150x
gainmax_vz= -46.7065     at=  21.3304k
            from= 100.0000     to=   1.0000g
f3db_vz= 105.6056x

         ***** job concluded
****** HSPICE -- I-2013.12-SP2 64-BIT (May 27 2014) RHEL64 ******
******
* design problem, ee114/214a-2015
```

```
 ****** job statistics summary tnom=  25.000 temp=  25.000 ******


 ******  Machine Information  ******
CPU:
model name	: Quad-Core AMD Opteron(tm) Processor 2384
cpu MHz		: 800.000

OS:
Linux version 3.13.0-53-generic (buildd@phianna) (gcc version 4.8.2 (Ubuntu 4.8.2-19ubuntu1) ) #89-Ubuntu SMP Wed May 20 10:34:39 UTC 2015


  ******  HSPICE Threads Information  ******

  Command Line Threads Count :     1
  Available CPU Count        :     8
  Actual Threads Count       :     1


  ******  Circuit Statistics  ******
  # nodes       =      13 # elements   =      28
  # resistors   =       6 # capacitors =       2 # inductors   =       0
  # mutual_inds =       0 # vccs       =       0 # vcvs        =       0
  # cccs        =       0 # ccvs       =       0 # volt_srcs   =       2
  # curr_srcs   =       1 # diodes     =       0 # bjts        =       0
  # jfets       =       0 # mosfets    =      17 # U elements  =       0
  # T elements  =       0 # W elements =       0 # B elements  =       0
  # S elements  =       0 # P elements =       0 # va device   =       0
  # vector_srcs =       0 # N elements =       0


  ******  Runtime Statistics (seconds)  ******

  analysis           time    # points   tot. iter  conv.iter
  op point           0.00           1          10
  ac analysis        0.08        7001        7001
  readin             0.01
  errchk             0.00
  setup              0.00
  output             0.00


           peak memory used        176.94 megabytes
           total cpu time            0.09 seconds
           total elapsed time        1.19 seconds
           job started at     06:46:11 12/04/2015
           job ended   at     06:46:13 12/04/2015


lic: Release hspice token(s)
lic: total license checkout elapse time:        1.01(s)
```

7.3 Amplifier - Enlarged



7.4 Bias Circuit - Enlarged