2015 EE214A Design Project

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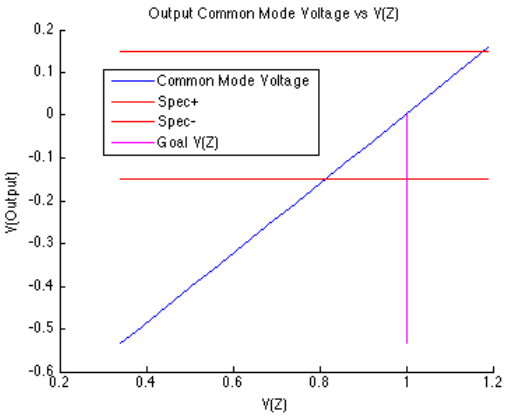
Abstract

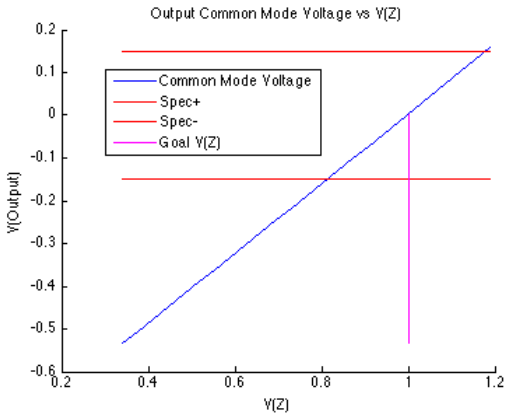
Area Breakdown:

- PMOS Bias Gen: 25%
- NMOS Bias Gen: 25%
- Core circuit: 25%
- Resistors: 25%

1 Design Outline

O ur approach to this design was to first develop sizing ratios of the transistors and their DC relationships to Vx, Vy, Vz and Vo. We developed the equations necessary to 'program' those voltages and to develop what their reasonable ranges are. Here are some graphs that show the relationships between the output common mode voltage and Vz, and then Vz to Vy given our sizing decisions. We developed a MATLAB program to quickly estimate critical parameters for a given design, to allow easy investigation of parametric variation.





These graphs give rise to a process to choose exactly the value of those voltages based on the size of the transistors. Here, given the common mode output spec, choosing a size for MN10, and estimating the MN10 backgate gives the needed value of Vz. Given a size ratio for MN7 to MP8 gives the needed value of Vy, knowing Vz. Given the size ratio for MP4 to MN6 and knowing the value of Vy gives the gives the necessary ratio of R3 to R4 to program the value of Vy.

2 Design Schematic

Text of design schematic

3 Calculation of Key Design Parameters

Choice of L

- All devices used in current source have a minimum length of 2um.
- All other devices in the amplifier have minimum length of 1um. Mimimum length is used as $f_t$is inversely proportional to L.
- All devices in bias generator circuit have length >=2um.

Bias Generator circuit

- Constant gm reference based design is used as bias circuit to reduce mismatch errors.
- Transconductance of bias device (mn300) depends only on R2 and m (m is the ratio of MN300/MN400). Therefore gm can be set precisely.
- Start-up circuit is used to force the circuit to the desired operating point.

Approximations for hand calculations
For simpler hand calculations, following approximations are used.

1. $Cdb = Csb = 0.35Cgs$
2. $Cgs = (\frac{2}{3})WLCox + Cov'W$
3. $Cgd = Cov'W$
4. $gmb = 0.2gm$

Stage4

- As per the spec, common mode output voltage (vout) has to be within -0.15v to 0.15v. Since the body is connected to vss, MN10 experiences back gate effect and the threshold voltage is given by

$Vt = Vt0+?(\sqrt{2\emptyset f + Vsb} - \sqrt{2}\emptyset f$ where $t0 = 0.5v$, $? = 0.6$, $2\emptyset f = 0.8$

- Stage 4 is a source follower which has a gain given by $A4 = \frac{gm10}{gm10+gmb10+(\frac{1}{RL})}$

Gain of stage4 (A4) <1 due to back gate effect and the output load.

1. To achieve gain closer to 1 (0.6 - 0.7), it is important to size and bias MN10 such that (gm10+ gmb10) >> (1/RL).
    - Transconductance of gm10 is given by $gm10 = \mu nCox(\frac{W}{L})Vov10$

Drain current $Id10 = 0.5\mu nCox(\frac{W10}{L10})Vov10^2(1 + \lambda(Vdd - Vout)$

- MN9 (bias device for source follower) is sized such that I_{d10}+ I_{RL}= $I_{d9}$and the common mode output voltage does not fall out of range. This device is chosen to be of smaller size to reduce loading on Vout node.
- $\tau stage4(atVout) = (RL||(\frac{1}{1.2gm10}))(CL + Csb10 + Cgd9 + Cdb9)$

Cgs10 is assumed to be very small due to boot-strapping.

Stage 3

- Loading at node Vy increases with the increase in gain of stage 3 due to miller effect. Hence gain of stage3 is kept low and is fixed at sqrt(2) to compensate for the gain lost in stage 4.

Gain of stage3 (CS amplifier with diode connected load)

$abs(A3) = \frac{gm7}{gm8} = \frac{Vov8}{Vov7} = \frac{Vdd-Vz-abs(Vtp)}{Vy-Vss-Vtn} = \sqrt{2}$

Choice of Vz from above (stage4) determines Vy.

- Minimum device sizes (W=2um, L=1um) are used for both MN7 and MP8 to reduce loading on Vy and Vz.

Drain current $Id7 = Id8 = 0.5\mu nCox(\frac{W7}{L7})Vov7^2(1 + \lambda(Vz - Vss)$

- $\tau stage3(atVz) = (\frac{1}{gm8})(Cgs8 + Cdb8 + Cgd10 + Cgd7(1 + \frac{1}{abs(A3)}) + Cdb7)$

Stage 2

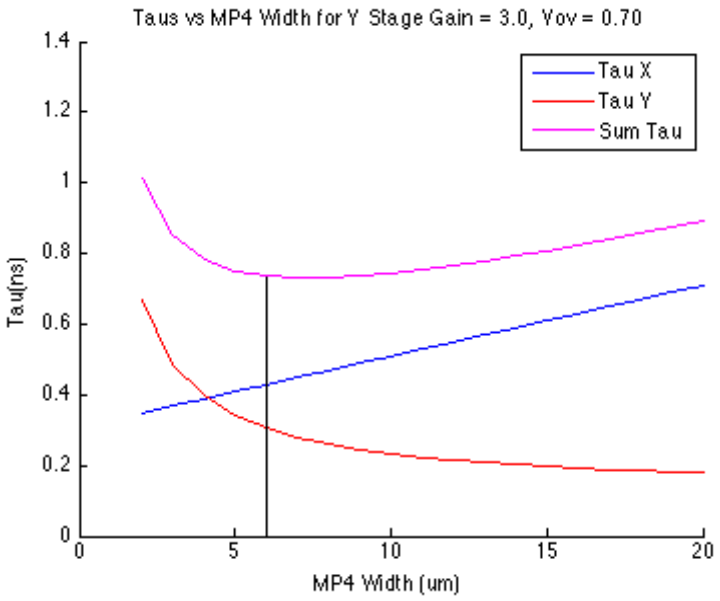
- Vy from stage 3 above determines the ratio of R3 and R4.

$y(\frac{R4}{R3}) = \frac{Vss}{Vy} - 1$

- Gain of stage 2 (Cascode amplifier) is set to 3.

$abs(A2) = gm4(R3||R4)$

- Vov4 and $W_4$are optimized to reduce $\tau stage3$ at Vx.



- MN6 is sized such that current through MN6 is same as the current through MP4 and MP5.

$Id4 = Id5 = Id6 = 0.5\mu pCox(\frac{W4}{L4})(Vdd - Vx - abs(Vtp))^2(1 + \lambda(Vdd - Vw)$

- Current through R3 and R4

$IR3 + R4 = Vss/(R3 + R4)$

- $\tau stage2(Vy)$

$= (R3||R4)(Cgs7 + Cgd7(1 + abs(A3)) + Cgd6 + Cdb6 + Cgd5 + Cdb5)$

Stage 1

- Vov4 from stage 2 sets Vx which in turn sets the ratio of R1 and R2.

  $Vov4 = Vdd - Vx - abs(Vtp)$

  $x(\frac{R1}{R2}) = \frac{Vdd}{Vx} - 1$

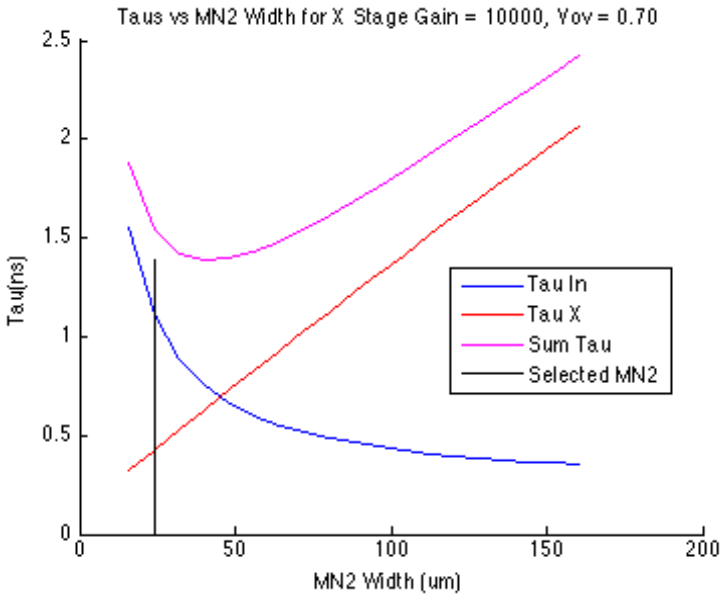
- Gain of stage 1 (Common gate amplifier) is set to 10000.

$abs(A1) = (R1||R2)$

- MN1 and MP3 are sized such that Id1 = Id3.
- MN2 is sized to reduce Tau at n_iin node. Tau (n_iin) is inversely proportional to gm2.

$\tau stage1(n_iin) = (\frac{1}{gm2})(Cin + Cgd1 + Cdb1 + Cgs2 + Csb2)$

$\tau stage1(Vx) = (R1||R2)(Cgd2 + Cbd2 + Cgd3 + Cdb3 + Cgs4 + Cgd4(2))$



- Current through MN1, MN2 and MP3

$Id1, 2, 3 = 0.5\mu pCox(\frac{W3}{L3})(Vdd - VbiasP - abs(Vtp))^2(1 + \lambda(Vdd - Vx))$

- Current through R1 and R2

$IR1 + R2 = Vdd/(R1 + R2)$

Vovn, Vovp

- Vovn and Vovp are chosen to achieve a reasonable balance between gain, Tau total and Power.

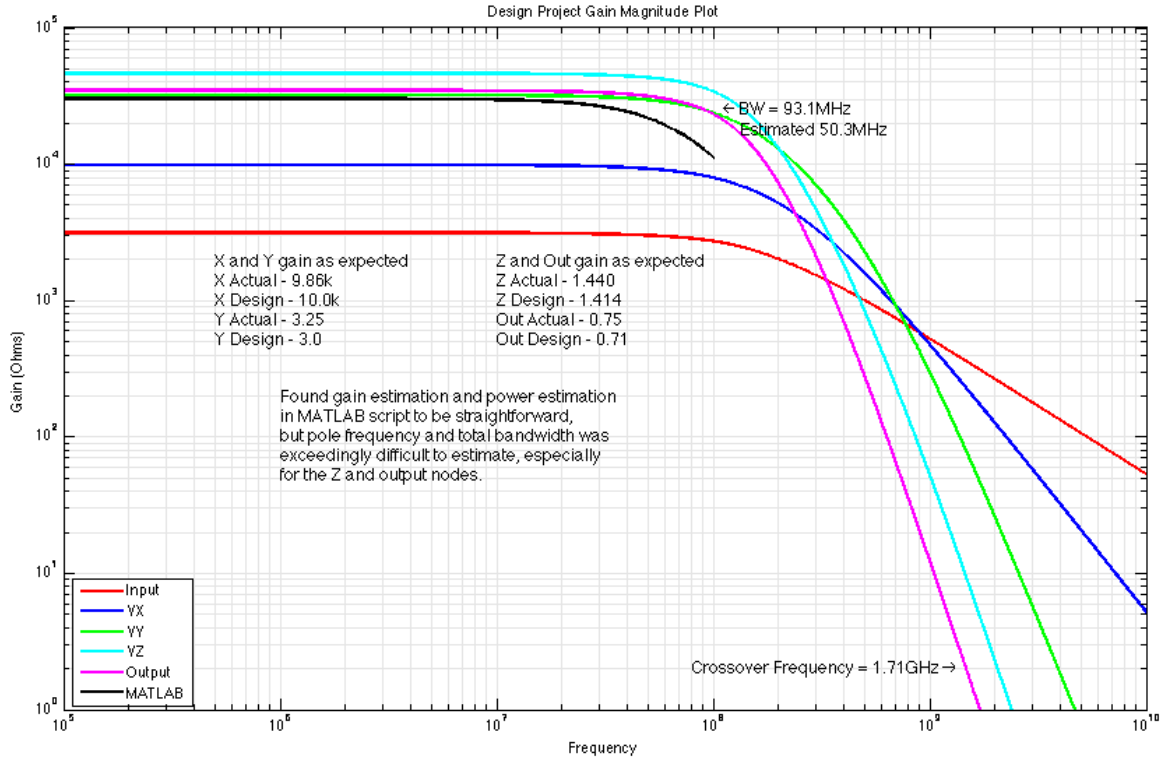
$Gaintotal(A) = A1A2A3A4$

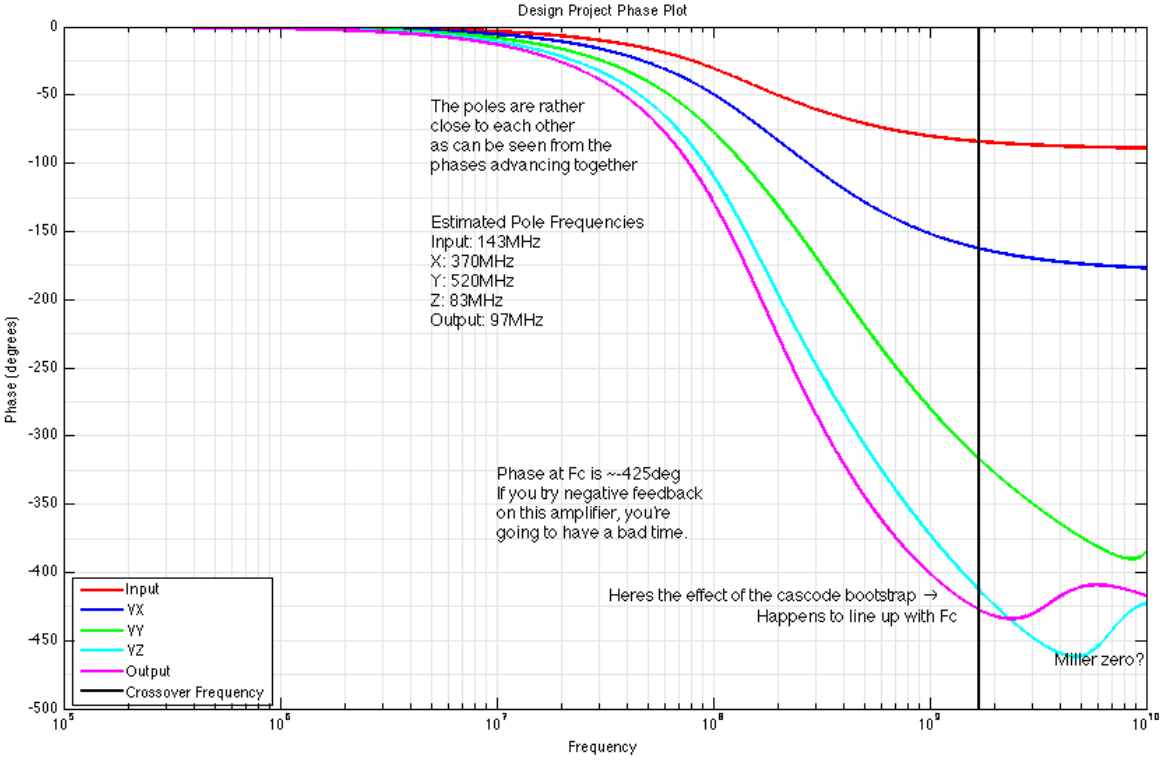
$\tau total = \tau stage1(n_{iin}) + \tau stage1(Vx) + \tau stage2(Vy) + \tau stage3(Vz) + \tau stage1(Vout)$

$Power = (Vdd - Vss)(Id1 + Id4 + Id7 + Id10) + (\frac{Vdd^2}{R1+R2}) + (\frac{Vss^2}{R3+R4})$

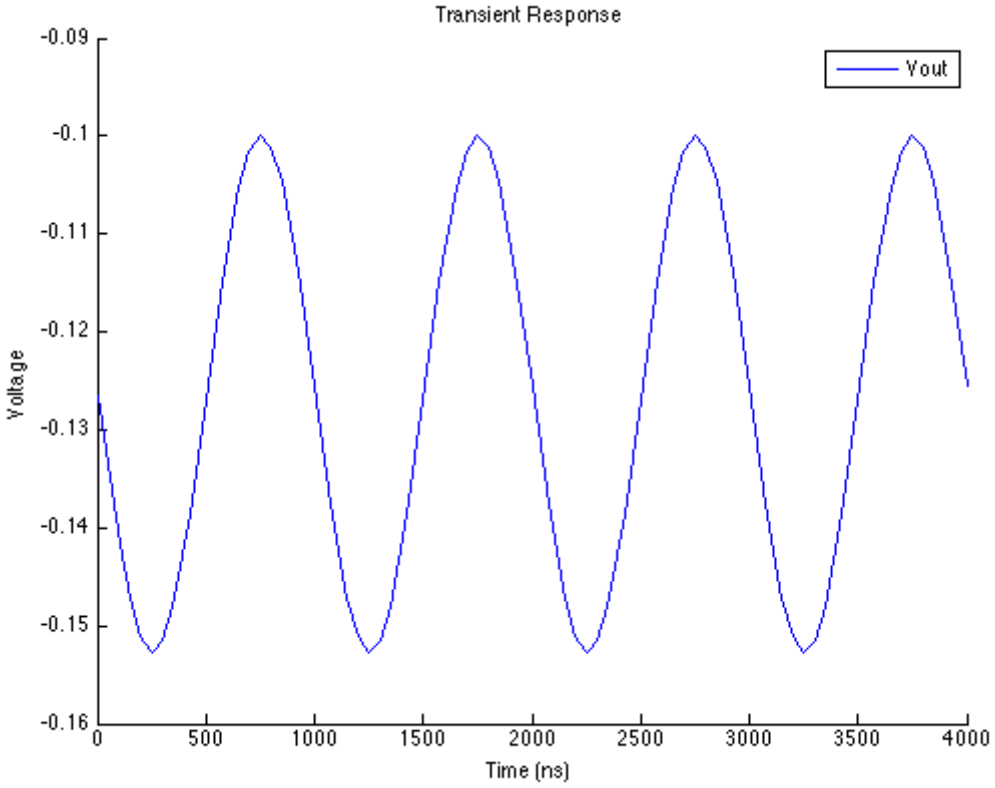
Stage1	Hand calculation	Spice	%Error	Reason for error
Id1				
Vx				
A1 (Gain of stage1)				
gm2				
Tau (iin)				
Stage2	Hand calculation	Spice	%Error	Reason for error
Id4				
Vw				
Vy				
gm4				
A2 (Gain of stage2)				
Tau (Vy)				
Stage3	Hand calculation	Spice	%Error	Reason for error
Id7				
Vz				
gm7				
gm8				
A3 (Gain of stage3)				
Tau (Vz)				
Stage4	Hand calculation	Spice	%Error	Reason for error
Id10				
Vout				
Vt10				
gm10				
gmb10				
A4 (Gain of stage4)				
Tau (vout)				
Total Power				
Total Gain				

4 Simulated Bode Plots





5 Simulated Transient Response



6 Comments and Conclusion

- Resistors contribute to a large part of the overall gain. From manufacturability perspective, passive components are not friendly and also occupy more area on the chip.
- The output source follower stage is very sensitive to biasing due to back gate effect. Small variations on Vz can drive the output to fall out of desired common mode voltage or drive MN10 into cutoff region and lose all the gain from previous stages.
- Any variations in supply voltage causes variation in Vov of MN7 directly (as the device is biased through R3 & R4) causing Vz to vary and thereby impacting the biasing of MN10 and gain.
- Common source stage with diode connected load attributes to miller cap loading effect on cascade stage. This is limiting the gain of common source stage to smaller values.
- Since the output is single ended, it is susceptible to noise. Differential configuration will be better.

7 Appendix I

Netlist here