2015 EE214A Design Project

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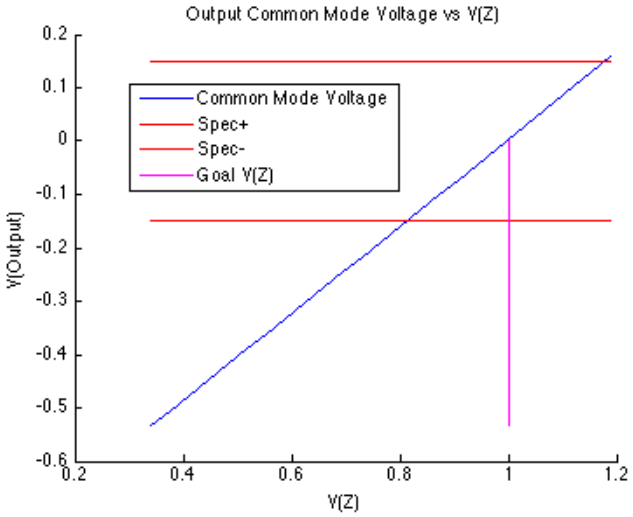
December 4, 2015

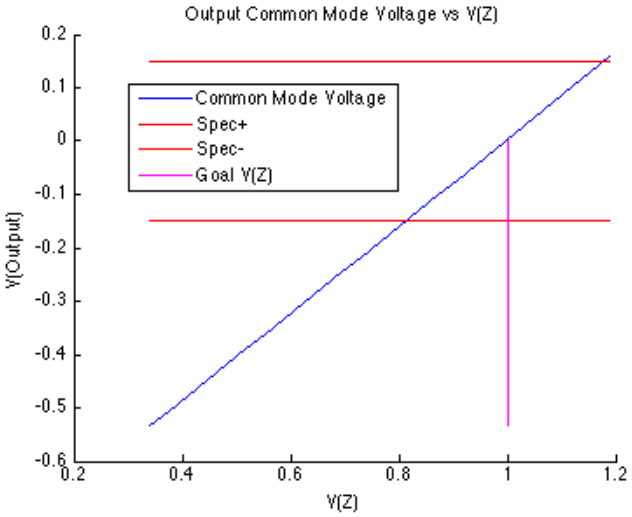
Specfications	Given Spec	Achieved Spec
Gain	30kΩ	34.7kΩ
Bandwidth	90MHz	93MHz
Power	2.0mW	1.0mW
FOM	1350	3043

Area Breakdown	% Core Area	Area (um)
Core Area	100%	$112\mu m^2$
VNMOS-bias	19.6%	$22\mu m^2$
VPMOS-bias	10.7%	$12\mu m^2$
Bias Generator	73.1%	$82\mu m^2$

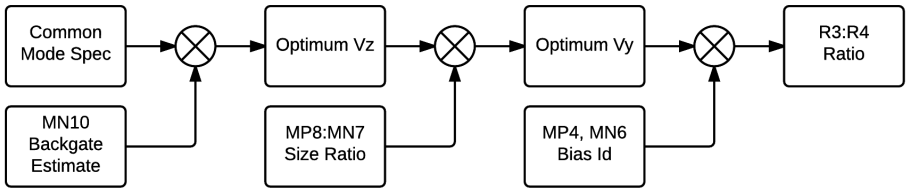
1 Design Outline

Our approach to this design was to first develop sizing ratios of the transistors and their DC relationships to Vx, Vy, Vz and Vo. We developed the equations necessary to 'program' those voltages and to develop what their reasonable ranges are. Here are some graphs that show the relationships between the output common mode voltage and Vz, and then Vz to Vy given our sizing decisions. We developed a MATLAB program to quickly estimate critical parameters for a given design, to allow easy investigation of parametric variation.

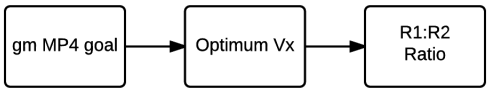




These graphs give rise to a process to choose exactly the value of those voltages based on the size of the transistors. Here, given the common mode output spec, choosing a size for MN10, and estimating the MN10 backgate gives the needed value of Vz. Given a size ratio for MN7 to MP8 gives the needed value of Vy, knowing Vz. Given the size ratio for MP4 to MN6 and knowing the value of Vy gives the gives the necessary ratio of R3 to R4 to program the value of Vy.



Similarly for Vx, given a goal for MP4 gm (from our chosen distribution of stage gain) we can solve for the ratio of R1 to R2 to program the value of Vx. Since we have set the K value of MN1 and MP3 equal, the voltage at Vx is selected purely by the ratio of R1 and R2.

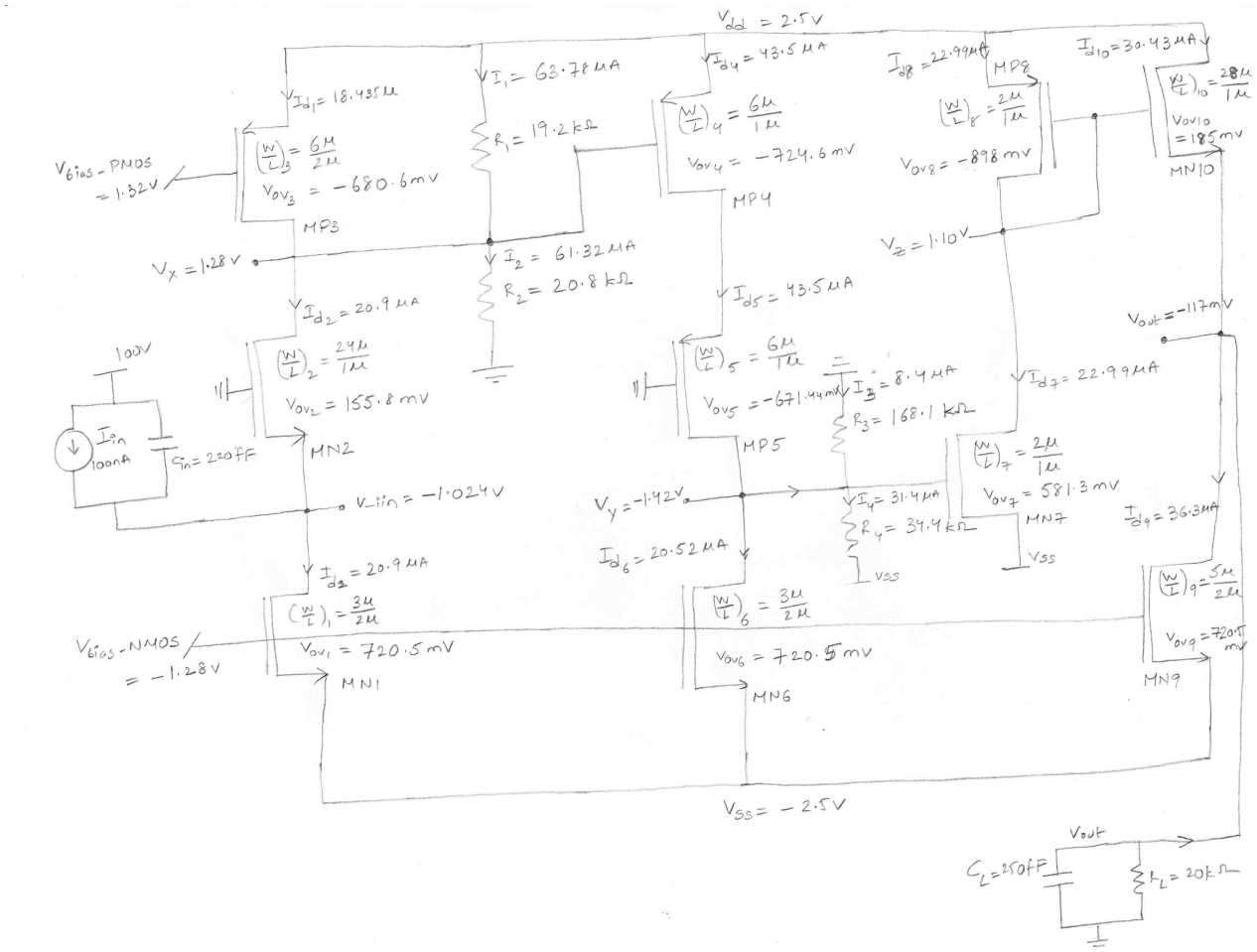


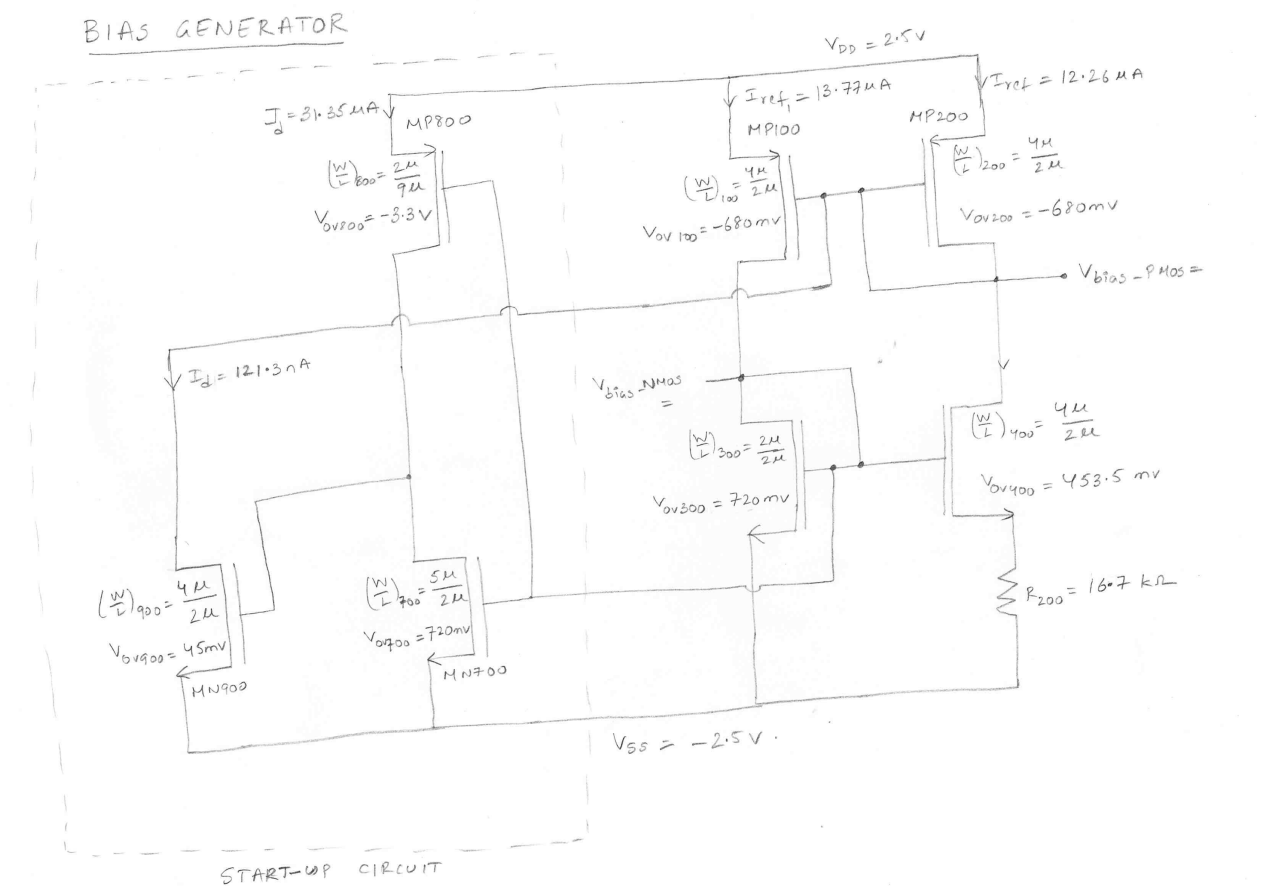
Once the math was developed to decouple the selection of stage gain to the DC biasing selection, the focus was on gain/speed. First we distributed the desired gain for each stage, then choose the vov level to drive the transistors based on the gm/Id plots, and then sized the transistors to minimize tau for adjacent stages.

The gain budget was based on the X stage having the most gain, since it's easy to get there, getting the balance of gain from the Y stage and then setting the Z stage to cancel out the gain loss of the output CD stage. Thus total gain simplifies to X * Y = 30k.

By making plots of the sum of tau for adjacent stages vs critical transistor sizing we were able to minimize total tau for the design, with the given gain budget.

2 Design Schematic





3 Calculation of Key Design Parameters

Choice of L

- All devices used in current source have a minimum length of 2μm.
- All other devices in the amplifier have minimum length of 1μm. Minimum length is used as f_t is inversely proportional to L.
- All devices in bias generator circuit have length >=2μm.

Bias Generator circuit

- Constant gm reference based design is used as bias circuit to reduce mismatch errors.
- Transconductance of bias device (mn300) depends only on R2 and m (m is the ratio of MN300/MN400). Therefore gm can be set precisely.
- Start-up circuit is used to force the circuit to the desired operating point.

Approximations for hand calculations

For simpler hand calculations, following approximations are used.

1. $Cdb = Csb = 0.35Cgs$
2. $Cgs = (\frac{2}{3})WLCox + Cov'W$
3. $Cgd = Cov'W$
4. $gmb = 0.2gm$

Stage4

- As per the spec, common mode output voltage (vout) has to be within -0.15v to 0.15v. Since the body is connected to vss, MN10 experiences back gate effect and the threshold voltage is given by:

$$\begin{aligned} Vt &= Vt_0 + \gamma(\sqrt{2\phi f + V_{sb}} - \sqrt{2}\phi f \\ Vt_0 &= 0.5V, \gamma = 0.6, 2\phi f = 0.8 \end{aligned} \tag{1}$$

- Stage 4 is a source follower which has a gain given by

$$A4 = \frac{gm_{10}}{gm_{10} + gmb_{10} + (\frac{1}{R_L})} \tag{2}$$

- Gain of stage4 (A4) <1 due to back gate effect and the output load.
- To achieve gain closer to 1 (0.6 - 0.7), it is important to size and bias MN10 such that $(gm_{10} + gmb_{10}) >> (1/R_L)$.
- Transconductance of and drain current of MN_{10} is given by

$$gm_{10} = \mu nCox(\frac{W}{L})vov_{10} \tag{3}$$

$$Id_{10} = 0.5\mu nCox(\frac{W_{10}}{L_{10}})vov_{10}^2(1 + \lambda(Vdd - Vout)) \tag{4}$$

- MN_9 (bias device for source follower) is sized such that $Id_{10} + I_{R_L} = Id_9$ and the common mode output voltage does not fall out of range. This device is chosen to be of smaller size to reduce loading on Vout node.

$$\tau_{OUTPUT} = (R_L || \frac{1}{1.2gm_{10}})(C_L + Csb_{10} + Cgd_9 + Cdb_9) \tag{5}$$

- Cgs10 is assumed to be very small due to boot-strapping.

Stage 3

- Loading at node Vy increases with the increase in gain of stage 3 due to the miller effect. Hence gain of stage3 is kept low and is fixed at sqrt(2) to compensate for the gain lost in stage 4. Gain of stage3 (CS amplifier with diode connected load):

$$|A3| = \frac{gm7}{gm8} = \frac{Vov8}{Vov7} = \frac{Vdd - Vz - abs(Vtp)}{Vy - Vss - Vtn} = \sqrt{2} \tag{6}$$

- Choice of Vz from above (stage4) determines Vy.
- Minimum device sizes (W=2μm, L=1μm) are used for both MN7 and MP8 to reduce loading on Vy and Vz.

$$Id_7 = Id_8 = 0.5\mu nCox(\frac{W_7}{L_7})vov_7^2(1 + \lambda(Vz - Vss)) \tag{7}$$

$$\tau_Z = (\frac{1}{gm_8})(Cgs_8 + Cdb_8 + Cgd_{10} + Cgd_7(1 + \frac{1}{|A3|}) + Cdb_7) \tag{8}$$

Stage 2

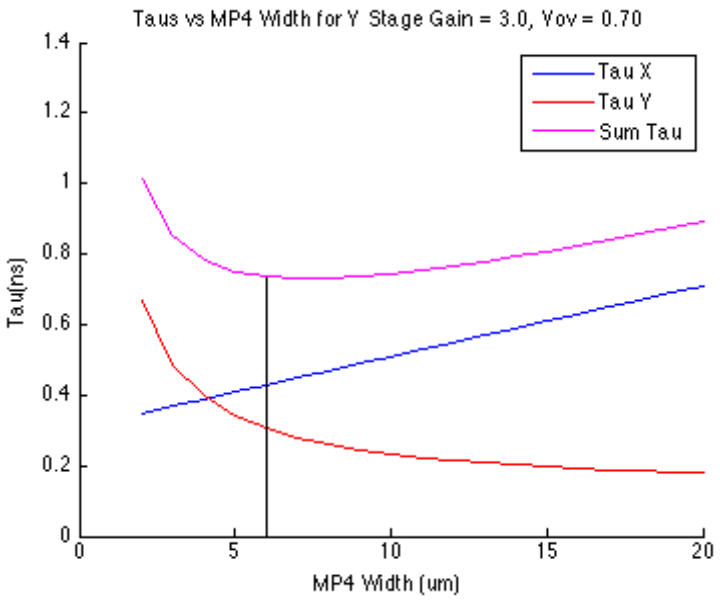
- Vy from stage Z above determines the required ratio of R3 and R4.

$$(\frac{R4}{R3}) = \frac{Vss}{Vy} - 1 \tag{9}$$

- Gain of stage Y (Cascode amplifier) is set to 3.

$$|A2| = gm4(R3||R4) \tag{10}$$

- Vov_4 and W_4 are optimized to reduce τ_X.



- MN6 is sized such that current through MN6 is same as the current through MP4 and MP5.

$$Id4 = Id5 = Id6 = 0.5\mu pCox(\frac{W4}{L4})(Vdd - Vx - abs(Vtp))^2(1 + \lambda(Vdd - Vw) \tag{11}$$

- Current through R3 and R4

$$I_{R3} + I_{R4} = Vss/(R3 + R4) \tag{12}$$

$$\tau_Y = (R3||R4)(Cgs_7 + Cgd_7(1 + |A3|) + Cgd_6 + Cdb_6 + Cgd_5 + Cdb_5) \tag{13}$$

Stage 1

- Vov_4 from stage 2 sets V_X which in turn sets the ratio of R1 and R2.

$$Vov_4 = Vdd - Vx - |Vtp| \tag{14}$$

$$(\frac{R1}{R2}) = \frac{Vdd}{Vx} - 1 \tag{15}$$

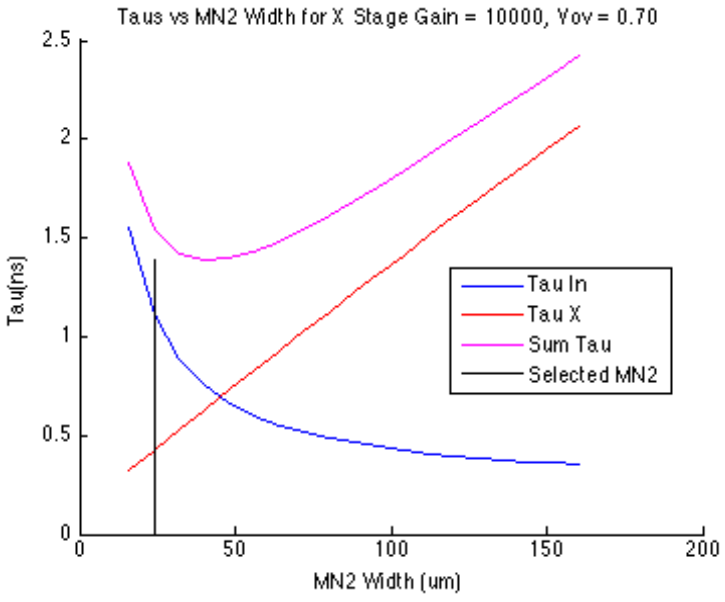
- Gain of stage 1 (Common gate amplifier) is set to 10000.

$$|A1| = (R1||R2) \tag{16}$$

- MN1 and MP3 are sized such that Id1 = Id3.
- MN2 is sized to reduce τ_{IIN} node. τ_{IIN} is inversely proportional to gm_2.

$$\tau_{IIN} = (\frac{1}{gm2})(Cin + Cgd_1 + Cdb_1 + Cgs_2 + Csb_2) \tag{17}$$

$$\tau_X = (R1||R2)(Cgd_2 + Cdb_2 + Cgd_3 + Cdb_3 + Cgs_4 + Cgd_4) \tag{18}$$



- Current through MN1, MN2 and MP3

$$Id_{1,2,3} = 0.5\mu pCox(\frac{W_3}{L_3})(Vdd - VbiasP - |Vtp|)^2(1 + \lambda(Vdd - Vx)) \tag{19}$$

- Current through R1 and R2

$$I_{R1} + I_{R2} = Vdd/(R1 + R2) \tag{20}$$

Vovn, Vovp

- Vovn and Vovp are chosen to achieve a reasonable balance between gain, Tau total and Power, and our choice was educated by the gm/Id technology plots.

Total Design Performance

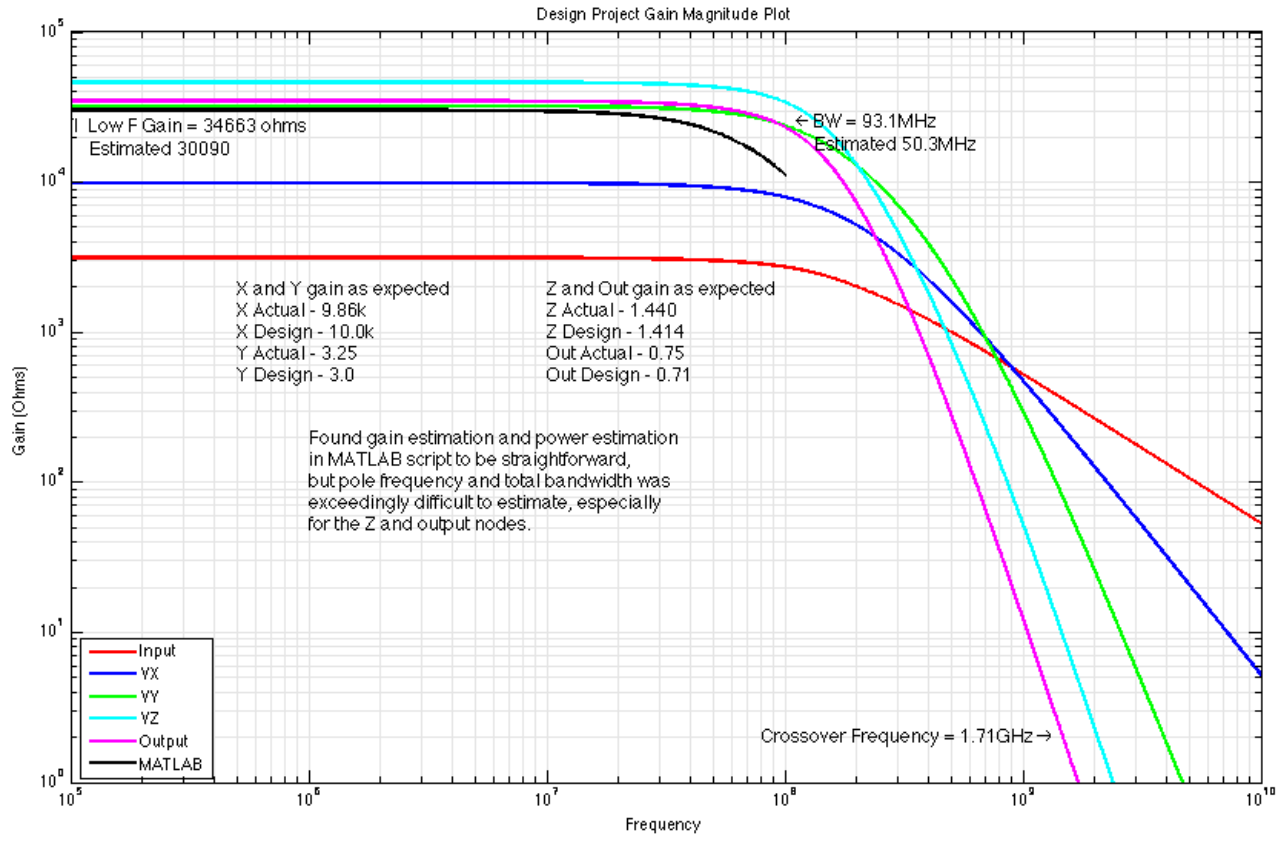
$$|A_{TOTAL}| = A1 * A2 * A3 * A4 \tag{21}$$

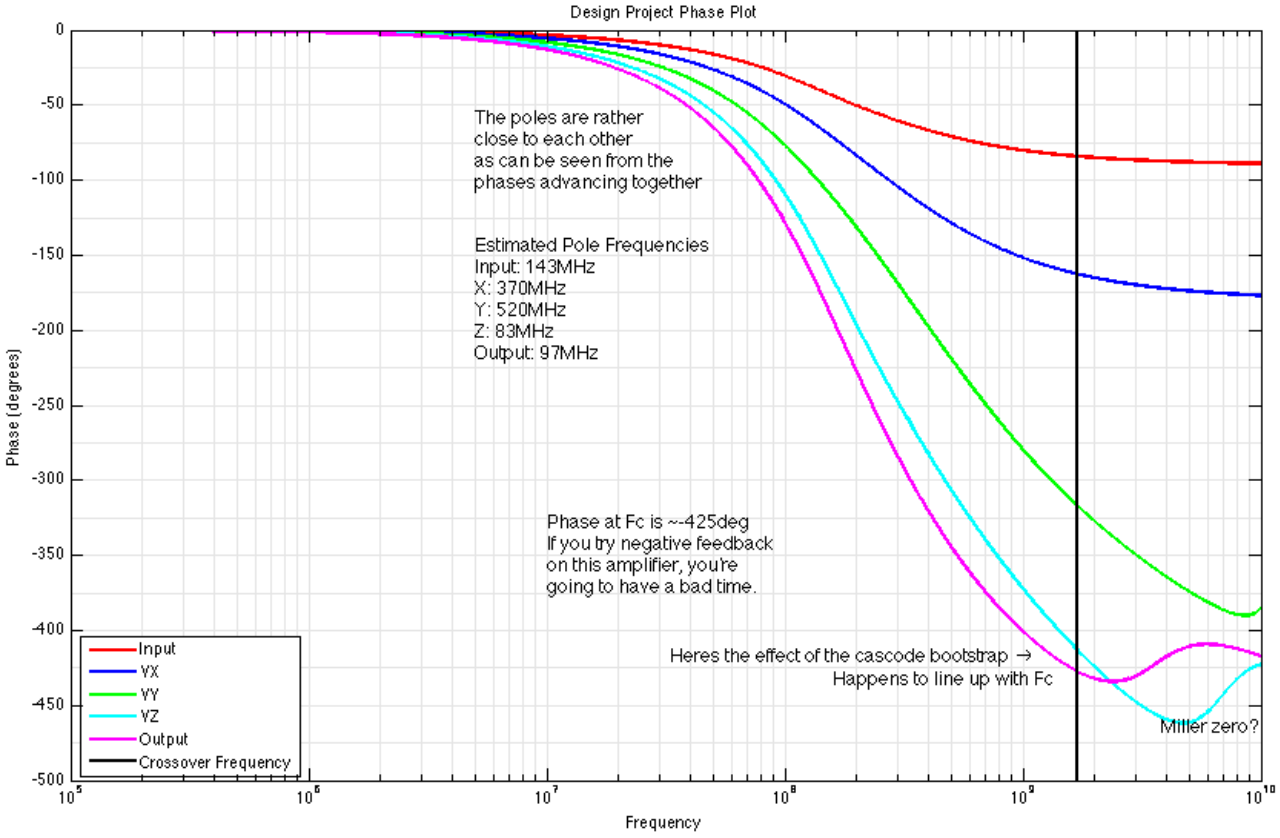
$$\tau_{TOTAL} = \tau_{IIN} + \tau_X + \tau_Y + \tau_Z + \tau_{OUTPUT} \tag{22}$$

$$Power = (Vdd - Vss)(Id_1 + Id_4 + Id_7 + Id_{10}) + (\frac{Vdd^2}{R1 + R2}) + (\frac{Vss^2}{R3 + R4}) \tag{23}$$

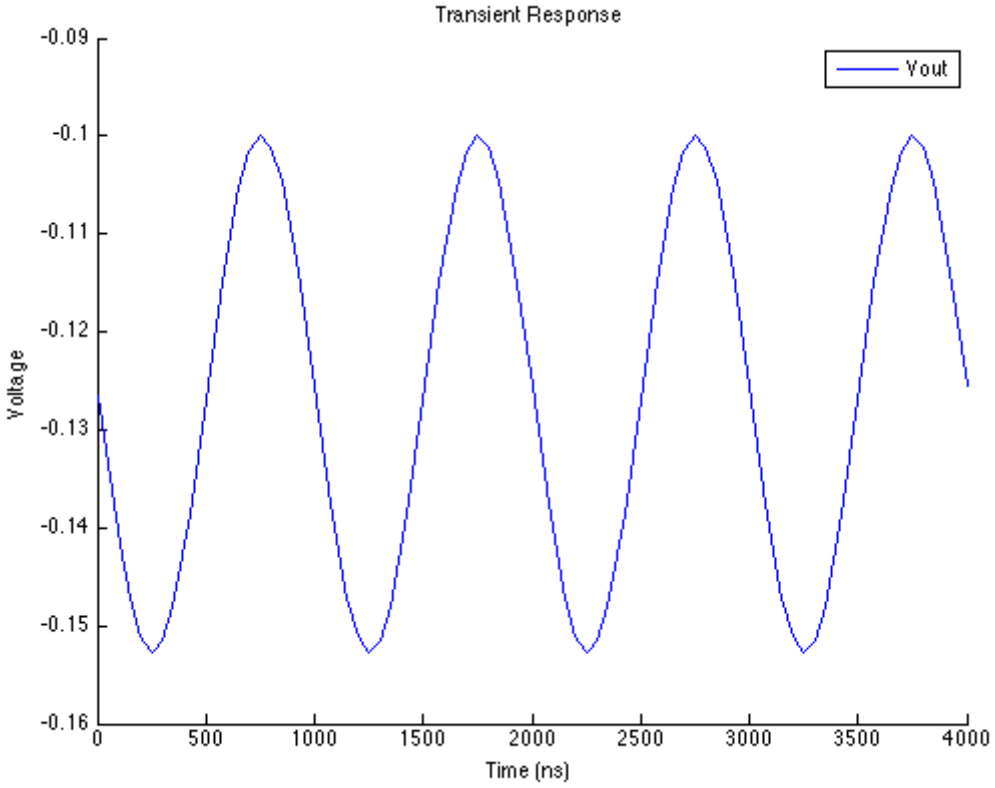
Bias Generator	Hand calc	Spice	%Error	Reason for error
V_{BiasN}	-1.300V	-1.279V	-1.6%	Startup circuit bias
V_{BiasP}	1.300V	1.319V	1.5%	Startup circuit bias
Stage1	Hand calc	Spice	%Error	Reason for error
Id_1	18.3μA	20.9μA	14.2%	Bias generator error
Vx	1.300V	1.275V	-1.9%	
A_X	10kΩ	9.86kΩ	-1.4%	Finite MN_1 and MP_3 output resistance
gm_2	210μS	268μS	27.6%	Bias generator error
τ_{IN}	1.11ns			
τ_X	420ps			
Stage2	Hand calc	Spice	%Error	Reason for error
Id_4	36.75μA	43.5μA	18.4%	
V_W	1.496V	1.450V	-3.2%	
V_Y	-1.550V	-1.418V	-8.5%	Imbalance between MP_4 and MN_6 current
gm_4	105μS	120μS	14.3%	Error in V_Y
A_Y	-3.0	-3.25	8.3%	Error estimating gm_4
τ_Y	306ps			
Stage3	Hand calc	Spice	%Error	Reason for error
Id_7	10.25μA	22.9μA	123%	Error in V_Y plus finite output resistance
V_Z	1.364	1.102V	-19.2%	Error in V_Y
gm_7	45μS	79μS	75.5%	Error in Id_7
gm_8	31.2μS	51μS	63.5%	Error in Id_7
A_Z	1.414	1.440	1.8%	The benefit of ratiometric design
τ_Z	1.92ns			Error in estimating gm_8
Stage4	Hand calc	Spice	%Error	Reason for error
Id_{10}	2.96μA	30.43μA	928%	MN_{10}'s large width is a big error amplifier
V_{OUT}	0.299	-0.117V	-139%	
Vt_{10}	0.999	1.034V	3.5%	
gm_{10}	91.1μS	327μS	258%	
gmb_{10}	13.0μS	55.1μS	323%	
A_{OUT}	0.71	0.75	5.6%	
τ_{OUT}	1.63ns			Error in estimating gm_{10}
Total Power	578μW	1.065mW	84%	Not accounting for bias gen
Total Gain	30.04kΩ	34.66kΩ	15.5%	Error in estimating gm

4 Simulated Bode Plots





5 Simulated Transient Response



6 Comments and Conclusion

- Resistors contribute to a large part of the overall gain. From manufacturability perspective, passive components are not friendly and also occupy more area on the chip.
- The output source follower stage is very sensitive to biasing due to back gate effect. Small variations on Vz can drive the output to fall out of desired common mode voltage or drive MN10 into cutoff region and lose all the gain from previous stages.
- Any variations in supply voltage causes variation in Vov of MN7 directly (as the device is biased through R3 & R4) causing Vz to vary and thereby impacting the biasing of MN10 and gain.
- Common source stage with diode connected load attributes to miller cap loading effect on cascade stage. This is limiting the gain of common source stage to smaller values.
- Since the output is single ended, it is susceptible to noise. Differential configuration will be better.

7 Appendix I

```
* Design Problem, ee114/214A-2015
* Team Member 1 Name: Usha Kankanala
* Team Member 2 Name: Samuel Lenius
* Please fill in the specification achieved by your circuit
* before you submit the netlist
*************************************************************
* sunetids of team members:
*   ukankana@stanford.edu:  06091239
*   lenius@stanford.edu:    06091240
* The specification that this script achieves are:
* Power          1.06mW    <= 2.00 mW      Meets Spec
* Gain           34.6kOhm  >=  30.0 kOhm   Meets Spec
* BandWidth      93.0MHz   >= 90.0 MHz     Meets Spec
* FOM            3043      >= 1350         Meets Spec
*************************************************************

* Including the model file
.include /usr/class/ee114/hspice/ee114_hspice.sp


* Defining Top level circuit parameters
.param p_Cin = 220f
.param p_CL  = 250f
.param p_RL  = 20k

* Defining the supply voltages
vdd     n_vdd   0       2.5
vss     n_vss   0       -2.5

*Defining the input current source
** For ac simulation uncomment the following 2 lines**
Iin     n_iin   0       ac      100n
*Iin     n_iin   0       ac      1

** For transient simulation uncomment the following 2 lines**
*Iin    n_iin    0    sin(0 0.5u 1e6)

* Defining Input capacitance
Cin    n_iin    0    'p_Cin'

* Defining the load
RL      n_vout  0       'p_RL'
CL      n_vout  0       'p_CL'

*** Your Trans-impedance Amplifier here ***
***     d       g       s       b       n/pmos114       w       l

*** Vx/Iin = V(n_x) / Iin, use "n_x" as the node label for Vx ***
MN1     n_iin   n_bias_n  n_vss   n_vss nmos114 w=3.0u l=2.0u
MN2     n_x     0         n_iin   n_vss  nmos114 w=28.0u l=1.0u
MP3     n_x     n_bias_p  n_vdd   n_vdd  pmos114 w=6.0u l=2.0u
```

```
R1      n_vdd   n_x       19200
R2      n_x     0         20800

*** Vy/Vx = V(n_y) / V(n_x), use "n_y" as the node label for Vy ***
MP4     n_w     n_x       n_vdd  n_vdd  pmos114 w=6.0u l=1.0u
MP5     n_y     0         n_w    n_vdd  pmos114 w=6.0u l=1.0u
MN6     n_y     n_bias_n  n_vss  n_vss  nmos114 w=3.0u l=2.0u
R3      n_y     0         168100
R4      n_y     n_vss     34400

*** Vz/Vy = V(n_z) / V(n_y), use "n_z" as the node label for Vz ***
MN7     n_z     n_y       n_vss  n_vss  nmos114 w=2.0u l=1.0u
MP8     n_z     n_z       n_vdd  n_vdd  pmos114 w=2.0u l=1.0u

*** Vout/Vz = V(n_vout) / V(n_z), use "n_vout" as the node label for Vout ***
MN9     n_vout  n_bias_n  n_vss  n_vss  nmos114 w=5.0u l=2.0u
MN10    n_vdd   n_z       n_vout n_vss  nmos114 w=28.0u l=1.0u

*** Your Bias Circuitry goes here ***
MP100   n_bias_n n_bias_p n_vdd n_vdd  pmos114 w=4u  l=2u
MP200   n_bias_p n_bias_p n_vdd n_vdd  pmos114 w=4u  l=2u
MN300   n_bias_n n_bias_n n_vss n_vss  nmos114 w=2u  l=2u
MN400   n_bias_p n_bias_n n_biasr2   n_vss  nmos114 w=4u l=2u
R200    n_biasr2 n_vss  16.7k
MP800   n_biasn9 n_bias_n n_vdd n_vdd pmos114 w=2u  l=9u
MN700   n_biasn9 n_bias_n n_vss n_vss nmos114 w=5u  l=2u
MN900   n_bias_p n_biasn9 n_vss n_vss nmos114 w=4u  l=2u

*** defining the analysis ***
.op
.option post brief nomod

** For ac simulation uncomment the following line**
.ac dec 1k 100 1g

.measure ac gainmax_vout max vdb(n_vout)
.measure ac f3db_vout when vdb(n_vout)='gainmax_vout-3'

.measure ac gainmax_vx max vdb(n_x)
.measure ac f3db_vx when vdb(n_x)='gainmax_vx-3'

.measure ac gainmax_vy max vdb(n_y)
.measure ac f3db_vy when vdb(n_y)='gainmax_vy-3'

.measure ac gainmax_vz max vdb(n_z)
.measure ac f3db_vz when vdb(n_z)='gainmax_vz-3'

** For transient simulation uncomment the following line **
*.tran 0.01u 4u

.end
```