# 2015 EE214A Design Project

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| Specfications | Given Spec | Achieved Spec |
|---|---|---|
| Gain | 30kΩ | 34.7kΩ |
| Bandwidth | 90MHz | 93MHz |
| Power | 2.0mW | 1.0mW |
| FOM | 1350 | 3043 |

| Area Breakdown | % Core Area | Area (um) |
|---|---|---|
| Core Area | 100% | $112\mu\text{m}^2$ |
| VNMOS-bias | 19.6% | $22\mu\text{m}^2$ |
| VPMOS-bias | 10.7% | $12\mu\text{m}^2$ |
| Bias Generator | 73.1% | $82\mu\text{m}^2$ |

# 1 Design Outline

Our approach to this design was to first develop sizing ratios of the transistors and their DC relationships to Vx, Vy, Vz and Vo. We developed the equations necessary to 'program' those voltages and to develop what their reasonable ranges are. Here are some graphs that show the relationships between the output common mode voltage and Vz, and then Vz to Vy given our sizing decisions. We developed a MATLAB program to quickly estimate critical parameters for a given design, to allow easy investigation of parametric variation.
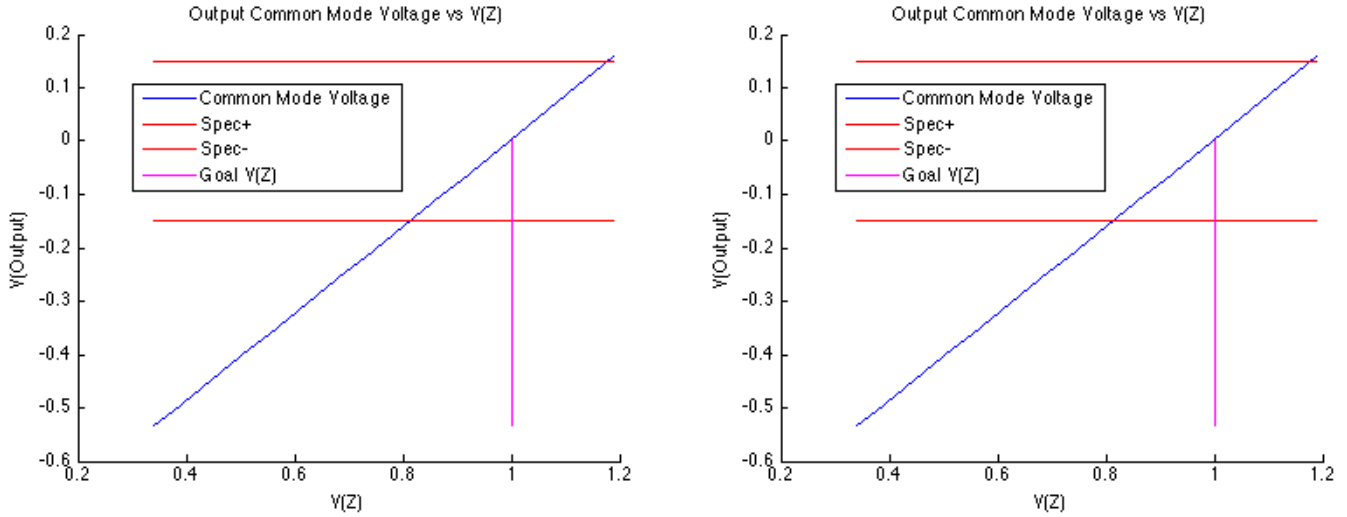
These graphs give rise to a process to choose exactly the value of those voltages based on the size of the transistors. Here, given the common mode output spec, choosing a size for MN10, and estimating the MN10 backgate gives the needed value of Vz. Given a size ratio for MN7 to MP8 gives the needed value of Vy, knowing Vz. Given the size ratio for MP4 to MN6 and knowing the value of Vy gives the gives the necessary ratio of R3 to R4 to program the value of Vy.
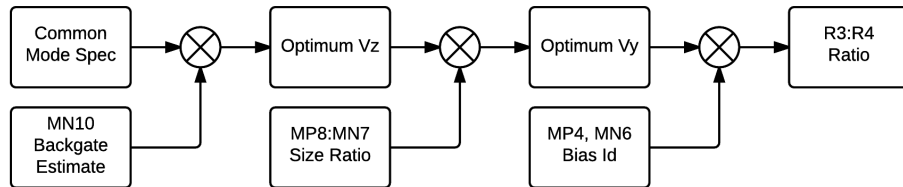
Similarly for Vx, given a goal for MP4 gm (from our chosen distribution of stage gain) we can solve for the ratio of R1 to R2 to program the value of Vx. Since we have set the K value of MN1 and MP3 equal, the voltage at Vx is selected purely by the ratio of R1 and R2.
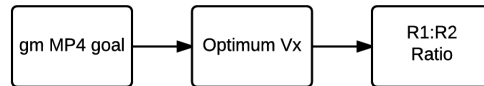
Once the math was developed to decouple the selection of stage gain to the DC biasing selection, the focus was on gain/speed. First we distributed the desired gain for each stage, then choose the vov level to drive the transistors based on the gm/Id plots, and then sized the transistors to minimize tau for adjacent stages.

The gain budget was based on the X stage having the most gain, since it's easy to get there, getting the balance of gain from the Y stage and then setting the Z stage to cancel out the gain loss of the output CD stage. Thus total gain simplifies to X * Y = 30k.

By making plots of the sum of tau for adjacent stages vs critical transistor sizing we were able to minimize total tau for the design, with the given gain budget.

# 2 Design Schematic



$V_{dd} = 2.5V$

$V_{I_{d1}} = 18.435\mu$

$V_{6ias-PMOS} = 1.32V$

$\left(\frac{W}{L}\right)_3 = \frac{6\mu}{2\mu}$

$V_{ov3} = -680.6mv$

MP3

$V_X = 1.28V$

$V_{I_{d2}} = 20.9\mu A$

$\left(\frac{W}{L}\right)_2 = \frac{24\mu}{1\mu}$

$V_{ov2} = 155.8mv$

$100V$

$I_{in}$
$100nA$

$C_{in} = 220fF$

MN2

$V_{-iin} = -1.024V$

$V_{I_{d1}} = 20.9\mu A$

$\left(\frac{W}{L}\right)_1 = \frac{3\mu}{2\mu}$
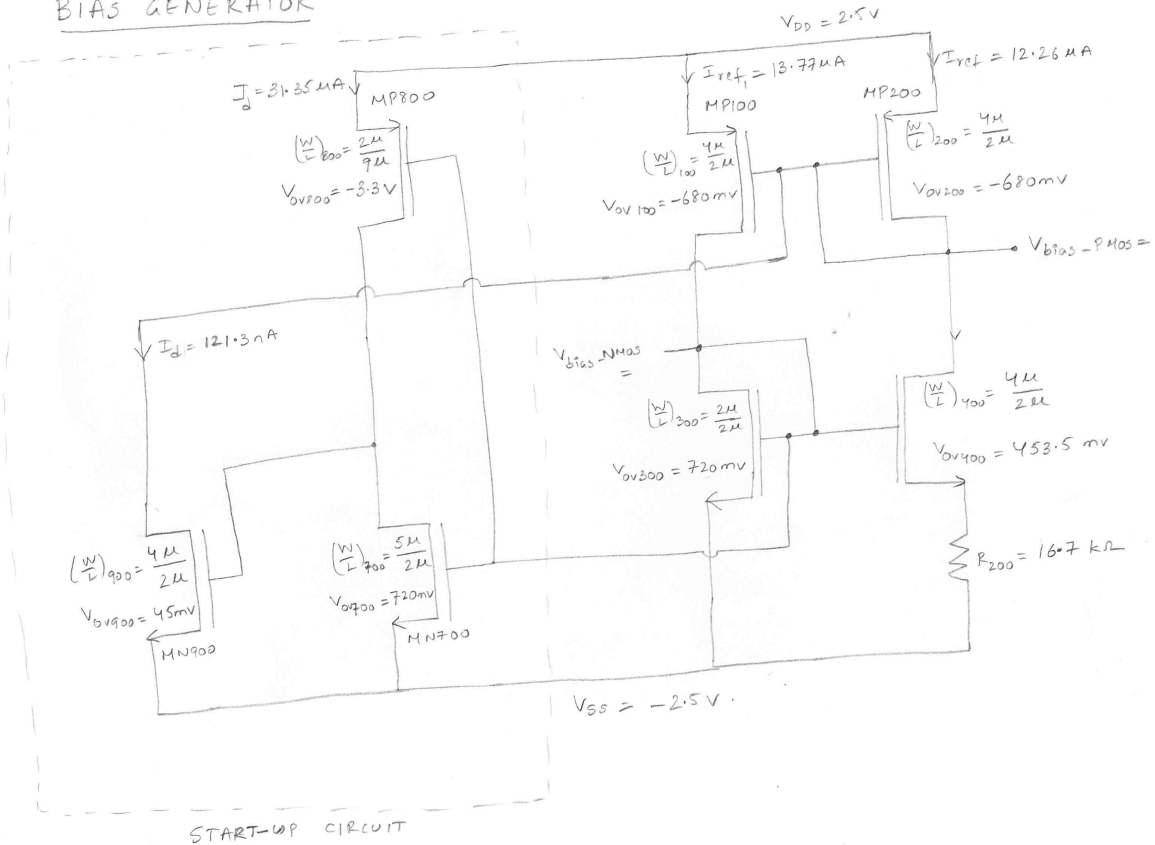
$V_{6ias-NMOS} = -1.28V$

$V_{ov1} = 720.5mv$

MN1

$V_{I_1} = 63.78\mu A$

$R_1 = 19.2k\Omega$

$V_{I_2} = 61.32\mu A$

$R_2 = 20.8k\Omega$

$V_{I_{d4}} = 43.5\mu A$

$\left(\frac{W}{L}\right)_4 = \frac{6\mu}{1\mu}$

$V_{ov4} = -724.6mv$

MP4

$V_{I_{d5}} = 43.5\mu A$

$\left(\frac{W}{L}\right)_5 = \frac{6\mu}{1\mu}$

$V_{ov5} = -671.44mv$

MP5

$V_y = -1.42V_a$

$I_{d6} = 20.52\mu A$

$\left(\frac{W}{L}\right)_6 = \frac{3\mu}{2\mu}$

$V_{ov6} = 720.5mv$

MN6

$I_{d8} = 22.99\mu A$   MP8

$\left(\frac{W}{L}\right)_8 = \frac{2\mu}{1\mu}$

$V_{ov8} = -898mv$

$V_z = 1.10V$

$I_3 = 8.4\mu A$

$R_3 = 168.1k\Omega$

$I_{d7} = 22.99\mu A$

$\left(\frac{W}{L}\right)_7 = \frac{2\mu}{1\mu}$

$V_{ov7} = 581.3mv$

$I_4 = 31.4\mu A$       MN7

$R_4 = 34.4k\Omega$

$V_{ss}$

$V_{ss}$

$I_{d10} = 30.43\mu A$

$\left(\frac{W}{L}\right)_{10} = \frac{28\mu}{1\mu}$

$V_{ov10} = 185mv$

MN10

$V_{out} = -117mv$

$I_{dq} = 36.3\mu A$

$\left(\frac{W}{L}\right)_9 = \frac{5\mu}{2\mu}$

$V_{ov9} = \frac{720.7}{mv}$

MN9

$V_{SS} = -2.5V$

$C_L = 250fF$   $V_{out}$   $R_L = 20k\Omega$

---

## BIAS GENERATOR



$V_{DD} = 2.5V$

$I_d = 31.35\mu A$   MP800

$\left(\frac{W}{L}\right)_{800} = \frac{2\mu}{9\mu}$

$V_{ov800} = -3.3V$

$I_d = 121.3nA$

$\left(\frac{W}{L}\right)_{900} = \frac{4\mu}{2\mu}$

$V_{ov900} = 45mv$

MN900

$I_{ref_1} = 13.77\mu A$

MP100

$\left(\frac{W}{L}\right)_{100} = \frac{4\mu}{2\mu}$

$V_{ov100} = -680mv$

$V_{bias-NMOS} =$

$\left(\frac{W}{L}\right)_{300} = \frac{2\mu}{2\mu}$

$V_{ov300} = 720mv$

$\left(\frac{W}{L}\right)_{700} = \frac{5\mu}{2\mu}$

$V_{ov700} = 720mv$

MN700

$V_{ref} = 12.26\mu A$

MP200

$\left(\frac{W}{L}\right)_{200} = \frac{4\mu}{2\mu}$

$V_{ov200} = -680mv$

$V_{bias-PMOS} =$

$\left(\frac{W}{L}\right)_{400} = \frac{4\mu}{2\mu}$

$V_{ov400} = 453.5mv$

$R_{200} = 16.7k\Omega$

$V_{SS} = -2.5V.$

START-UP CIRCUIT

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[1]Drawings also attached to end of appendix in full size

# 3   Calculation of Key Design Parameters

**Choice of L**

- All devices used in current source have a minimum length of $2\mu$m.

- All other devices in the amplifier have minimum length of $1\mu$m. Minimum length is used as $f_t$ is inversely proportional to L.

- All devices in bias generator circuit have length $>=2\mu$m.

**Bias Generator circuit**

- Constant gm reference based design is used as bias circuit to reduce mismatch errors.

- Transconductance of bias device (mn300) depends only on R2 and m ( m is the ratio of MN300/MN400). Therefore gm can be set precisely.

- Start-up circuit is used to force the circuit to the desired operating point.

**Approximations for hand calculations**
For simpler hand calculations, following approximations are used.

1. $Cdb = Csb = 0.35Cgs$

2. $Cgs = (\frac{2}{3})WLCox + Cov'W$

3. $Cgd = Cov'W$

4. $gmb = 0.2gm$

**Stage4**

- As per the spec, common mode output voltage (vout) has to be within -0.15v to 0.15v. Since the body is connected to vss, MN10 experiences back gate effect and the threshold voltage is given by:

$$Vt = Vt_0 + \gamma(\sqrt{2\phi f + V_{sb}} - \sqrt{2}\phi f$$
$$Vt_0 = 0.5V, \gamma = 0.6, 2\phi f = 0.8 \tag{1}$$

- Stage 4 is a source follower which has a gain given by

$$A4 = \frac{gm_{10}}{gm_{10} + gmb_{10} + (\frac{1}{R_L})} \tag{2}$$

- Gain of stage4 (A4) <1 due to back gate effect and the output load.

- To achieve gain closer to 1 (0.6 - 0.7), it is important to size and bias MN10 such that $(gm_{10} + gmb_{10}) >> (1/R_L)$.

- Transconductance of and drain current of $MN_{10}$ is given by

$$gm_{10} = \mu nCox(\frac{W}{L})vov_{10} \tag{3}$$

$$Id_{10} = 0.5\mu nCox(\frac{W_{10}}{L_{10}})vov_{10}^2(1 + \lambda(Vdd - Vout)) \tag{4}$$

- $MN_9$ (bias device for source follower) is sized such that $Id_{10} + I_{R_L} = Id_9$ and the common mode output voltage does not fall out of range. This device is chosen to be of smaller size to reduce loading on Vout node.

$$\tau_{OUTPUT} = (R_L || \frac{1}{1.2gm_{10}})(C_L + Csb_{10} + Cgd_9 + Cdb_9) \tag{5}$$

- Cgs10 is assumed to be very small due to boot-strapping.

**Stage 3**

- Loading at node Vy increases with the increase in gain of stage 3 due to the miller effect. Hence gain of stage3 is kept low and is fixed at sqrt(2) to compensate for the gain lost in stage 4. Gain of stage3 (CS amplifier with diode connected load):

$$|A3| = \frac{gm7}{gm8} = \frac{Vov8}{Vov7} = \frac{Vdd - Vz - abs(Vtp)}{Vy - Vss - Vtn} = \sqrt{2} \tag{6}$$

- Choice of Vz from above (stage4) determines Vy.

- Minimum device sizes (W=2$\mu$m, L=1$\mu$m) are used for both MN7 and MP8 to reduce loading on Vy and Vz.

$$Id_7 = Id_8 = 0.5\mu nCox(\frac{W_7}{L_7})vov_7^2(1 + \lambda(Vz - Vss)) \tag{7}$$

$$\tau_Z = (\frac{1}{gm_8})(Cgs_8 + Cdb_8 + Cgd_{10} + Cgd_7(1 + \frac{1}{|A3|}) + Cdb_7) \tag{8}$$
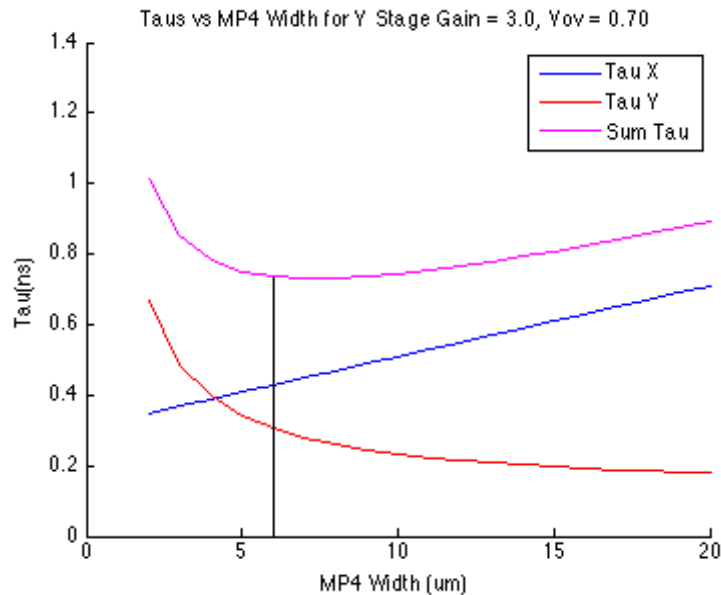
**Stage 2**

- Vy from stage Z above determines the required ratio of R3 and R4.

$$(\frac{R4}{R3}) = \frac{Vss}{Vy} - 1 \tag{9}$$

- Gain of stage Y (Cascode amplifier) is set to 3.

$$|A2| = gm4(R3||R4) \tag{10}$$

- $Vov_4$ and $W_4$ are optimized to reduce $\tau_X$.



Taus vs MP4 Width for Y Stage Gain = 3.0, Vov = 0.70

4

- MN6 is sized such that current through MN6 is same as the current through MP4 and MP5.

$$Id4 = Id5 = Id6 = 0.5\mu pCox(\frac{W4}{L4})(Vdd - Vx - abs(Vtp))^2(1 + \lambda(Vdd - Vw) \tag{11}$$

- Current through R3 and R4

$$I_{R3} + I_{R4} = Vss/(R3 + R4) \tag{12}$$

$$\tau_Y = (R3||R4)(Cgs_7 + Cgd_7(1 + |A3|) + Cgd_6 + Cdb_6 + Cgd_5 + Cdb_5) \tag{13}$$

**Stage 1**

- $Vov_4$ from stage 2 sets $V_X$ which in turn sets the ratio of R1 and R2.

$$Vov_4 = Vdd - Vx - |Vtp| \tag{14}$$

$$(\frac{R1}{R2}) = \frac{Vdd}{Vx} - 1 \tag{15}$$

- Gain of stage 1 (Common gate amplifier) is set to 10000.

$$|A1| = (R1||R2) \tag{16}$$

- MN1 and MP3 are sized such that Id1 = Id3.

- MN2 is sized to reduce $\tau_{IIN}$ node. $\tau_{IIN}$ is inversely proportional to $gm_2$.

$$\tau_{IIN} = (\frac{1}{gm2})(Cin + Cgd_1 + Cdb_1 + Cgs_2 + Csb_2) \tag{17}$$

$$\tau_X = (R1||R2)(Cgd_2 + Cdb_2 + Cgd_3 + Cdb_3 + Cgs_4 + Cgd_4) \tag{18}$$
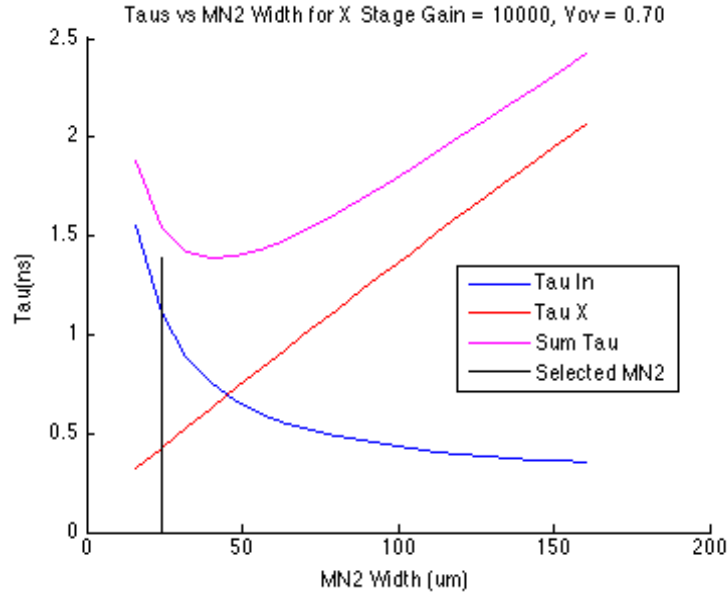


- Current through MN1, MN2 and MP3

$$Id_{1,2,3} = 0.5\mu pCox(\frac{W_3}{L_3})(Vdd - VbiasP - |Vtp|)^2(1 + \lambda(Vdd - Vx)) \tag{19}$$

- Current through R1 and R2

$$I_{R1} + I_{R2} = Vdd/(R1 + R2) \tag{20}$$

5

### Vovn, Vovp

- Vovn and Vovp are chosen to achieve a reasonable balance between gain, Tau total and Power, and our choice was educated by the gm/Id technology plots.
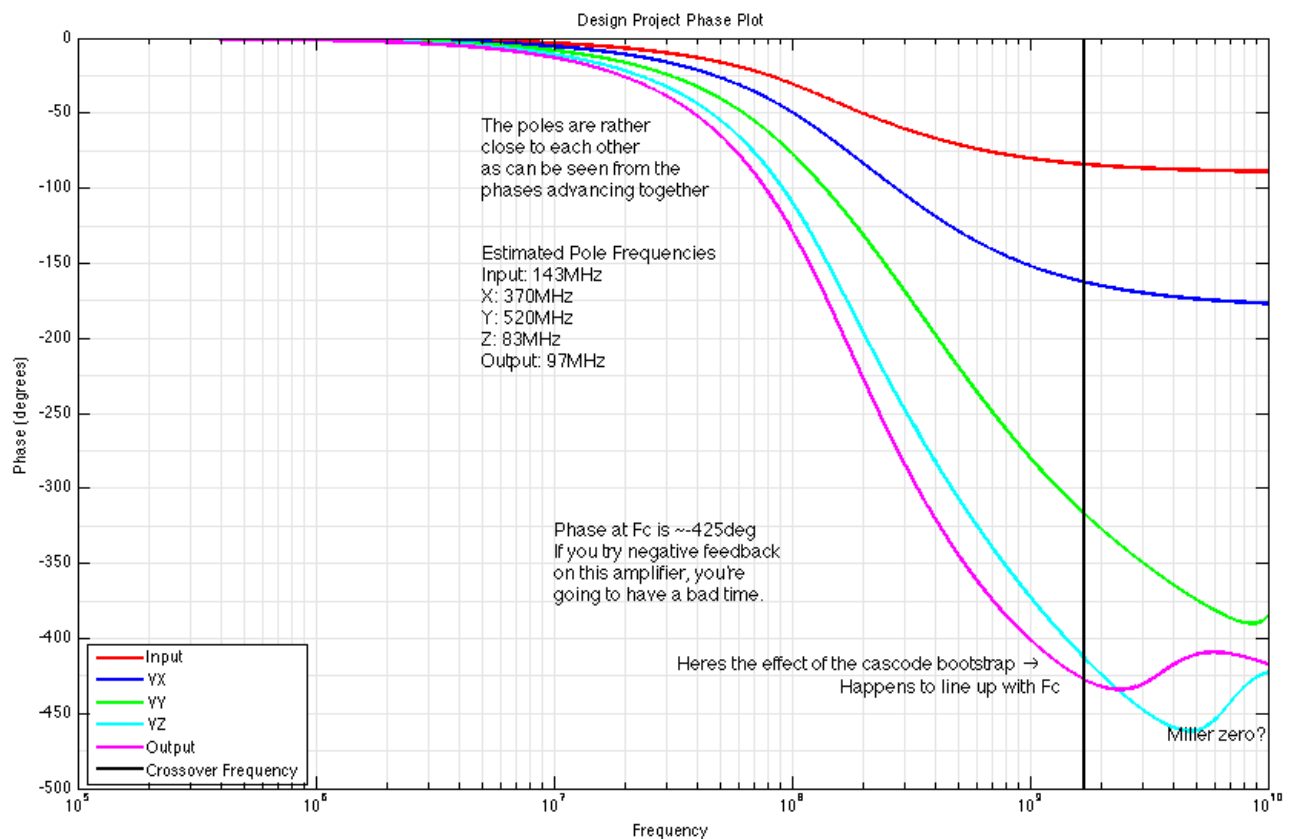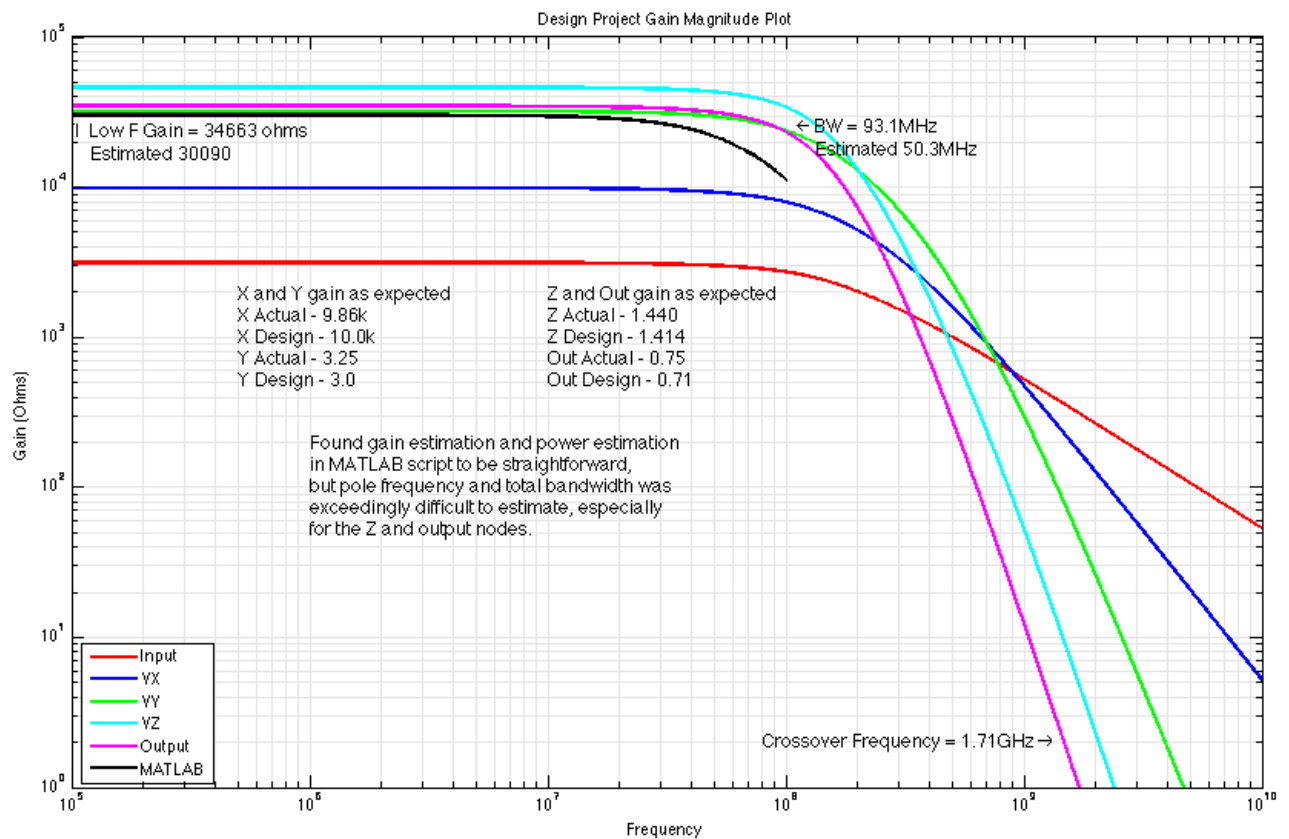
### Total Design Performance

$$|A_{TOTAL}| = A1 * A2 * A3 * A4 \tag{21}$$

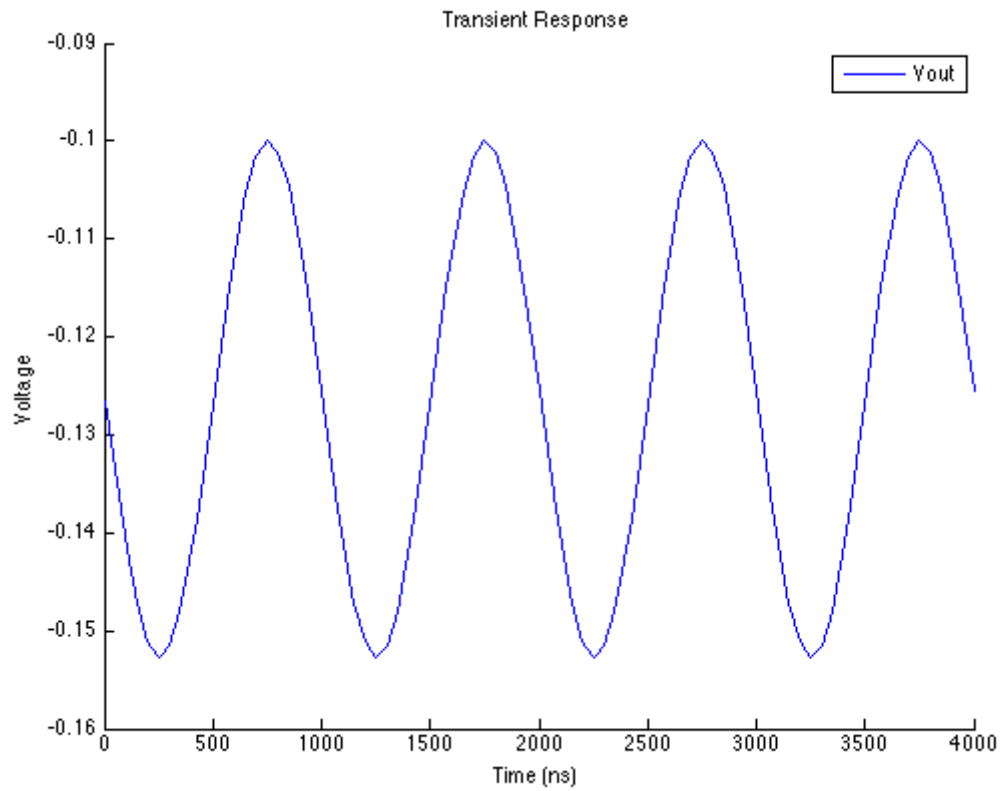$$\tau_{TOTAL} = \tau_{IIN} + \tau_X + \tau_Y + \tau_Z + \tau_{OUTPUT} \tag{22}$$

$$Power = (Vdd - Vss)(Id_1 + Id_4 + Id_7 + Id_{10}) + (\frac{Vdd^2}{R1 + R2}) + (\frac{Vss^2}{R3 + R4}) \tag{23}$$

| Bias Generator | Hand calc | Spice | %Error | Reason for error |
|---|---|---|---|---|
| $V_{BiasN}$ | -1.300V | -1.279V | -1.6% | Startup circuit bias |
| $V_{BiasP}$ | 1.300V | 1.319V | 1.5% | Startup circuit bias |
| | | | | |
| **Stage1** | Hand calc | Spice | %Error | Reason for error |
| $Id_1$ | 18.3$\mu$A | 20.9$\mu$A | 14.2% | Bias generator error |
| Vx | 1.300V | 1.275V | -1.9% | |
| $A_X$ | 10k$\Omega$ | 9.86k$\Omega$ | -1.4% | Finite $MN_1$ and $MP_3$ output resistance |
| $gm_2$ | 210$\mu$S | 268$\mu$S | 27.6% | Bias generator error |
| $\tau_{IN}$ | 1.11ns | | | |
| $\tau_X$ | 420ps | | | |
| | | | | |
| **Stage2** | Hand calc | Spice | %Error | Reason for error |
| $Id_4$ | 36.75$\mu$A | 43.5$\mu$A | 18.4% | |
| $V_W$ | 1.496V | 1.450V | -3.2% | |
| $V_Y$ | -1.550V | -1.418V | -8.5% | Imbalance between $MP_4$ and $MN_6$ current |
| $gm_4$ | 105$\mu$S | 120$\mu$S | 14.3% | Error in $V_Y$ |
| $A_Y$ | -3.0 | -3.25 | 8.3% | Error estimating $gm_4$ |
| $\tau_Y$ | 306ps | | | |
| | | | | |
| **Stage3** | Hand calc | Spice | %Error | Reason for error |
| $Id_7$ | 10.25$\mu$A | 22.9$\mu$A | 123% | Error in $V_Y$ plus finite output resistance |
| $V_Z$ | 1.364 | 1.102V | -19.2% | Error in $V_Y$ |
| $gm_7$ | 45$\mu$S | 79$\mu$S | 75.5% | Error in $Id_7$ |
| $gm_8$ | 31.2$\mu$S | 51$\mu$S | 63.5% | Error in $Id_7$ |
| $A_Z$ | 1.414 | 1.440 | 1.8% | The benefit of ratiometric design |
| $\tau_Z$ | 1.92ns | | | Error in estimating $gm_8$ |
| | | | | |
| **Stage4** | Hand calc | Spice | %Error | Reason for error |
| $Id_{10}$ | 2.96$\mu$A | 30.43$\mu$A | 928% | $MN_{10}$'s large width is a big error amplifier |
| $V_{OUT}$ | 0.299 | -0.117V | -139% | |
| $Vt_{10}$ | 0.999 | 1.034V | 3.5% | |
| $gm_{10}$ | 91.1$\mu$S | 327$\mu$S | 258% | |
| $gmb_{10}$ | 13.0$\mu$S | 55.1$\mu$S | 323% | |
| $A_{OUT}$ | 0.71 | 0.75 | 5.6% | |
| $\tau_{OUT}$ | 1.63ns | | | Error in estimating $gm_{10}$ |
| Total Power | 578$\mu$W | 1.065mW | 84% | Not accounting for bias gen |
| Total Gain | 30.04k$\Omega$ | 34.66k$\Omega$ | 15.5% | Error in estimating gm |

# 4  Simulated Bode Plots



Design Project Gain Magnitude Plot

Low F Gain = 34663 ohms
Estimated 30090

← BW = 93.1MHz
Estimated 50.3MHz

X and Y gain as expected
X Actual - 9.86k
X Design - 10.0k
Y Actual - 3.25
Y Design - 3.0

Z and Out gain as expected
Z Actual - 1.440
Z Design - 1.414
Out Actual - 0.75
Out Design - 0.71

Found gain estimation and power estimation
in MATLAB script to be straightforward,
but pole frequency and total bandwidth was
exceedingly difficult to estimate, especially
for the Z and output nodes.

Crossover Frequency = 1.71GHz →

Input
VX
VY
VZ
Output
MATLAB



Design Project Phase Plot

The poles are rather
close to each other
as can be seen from the
phases advancing together

Estimated Pole Frequencies
Input: 143MHz
X: 370MHz
Y: 520MHz
Z: 83MHz
Output: 97MHz

Phase at Fc is ~-425deg
If you try negative feedback
on this amplifier, you're
going to have a bad time.

Heres the effect of the cascode bootstrap →
Happens to line up with Fc

Miller zero?

Input
VX
VY
VZ
Output
Crossover Frequency

# 5 Simulated Transient Response

# 6 Comments and Conclusion

## 6.1 Notes about Design

- Resistors contribute to a large part of the overall gain. From manufacturability perspective, passive components are not friendly and also occupy more area on the chip. We feel that while the large value resistors helped us achieve a high gain and low power that they result in a possibly overly acedemic design thats not suitable for actual production.

- The output source follower stage is very sensitive to biasing due to back gate effect. Small variations on $V_Z$ can drive the output to fall out of desired common mode voltage or drive $MN_10$ into cutoff region and lose all the gain from previous stages.

- Any variations in supply voltage causes variation in Vov of MN7 directly (as the device is biased through R3 & R4) causing $V_Z$ to vary and thereby impacting the biasing of MN10 and gain. This is a great node to lose any and all PSRR.

- Common source stage with diode connected load attributes to miller cap loading effect on cascade stage. This is limiting the gain of common source stage to smaller values.

- Since the output is single ended, it is susceptible to noise, a differential configuration will be better.

## 6.2 Notes on Project

- We found it very difficult to balance the many simultaneous requirements, and I felt that this was a very useful exercise that's directly applicable to industry, and not only to chip design. Many times I have found myself trying to explore design spaces that have myrid of opposing non-orthogonal requirements. I feel like I have learned interesting ways to approach these problems both mathematically and strategically.

# 7 Appendix I

## 7.1 SPICE Netlist

```
1  * Design Problem , ee114/214A -2015
2  * Team Member 1 Name: Usha Kankanala
3  * Team Member 2 Name: Samuel Lenius
4  * Please fill in the specification achieved by your circuit
5  * before you submit the netlist
6  ********************************************************************
7  * sunetids of team members:
8  *    ukankana@stanford.edu:   06091239
9  *    lenius@stanford.edu:      06091240
10 * The specification that this script achieves are:
11 * Power            1.06mW      <=  2.00 mW        Meets Spec
12 * Gain             34.6kOhm    >=   30.0 kOhm     Meets Spec
13 * BandWidth        93.0MHz     >= 90.0 MHz        Meets Spec
14 * FOM              3043        >= 1350            Meets Spec
15 ********************************************************************
16
17 * Including the model file
18 .include /usr/class/ee114/hspice/ee114_hspice.sp
19
20 * Defining Top level circuit parameters
21 .param p_Cin = 220f
22 .param p_CL  = 250f
23 .param p_RL  = 20k
24
25 * Defining the supply voltages
26 vdd       n_vdd    0        2.5
27 vss       n_vss    0        -2.5
28
29 *Defining the input current source
30 ** For ac simulation uncomment the following 2 lines**
31 Iin       n_iin    0        ac        100n
32 *Iin       n_iin    0        ac        1
33
34 ** For transient simulation uncomment the following 2 lines**
35 *Iin      n_iin     0     sin( 0 0.5u 1e6)
36
37 * Defining Input capacitance
38 Cin     n_iin     0     'p_Cin'
39
40 * Defining the load
41 RL        n_vout   0          'p_RL'
42 CL        n_vout   0          'p_CL'
43
44 *** Your Trans -impedance Amplifier here ***
45 ***     d       g       s       b       n/pmos114        w        l
46
47 *** Vx/Iin = V(n_x) / Iin , use "n_x" as the node label for Vx ***
48 MN1     n_iin    n_bias_n  n_vss   n_vss nmos114 w=3.0u l=2.0u
49
50 * Increasing the size of MN2 here is a power -free trick to improve the input
51 * pole performance.
52 MN2     n_x       0          n_iin   n_vss  nmos114 w=28.0u l=1.0u
53 MP3     n_x       n_bias_p  n_vdd   n_vdd  pmos114 w=6.0u l=2.0u
54
55 * The parallel combination of these resistors provide the first stage gain.
56 R1        n_vdd   n_x          19200
57 R2        n_x     0            20800
58
59 *** Vy/Vx = V(n_y) / V(n_x), use "n_y" as the node label for Vy ***
```

```
60  * MP4 both provides gain to the second stage and provides most of the node
61  * capacitance to the first stage, hence it's sizing is a delicate balance.
62  MP4       n_w       n_x         n_vdd  n_vdd  pmos114 w=6.0u l=1.0u
63  MP5       n_y       0           n_w    n_vdd  pmos114 w=6.0u l=1.0u
64  MN6       n_y       n_bias_n    n_vss  n_vss  nmos114 w=3.0u l=2.0u
65  * We used asymmetry on MN6 in order to make Vy faster, and allow a higher Vov on
66  * MN6 however it made selecting the resistor values a lot tougher.
67
68  * These resistors provide the second stage gain, when combined with gm4.
69  * Asymmetry in MN6:MP4 sizing leads to a bit of a wonky ratio as they need to
70  * accoutn for the imbalanced current.
71  R3        n_y       0           168100
72  R4        n_y       n_vss       34400
73
74  *** Vz/Vy = V(n_z) / V(n_y), use "n_z" as the node label for Vz ***
75  * The size of these transistors sets up the gain of the third stage. Here it's
76  * approximately sqrt(2)
77  MN7       n_z       n_y         n_vss  n_vss  nmos114 w=2.0u l=1.0u
78  MP8       n_z       n_z         n_vdd  n_vdd  pmos114 w=2.0u l=1.0u
79
80  *** Vout/Vz = V(n_vout) / V(n_z), use "n_vout" as the node label for Vout ***
81  * MN10 is very tricky to bias right. You need to account for it's large Vt due
82  * to backgate and you tend to have a lot of error stacked up by the time that Vz
83  * is biased. Hence it required a small amount of monkeying to get it just right
84  * after we hand calculated the values.
85  MN9       n_vout  n_bias_n   n_vss  n_vss  nmos114 w=5.0u l=2.0u
86  MN10      n_vdd   n_z        n_vout n_vss  nmos114 w=28.0u l=1.0u
87
88  *** Your Bias Circuitry goes here ***
89
90  * This design is a self-biasing delta-Vgs / constant gm reference with startup
91  * circuit. The design was taken from lecture notes 14.
92
93  * These transistors provide the PMOS bias
94  MP100    n_bias_n n_bias_p n_vdd n_vdd  pmos114 w=4u  l=2u
95  MP200    n_bias_p n_bias_p n_vdd n_vdd  pmos114 w=4u  l=2u
96
97  * These transistors provide the NMOS bias and are the source of the delta
98  * Vgs reference. The ratio between the widths of these transistors defines m.
99  MN300    n_bias_n n_bias_n n_vss n_vss  nmos114 w=2u  l=2u
100 MN400    n_bias_p n_bias_n n_biasr2   n_vss  nmos114 w=4u l=2u
101
102 * This resistor is the denominator of the reference vov equation.
103 R200     n_biasr2 n_vss  16.7k
104
105 * These transistors are the startup circuit that enforces that it stay at
106 * the upper stable point, as the system is bistable.
107 MP800    n_biasn9 n_bias_n n_vdd n_vdd pmos114 w=2u  l=9u
108 MN700    n_biasn9 n_bias_n n_vss n_vss nmos114 w=5u  l=2u
109 MN900    n_bias_p n_biasn9 n_vss n_vss nmos114 w=4u  l=2u
110
111 *** defining the analysis ***
112 .op
113 .option post brief nomod
114
115 ** For ac simulation uncomment the following line**
116 .ac dec 1k 100 1g
117
118 .measure ac gainmax_vout max vdb(n_vout)
119 .measure ac f3db_vout when vdb(n_vout)='gainmax_vout-3'
120
121 .measure ac gainmax_vx max vdb(n_x)
122 .measure ac f3db_vx when vdb(n_x)='gainmax_vx-3'
123
```

```
124 | .measure ac gainmax_vy max vdb(n_y)
125 | .measure ac f3db_vy when vdb(n_y)='gainmax_vy-3'
126 |
127 | .measure ac gainmax_vz max vdb(n_z)
128 | .measure ac f3db_vz when vdb(n_z)='gainmax_vz-3'
129 |
130 | ** For transient simulation uncomment the following line **
131 | *.tran 0.01u 4u
132 |
133 | .end
```

## 7.2 SPICE .op Output

```
 1 | ****** HSPICE -- I-2013.12-SP2 64-BIT (May 27 2014) RHEL64 ******
 2 |  Copyright (C) 2014 Synopsys, Inc. All Rights Reserved.
 3 |  Unpublished-rights reserved under US copyright laws.
 4 |  This program is protected by law and is subject to the
 5 |  terms and conditions of the license agreement from Synopsys.
 6 |  Use of this program is your acceptance to be bound by the
 7 |  license agreement. HSPICE is the trademark of Synopsys, Inc.
 8 |  Input File: Final_Samuel_Lenius_Usha_Kankanala_1p0_34p6_93p0_3043.sp
 9 |  Command line options: Final_Samuel_Lenius_Usha_Kankanala_1p0_34p6_93p0_3043.sp
10 | lic:
11 | lic: FLEXlm: v10.9.8
12 | lic: USER:    lenius                HOSTNAME: corn27.stanford.edu
13 | lic: HOSTID: 001b213a6bad          PID:       9885
14 | lic: Using FLEXlm license file:
15 | lic: 27000@cadlic0
16 | lic: Checkout 1 hspice
17 | lic: License/Maintenance for hspice will expire on 09-jan-2016/2015.06
18 | lic: 2(in_use)/200(total) FLOATING license(s) on SERVER 27000@cadlic0
19 | lic:
20 |
21 |
22 | *********************************************************************
23 | ******   option summary
24 | ******
25 | runlvl  = 3           bypass  = 2
26 | **info** dc convergence successful at Newton-Raphson method
27 | ****** HSPICE -- I-2013.12-SP2 64-BIT (May 27 2014) RHEL64 ******
28 | ******
29 | * design problem, ee114/214a-2015
30 |
31 | ****** operating point information tnom=  25.000 temp=  25.000 ******
32 | ****** operating point status is all        simulation time is     0.
33 |    node    =voltage         node    =voltage         node    =voltage
34 |
35 | +0:n_bias_n=  -1.2795  0:n_bias_p=   1.3194  0:n_biasn9=  -1.9549
36 | +0:n_biasr2=  -2.2972  0:n_iin  =  -1.0243  0:n_vdd  =   2.5000
37 | +0:n_vout  =-117.4867m 0:n_vss   =  -2.5000  0:n_w    =   1.4507
38 | +0:n_x     =   1.2754  0:n_y     =  -1.4186  0:n_z    =   1.1019
39 |
40 |
41 | **** voltage sources
42 |
43 |  subckt
44 | element  0:vdd       0:vss
45 |  volts       2.5000     -2.5000
46 |  current -236.5422u  189.5402u
47 |  power     591.3555u  473.8505u
48 |
49 |    total voltage source power dissipation=    1.0652m        watts
50 |
51 |
```

12

```
**** current sources

subckt
element   0:iin
 volts       -1.0243
 current      0.
 power        0.


     total current source power dissipation=    0.              watts

**** resistors

subckt
element   0:rl        0:r1        0:r2        0:r3        0:r4        0:r200
 r value   20.0000k    19.2000k    20.8000k    168.1000k   34.4000k    16.7000k
 v drop    -117.4867m   1.2246      1.2754      -1.4186     1.0814      202.7945m
 current   -5.8743u    63.7831u    61.3156u    -8.4393u    31.4349u    12.1434u
 power     690.1559n   78.1111u    78.1997u    11.9723u    33.9924u    2.4626u



**** mosfets


subckt
element   0:mn1       0:mn2       0:mp3       0:mp4       0:mp5       0:mn6
model     0:nmos114.  0:nmos114.  0:pmos114.  0:pmos114.  0:pmos114.  0:nmos114.
region     Saturati    Saturati    Saturati    Saturati    Saturati    Saturati
 id        20.9028u    20.9028u    -18.4353u   -43.5146u   -43.5146u   20.5190u
 ibs       0.          -14.7571f   0.          0.          10.4928f    0.
 ibd       -14.7571f   -37.7536f   12.2464f    10.4928f    39.1864f    -10.8136f
 vgs       1.2205      1.0243      -1.1806     -1.2246     -1.4507     1.2205
 vds       1.4757      2.2997      -1.2246     -1.0493     -2.8694     1.0814
 vbs       0.          -1.4757     0.          0.          1.0493      0.
 vth       500.0000m   868.4718m   -500.0000m  -500.0000m  -779.2740m  500.0000m
 vdsat     720.4904m   155.8143m   -680.6195m  -724.6359m  -671.4420m  720.4904m
 vod       720.4904m   155.8143m   -680.6195m  -724.6359m  -671.4420m  720.4904m
 beta      80.5339u    1.7220m     79.5924u    165.7393u   193.0403u   79.0551u
 gam eff   600.0000m   600.0000m   600.0000m   600.0000m   600.0000m   600.0000m
 gm        58.0239u    268.3046u   54.1721u    120.1006u   129.6154u   56.9584u
 gds       973.3246n   1.6995u     868.5804n   3.9382u     3.3813u     973.3246n
 gmb       19.4618u    53.3569u    18.1699u    40.2830u    28.5941u    19.1044u
 cdtot     5.3930f     27.9761f    9.8099f     10.0272f    7.8875f     5.6372f
 cgtot     12.3208f    72.3462f    24.6430f    15.3124f    15.3250f    12.3136f
 cstot     16.1000f    74.6671f    31.0001f    21.8000f    19.2080f    16.1000f
 cbtot     9.3595f     32.7274f    16.5627f    16.7010f    11.9148f    9.6109f
 cgs       10.7000f    56.9335f    21.4001f    12.2000f    12.2000f    10.7000f
 cgd       1.5272f     14.1975f    3.0451f     3.0193f     3.0528f     1.5199f




subckt
element   0:mn7       0:mp8       0:mn9       0:mn10      0:mp100     0:mp200
model     0:nmos114.  0:pmos114.  0:nmos114.  0:nmos114.  0:pmos114.  0:pmos114.
region     Saturati    Saturati    Saturati    Saturati    Saturati    Saturati
 id        22.9857u    -22.9857u   36.3091u    30.4348u    -13.7696u   -12.2647u
 ibs       0.          0.          0.          -23.8251f   0.          0.
 ibd       -36.0186f   13.9814f    -23.8251f   -50.0000f   37.7951f    11.8062f
 vgs       1.0814      -1.3981     1.2205      1.2194      -1.1806     -1.1806
 vds       3.6019      -1.3981     2.3825      2.6175      -3.7795     -1.1806
 vbs       0.          0.          0.          -2.3825     0.          0.
 vth       500.0000m   -500.0000m  500.0000m   1.0337      -500.0000m  -500.0000m
```

```
116    vdsat      581.3598m  -898.1364m   720.4904m    185.6306m  -680.6195m  -680.6195m
117    vod        581.3598m  -898.1364m   720.4904m    185.6306m  -680.6195m  -680.6195m
118    beta       136.0186u    56.9907u   139.8907u      1.7664m    59.4488u    52.9515u
119    gam eff    600.0000m   600.0000m   600.0000m    600.0000m   600.0000m   600.0000m
120    gm          79.0758u    51.1854u   100.7899u    327.9067u    40.4620u    36.0399u
121    gds          1.6899u     2.0166u     1.6222u      2.4121u   579.0536n   579.0536n
122    gmb         26.5228u    17.1681u    33.8060u     55.1425u    13.5714u    12.0881u
123    cdtot        3.6813f     4.2306f     7.0089f     26.8604f     5.7669f     7.1139f
124    cgtot        5.1272f     5.1004f    20.5625f     72.0600f    16.4914f    16.4276f
125    cstot        8.6667f     8.6667f    24.8334f     72.6537f    21.3667f    21.3667f
126    cbtot        7.2976f     7.8472f    11.5918f     29.2575f    10.9061f    12.3169f
127    cgs          4.0667f     4.0667f    17.8334f     56.9335f    14.2667f    14.2667f
128    cgd          1.0221f     1.0086f     2.5731f     14.2248f     2.0927f     2.0290f
129
130
131
132    subckt
133    element   0:mn300     0:mn400     0:mp800     0:mn700     0:mn900
134    model     0:nmos114.  0:nmos114.  0:pmos114.  0:nmos114.  0:nmos114.
135    region      Saturati    Saturati    Saturati      Linear    Saturati
136     id         13.7696u    12.1434u   -31.3543u     31.3543u   121.3242n
137     ibs         0.          -2.0279f    0.           0.          0.
138     ibd       -12.2049f    -38.1938f   44.5486f     -5.4514f    -38.1938f
139     vgs         1.2205      1.0177     -3.7795       1.2205     545.1376m
140     vds         1.2205      3.6166     -4.4549     545.1376m     3.8194
141     vbs         0.        -202.7945m    0.           0.          0.
142     vth       500.0000m   564.1814m  -500.0000m   500.0000m   500.0000m
143     vdsat     720.4904m   453.5145m    -3.2795    545.1376m    45.1376m
144     vod       720.4904m   453.5145m    -3.2795    720.4904m    45.1376m
145     beta       53.0512u   118.0829u     5.8305u    128.4071u   119.0969u
146     gam eff   600.0000m   600.0000m   600.0000m   600.0000m   600.0000m
147     gm         38.2229u    53.5523u    19.1213u     69.9995u     5.3757u
148     gds       648.8830n   514.1885n   331.9501n     24.0427u     5.0935n
149     gmb        12.8204u    16.0433u     6.4135u     23.4786u     1.8031u
150     cdtot       4.4573f     5.5601f     3.5781f     13.8464f     5.5651f
151     cgtot       8.2107f    16.5346f    29.9091f     25.3172f    17.7794f
152     cstot      11.7334f    20.0468f    33.2001f     24.2459f    20.4667f
153     cbtot       8.1048f     9.4306f     6.9952f     13.0872f    11.0903f
154     cgs         7.1334f    14.2667f    28.6001f     17.2459f    14.2667f
155     cgd         1.0150f     2.0887f     1.2459f      7.9152f     2.0937f
156
157
158
159    ******
160    * design problem, ee114/214a-2015
161
162    ****** ac analysis tnom=   25.000 temp=   25.000 ******
163    gainmax_vout= -49.2028      at=    5.3333k
164              from= 100.0000      to=    1.0000g
165    f3db_vout=  92.9703x
166    gainmax_vx=  -60.1155      at=   36.1410k
167              from= 100.0000      to=    1.0000g
168    f3db_vx= 131.9439x
169    gainmax_vy=  -49.8772      at=   21.4289k
170              from= 100.0000      to=    1.0000g
171    f3db_vy= 108.3150x
172    gainmax_vz=  -46.7065      at=   21.3304k
173              from= 100.0000      to=    1.0000g
174    f3db_vz= 105.6056x
175
176            ***** job concluded
177    ****** HSPICE -- I-2013.12-SP2 64-BIT (May 27 2014) RHEL64 ******
178    ******
179    * design problem, ee114/214a-2015
```
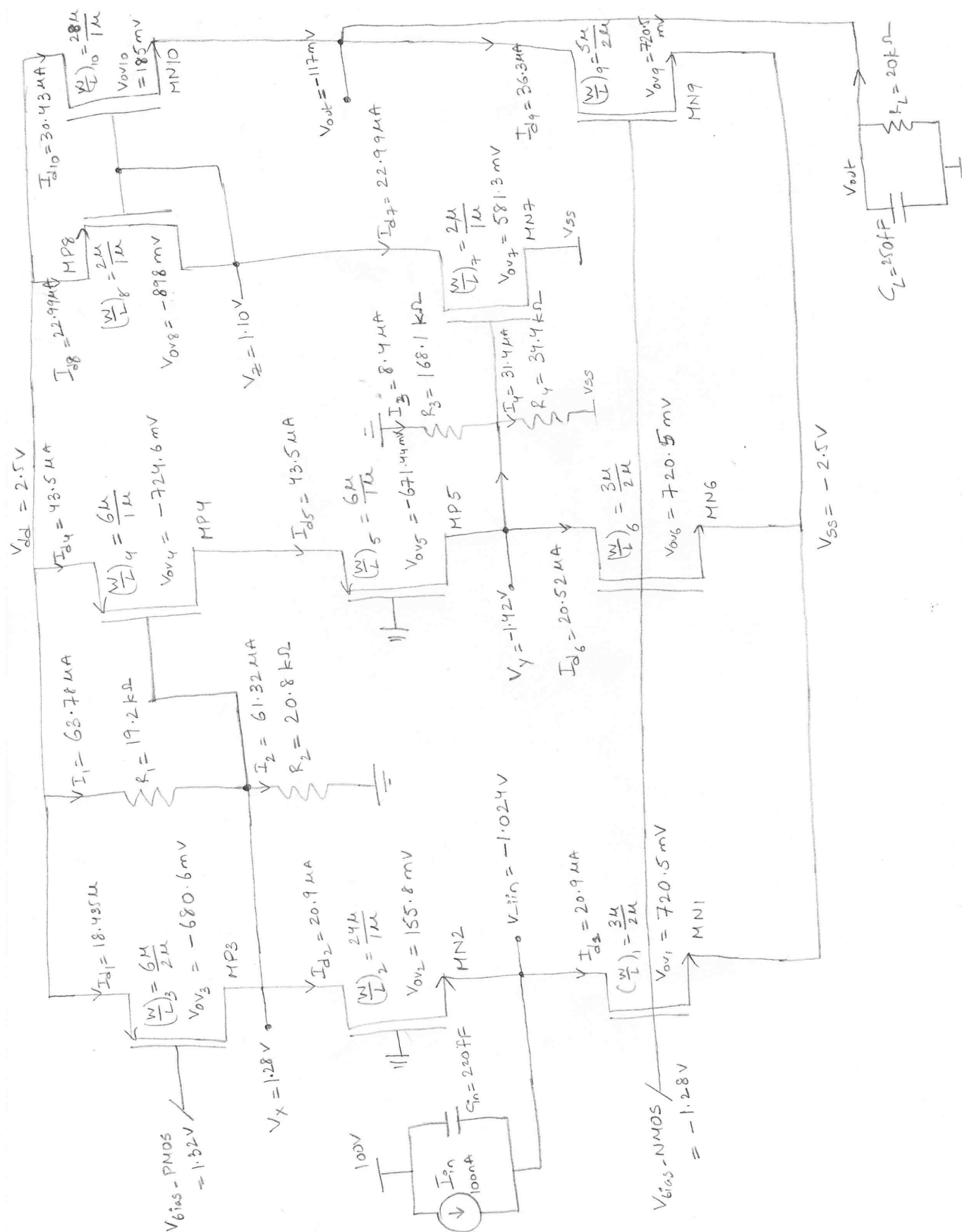
```
180
181   ****** job statistics summary tnom=  25.000 temp=  25.000 ******
182
183
184   ******   Machine Information   ******
185   CPU:
186   model name      : Quad-Core AMD Opteron(tm) Processor 2384
187   cpu MHz         : 800.000
188
189   OS:
190   Linux version 3.13.0-53-generic (buildd@phianna) (gcc version 4.8.2 (Ubuntu
          4.8.2-19ubuntu1) ) #89-Ubuntu SMP Wed May 20 10:34:39 UTC 2015
191
192
193    ******   HSPICE Threads Information   ******
194
195    Command Line Threads Count :     1
196    Available CPU Count         :     8
197    Actual Threads Count        :     1
198
199
200    ******   Circuit Statistics   ******
201    # nodes         =        13 # elements    =        28
202    # resistors     =         6 # capacitors  =         2 # inductors    =         0
203    # mutual_inds   =         0 # vccs         =         0 # vcvs         =         0
204    # cccs          =         0 # ccvs         =         0 # volt_srcs    =         2
205    # curr_srcs     =         1 # diodes       =         0 # bjts         =         0
206    # jfets         =         0 # mosfets      =        17 # U elements   =         0
207    # T elements    =         0 # W elements   =         0 # B elements   =         0
208    # S elements    =         0 # P elements   =         0 # va device    =         0
209    # vector_srcs   =         0 # N elements   =         0
210
211
212    ******   Runtime Statistics (seconds)   ******
213
214    analysis            time     # points    tot. iter   conv.iter
215    op point            0.00            1           10
216    ac analysis         0.08         7001         7001
217    readin              0.01
218    errchk              0.00
219    setup               0.00
220    output              0.00
221
222
223          peak memory used        176.94 megabytes
224          total cpu time            0.09 seconds
225          total elapsed time        1.19 seconds
226          job started at     06:46:11 12/04/2015
227          job ended   at     06:46:13 12/04/2015
228
229
230   lic: Release hspice token(s)
231   lic: total license checkout elapse time:        1.01(s)
```

## 7.3 Amplifier - Enlarged

$\left(\frac{W}{L}\right)_{10} = \frac{28\mu}{1\mu}$

$V_{ov10} = 185\,mV$

MN10

$I_{d10} = 30.43\,\mu A$

$V_{dd} = 2.5\,V$

$I_{d8} = 22.99\,\mu A$

MP8

$\left(\frac{W}{L}\right)_8 = \frac{2\mu}{1\mu}$

$V_{ov8} = -898\,mV$

$V_z = 1.10\,V$

$V_{out} = -117\,mV$

$I_{d7} = 22.99\,\mu A$

$I_{d9} = 36.3\,\mu A$

$\left(\frac{W}{L}\right)_9 = \frac{5\mu}{2\mu}$

$V_{ov9} = 720.5\,mV$

MN9

$\left(\frac{W}{L}\right)_7 = \frac{2\mu}{1\mu}$

$V_{ov7} = 581.3\,mV$

MN7

$V_{SS}$

$R_4 = 20\,k\Omega$

$V_{out}$

$C_L = 250\,fF$

$I_{d4} = 43.5\,\mu A$

$\left(\frac{W}{L}\right)_4 = \frac{6\mu}{1\mu}$

$V_{ov4} = -724.6\,mV$

MP4

$I_{d5} = 43.5\,\mu A$

$\left(\frac{W}{L}\right)_5 = \frac{6\mu}{1\mu}$

$V_{ov5} = -671.44\,mV$

MP5

$I_3 = 8.4\,\mu A$

$R_3 = 168.1\,k\Omega$

$I_4 = 31.4\,\mu A$

$R_4 = 34.4\,k\Omega$

$V_{SS}$

$V_{SS} = -2.5\,V$

$I_1 = 63.78\,\mu A$

$R_1 = 19.2\,k\Omega$

$I_2 = 61.32\,\mu A$

$R_2 = 20.8\,k\Omega$

$V_y = 1.92\,V$

$I_{d6} = 20.52\,\mu A$

$\left(\frac{W}{L}\right)_6 = \frac{3\mu}{2\mu}$

$V_{ov6} = 720.5\,mV$

MN6

$I_{d1} = 18.435\,\mu$

$\left(\frac{W}{L}\right)_3 = \frac{6\mu}{2\mu}$

$V_{ov3} = -680.6\,mV$

MP3

$V_{bias-PMOS} = 1.32\,V$

$V_x = 1.28\,V$

$I_{P2} = 20.9\,\mu A$

$\left(\frac{W}{L}\right)_2 = \frac{24\mu}{1\mu}$

$V_{ov2} = 155.8\,mV$

MN2

$V_{\sin} = -1.024\,V$

$I_{d2} = 20.9\,\mu A$

$\left(\frac{W}{L}\right)_1 = \frac{3\mu}{2\mu}$

$V_{ov1} = 720.5\,mV$

MN1

$V_{bias-NMOS} = -1.28\,V$

$100\,V$

$C_{in} = 220\,fF$

$I_{in}$
$100\,nA$

## 7.4 Bias Circuit - Enlarged



BIAS GENERATOR

$V_{DD} = 2.5V$

$I_{ref} = 12.26\mu A$

$I_{ref_1} = 13.77\mu A$

MP100

MP200

$\left(\frac{W}{L}\right)_{200} = \frac{4\mu}{2\mu}$

$V_{ov200} = -680mV$

$\left(\frac{W}{L}\right)_{100} = \frac{4\mu}{2\mu}$

$V_{ov100} = -680mV$

$V_{bias} - PMOS =$

$\left(\frac{W}{L}\right)_{400} = \frac{4\mu}{2\mu}$

$V_{ov400} = 453.5 mV$

$R_{200} = 16.7 k\Omega$

$V_{bias} - NMOS =$

$\left(\frac{W}{L}\right)_{300} = \frac{2\mu}{2\mu}$

$V_{ov300} = 720mV$

$V_{SS} = -2.5V.$

$I_d = 31.35\mu A$

MP800

$\left(\frac{W}{L}\right)_{800} = \frac{2\mu}{9\mu}$

$V_{ov800} = -3.3V$

$I_d = 121.3nA$

$\left(\frac{W}{L}\right)_{700} = \frac{5\mu}{2\mu}$

$V_{ov700} = 720mV$

MN700

$\left(\frac{W}{L}\right)_{900} = \frac{4\mu}{2\mu}$

$V_{ov900} = 45mV$

MN900

START-UP CIRCUIT