Homework #4

(Due: Wednesday, February 3, 2016, 5 PM)

1. Slide 32 of chapter 5 of the course reader shows how to use the EE214B "lookup" function to find the angular transit frequency ω_T and the current density I_D/W for a minimum length NMOS at a given g_m/I_D. Use the lookup function to determine the following parameters:
   a) The transit frequency (in Hz) for minimum-length NMOS and PMOS devices for g_m/I_D = 8 S/A. What is the ratio of the two numbers f_{TN}/f_{TP}?
   b) The current density for minimum-length NMOS and PMOS devices for g_m/I_D = 8 S/A. What is the ratio of the two numbers $(I_D/W)_N/(I_D/W)_P$?
   c) Repeat parts (a) and (b) for L = 0.36um. By which factor did f_T and I_D/W change for each case? Which factor would you have expected assuming the square law?

2. In this problem, you will re-design the amplifier shown on slide 34 of chapter 5. In order to obtain a larger 3-dB bandwidth, you decide to bias the device such that g_m/I_D = 7 S/A. All passive component sizes, the low-frequency gain target and the channel length are left unchanged from the example in the course reader.

   a) Compute the required bias current I_{TAIL}.
   b) Determine the device width using the current density chart (or the "lookup" function).
   c) Use the transit frequency chart (or the "lookup" function) to determine the device f_T and calculate all device capacitances as done in the example. Use an OCT estimate to calculate the 3-dB bandwidth of the circuit. There is no need to calculate the non-dominant pole frequency.
   d) An alternative way to calculate the device capacitance is to use the technology parameters given on slide 14 of chapter 4 together with the width determined in part (b). Compute all capacitances using this approach and compare to the values from part (c). The values should match reasonably well, and therefore a direct capacitance calculation is also viable once the device width is known.
   e) Verify the design using an HSpice .ac simulation, with 100 points per decade from 100 kHz to 10 GHz. Submit the .op bias point information for the transistors as well as a log-log plot of the frequency response with the annotated 3-dB bandwidth. Quantify the % error in 3-dB bandwidth between hand analysis and simulation.
   f) The design you have created in this problem achieves higher bandwidth than the one presented in class, but requires a larger tail current. Calculate the ratio f_{3dB}/I_{TAIL} for your design from part (e) and compare this number to what was achieved in class.

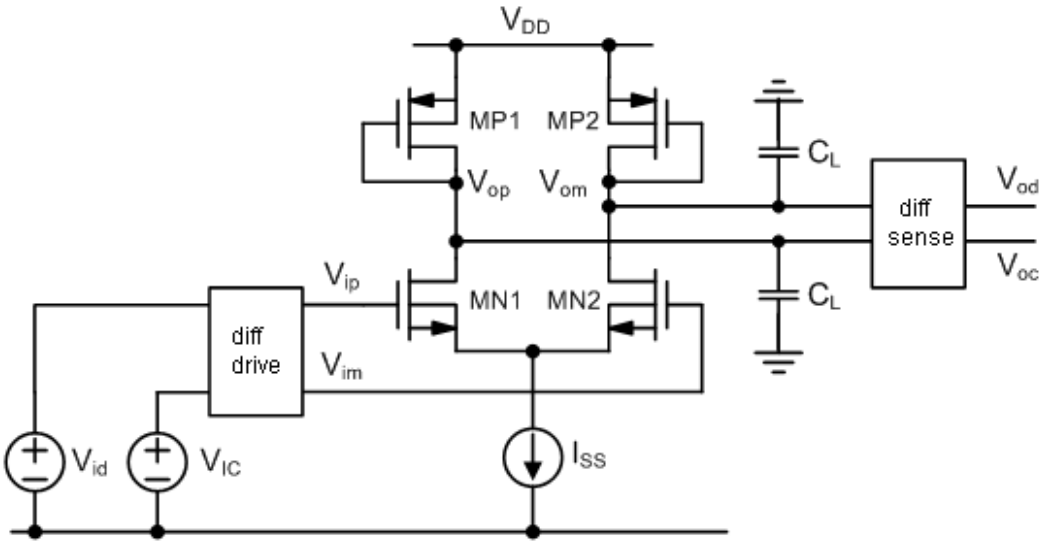
3. Consider the unity gain buffer amplifier shown below. The goal of this design is to achieve a DC gain of A_{v0} = 1 and a 3-dB bandwidth of f_{3dB} = 1.1 GHz for C_L = 500 fF, while minimizing the tail current I_{SS}. Assume an ideal voltage source input.

Assume that all channel lengths are identical, i.e. $L_P = L_N = L = 0.24\mu m$, $V_{IC} = 1.2$ V and $V_{DD} = 1.8$ V.

a) Write an expression for the low-frequency gain, A_{v0}. Neglect finite r_o.

b) Write an expression for the circuit's bandwidth, ignoring all device capacitances and finite r_o. In other words, include only g_m and C_L. Calculate the required transconductance for all transistors.

c) Assuming that g_m/I_D for the PMOS devices, $(g_m/I_D)_P$, is chosen to be 8 S/A[1], determine I_{SS} and the device widths for all transistors using the "lookup" function.



d) Simulate the design in HSpice. Note: "diffdrive" and "diffsense" blocks take care of the common/differential conversion. Please refer to the EE214B library file (/usr/class/ee214b/hspice/ee214_hspice.sp) for the examples on how to hook up these blocks. Find the actual 3-dB bandwidth and calculate the percent error relative to the design target. Since we have neglected all extrinsic capacitances, you should see a relatively large discrepancy. Submit a printout of your simulated ac response as well as the .op data for all transistors.

e) Calculate the following scale factor for your circuit

$$k = \frac{1}{2 - \frac{f_{3dB,desired}}{f_{3dB,simulated}}}$$

f) Multiply all device widths and I_{SS} by k and re-run your simulation. The bandwidth of the amplifier should now be very close to the desired 3-dB bandwidth. What are the new values for I_{SS} and f_{3dB}? Is there a change in the

[1] In practice, the choice of g_m/I_D at this point of the design procedure may come e.g. from requirements on the linearity of the circuit; to be covered later in this course.

g_m/I_D of the transistors? Why/why not? Submit a printout of your simulated ac response as well as the .op data for all transistors.

g) Explain (using basic algebra) how the magic "k-factor scaling" works, i.e. why does the design meet the bandwidth spec after scaling by k?

h) Unfortunately, the magic "k-factor scaling" applies only to simple examples where the bandwidth degradation is linearly proportional to the added parasitic capacitance. However, in more complex scenarios, it is still possible to achieve the proper sizing using an iterative "annealing" approach, outlined as follows:

1. Set $C_{self} = 0$.
2. Size the circuit to meet the 3-dB bandwidth requirement for $C_L + C_{self}$ (for the first iteration, this means that we are ignoring C_{self}).
3. Estimate C_{self} for the obtained design (using the device widths).
4. Go to step 2 using the new C_{self} estimate.

Typically, fewer than 10 iterations are sufficient for convergence. The code in `hw4p3.m` implements this method and provides the expression for the NMOS contribution to C_{self}. Why is C_{dbn} the only NMOS capacitance included? Determine which PMOS capacitances are relevant and add the corresponding expressions to the code. Submit a plot of I_{SS} over the 5 iterations. To what value did I_{SS} converge? What is the ratio of the final I_{SS} to the initial I_{SS}? This ratio tells us, in relative terms, how much additional power is required to maintain the 3-dB bandwidth in the presence of parasitic capacitances.

i) Determine the device widths for all transistors based on the design point obtained from the final iteration in part (h).

j) Simulate the design in HSpice to find the actual 3-dB bandwidth and calculate the percent error relative to the design target. Submit a printout of your simulated ac response as well as the .op data for all transistors.

4. In this problem you will redesign the circuit from problem 3, assuming that all specs remain the same, except that there is now no constraint on g_m/I_D. We wish to find the optimum g_m/I_D for the NMOS and PMOS devices that minimizes I_{SS}. We will accomplish this by adding an outer loop over values of $(g_m/I_D)_P$ from 5 S/A to 20 S/A. The inner loop will determine the I_{SS} required to meet the 3-dB bandwidth requirement using the iterative approach as before.

a) Modify the code in `hw4p4.m` to include expressions for the PMOS capacitances you chose to model in problem 3.

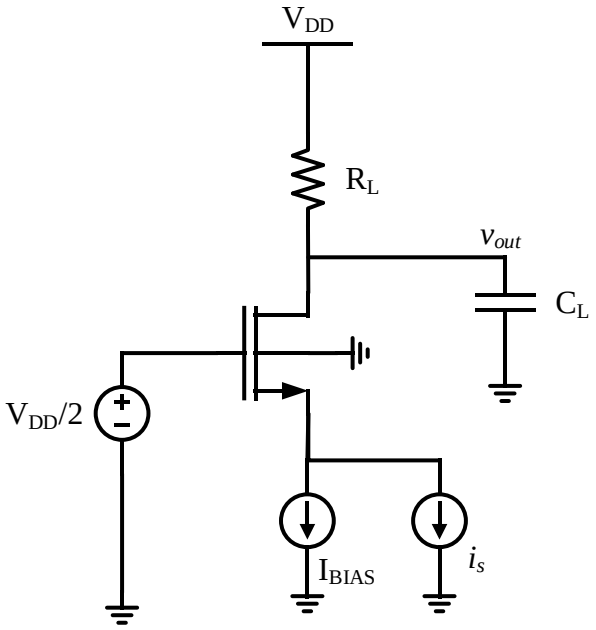
b) Submit a plot of I_{SS} over the range of $(g_m/I_D)_P$ from 5 S/A to 20 S/A. Using this plot, estimate the value of $(g_m/I_D)_P$ that minimizes I_{SS}. Annotate this design point on your plot.

c) Determine the device widths for all transistors based on the design point obtained in part (b).

d) Simulate the design in HSpice to find the actual 3-dB bandwidth and calculate the percent error relative to the design target. Submit a printout of your simulated ac response as well as the .op data for all transistors.

5. You are given a common-gate circuit as shown in the figure below. When this circuit is used in a feedback circuit, a typical sizing problem is to push the non-dominant pole to a sufficiently high frequency. In this example, the gate of the transistor is biased at $V_{DD}/2$ and the bulk is grounded. Other parameters are:

   $R_L = 6k\Omega$, $C_L = 100fF$, $I_{BIAS} = 100uA$, $V_{DD} = 1.8V$, $L = 0.18\mu m$.



   a) We will first consider the first order behavior of this stage by modeling the transistor with only C_{gs} and g_m. Draw a small-signal model and derive an expression for the transfer function from i_s to v_{out}.
   b) Write expressions for the frequency of the dominant pole, ω_{p1}, and the frequency of the non-dominant pole, ω_{p2}. Hint: look at chapter 5 slide 17 to get a feel for which pole will be dominant.
   c) Determine the value of g_m/C_{gs} required such that $\omega_{p2}/\omega_{p1} = 100$.
   d) We will now use the small-signal model of the transistor shown on chapter 4 slide 8. Using this model, derive an expression for the transfer function from i_s to v_{out}. You may neglect the output conductance g_o.
   e) Use your transfer function to show the following:

$$\omega_{p2} = \omega_T \left(\frac{C_{gg}}{C_{ss}}\right)\left(1 + \frac{g_{mb}}{g_m}\right)$$

$$\omega_{p1} = \frac{1}{R_L\left[C_L + \left(\frac{C_{dd}}{C_{gg}}\right)\left(\frac{1}{\omega_T}\right)\left(\frac{g_m}{I_D}\right)I_{BIAS}\right]}$$

Recall the definitions of C_{gg}, C_{dd}, and C_{ss}:

$$C_{gg} = C_{gs} + C_{gb} + C_{gd}$$

$$C_{dd} = C_{gd} + C_{db}$$

$$C_{ss} = C_{gs} + C_{sb}$$

f) In part (e), we wrote the two frequencies in terms of width-independent ratios that we can determine from the g_m/I_D of a transistor using the lookup function. Fill in the expression for ω_{p2} in `hw4p5.m`, and plot ω_{p2}/ω_{p1} over the range of g_m/I_D from 5 S/A to 20 S/A. Using the plot, estimate the required value of g_m/I_D such that $\omega_{p2}/\omega_{p1} = 100$. Submit your plot with this value of g_m/I_D annotated.

g) Lookup I_D/W and ω_T using the value of g_m/I_D you found in part (f). Use I_D/W to size the transistor.

h) Simulate the circuit in HSpice using a .op analysis. Write down the values of ω_T and g_m/I_D from simulation and compare to the values from part (g). Note: in terms of HSpice model elements, ω_T = `gm/cgtot`.

i) Run a .pz analysis. State the percent error between ω_{p2}/ω_{p1} from simulation and the design target value of 100.

j) Did the value of g_m/C_{gs} you calculated in part (c) provide a reasonable approximation for the value of ω_T found with the .op simulation?