2016 EE214B Design Project - Part I

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1 Bias Calculations

1.1 Node Definitions

$V_{C1} = V_{E2} = V_W$
$V_{B3} = V_{C2} = V_{B4} = V_X$
$V_{E3} = V_Y$
$V_{E4} = V_Z$
$V_{B1} = V_{IN}$

1.2 Bias Voltages

$$V_{IN} = V_{BE} = 0.8V \tag{1}$$

$$V_{B2} = 1.6V => V_W = 1.6 - V_{BE} = 0.8V \tag{2}$$

Assuming Ib = 0

$$V_{IN} = V_Y => V_Y = 0.8V \tag{3}$$

$$V_X = V_Y + V_{BE} => V_X = 1.6V \tag{4}$$

$$V_Z = V_X - V_{BE} => V_Z = 0.8V \tag{5}$$

$$V_O = V_{CC} - IB4R_{C4} => V_O = 2.3V \tag{6}$$

$$I_{C1} = I_{C2} = \frac{V_{CC} - V_{B3}}{R_{C2}} = 3.6mA \tag{7}$$

$$I_{C3} = I_{Bias3} = 4.5mA \tag{8}$$

$$I_{C4} = I_{Bias4} = 2.0mA \tag{9}$$

Parameter	Hand Calc	Spice Value	Percent Error%
V_{IN}	0.800V	0.801V	-0.12%
V_W	0.800V	0.798V	0.25%
V_X	1.600V	1.605V	-0.31%
V_Y	0.800V	0.804V	-0.49%
V_Z	0.800V	0.813V	-1.50%
V_O	2.300V	2.301V	-0.04%
gm_1	120.7mS	120.7mS	-0.03%
gm_2	120.3mS	120.3mS	-0.03%
gm_3	152.3mS	152.3mS	0.02%
gm_4	70mS	70mS	-0.04%
$r\pi_1$	2.14kΩ	1.875kΩ	14.3%
$r\pi_2$	2.14kΩ	1.883kΩ	13.64%
$r\pi_3$	1.71kΩ	1.502kΩ	13.84%
$r\pi_4$	3.85kΩ	3.515kΩ	9.5%

2 Calculations and plots for part I (c) through (f)

After applying two-port analysis for loop gain calculation:

$$a = (r_{\pi 1}||R_F) \cdot (-gm_1 R_{C2}) \cdot \frac{gm_3 R_F}{1 + gm_3 R_F} = -5.486k\Omega \tag{10}$$

$$f = \frac{-1}{R_F} = -4.5mS \tag{11}$$

$$t = af = 26.57 = 28.48dB \tag{12}$$

Mid-band transresistance of the overall amplifier:

$$A_{CL,MidBiand} = \frac{a}{1+t} \cdot \frac{-gm_4 R_{C4}}{1 + gm_4 R_{E4}} = 724 = 57.2dB \tag{13}$$

Calculating node resistances and capacitances:

$$C_X = C_{\mu 2} + \frac{C_{\pi 3}}{1 + gm_3 R_F} + \frac{C_{\pi 4}}{1 + gm_4 R_{E4}} + C_{\mu 3} + C_{\mu 4}(1 + gm_4 R_{C4}) = 99fF \tag{14}$$

$$R_X = R_{C2}||r_{\pi 3}(1 + gm_3 R_F)||r_{\pi 4}(1 + gm_4 R_{E4}) = 241\Omega \approx R_{C2} \tag{15}$$

$$C_{IN} = C_D + C_{\pi 1} + C_{\mu 1} = 324fF \tag{16}$$

$$R_{IN} = r_{\pi 1}||R_F = 199\Omega \approx R_F \tag{17}$$

Calculation of most significant poles:

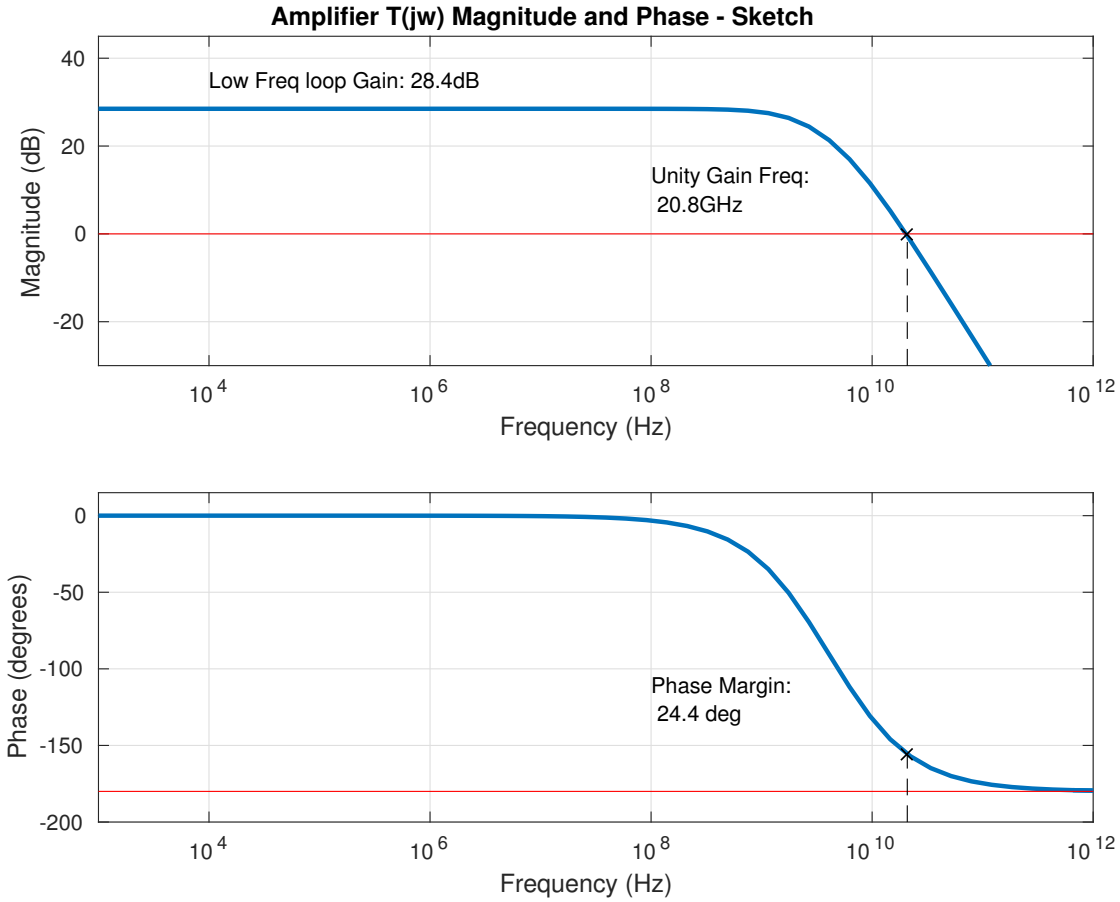
$$f_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} = 2.46GHz \tag{18}$$

$$f_X = \frac{1}{2\pi R_X C_X} = 6.63GHz \tag{19}$$

Calculation of $T(j\omega)$ Unity Gain Frequency and Phase Margin

$$f_u = \sqrt{T_0 * f_{IN} * f_X} = 20.8GHz \tag{20}$$

$$PM = 180^\circ - atan(\frac{f_u}{f_{IN}}) - atan(\frac{f_u}{f_X}) = 24.4^\circ \tag{21}$$



The low value of phase margin suggests that significant peaking will be observed.

$$a(s) = (R_{IN}||\frac{1}{sC_{IN}}) \cdot gm_1 \cdot (R_X||\frac{1}{sC_X}) \cdot \frac{gm_3 R_f}{1 + gm_3 R_F} \tag{22}$$

$$\frac{v_{E3}}{i_s} = \frac{a(s)}{1 + a(s)f} \tag{23}$$

$$\frac{v_{E3}}{i_s} = \frac{a(s)}{1 + a(s)f} \tag{24}$$

$$f_0 = \sqrt{(1 + T_0) * f_{IN} * f_X} \approx f_u \tag{25}$$

$$Q = \frac{\sqrt{(1 + T_0)\omega_X \omega_{IN}}}{\omega_X + \omega_{IN}} = 2.29 \tag{26}$$

3 Old

Choice of L

- All devices used in current source have a minimum length of 2μm.
- All other devices in the amplifier have minimum length of 1μm. Minimum length is used as f_t is inversely proportional to L.
- All devices in bias generator circuit have length >=2μm.

Bias Generator circuit

- Constant gm reference based design is used as bias circuit to reduce mismatch errors.
- Transconductance of bias device (mn300) depends only on R2 and m (m is the ratio of MN300/MN400). Therefore gm can be set precisely.
- Start-up circuit is used to force the circuit to the desired operating point.

Approximations for hand calculations
For simpler hand calculations, following approximations are used.

1. $Cdb = Csb = 0.35Cgs$
2. $Cgs = (\frac{2}{3})WLCox + Cov'W$
3. $Cgd = Cov'W$
4. $gmb = 0.2gm$

Stage4

- As per the spec, common mode output voltage (vout) has to be within -0.15v to 0.15v. Since the body is connected to vss, MN10 experiences back gate effect and the threshold voltage is given by:

$$\begin{aligned} Vt &= Vt_0 + \gamma(\sqrt{2\phi f + V_{sb}} - \sqrt{2}\phi f \\ Vt_0 &= 0.5V, \gamma = 0.6, 2\phi f = 0.8 \end{aligned} \tag{27}$$

- Stage 4 is a source follower which has a gain given by

$$A4 = \frac{gm_{10}}{gm_{10} + gmb_{10} + (\frac{1}{R_L})} \tag{28}$$

- Gain of stage4 (A4) <1 due to back gate effect and the output load.
- To achieve gain closer to 1 (0.6 - 0.7), it is important to size and bias MN10 such that $(gm_{10} + gmb_{10}) >> (1/R_L)$.
- Transconductance of and drain current of MN_{10} is given by

$$gm_{10} = \mu nCox(\frac{W}{L})vov_{10} \tag{29}$$

$$Id_{10} = 0.5\mu nCox(\frac{W_{10}}{L_{10}})vov_{10}^2(1 + \lambda(Vdd - Vout)) \tag{30}$$

- MN_9 (bias device for source follower) is sized such that $Id_{10} + I_{R_L} = Id_9$ and the common mode output voltage does not fall out of range. This device is chosen to be of smaller size to reduce loading on Vout node.

$$\tau_{OUTPUT} = (R_L || \frac{1}{1.2gm_{10}})(C_L + Csb_{10} + Cgd_9 + Cdb_9) \tag{31}$$

- Cgs10 is assumed to be very small due to boot-strapping.

Stage 3

- Loading at node Vy increases with the increase in gain of stage 3 due to the miller effect. Hence gain of stage3 is kept low and is fixed at sqrt(2) to compensate for the gain lost in stage 4. Gain of stage3 (CS amplifier with diode connected load):

$$|A3| = \frac{gm7}{gm8} = \frac{Vov8}{Vov7} = \frac{Vdd - Vz - abs(Vtp)}{Vy - Vss - Vtn} = \sqrt{2} \tag{32}$$

- Choice of Vz from above (stage4) determines Vy.

- Minimum device sizes (W=2μm, L=1μm) are used for both MN7 and MP8 to reduce loading on Vy and Vz.

$$Id_7 = Id_8 = 0.5\mu nCox(\frac{W_7}{L_7})vov_7^2(1 + \lambda(Vz - Vss)) \tag{33}$$

$$\tau_Z = (\frac{1}{gm_8})(Cgs_8 + Cdb_8 + Cgd_{10} + Cgd_7(1 + \frac{1}{|A3|}) + Cdb_7) \tag{34}$$

Stage 2

- Vy from stage Z above determines the required ratio of R3 and R4.

$$(\frac{R4}{R3}) = \frac{Vss}{Vy} - 1 \tag{35}$$

- Gain of stage Y (Cascode amplifier) is set to 3.

$$|A2| = gm4(R3||R4) \tag{36}$$

- Vov_4 and W_4 are optimized to reduce τ_X.

- MN6 is sized such that current through MN6 is same as the current through MP4 and MP5.

$$Id4 = Id5 = Id6 = 0.5\mu pCox(\frac{W4}{L4})(Vdd - Vx - abs(Vtp))^2(1 + \lambda(Vdd - Vw) \tag{37}$$

- Current through R3 and R4

$$I_{R3} + I_{R4} = Vss/(R3 + R4) \tag{38}$$

$$\tau_Y = (R3||R4)(Cgs_7 + Cgd_7(1 + |A3|) + Cgd_6 + Cdb_6 + Cgd_5 + Cdb_5) \tag{39}$$

Stage 1

- Vov_4 from stage 2 sets V_X which in turn sets the ratio of R1 and R2.

$$Vov_4 = Vdd - Vx - |Vtp| \tag{40}$$

$$(\frac{R1}{R2}) = \frac{Vdd}{Vx} - 1 \tag{41}$$

- Gain of stage 1 (Common gate amplifier) is set to 10000.

$$|A1| = (R1||R2) \tag{42}$$

- MN1 and MP3 are sized such that Id1 = Id3.
- MN2 is sized to reduce τ_{IIN} node. τ_{IIN} is inversely proportional to gm_2.

$$\tau_{IIN} = (\frac{1}{gm2})(Cin + Cgd_1 + Cdb_1 + Cgs_2 + Csb_2) \tag{43}$$

$$\tau_X = (R1||R2)(Cgd_2 + Cdb_2 + Cgd_3 + Cdb_3 + Cgs_4 + Cgd_4) \tag{44}$$

- Current through MN1, MN2 and MP3

$$Id_{1,2,3} = 0.5\mu pCox(\frac{W_3}{L_3})(Vdd - VbiasP - |Vtp|)^2(1 + \lambda(Vdd - Vx)) \tag{45}$$

- Current through R1 and R2

$$I_{R1} + I_{R2} = Vdd/(R1 + R2) \tag{46}$$

Vovn, Vovp

- Vovn and Vovp are chosen to achieve a reasonable balance between gain, Tau total and Power, and our choice was educated by the gm/Id technology plots.

Total Design Performance

$$|A_{TOTAL}| = A1 * A2 * A3 * A4 \tag{47}$$

$$\tau_{TOTAL} = \tau_{IIN} + \tau_X + \tau_Y + \tau_Z + \tau_{OUTPUT} \tag{48}$$

$$Power = (Vdd - Vss)(Id_1 + Id_4 + Id_7 + Id_{10}) + (\frac{Vdd^2}{R1 + R2}) + (\frac{Vss^2}{R3 + R4}) \tag{49}$$

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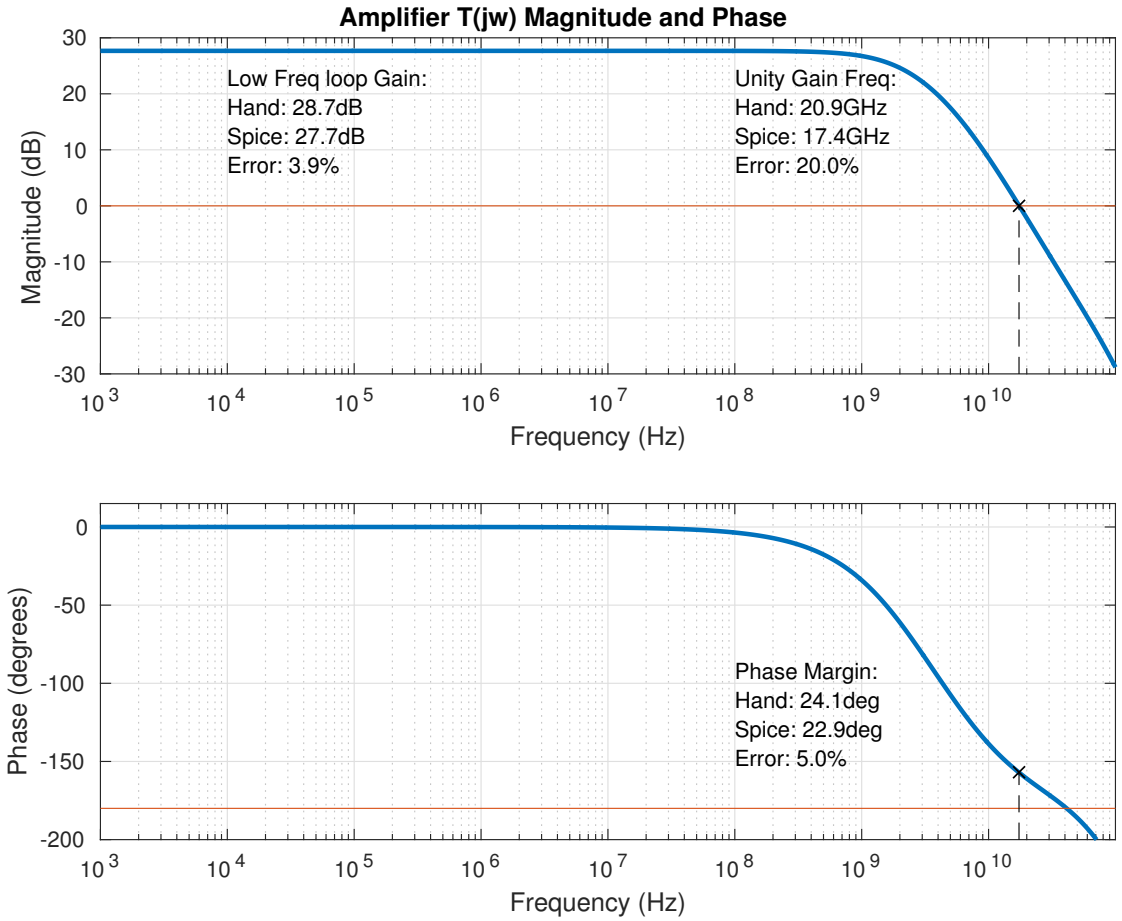
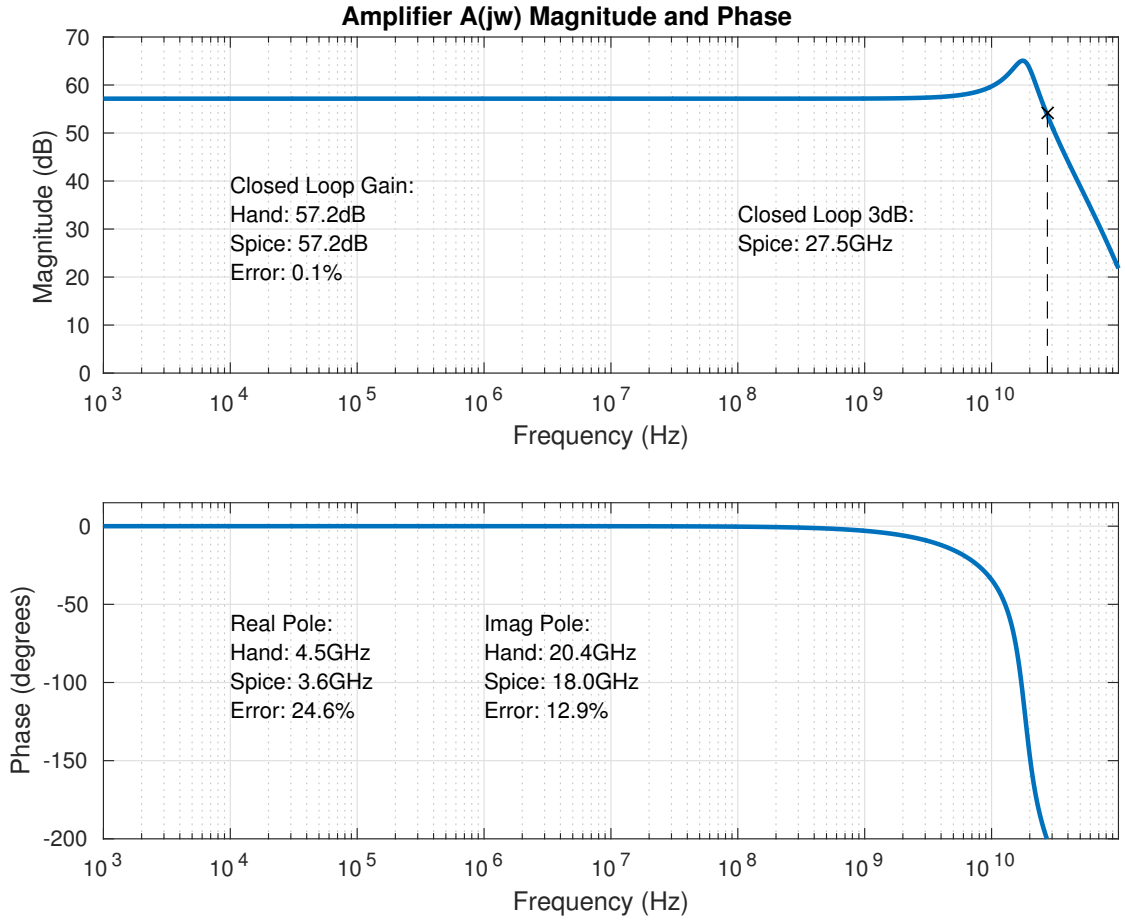
4 Bode Plots and PZ Outputs - Part I(g,h)






```
**************************************************
   ******   pole/zero analysis
   input =  0:is          output = v(vo)
   poles (rad/sec)                 poles ( hertz)
   real            imag            real            imag
   -33.1562m       0.              -5.27698m       0.
   -22.9305g       113.319g        -3.64950g       18.0353g
   -22.9305g       -113.319g       -3.64950g       -18.0353g
   -473.782g       0.              -75.4048g       0.
   -1.12800t       0.              -179.526g       0.
   -1.18039t       0.              -187.865g       0.

   zeros (rad/sec)                 zeros ( hertz)
   real            imag            real            imag
   0.              0.              0.              0.
   -1.10418t       0.              -175.736g       0.
```

5 Calculations for Part I(i)

A feedback capacitor can be used to introduce a zero into the feedback loop in order to push the higher frequency pole out and flatten the response of the closed loop amplifier. The optimally flat response of the amplifier occurs when Q = $\sqrt{2}$. Hence:

$$\omega_0 = 1.09e11 rad/s \tag{50}$$

$$\omega_Z = \frac{\omega_0}{\sqrt{2} - \frac{\omega_{P1}+\omega_{P2}}{\omega_0}} \tag{51}$$

$$C_F = \frac{1}{\omega_Z R_F} = 57fF \tag{52}$$

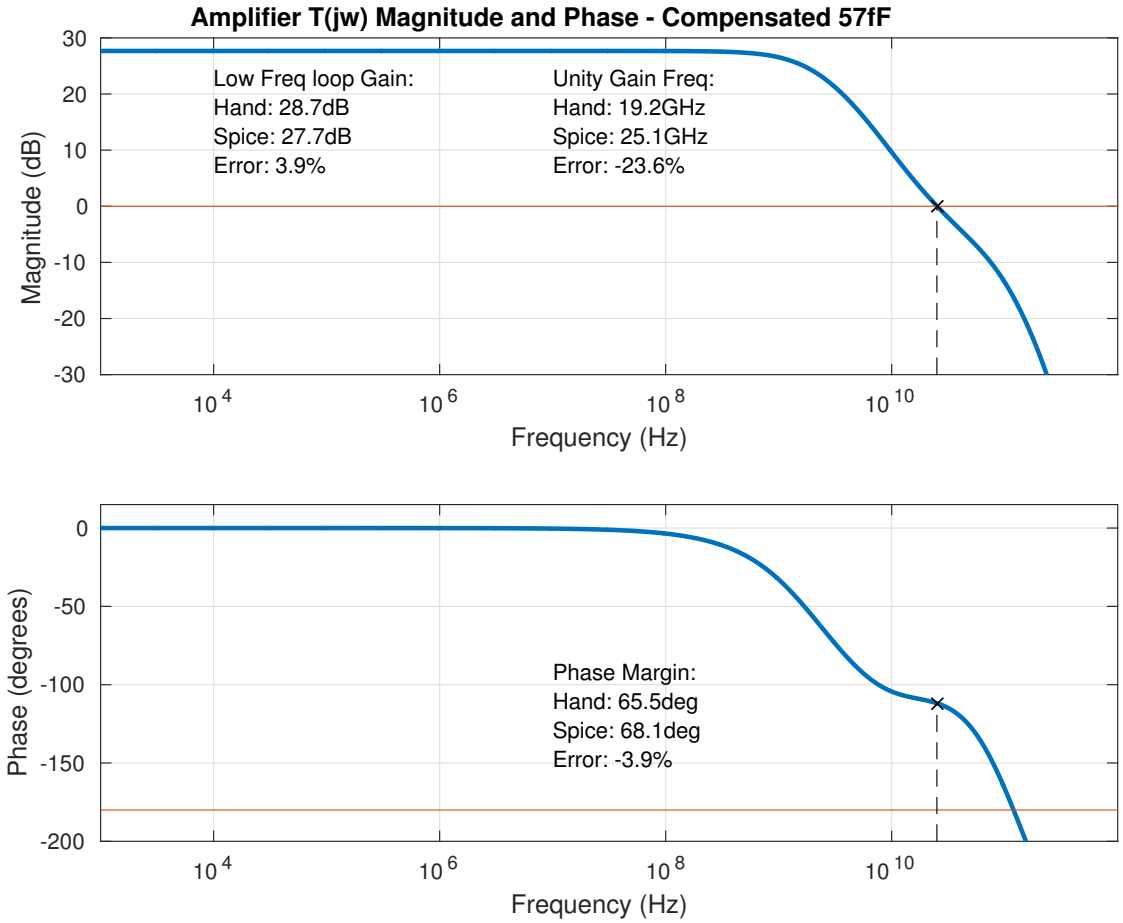
From this, the new closed loop bandwidth can be calculated as such:

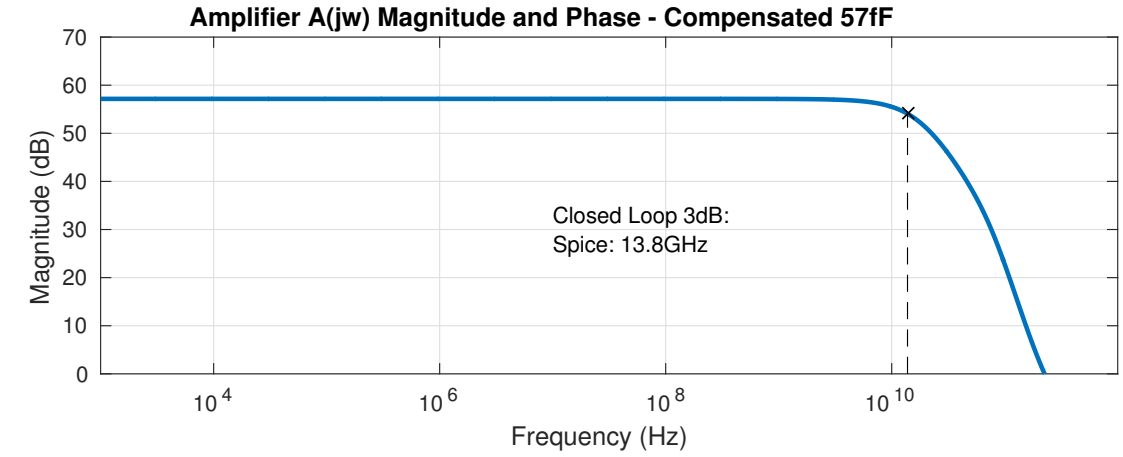
$$C_{in,C_F} = C_{in} + C_F \tag{53}$$

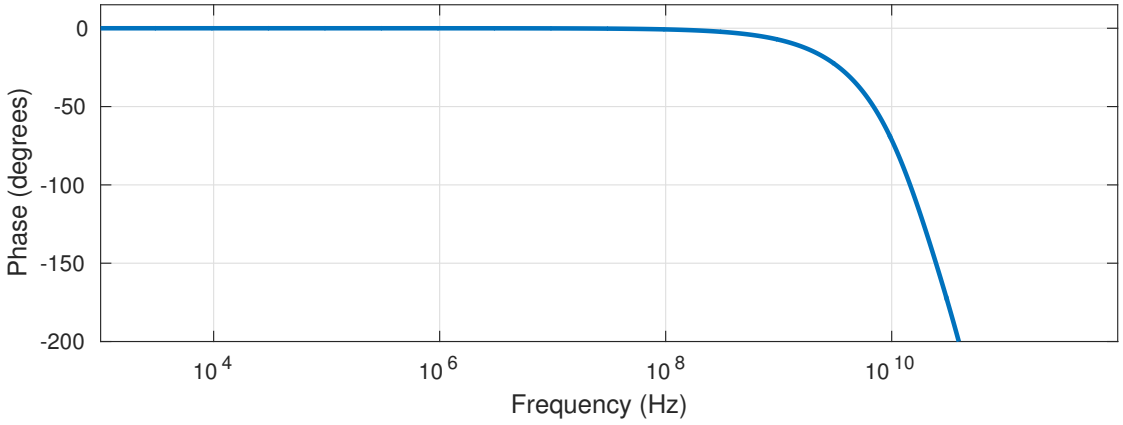
$$k = \frac{R_{in} * Q1_{gm} * R_x * A_{V3}}{R_F} \tag{54}$$

$$BW_{CL,C_F} = \frac{\sqrt{1+k}}{2\pi R_{in} C_{in} R_x C_x} = 19.2Ghz \tag{55}$$

6 Bode Plots and PZ Outputs - Part I(j)








```
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   poles (rad/sec)                poles ( hertz)
   real            imag           real            imag
   -33.1562m       0.             -5.27698m       0.
   -102.336g       -49.5561g      -16.2872g       -7.88710g
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   -321.575g       358.533g       -51.1803g       57.0622g
   -321.575g       -358.533g      -51.1803g       -57.0622g
   -1.11894t       0.             -178.085g       0.
   -1.35128t       0.             -215.063g       0.
   -1.88412t       0.             -299.868g       0.

   zeros (rad/sec)                zeros ( hertz)
   real            imag           real            imag
   0.              0.             0.              0.
   -1.09418t       0.             -174.144g       0.
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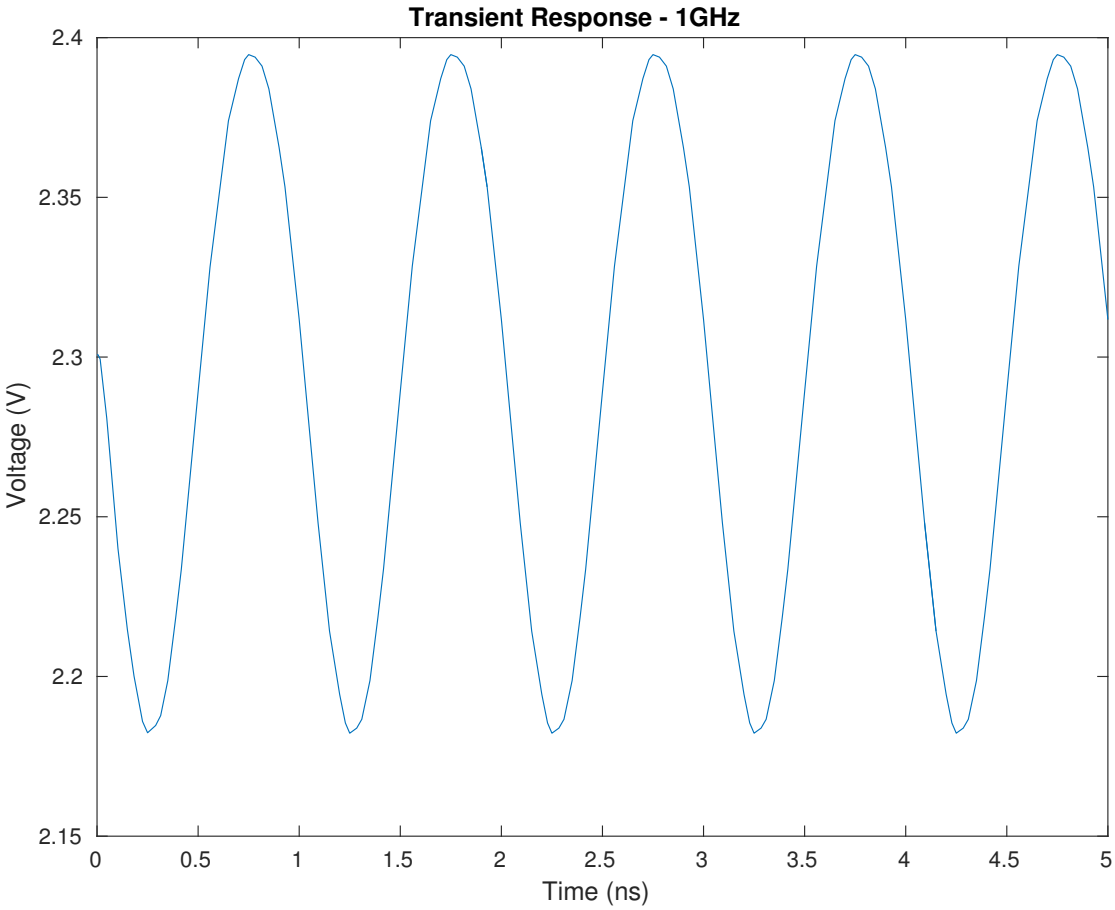
7 Transient Response - Part I(m)