40 Gbit/s transimpedance amplifier with high linearity range in 0.13 μm SiGe BiCMOS

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A 40 Gbit/s transimpedance amplifier (TIA) implemented in 0.13 μm SiGe BiCMOS with high linearity range is presented. The TIA features 24.2 dB (65.2 dB Ω) gain, a bandwidth of 34.2 GHz and a power consumption of only 80 mW from a 2.5 V supply. Total harmonic distortion is less than 5% up to an input current of 1.3 mA_{pp}.

Introduction: Until recently, optical communication systems have mainly used on–off keying (OOK). Currently, long-haul transport systems are starting to adapt quadrature phase-shift keying (QPSK) modulation schemes for 40 Gbit/s and 100 Gbit/s data transmission. Owing to the multi-level nature of the received signal in these systems, and in order to make digital dispersion cancellation possible, the TIA in such systems needs to operate in the linear mode. Specifications such as [1] define a maximal total harmonic distortion (THD) of 5% within the dynamic range of the TIA. This Letter presents a TIA implemented in a 0.13 μm SiGe BiCMOS technology with 24.2 dB (65.2 dB Ω) gain, a bandwidth of 34.2 GHz and a power consumption of only 80 mW from a 2.5 V supply, which fulfils the THD specification up to an input current of 1.3 mA_{pp}. It is therefore suitable for both 40 Gbit/s OOK and 100 Gbit/s QPSK communication systems. To the best of the authors' knowledge, this is the first realisation of such a linear TIA at 40 Gbit/s in the literature.

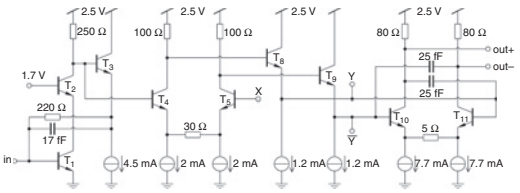

Fig. 1 *TIA schematic*

Auto-zero feedback loop is connected between points X, Y and Ȳ, 1.7 V generated on-chip

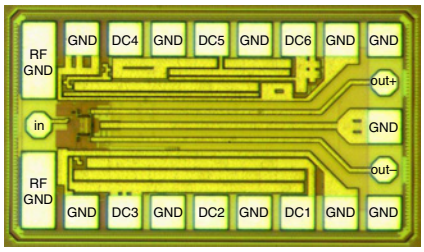

Fig. 2 *Chip micrograph (chip dimensions 0.5 × 1 mm)*

Circuit design: The schematic of the TIA is shown in Fig. 1. The circuit features three gain stages. A low-frequency auto-zero feedback amplifier (not shown in Fig. 1) senses nodes Y, Ȳ and adjusts the voltage at node X in order to keep the differential pair T_4/T_5 in balanced operation for all DC input currents. The circuit has been carefully optimised for increased input linearity. First, the nonlinear distortions created in the input stage are reduced by strong shunt-shunt feedback. The output node of the feedback stage is the collector of T_2 instead of the emitter of T_3. This enables the circuit to work with a low supply voltage of 2.5 V. An additional feedback capacitance (17 fF) is used for pole shifting in order to ensure a smooth frequency response. A DC input current exists because the photodiode senses optical power and thus always delivers positive currents. If this current flows into the TIA input and then into the feedback resistor, the voltage headroom of the current source of T_3 will be reduced. This can create distortion, if the output transistor of the current source enters the saturation region. Also this can cause nonlinear variations in the base-emitter voltage of T_3, which in turn distorts the output voltage of the stage. To prevent this, the bias current of T_3 is chosen sufficiently higher than the maximum input current, and the transistors are sized fairly large. Secondly, the middle stage creates distortion, if the transistors leave the pure class-A operation range. Emitter degeneration is used to expand the linear range of this stage. This leads to lower output voltage swing and gain, but bandwidth is enhanced. Therefore no inductive peaking is needed, enabling a smaller circuit footprint. Finally, for the output stage, negative Miller capacitances increase the linearity and bandwidth.

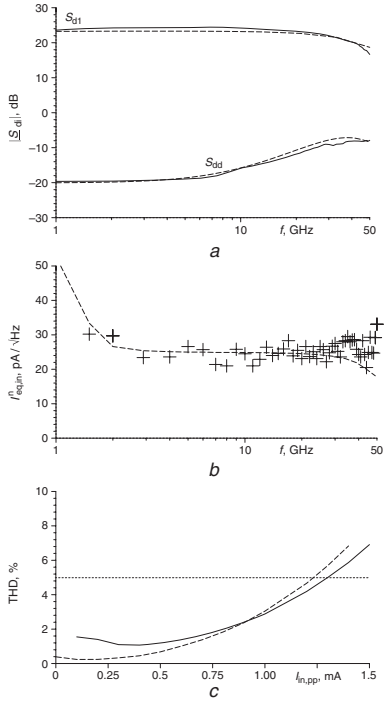

Fig. 3 *Measurement results (solid line) compared to simulations (dashed line)*

a S-parameters, differential gain S_{d1} and output matching S_{dd}
b Input-referred noise current density
c Linearity

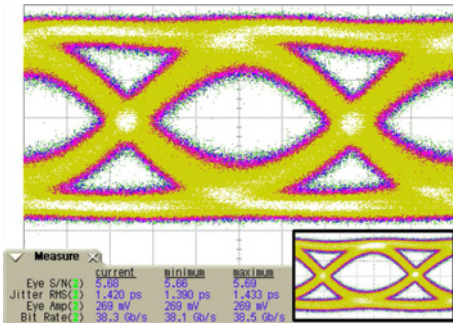

Fig. 4 *40 Gbit/s output eye diagram*

Input eye is shown in bottom right corner, with amplitude of 1 mA_{pp}

Measurement results: The circuit was implemented in the IHP 0.13 μm SiGe BiCMOS process with $f_{T,max}$ of 240 GHz [2], A chip micrograph is shown in Fig. 2. *S*-parameters were measured on-wafer using a Rohde & Schwarz ZVA67 vector network analyser. Results are shown in Fig. 3*a*. The TIA has a gain of 24.2 dB and a transimpedance of 65.2 dB Ω (1800 Ω) with a bandwidth of 34.2 GHz. Differential output matching is better than −7 dB over the entire bandwidth. The measured input resistance is lower than 20 Ω up to 10 GHz, and less than 40 Ω over the entire bandwidth. Noise measurements, leaving the input open, show an input referred noise current density of ∼25 pA/√Hz up to 20 GHz and <30 pA/√Hz up to 50 GHz, as shown in Fig. 3*b*. The linearity of the TIA was evaluated by measuring the THD using a Rohde & Schwarz FSU67 spectrum analyser according to specifications in [1] using a 1 GHz input signal. The THD was determined taking account the power of the first 10 harmonics. The input DC current was adjusted according to the amplitude assuming an extinction ratio (ER) of 6 dB. Measurements show that the input DC current does not have any significant influence on the THD, so that similar results should be obtainable for different values of ER. The THD at input current amplitudes below

100 μA could not be measured as the results then are dominated by noise. As shown in Fig. 3*c*, the TIA shows very low harmonic distortion (below 5%) in a wide input range up to 1.3 mA_{pp}. Large-signal measurements showed open eyes within that range and well beyond. An example 40 Gbit/s output eye diagram for an input current of 1 mA_{pp} is given in Fig. 4. Eye amplitude is 270 mV, and RMS jitter is 1.4 ps. Power consumption is 80 mW from a single 2.5 V supply.

Conclusions: A 40 Gbit/s TIA with high linearity range has been successfully demonstrated. Despite being the first device explicitly optimised for a high linearity range and the trade-offs between linearity and gain/power/noise described above, the presented TIA still has a low power consumption compared to the state of the art in 40 Gbit/s TIAs given in Table 1.

Table 1: Comparison to state of the art in silicon-based 40 Gbit/s TIAs

Ref.	Bandwidth (GHz)	Transimpedance (Ω)	Noise current pA/√Hz	Linearity range (mA_{pp})	Supply voltage (V)	DC power (mW)	Technology
[3]	31	350	56	N/A	1.8	60*	0.18 μm CMOS
[4]	30	4500	N/A	N/A	1.8	32*	0.25 μm BiCMOS
[5]	50	140	30	N/A	5.2	182	200 GHz BiCMOS
[6]	38	6000	20	0.3	3.3	150	0.25 μm BiCMOS
This work	**34**	**1800**	**25**	**1.3**	**2.5**	**80**	**0.13 μm BiCMOS**

*single-ended output

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One or more of the Figures in this Letter are available in colour online.

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