A 1V, 8GHz CMOS Integrated Phase Shifted Transmitter for Wideband and Varying Envelope Communication Systems

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Abstract

A novel fully integrated Phase Shifted (PS) transmitter is presented in this paper. The PS transmitter employs switching power amplifiers, operates without mixers and provides an intermodulation distortion free output spectrum making it a suitable choice for mobile communication systems. The RF blocks of the PS transmitter include a local oscillator, phase shifters, switching class F power amplifiers and wideband output combiners. The PS transmitter is implemented in a standard 0.18μm CMOS technology, with 1 level of polysilicon and 6 levels of metallization, and occupies an area of 5000×1000μm^2. It operates from a 1V supply and provides 35dBc adjacent channel power ratio for output bandwidths up to 50 MHz at 8GHz. The combined class F PAs in the PS transmitter provide 20dBm output power with a 38% power added efficiency.

1. Introduction

Wireless, mobile phone systems support communication between a large number of users and the base station in cellular networks. For the uplink, when the mobile users transmit voice, image and data signals to the base station, QPSK modulation and CDMA multiplexing ensure efficient spectral usage for high bit-rate and high quality communications. Compared to other modulation and multiplexing schemes, a QPSK-CDMA system, generates a varying envelope signal which must be linearly amplified to high power levels for long range communications.

Linear power amplifiers (PAs) designed in bipolar technologies are commonly used in direct upconversion QPSK-CDMA transmitters due to their good linearity and performance [1-4]. However, for high level integration of compact mobile handsets, the RF transmitters must be integrated in the same CMOS technology used to implement the digital back-end circuits in the handsets.

At high output power levels, CMOS PAs exhibit limited efficiency as well as nonlinearities which lead to spectral regrowth and signal distortion [5]. As a result, PAs for varying envelope signals in direct up conversion transmitters require linearization. Use of digital adaptive predistortion, envelope elimination and restoration (EER), and diode linearizers have been reported [6-8]. However, when CMOS PAs are linearized, their efficiency is further reduced.

Design of efficient transmitter front-ends in low voltage submicron CMOS technologies for varying envelope signals is difficult to achieve for long range communication systems with stringent linearity requirements and large bandwidth to support high data rates at high RF frequency. None of the linearized transmitters reported to date satisfy such requirements simultaneously. This paper presents the design and implementation of a new Phase Shifted (PS) transmitter to achieve the required objectives. The design uses switching power amplifiers for efficient and fast operation while maintaining the linearity of the amplified wideband RF signal.

2. Phase Shifted Transmitter

The Phase Shifted transmitter, shown in Fig. 1, is a new approach to realize a linear and efficient transmission based on the outphasing concept [9]. The essence of the outphasing techniques lies in the realization that any envelope and phase modulated signal can be represented by the summation of two components with fixed envelope but varying phases. The advantage of this transformation is that each phase modulated component can be amplified using highly nonlinear yet power efficient techniques without generating Adjacent Channel Interferences (ACI). The PS transmitter front-end is similar to that of other outphasing architectures such as LINC (LInear amplification using Nonlinear Components) [10], CALLUM (Combined Analog Locked Loop Universal Modulator) [11] and VLL (Vector Locked Loop) [12] systems. However, there is no mixer to upconvert the IF signal to RF or downconvert the RF signal to the baseband for reference feedback signals. Instead, two constant envelope varying phase RF signals are generated by direct phase variation of the RF signals using phase shifters. Elimination of the IF Signal Component Separator (SCS), mixers and the feedback in the PS transmitter results in high speed and wideband operation, cancellation of gain and phase misalignments between the two constant envelope signals and an intermodulation distortion free output spectrum.

The baseband DSP in the PS transmitter converts the input data into in-phase and quadrature components $s_i(t)$ and $s_q(t)$ similar to the baseband DSP of a direct upconversion transmitter. In a direct upconversion transmitter, the RF signal s(t) after upconversion is given by

$$s(t) = [s_i(t) + js_q(t)] \times e^{j[\omega_0 t]} \quad (1)$$

or

$$s(t) = r(t) \times e^{j[\omega_0 t + \phi(t)]} \quad (2)$$

where

$$r(t) = \sqrt{s_i^2(t) + s_q^2(t)} \quad (3)$$

and $\phi(t)$ is given by

$$\phi(t) = \tan^{-1}\left[\frac{s_q(t)}{s_i(t)}\right] \quad (4)$$

The signal s(t) can also be expressed as sum of two,

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constant envelope, varying phase, signals as

$$s(t) = s_1(t) + s_2(t) \quad (5)$$

where $s_1(t)$ and $s_2(t)$ are given by

$$s_1(t) = r_{max} e^{j[\omega_0 t + \phi(t) + \theta(t)]} \quad (6)$$

and

$$s_2(t) = r_{max} e^{j[\omega_0 t + \phi(t) - \theta(t)]} \quad (7)$$

where $\theta(t)$ is given by

$$\theta(t) = \cos^{-1}\left[\frac{r(t)}{2r_{max}}\right] \quad (8)$$

and r_{max} is the peak of the s(t) envelope.

The baseband phase control voltage generator in the PS transmitter, generates two output voltages V_p and V_m, proportional to $\phi(t)+\theta(t)$ and $\phi(t)-\theta(t)$ respectively, which are fed to the phase shifters to adjust the phase of the two RF signals provided by the local oscillator and generate the signals $s_1(t)$ and $s_2(t)$. The two signals are amplified through nonlinear PAs and are finally added together through the combiner to produce an amplified linear replica of the upconverted signal As(t).

The circuit design and implementation of RF section of the PS transmitter are presented in the following sections.

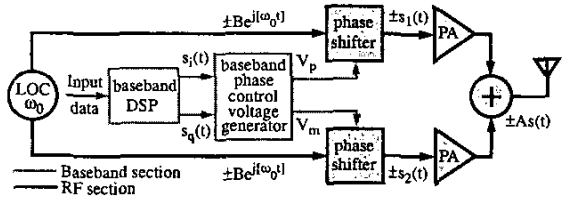

Fig. 1. The Phase Shifted transmitter architecture

A. Local Oscillator

The local oscillator of the PS transmitter is designed using a negative transconductance architecture [13], as shown in Fig. 2. The advantages of this architecture are simplicity and large signal swing at RF, required to drive the following stages.

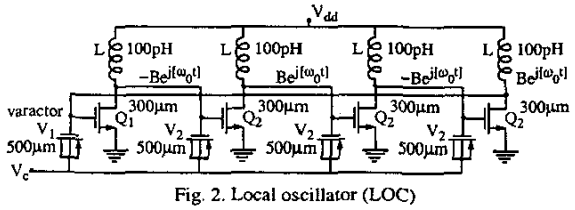

Fig. 2. Local oscillator (LOC)

B. Phase Shifter

The phase shifter of the PS transmitter is realized using a half wavelength ($\lambda_0/2$) lumped line connected between driving amplifiers as shown in Fig. 3 [14]. A $\lambda_0/2$ lumped line is realized using cascades of two quarter wavelength ($\lambda_0/4$) lumped lines. Each $\lambda_0/4$ lumped line is realized using cascades of n segments of LC ladder networks. Assuming that the PMOST varactors with a channel width of W have an average capacitance of C, the values of L and C to emulate the delay characteristics of a $\lambda_0/4$ transmission line are selected as follows [15]

$$L = \frac{Z_0}{4nf_0} \quad (9)$$

$$C = \frac{1}{4nf_0 Z_0} \quad (10)$$

where Z_0 is the characteristic impedance of the $\lambda_0/4$ lumped line and f_0 is the frequency of the RF signal. The varying phase shift, $\phi(t)\pm\theta(t)$, provided by the lumped lines is given by

$$\phi(t) \pm \theta(t) = 2\pi n f_0 \sqrt{L \cdot \Delta C} \quad (11)$$

where ΔC represent the change in varactor capacitors with respect to the phase control voltage applied to the varactor terminals. As a result, the phase shift can be curve fitted and be represented by the equation

$$\phi(t) \pm \theta(t) = K \cdot f(V) \quad (12)$$

where K is a constant and V represents either V_p or V_m phase control voltages. The phase-voltage transfer function of the phase shifter can be approximated by a sine function [14] and the phase shifter provides up to $\pm\pi$ (rad) relative phase shift between the two constant envelope signals. This phase shift is sufficient enough to generate varying envelope signals with large peak-to-average ratios at the output of the PS transmitter.

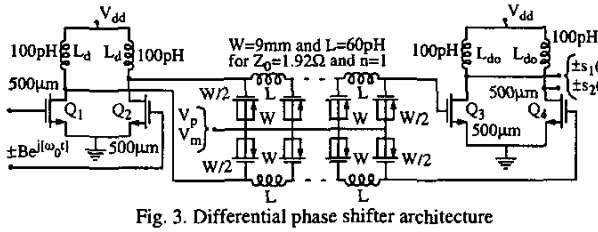

Fig. 3. Differential phase shifter architecture

C. Power Amplifier and Output Combiners

The power amplifiers in the PS transmitter can be realized using one of the nonlinear switching architectures such as class E or class F. A class E PA, can achieve maximum efficiency at low supply voltages because of its higher optimum load compared to a class F design. However, the class E PA requires the power switch to handle higher voltages than a class F design making the class F the preferred alternative to realize the PAs.

A possible realization of the PS transmitter front-end using class F PAs and single stage $\lambda_0/4$ transmission lines is illustrated in Fig. 4. The $\lambda_0/4$ transmission lines connected between the switching transistors and the antenna perform three tasks. First, they form the class F PA architectures [16], second, they make the summation of the two constant envelope with varying phase signals feasible at the antenna [15] and third, they match the output resistance of the switching transistors to the antenna through the transformation

$$Z_{in} = \frac{Z_0^2}{Z_{out}} \quad (13)$$

where Z_{in} is the effective impedance at the drain of the power transistors and Z_{out} is the impedance of the antenna.

Impedance matching using a single $\lambda_0/4$ line, as illustrated in Fig. 4, uses one step to transform Z_{in} to Z_{out}. For large impedance transformation ratios, the reflection coefficient between the two impedances increases resulting in a narrowband impedance transformation.

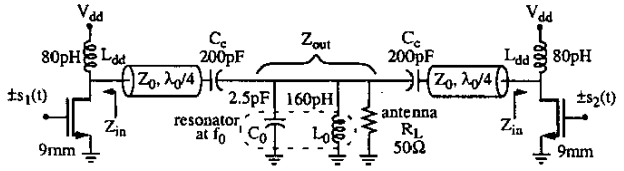

Fig. 4. Realization of the PS transmitter front-end

To achieve wideband impedance matching, transformation must be performed in smaller ratios to reduce the reflection coefficients between the transformed impedances [17]. The impedance matching using a cascade of three lines, employed in the design of the PS transmitter, is illustrated in Fig. 5(a). The three stage wideband $\lambda_0/4$ lumped lines were designed to add two 8GHz signals and to match 0.55Ω source resistance to a 50Ω antenna and ideally deliver 1.5W power from a 1V class F power amplifier as shown in Fig. 5(b) [17]. To deliver the output power to the antenna, a large power transistor with high current handling capability is required. Such a transistor has a large parasitic capacitance at its drain which can be included in the realization of the large input capacitance of Z_{01}.

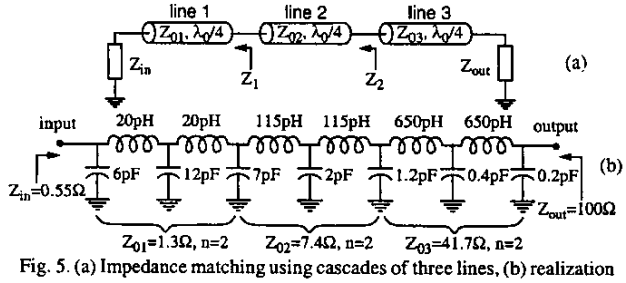

Fig. 5. (a) Impedance matching using cascades of three lines, (b) realization of the three stage wideband $\lambda_0/4$ lumped line

3. Implementation and Experimental Results

The fully differential PS transmitter was designed to operate from 1V with a fully symmetrical layout in a standard 0.18μm CMOS technology with 1 level of polysilicon and 6 levels of metallization. The chip micrograph of the PS transmitter and its corresponding block diagram are shown in Fig. 6. The designed fully differential PS transmitter occupies an area of $5000\times1000\mu m^2$.

The two differential 8GHz RF signals provided by the on-chip local oscillator are applied to the phase shifters. The phase shifters generate the two constant envelope with varying phase signals and apply them to the power transistors. These transistors have an aspect ratio of 9mm/0.18μm and are laid out using a checkerboard approach. Compared to the conventional interdigitated layout, this checkerboard approach reduces the gate, source and drain resistances of the large transistors resulting to better performance for switching power applications. The amplified varying phase signals are added through the combiners which are connected to output through 200pF MIM coupling capacitors. The phase shifted transmitter output includes an 8GHz on-chip resonator to allow direct connection to a 50Ω antenna. The capacitor in the output resonator is the bottom plate capacitance of the output coupling capacitors. All DC biasing pads are connected to 30pF on-chip MIM capacitors to reduce the effects of the bias insertion circuitry. All chip floor is covered by metal1 ground plane connected to the substrate everywhere, except under the inductors to maximize their self resonance frequency. The connection between the PAs and the output are realized using the two top metal layers in parallel to reduce the ohmic loss. For testing purposes, the phase control voltages V_p and V_m are provided by two external function generators.

The experimental output spectrum, corresponding to the maximum bandwidth generated by the PS transmitter, is shown in Fig. 7 with a wide range frequency span (10 times the bandwidth). The output spectrum provided by the PS transmitter is free of any intermodulation distortion and provides outputs bandwidths as high as 50MHz at 8GHz and the adjacent channel power ratio (ACPR) for various output power levels is better than 35dBc.

From the postlayout simulations, the power added efficiency (PAE) of each class F PA is as high as 60% at 30dBm output power (P_{out}). However, when the outputs of the class F PAs are combined together, the average PAE and Pout of the transmitter front-end will depend on the phase shift between the two constant envelope signals because of the constructive and destructive power addition. For relative phase shifts up to $\pm\pi/3$ (rad), sufficient enough to emulate the varying envelope of a QPSK-CDMA system, the average postlayout simulated and measured P_{out} and PAE of the combined class F PAs of the PS transmitter versus the supply voltage are shown in Fig. 8. At 1V supply voltage, the measured P_{out} and PAE are 20dBm and 38% respectively.

The characteristics of the PS transmitter are listed in Table I. It achieves high frequency and low voltage operation for a competitive performance compared to previously reported designs of varying envelope communication systems implemented in CMOS technologies, as documented in the table. It also provides an intermodulation distortion free output spectrum due to the elimination of mixers. The PS transmitter represents the first integrated approach to realizing a linearized transmitter based on the outphasing concept.

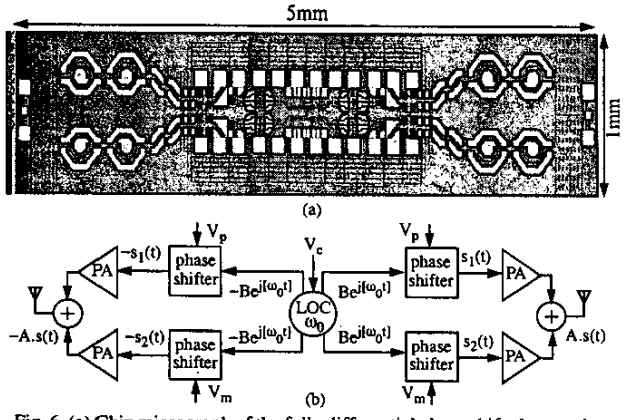

Fig. 6. (a) Chip micrograph of the fully differential phase shifted transmitter and (b) its corresponding block diagrams

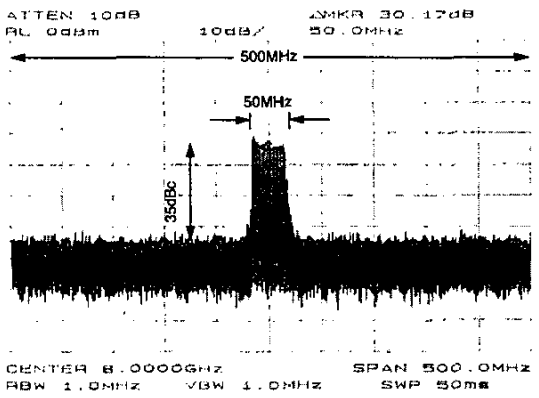

Fig. 7. The output spectrum of the PS transmitter with a wide range frequency span

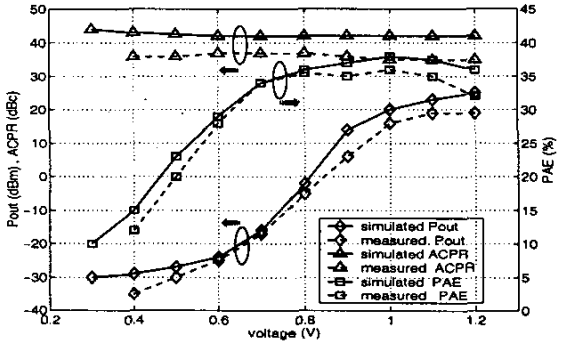

Fig. 8. Characteristics of the class F PAs of the PS transmitter

TABLE I. Characteristics of recently reported transmitter front-ends for varying envelope communication systems

ref.	technology	architecture and application	operating frequency	supply voltage	output power	PAE	linearization method	ACPR and bandwidth
this work	0.18μm CMOS	phase shifted WCDMA	8GHz	1V	20dBm	38%	outphasing	35dBc @ 50MHz
[6]	0.25μm CMOS	direct upconversion NCDMA	900MHz	3.5V	27dBm	48%[a]	digital adaptive predistortion	49dBc
[7]	0.8μm CMOS	direct upconversion NADC	900MHz	3.3V	26dBm	36%[a]	Envelope Elimination Restoration	30dBc @ 30KHz
[8]	0.25μm CMOS	direct upconversion WLAN	2.4GHz	2.5V	20dBm	28%	diode linearizing	28dBc

a. Uses off-chip GaAs power amplifier for measurement

4. Conclusion

A fully integrated and novel phase shifted transmitter suitable for mobile communication applications which operates without mixers and provides an intermodulation distortion free output spectrum was presented in this paper. The PS transmitter was designed in a standard 0.18μm CMOS with 1 level of polysilicon and 6 levels of metallization and occupies an area of $5000\times1000\mu m^2$. The transmitter uses a negative transconductance local oscillator, continuously adjustable phase shifters, class F power amplifiers and three stage wideband RF combiners. It operates from a 1V supply and provides 35dBc adjacent channel power ratio for output bandwidths up to 50 MHz at 8GHz. The combined class F PAs of the PS transmitter achieve 38% power added efficiency at 20dBm output power level.

Acknowledgment

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