

A 60 dBΩ 2.9 GHz 0.18 μm CMOS Transimpedance Amplifier for a Fiber Optic Receiver



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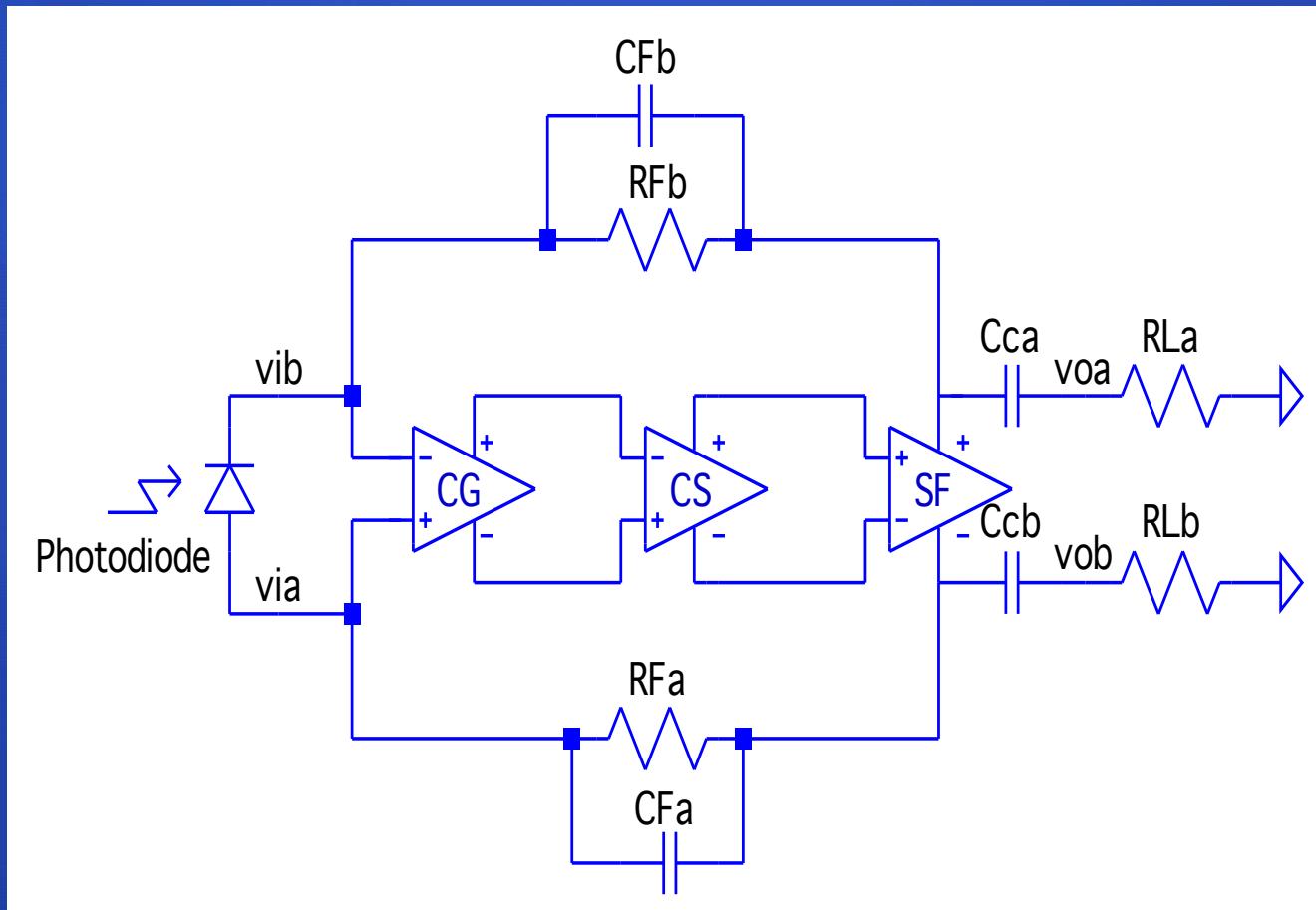


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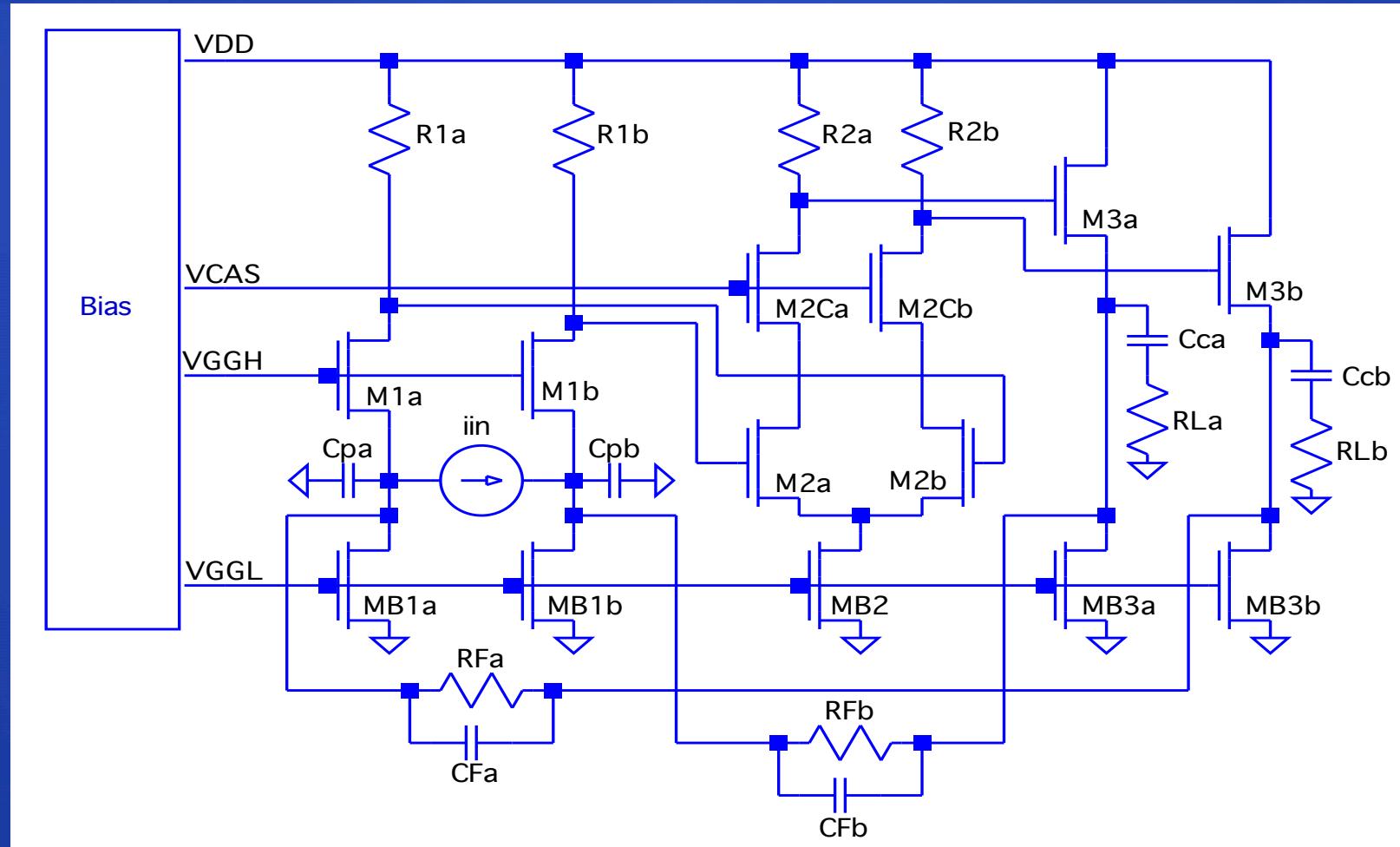


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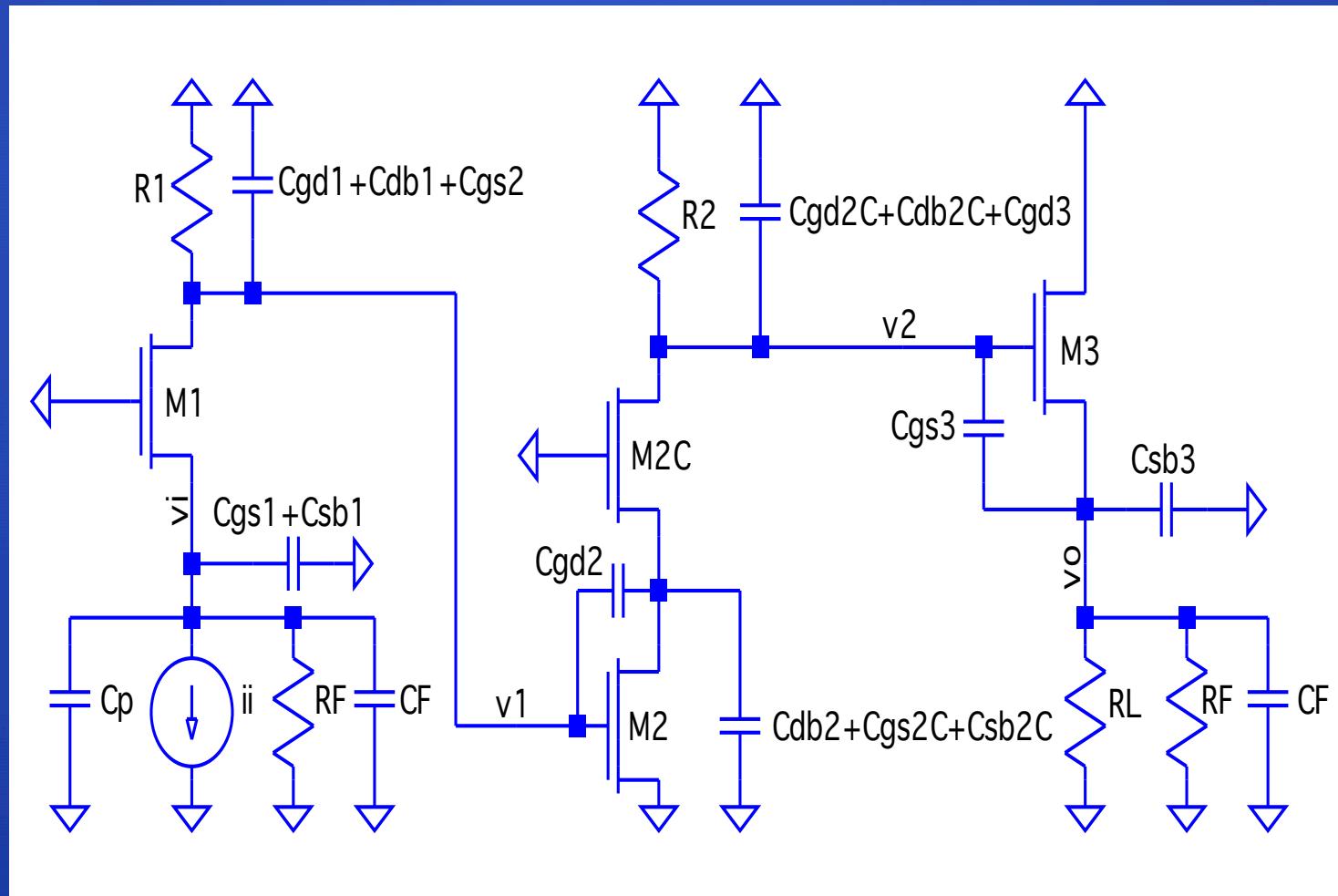
TIA's Topology



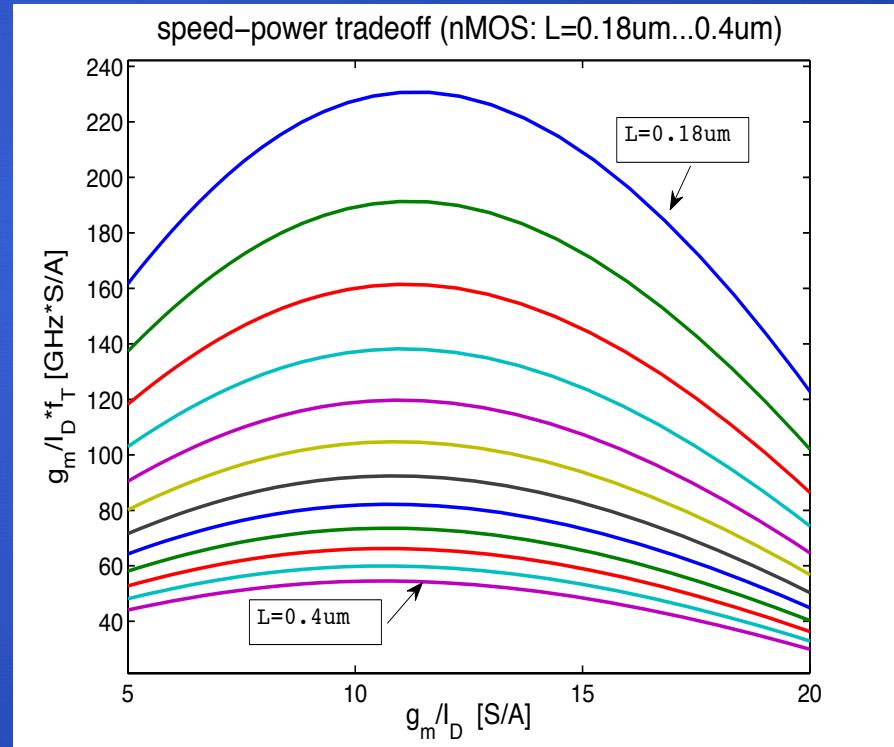
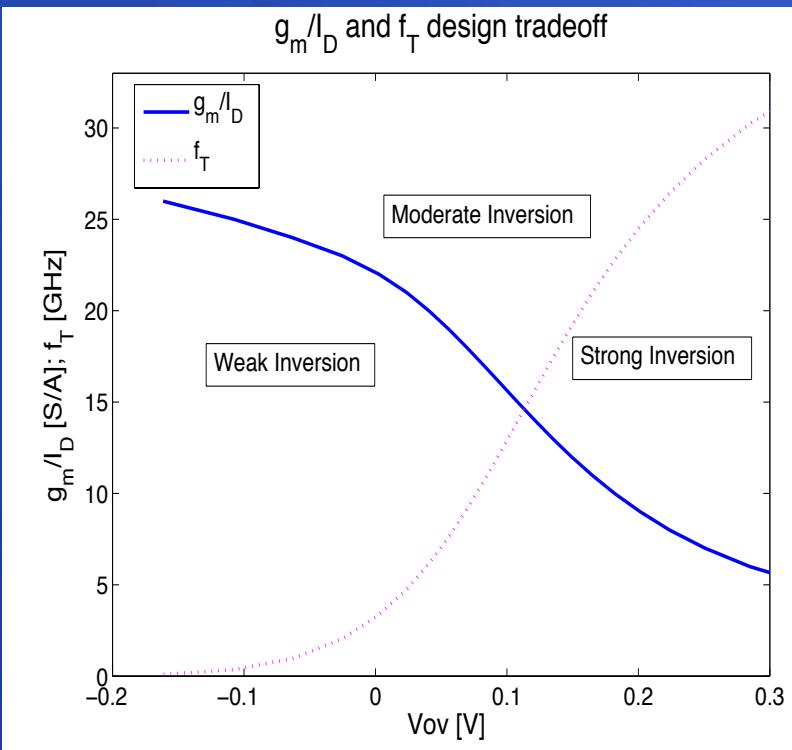
TIA's Schematic



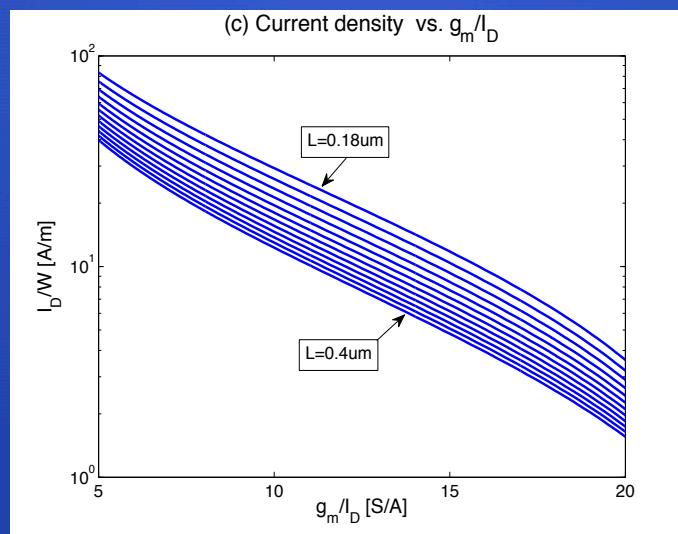
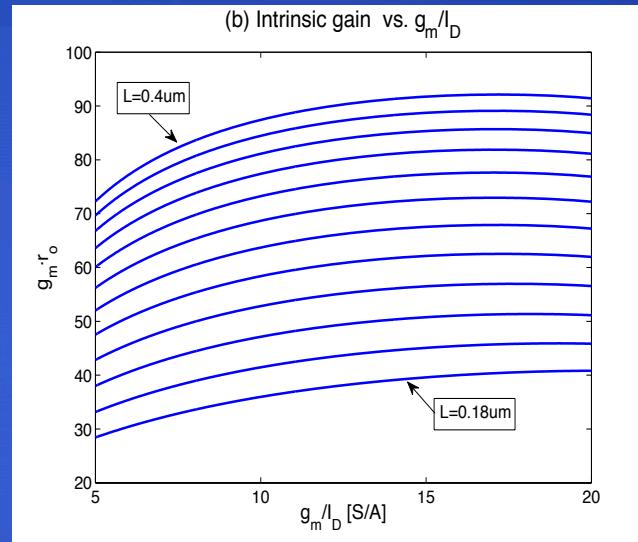
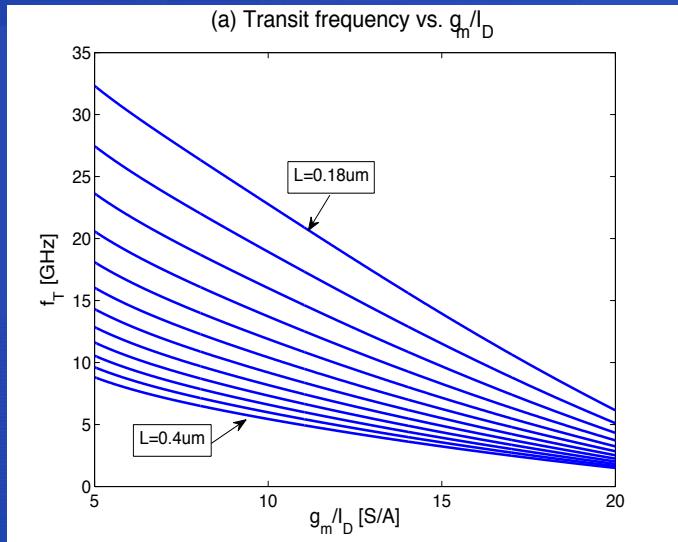
TIA's AC half circuit with FB loading and relevant capacitances



g_m/I_D Design Methodology



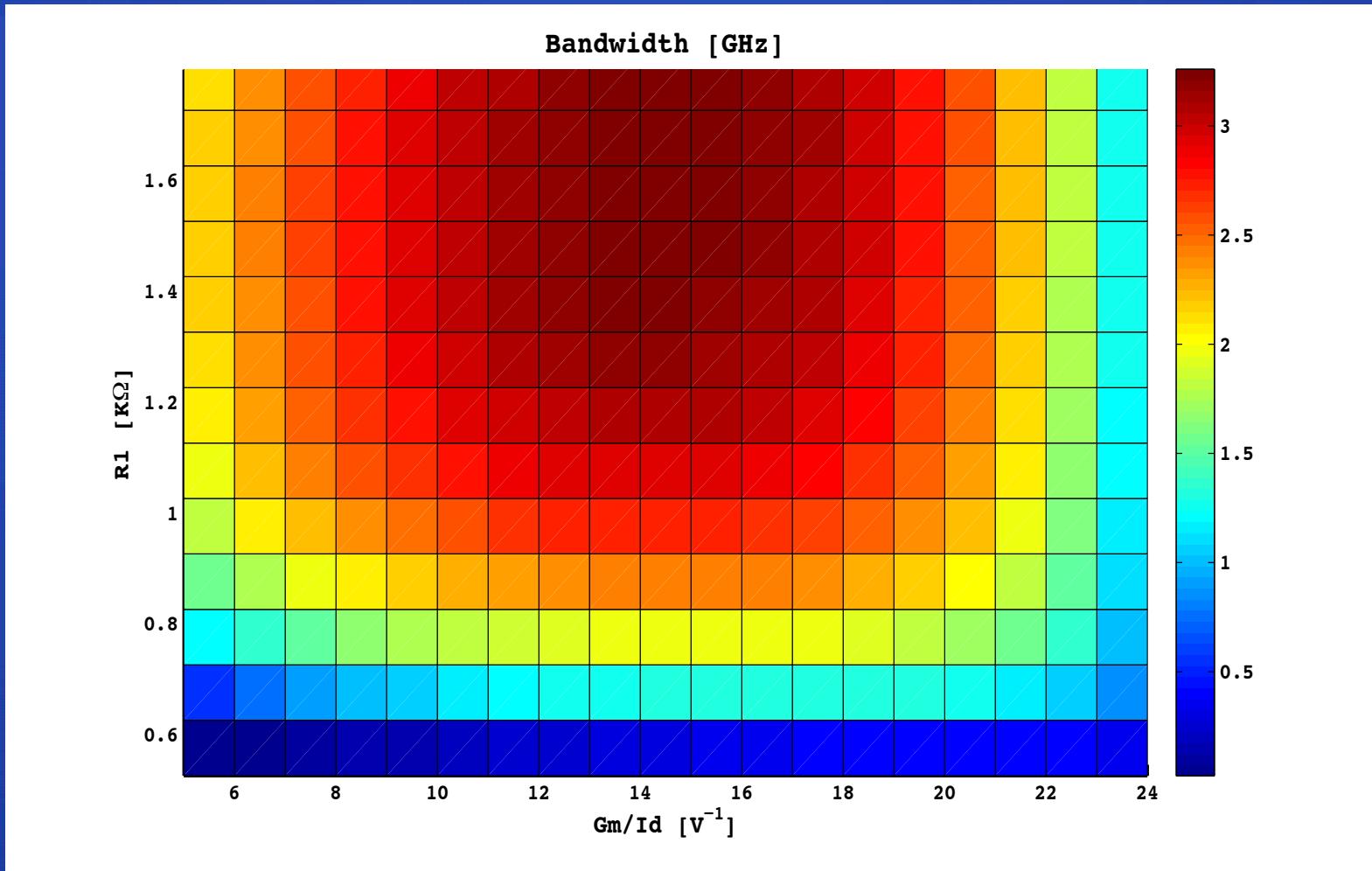
g_m/I_D Look-up Tables



Optimization Flow

- S1. Set the same initial bias current for each stage of the amplifier
- S2. Set the loop gain T_0 to an appropriate value ($T_0 \geq 10$) and derive R_F ($a_0 = A_0(1+T_0)/2$; $f_0 = T_0/a_0$; $R_F = 1/f_0$).
- S3. Determine g_m/I_D for the transistor M_3 (CD stage) based on the voltage bias allowing the max output signal swing and compute the corresponding transient frequency f_{T3} . Select an appropriate value of bias current $g_{m3}=I_{D3} \cdot g_{m3}/I_{D3}$ based on $C_{gg3}=g_{m3}/(2\pi f_{T3})$ such that the time constants associated with the CD stage are not dominant. Estimate the parasitic capacitances and compute the resulting A_{CD} .
- S4. Set the remaining bias current to be equally split between CS and CG stage and compute the amount of combined gain needed to meet specifications: $A_{CG}A_{CS} = a_0/A_{CD}$
- S5. Partition the required gain between CS and CG. An excessive value of A_{CS} causes a strong miller effect at the intermediate node between the transistors M_2 and M_{2C} and results in a non optimal value of the dominant time constant τ_2 . Similarly an excessive value of A_{CG} implies an excessive value of R_1 and results in a suboptimal value of the dominant time constant τ_2 . Appropriate values of A_{CS} and A_{CG} are in the following ranges: $1 \leq A_{CS} \leq 20$ and $a_0/A_{CD}/A_{CS_max} \leq A_{CG} \leq a_0/A_{CD}$
- S6. Set g_m/I_D for transistor M_1 and R_1 as the primary design variables. The values of g_{m1}/I_{D1} and R_1 set the value of A_{CG} . The value of A_{CG} set the value of A_{CS} and therefore the value of g_{m2}/I_{D2} and R_2 .
- S7. Sweep g_{m1}/I_{D1} from low inversion region ($g_{m1}/I_{D1}=25$ S/A) to high inversion region ($g_{m1}/I_{D1}=5$ S/A) and R_1 from A_{CG_min} to A_{CG_max} . Record the performance metrics of every feasible design in the explored space. Design feasibility and the current bias for the CG and CS are determined by the bias condition constrains.
- S8. Determine the TIA design with the best bandwidth, and summarize its parameters: g_{m1}/I_{D1} , I_{D1} , R_1 , A_{CG} , g_{m2}/I_{D2} , I_{D2} , R_2 , A_{CS} , g_{m3}/I_{D3} , I_{D3} , and A_{CD}
- S9. Determine transistor widths from g_m/I_D , the calculated I_D , and the current density (I_D/W) look-up tables.

TIA's Optimization Plot: BW vs. g_m/I_D and R_1



Results

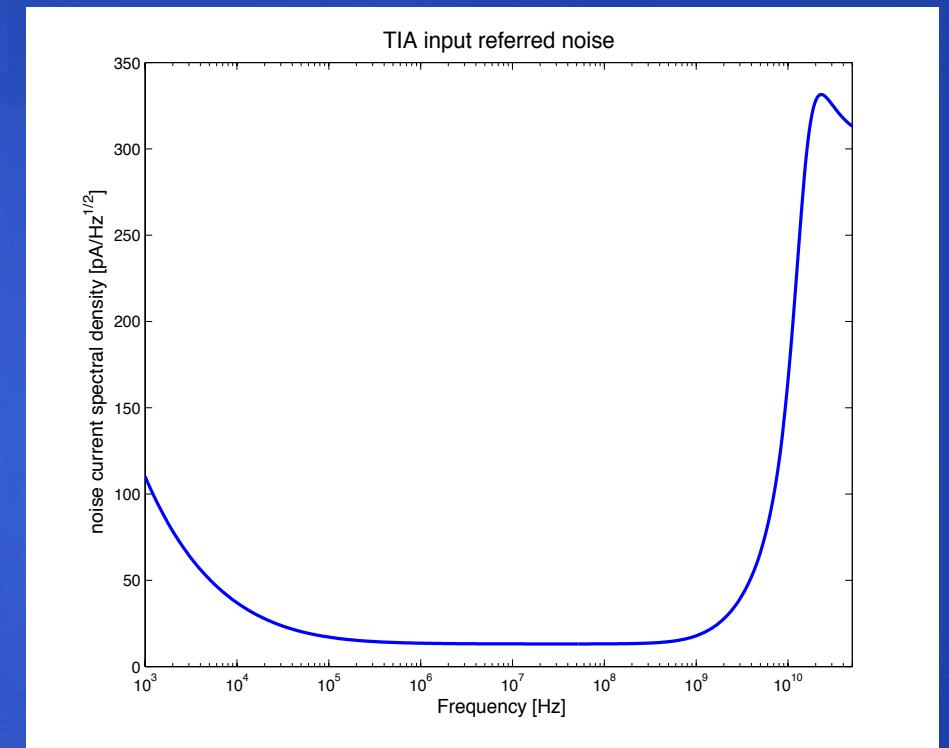
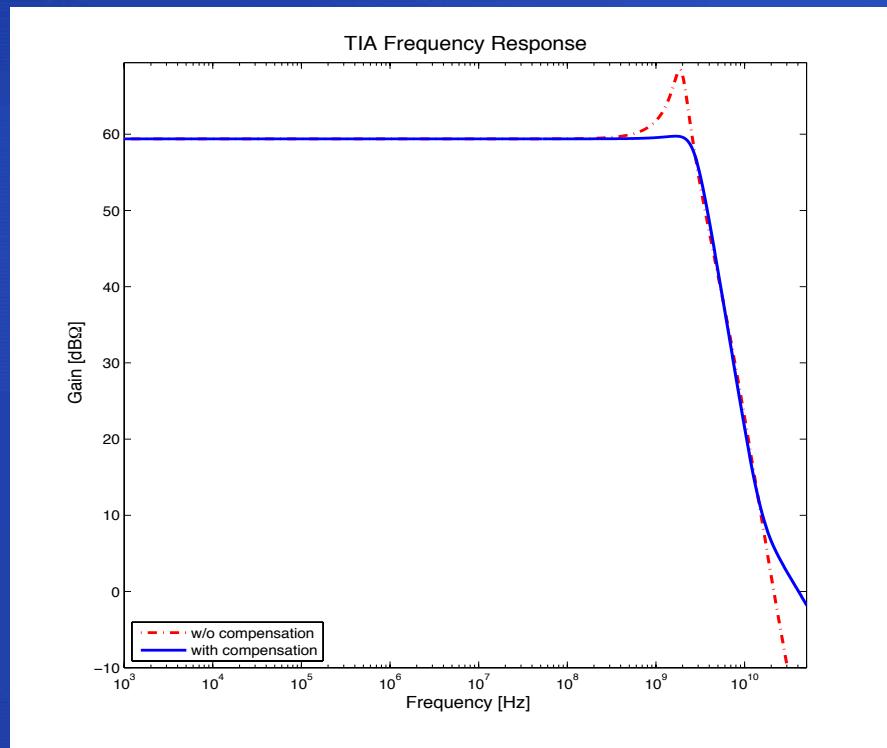


Figure of Merit	TIA Performances		
	Analysis	Simulation	% Relative Error
Gain [$\text{dB}\Omega$]	60	59.75	0.4
f _{3db} [GHz]	3.25	2.9	12.1
Input ref. noise [$\text{pA}/\sqrt{\text{Hz}}$]	13.9	13.14	5.8
Power dissipated [mW]	24.5	25.4	3.5

Comparisons

$$FOM = \frac{Gain * BW * C_{in}}{P_{DISS}}$$

Spec.	[1]	[2]	[3]	[4]	This Work
Gain [dBΩ]	58	76	66.02	94.96	59.75
BW [GHz]	0.95	2.5	22	0.0018	2.9
<u>C_{in}</u> [pF]	0.5	0.5	0.5	2	2
Input Ref. Noise [pA/ $\sqrt{\text{Hz}}$]	6.3	10	22	0.065	13.14
P _{DISS} [mW]	85	7.2	75	0.436	25.4
FOM [Ω*GHz*pF/mW]	4.44	1095	293.31	231.19	221.87
Process [μm]	0.6	0.18	0.09	0.18	0.18
Supply Voltage [V]	5	1.8	1.2	1.8	1.8