A 60dBΩ 2.9 GHz 0.18 μm CMOS Transimpedance Amplifier for a Fiber Optic Receiver Application

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***Abstract*—This paper presents the design and characterization of a high gain, high-speed differential transimpedance amplifier (TIA) to be used as the front-end interface for optical receiver applications. The TIA is realized in a standard 0.18-μm digital CMOS technology and it dissipates 25.4mW from a single 1.8 V supply. The objective of the design is to maximize the bandwidth. The main contribution of this work is the optimization procedure. The topology consists of a common gate input stage followed by a cascoded common source and a common drain stage surrounded by a global shunt-shunt feedback with phantom zero compensation to boost bandwidth and enhance stability. Using this approach the amplifier achieves transimpedance gain of 59.75 dbΩ, −3dB bandwidth of 2.9 GHz when connected to a 2-pF photodiode at the input and a 250 Ω load at the output, and 13.14 pA/√Hz input referred noise.**

Keywords—Broadband amplifier; CMOS; optical receiver; transimpedance amplifier.

I. INTRODUCTION

Front-end preamplifiers are a critical component in optical receivers: they affect overall system performance in terms of speed, signal-to-noise ratio, and sensitivity. Their design requires the careful optimization of a number of conflicting performance metrics including gain, bandwidth, noise and power consumption. In the past, due to the inherent high-speed and low noise characteristics of certain materials, these amplifiers were mainly designed using complex and costly technologies such as GaAs and InP. Recent advances in nanoscale CMOS technology, have made it possible to design CMOS preamplifiers that achieve performances comparable to the ones attainable with GaAs and InP technologies, but at a fraction of the cost [1].

It is well known that the input parasitic components, especially the photodiode capacitance is the main limitation affecting the preamplifier bandwidth and noise performance. Therefore, the main challenge for circuit designers is to develop topologies that make it possible to relax the input parasitic effects. Several circuit techniques have been proposed in the literature, including capacitive peaking, inductive peaking, common gate (CG) input configuration and common drain (CD) configuration [1][2][3][4]. In this paper we choose to implement the TIA using a cascade of three stages. To relax the effect of the large input capacitance contributed by the photodiode the first stage is a common-gate. The second stage is a common source (CS), and the third stage is a common drain. This toplogy is able to provide high gain (through the combination of the CG and the CS stages), the ability to drive small resistive loads (thanks to the low output impedance of the CD), and it presents a low input impedance (via the CG). Unfortunately, although in principle the choosen topology provides the right characteristics (that is, high gain, low input resistance and low output impedance) the relatively small gm achievable with a 180nm CMOS technology is not sufficient to lower the input resistance to the level required to achieve the bandwidth necessary for optical receiver applications. To extend the bandwith we added a global shunt-shunt feedback around the amplifier. As expected the feedback caused some peaking in the frequecny response of the amplifier. The peaking was compensated through the addition of a phanthom zero.

The rest of the paper is organized as follows. Section II introduces and motivates the topology selected for the design of the TIA. Section III describes the equations and approximations used to predict and optimize the performance metrics of the TIA. Section IV discusses simulation results and compares them with theoretical expectations. Finally, Section V summarizes the results of our work and provides conclusions.

II. CIRCUIT DESCRIPTION

A. Basic Topology Selection

We decided to implement the forward amplifier using a cascade of three stages: a common-gate at the input, a common source in the middle, and a common-drain at the output. The selection of the common-gate as input stage is based on the need to relax the time constant τ_{in} associated with the large input capacitance of the photodiode. The CG provides low input impedance, so it is an ideal choice to limit τ_{in}. Beside relaxing the effect of the photodiode's capacitance the main function of the CG it to convert the input current generated by the photodiode into a voltage signal, so having a CS stage following the CG has the benefit to further increase the gain. The CD at the output stage acts as a voltage buffer between the CS and the low output load R_L the amplifier has to drive. After selecting the topology of the forward amplifier we opted to implement it in differential form. This choice is motivated by two main advantages: 1) signal-to-noise ratio (SNR) is improved as the signal is effectively doubled and 2) biasing of the CS stage is simplified because the CS stage can be

implemented as a differential pair with a single tail bias current. Finally, we decided to maximize the bandwidth of the the TIA implementing a global shunt-shunt feedback around its forward amplifier. Shunt-shunt feedback (voltage-sensing/current-mixing) provides low closed loop input impedance and low closed loop output impedance, which are the essential characteristics of a transimpedance amplifier. In addition the use of shunt-shunt global feedback improves bandwidth, desensitizes the midband closed loop transimpedance gain from PVT variations, and it makes possible to use feedback-zero compensation (a.k.a. phantom zero compensation) to improve the stability of the closed loop amplifier. Fig.1 summarizes the basic topology used to design the TIA. The photodiode is equivalent to a signal source i_{in} and parasitic capacitances C_p.

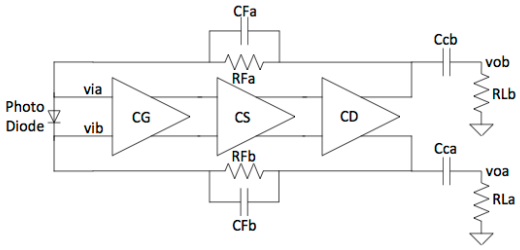

Fig. 1. Transimpedance amplifier topology

B. *Topology Enhancements*

The main bottleneck of the basic topology is the poor frequency response of the CS stage. This is due to the large time constant τ_2 at the input of the CS stage. The time constant τ_2 is determined by the relatively large load of the CG stage and the miller capacitance between gate and drain of the CS transistor. In order to reduce the effect of τ_2 we "cascoded" the CS stage. Cascoding provides two main advantages: 1) it reduces the miller multplication of the gate-to-drain capacitance and 2) it increases the intrinsinc gain of the stage. The trade off is a lower headroom voltage. Fortunatelly, the amplifier's specification does not require high voltage swing, so the gain and bandwidth benefits outweight the lost of headroom. A potential drawback of cascoding in the creation of an additional pole between the CS transistor and the cascode transistor. However, if the cascode stage is designed with care this pole is usually "isolated" by the other poles and it can be made occur at very high frequency so it doesn't affect bandwidth and stability.

A second enhancement concerns the sizing of the bias transistors. We used a channel length of 0.36μm for all biasing transistors. As long as using a longer channel length does not imply a width that would excessively increase capacitance this choice has two advantages: 1) higher output resistance ro (i.e., it reduces the loading caused by the bias transistors on the signal path transistors) and 2) lower sensitivity to PVT variations (i.e., it is a more robust biasing scheme). The trade off of using transistors with longer channel length is a higher $V_{DS,sat}$ and therefore reduced voltage headroom.

III. CIRCUIT ANALYSIS AND OPTIMIZATION

Fig. 2 shows the complete schematic of the amplifier. Fig. 3 shows the equivalent AC half-circuit of the forward amplifier with feedback loading and it is annotated with all capacitances affecting frequency response. The analysis and optimization of the amplifier is performed using a g_m/I_D lookup table based approach [5][6]. The look up tables are generated by characterizing the given technology through HSPICE. In nano-scale technologies, it is impossible to capture the physical behavior of the devices using closed form equations. The use of look-up tables provides a more accurate and practical choice. The ratio between g_m and I_D is a measure of the efficiency to translate currrent (i.e., power) into transconductance (i.e. gain). Using g_m/I_D as main figure of merit provides a unified design method for all regions of operation of the MOS transistor. In this way it is possible to take advantage of the moderate inversion region and optimize the speed-power trade off. The g_m/I_D look up table based approach allows accurate sizing of all transistors with a unified strategy from strong to weak inversion region. Both the lookup tables and the optimization process are organized in the form of MATLAB scripts.

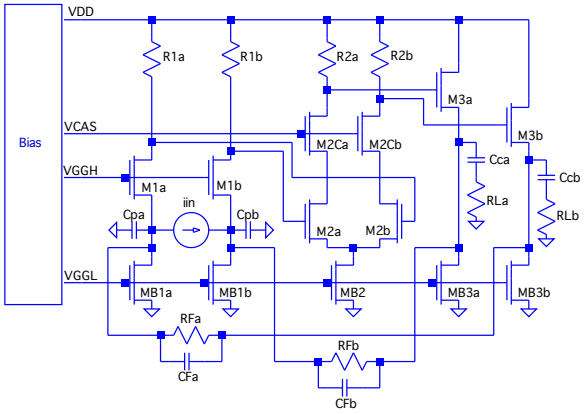

Fig. 2. Transimpedance amplifier schematic

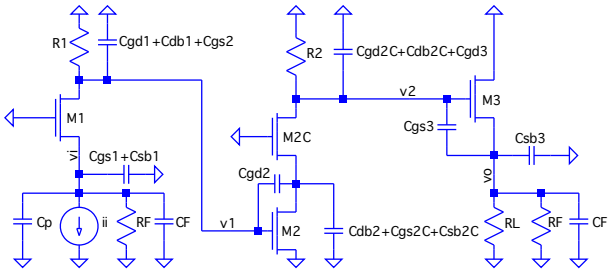

Fig. 3. AC half-circuit with feedback loading and relevant capacitances

The equations used to analyze the performances of the TIA are derived from the half circuit shown in Fig. 3. The transimpedance gain of the half circuit is:

$$a_0 = \frac{v_O}{i_i} \approx -\frac{g_{m1}^* R_F}{1 + g_{m1}^* R_F} R_1 \cdot g_{m2} R_2 \cdot \frac{g_{m3} R_{Lp}}{1 + g_{m3} R_{Lp}} \qquad (1)$$

where $g_{m1}^{*}= g_{m1}+g_{m1b}$ and $R_{Lp}=R_L||R_F||(1/g_{m3b})$. The overall closed loop transresistance gain is:

$$A_0 = v_o/i_{in} \approx \frac{2a0}{1+T0} \quad (2)$$

where $i_{in}=i_i/2$, $T_0=a_0f_0$ and $f_0=-1/R_F$. The time constant at the input of the CG is:

$$\tau_{in} \approx C_{in}\left(R_F||\frac{1}{g_{m1}^{*}}\right) \quad (3)$$

with $C_{in} = C_P + C_F + C_{gs1} + C_{sb1}$. The time constant at the output of the CG is:

$$\tau_2 \approx R_1C_2 \quad (4)$$

with $C_2 = C_{gd1}+C_{db1}+C_{gs2}+C_{gd2}(1+g_{m2}/g_{m2C}^{*})$. The time constant at the node between the CS transistor and the cascode transistor is:

$$\tau_{2C} = C_{2C}/g_{m2C}^{*} \quad (5)$$

with $C_{2C} = C_{db2}+C_{gs2C}+C_{sb2C}$. The time constants at the output of the CS stage are:

$$\tau_{3in} \approx R_2C_{3in} \; and \; \tau_{3m} \approx C_{gs3}\frac{R_2+R_{Lp}}{g_{m3}R_{Lp}+1} \quad (6)$$

with $C_{3in}=C_{db2C}+C_{gd2C}+C_{gd3}$. The time constant at the output of the CD stage is:

$$\tau_{3out} \approx R_{Lp}(C_F + C_{sb3}) \quad (7)$$

The –3dB bandwidth of the TIA is estimated using the ZVTC method:

$$f_{-3dB} \approx \frac{1+T_0}{2\pi(\tau_{in}+\tau_2+\tau_{2C}+\tau_{3in}+\tau_{3m}+\tau_{3out})} \quad (8)$$

The input referred current noise power spectral density (PSD) is due to three primary sources: 1) the input referred current noise PSD due to R_F, 2) the input referred current noise PSD due to M_{B1} and 3) the input referred current noise PSD due to R_1.

$$\frac{\overline{i_{in}^2}}{\Delta f} = \frac{1}{2}\left(\frac{4KT}{R_F} + 4KT\gamma g_m + \frac{4KT}{R_1}\frac{R_1^2}{A_{CG}^2}\right) \quad (9)$$

Given the TIA specifications (0.18µm CMOS technology, closed loop transimpedance gain of 60 dBΩ, 2 pF photodiode, 250 Ω load, total current budget up to 16mA, and input referred noise current PSD ≤ 140×10^{-24} A^2/Hz) the objective of the design was to maximize bandwidth. The optimization flow can be described as follows.

S1. Set the same initial bias current for each stage of the amplifier

S2. Set the loop gain T_0 to an appropriate value ($T_0 \geq 10$) and derive R_F ($a_0 = A_0(1+T_0)/2$; $f_0 = T_0/a_0$; $R_F = 1/f_0$).

S3. Determine g_m/I_D for the transistor M_3 (CD stage) based on the voltage bias allowing the max output signal swing and compute the corresponding transient frequency f_{T3}. Select an appropriate value of bias current $g_{m3}=I_{D3}*g_{m3}/I_{D3}$ based on $C_{gg3}=g_{m3}/(2\pi f_{T3})$ such that the time constants associated with the CD stage are not dominant. Estimate the parasitic capacitances and compute the resulting A_{CD}.

S4. Set the remaining bias current to be equally split between CS and CG stage and compute the amount of combined gain needed to meet specifications: $A_{CG}A_{CS} = a_0/A_{CD}$

S5. Partition the required gain between CS and CG. An excessive value of A_{CS} causes a strong miller effect at the intermediate node between the transistors M_2 and M_{2C} and results in a non optimal value of the dominant time constant τ_2. Similarly an excessive value of A_{CG} implies an excessive value of R_1 and results in a suboptimal value of the dominant time constant τ_2. Appropriate values of A_{CS} and A_{CG} are in the following ranges: $1\leq A_{CS}\leq 20$ and $a_0/A_{CD}/A_{CS\_max} \leq A_{GC} \leq a_0/A_{CD}$

S6. Set g_m/I_D for transistor M_1 and R_1 as the primary design variables. The values of g_{m1}/I_{D1} and R_1 set the value of A_{CG}. The value of A_{CG} set the value of A_{CS} and therefore the value of g_{m2}/I_{D2} and R_2.

S7. Sweep g_{m1}/I_{D1} from low inversion region (g_m/I_D=25 S/A) to high inversion region (g_m/I_D=5 S/A) and R_1 from A_{CG_min} to A_{CG_max}. Record the performance metrics of every feasible design in the explored space. Design feasibility and the current bias for the CG and CS are determined by the bias condition constrains.

S8. Determine the TIA design with the best bandwidth, and summarize its parameters: g_{m1}/I_{D1}, I_{D1}, R_1, A_{CG}, g_{m2}/I_{D2}, I_{D2}, R_2, A_{CS}, g_{m3}/I_{D3}, I_{D3}, and A_{CD}

S9. Determine transistor widths from g_m/I_D, the calculated I_D, and the current density (I_D/W) look-up tables.

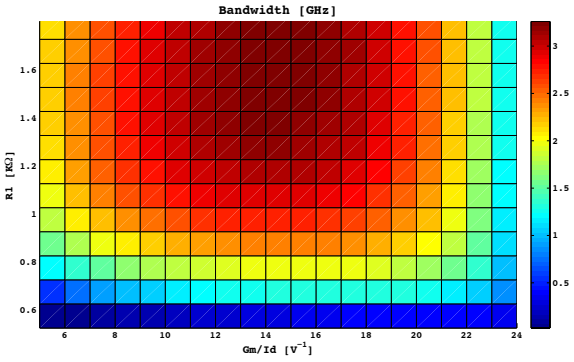

Fig. 4. TIA optimization plot: Bandwidth vs. g_{m1}/I_{D1} and R_1

IV. Results and Discussion

The proposed TIA has been implemented in a standard 0.18µm CMOS process. Fig. 4 illustrates the design space exploration process performed through the optimization flow. The experimental results obtained match very closely (within 12.1%) the analytical derivations. Table I summarizes and compares the results. Except for the width of bias transistors M_{B1}, no hand crafting of the transistor sizing is necessary to achieve the level of accuracy reported. The mismatch on the sizing of M_{B1} is due to the bias voltage mismatch at the terminals of the feedback resistor R_F. This causes a current leak through the feedback resistors R_F that has not be accounted for in the analytical derivations.

TABLE I. COMPARISON BETWEEN ANALYTICAL AND EXPERIMENTAL RESULTS

Figure of Merit	TIA Performances		
	Analysis	*Simulation*	*% Relative Error*
Gain [dBΩ]	60	59.75	0.4
f3db [GHz]	3.25	2.9	12.1
Input ref. noise [pA/√Hz]	13.9	13.14	5.8
Power dissipated [mW]	24.5	25.4	3.5

Table II summarizes the value of the devices of the TIA. Fig. 5 shows the frequency response of the TIA with and without compensation. The value of the compensation capacitance C_F is calculated using MATLAB root locus plot with the closed loop poles location detemined using HSPICE pole/zero analysis. The phase margin after compensation is about 86 degrees. Finally, Fig. 6 shows the input referred current spectral density.

TABLE II. TIA OPTIMIZED DEVICE SIZES

Device	TIA Device Sizing
CPa, CPb [pF]	2
RLa, RLb [Ω]	250
R1a, R1b [Ω]	1526
R2a, R2b [Ω]	409
RFa, RFb [Ω]	550
CFa, CFb [fF]	130
M1a, M1b [µm]	L=0.18; W=46.1
MB1a, MB1b [µm]	L=0.36; W=289
M2a, M2Ca, M2b, M2Cb [µm]	L=0.18; W=31.1
MB2 [µm]	L=0.36; W=994
M3a, M3b [µm]	L=0.18; W=31.5
MB3a, MB3b [µm]	L=0.36; W=174

V. CONCLUSION

This paper describes a CMOS differential transimpedance amplifier for fiber optic receiver applications. The TIA consists of a cascade of a common gate, a common source and a common drain surrounded by a shunt-shunt feedback with phantom zero compensation. It achieves a 59.75 dBΩ transimpedance gain, with a 2.9 GHz bandwidth and an input-referred current noise of 13.14 pA/√Hz. The amplifier is realized in a standard 0.18-µm digital CMOS technology and it dissipates 25.4mW from a single 1.8 V supply.

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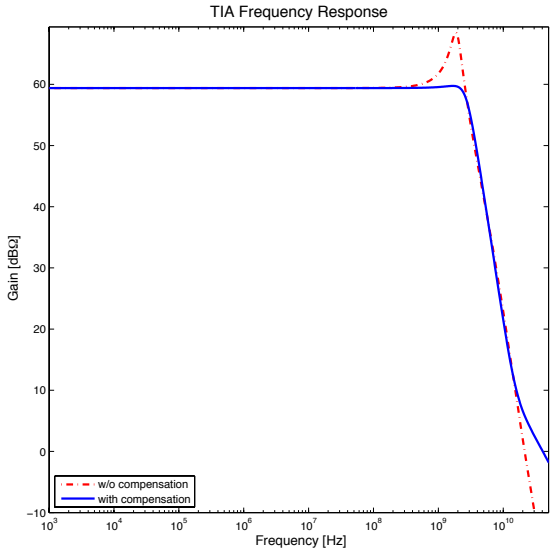

Fig. 5. TIA Frequency Response

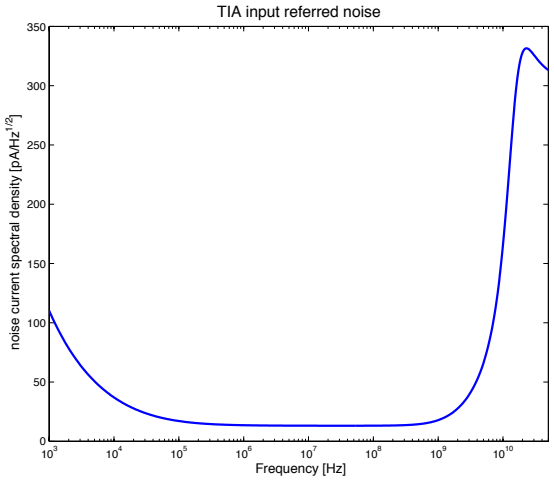

Fig. 6. TIA input referred current noise PSD