2016 EE214B Design Project - Part I

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1 Bias Calculations

Bias calculations go here.

2 Calculation of Key Design Parameters

Choice of L

- All devices used in current source have a minimum length of 2μm.
- All other devices in the amplifier have minimum length of 1μm. Minimum length is used as f_t is inversely proportional to L.
- All devices in bias generator circuit have length >=2μm.

Bias Generator circuit

- Constant gm reference based design is used as bias circuit to reduce mismatch errors.
- Transconductance of bias device (mn300) depends only on R2 and m (m is the ratio of MN300/MN400). Therefore gm can be set precisely.
- Start-up circuit is used to force the circuit to the desired operating point.

Approximations for hand calculations

For simpler hand calculations, following approximations are used.

1. $Cdb = Csb = 0.35Cgs$
2. $Cgs = (\frac{2}{3})WLCox + Cov'W$
3. $Cgd = Cov'W$
4. $gmb = 0.2gm$

Stage4

- As per the spec, common mode output voltage (vout) has to be within -0.15v to 0.15v. Since the body is connected to vss, MN10 experiences back gate effect and the threshold voltage is given by:

$$\begin{aligned} Vt = Vt_0 + \gamma(\sqrt{2\phi f + V_{sb}} - \sqrt{2}\phi f \\ Vt_0 = 0.5V, \gamma = 0.6, 2\phi f = 0.8 \end{aligned} \tag{1}$$

- Stage 4 is a source follower which has a gain given by

$$A4 = \frac{gm_{10}}{gm_{10} + gmb_{10} + (\frac{1}{R_L})} \tag{2}$$

- Gain of stage4 (A4) <1 due to back gate effect and the output load.
- To achieve gain closer to 1 (0.6 - 0.7), it is important to size and bias MN10 such that $(gm_{10} + gmb_{10}) >> (1/R_L)$.
- Transconductance of and drain current of MN_{10} is given by

$$gm_{10} = \mu nCox(\frac{W}{L})vov_{10} \tag{3}$$

$$Id_{10} = 0.5\mu nCox(\frac{W_{10}}{L_{10}})vov_{10}^2(1 + \lambda(Vdd - Vout)) \tag{4}$$

- MN_9 (bias device for source follower) is sized such that $Id_{10} + I_{R_L} = Id_9$ and the common mode output voltage does not fall out of range. This device is chosen to be of smaller size to reduce loading on Vout node.

$$\tau_{OUTPUT} = (R_L || \frac{1}{1.2gm_{10}})(C_L + Csb_{10} + Cgd_9 + Cdb_9) \tag{5}$$

- Cgs10 is assumed to be very small due to boot-strapping.

Stage 3

- Loading at node Vy increases with the increase in gain of stage 3 due to the miller effect. Hence gain of stage3 is kept low and is fixed at sqrt(2) to compensate for the gain lost in stage 4. Gain of stage3 (CS amplifier with diode connected load):

$$|A3| = \frac{gm7}{gm8} = \frac{Vov8}{Vov7} = \frac{Vdd - Vz - abs(Vtp)}{Vy - Vss - Vtn} = \sqrt{2} \tag{6}$$

- Choice of Vz from above (stage4) determines Vy.
- Minimum device sizes (W=2μm, L=1μm) are used for both MN7 and MP8 to reduce loading on Vy and Vz.

$$Id_7 = Id_8 = 0.5\mu nCox(\frac{W_7}{L_7})vov_7^2(1 + \lambda(Vz - Vss)) \tag{7}$$

$$\tau_Z = (\frac{1}{gm_8})(Cgs_8 + Cdb_8 + Cgd_{10} + Cgd_7(1 + \frac{1}{|A3|}) + Cdb_7) \tag{8}$$

Stage 2

- Vy from stage Z above determines the required ratio of R3 and R4.

$$(\frac{R4}{R3}) = \frac{Vss}{Vy} - 1 \tag{9}$$

- Gain of stage Y (Cascode amplifier) is set to 3.

$$|A2| = gm4(R3||R4) \tag{10}$$

- Vov_4 and W_4 are optimized to reduce τ_X.
- MN6 is sized such that current through MN6 is same as the current through MP4 and MP5.

$$Id4 = Id5 = Id6 = 0.5\mu pCox(\frac{W4}{L4})(Vdd - Vx - abs(Vtp))^2(1 + \lambda(Vdd - Vw) \tag{11}$$

- Current through R3 and R4

$$I_{R3} + I_{R4} = Vss/(R3 + R4) \tag{12}$$

$$\tau_Y = (R3||R4)(Cgs_7 + Cgd_7(1 + |A3|) + Cgd_6 + Cdb_6 + Cgd_5 + Cdb_5) \tag{13}$$

Stage 1

- Vov_4 from stage 2 sets V_X which in turn sets the ratio of R1 and R2.

$$Vov_4 = Vdd - Vx - |Vtp| \tag{14}$$

$$(\frac{R1}{R2}) = \frac{Vdd}{Vx} - 1 \tag{15}$$

- Gain of stage 1 (Common gate amplifier) is set to 10000.

$$|A1| = (R1||R2) \tag{16}$$

- MN1 and MP3 are sized such that Id1 = Id3.
- MN2 is sized to reduce τ_{IIN} node. τ_{IIN} is inversely proportional to gm_2.

$$\tau_{IIN} = (\frac{1}{gm2})(Cin + Cgd_1 + Cdb_1 + Cgs_2 + Csb_2) \tag{17}$$

$$\tau_X = (R1||R2)(Cgd_2 + Cdb_2 + Cgd_3 + Cdb_3 + Cgs_4 + Cgd_4) \tag{18}$$

- Current through MN1, MN2 and MP3

$$Id_{1,2,3} = 0.5\mu pCox(\frac{W_3}{L_3})(Vdd - VbiasP - |Vtp|)^2(1 + \lambda(Vdd - Vx)) \tag{19}$$

- Current through R1 and R2

$$I_{R1} + I_{R2} = Vdd/(R1 + R2) \tag{20}$$

Vovn, Vovp

- Vovn and Vovp are chosen to achieve a reasonable balance between gain, Tau total and Power, and our choice was educated by the gm/Id technology plots.

Total Design Performance

$$|A_{TOTAL}| = A1 * A2 * A3 * A4 \tag{21}$$

$$\tau_{TOTAL} = \tau_{IIN} + \tau_X + \tau_Y + \tau_Z + \tau_{OUTPUT} \tag{22}$$

$$Power = (Vdd - Vss)(Id_1 + Id_4 + Id_7 + Id_{10}) + (\frac{Vdd^2}{R1 + R2}) + (\frac{Vss^2}{R3 + R4}) \tag{23}$$

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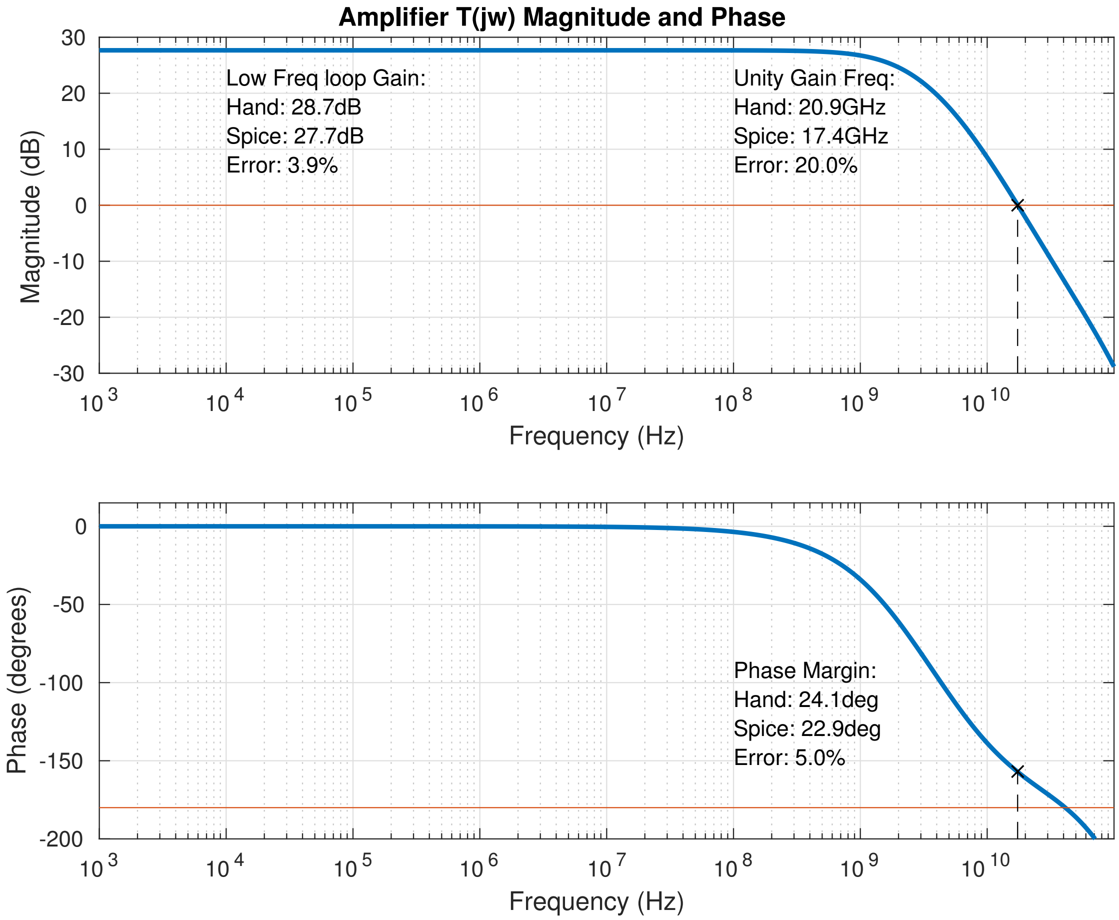
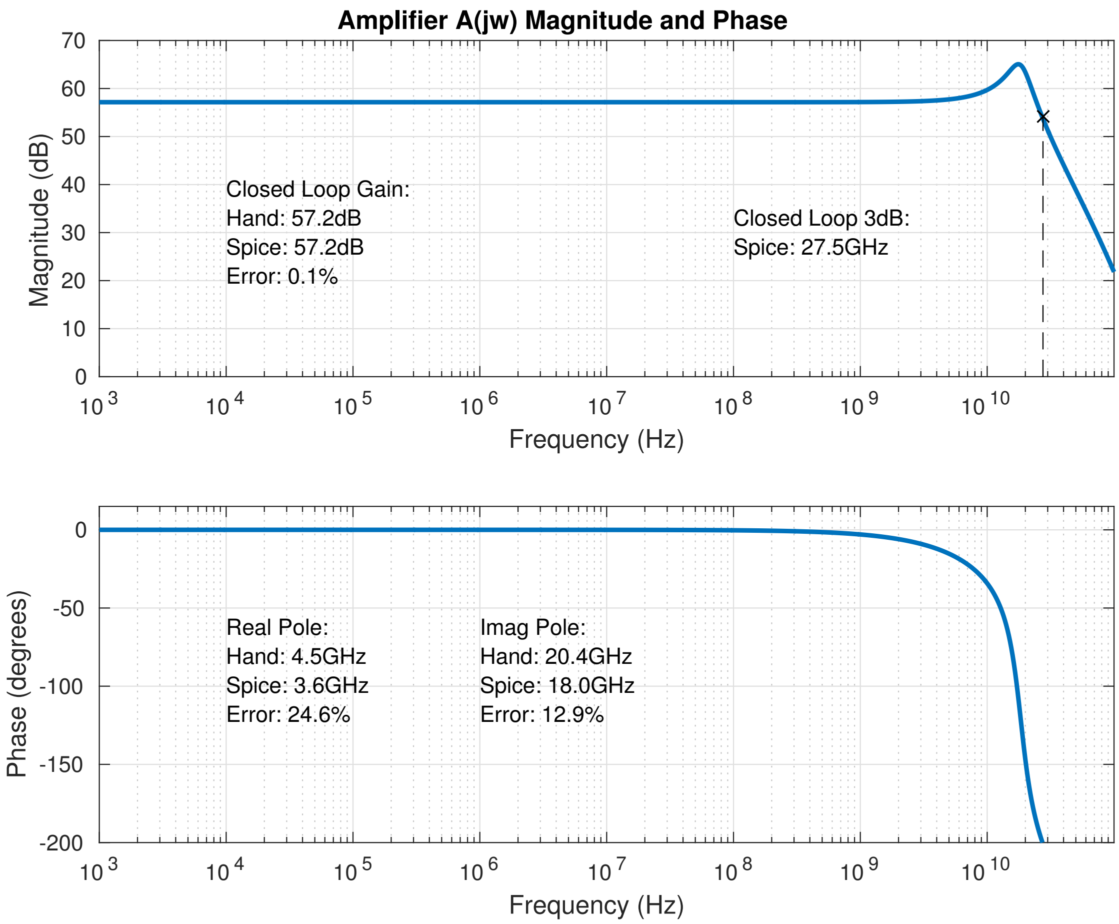
3 Bode Plots and PZ Outputs - Part I(g,h)



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***************************************************
   ******   pole/zero analysis
   input =   0:is           output = v(vo)
   poles (rad/sec)                  poles ( hertz)
   real             imag            real             imag
   -33.1562m        0.              -5.27698m        0.
   -22.9305g        113.319g        -3.64950g        18.0353g
   -22.9305g        -113.319g       -3.64950g        -18.0353g
   -473.782g        0.              -75.4048g        0.
   -1.12800t        0.              -179.526g        0.
   -1.18039t        0.              -187.865g        0.

   zeros (rad/sec)                  zeros ( hertz)
   real             imag            real             imag
   0.               0.              0.               0.
   -1.10418t        0.              -175.736g        0.
```

4 Calculations for Part I(i)

A feedback capacitor can be used to introduce a zero into the feedback loop in order to push the higher frequency pole out and flatten the response of the closed loop amplifier. The optimally flat response of the amplifier occurs when Q = $\sqrt{2}$. Hence:

$$\omega_0 = 1.09e11 rad/s \tag{24}$$

$$\omega_Z = \frac{\omega_0}{\sqrt{2} - \frac{\omega_{P1}+\omega_{P2}}{\omega_0}} \tag{25}$$

$$C_F = \frac{1}{\omega_Z R_F} = 57fF \tag{26}$$

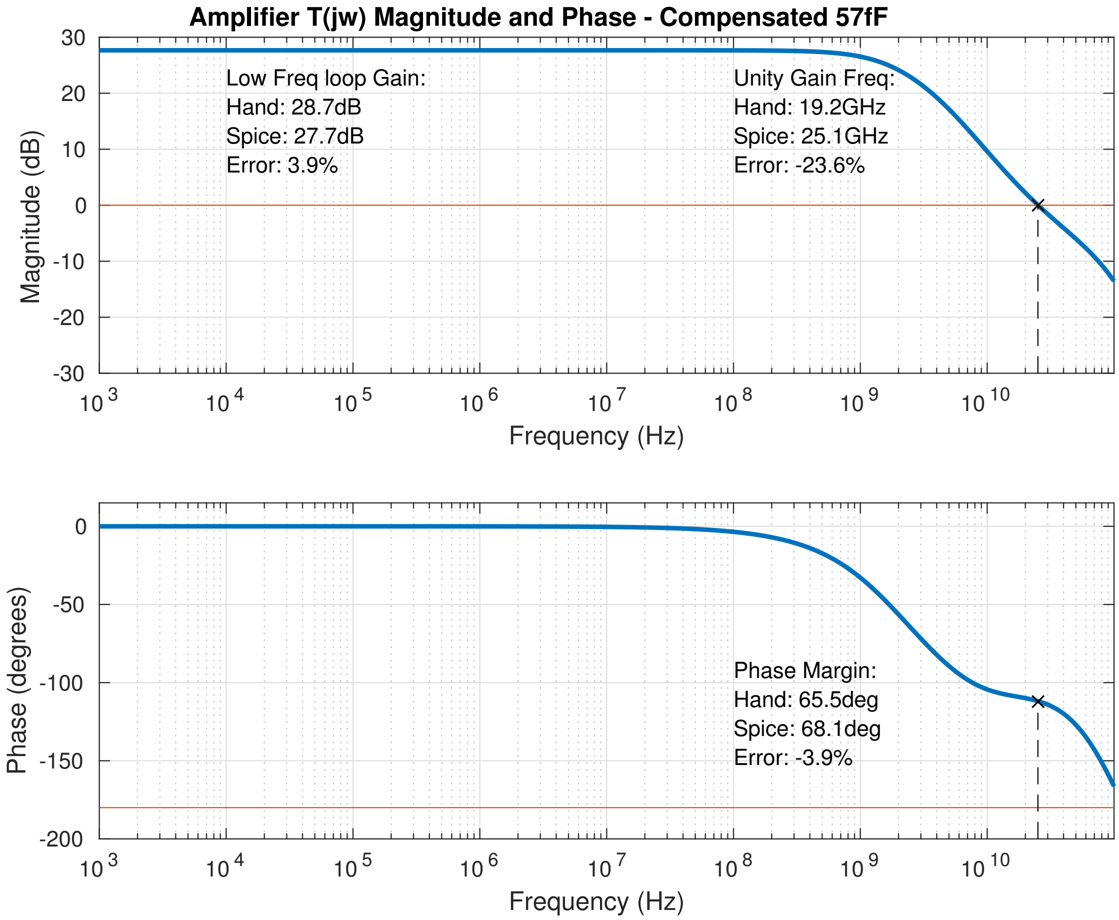
From this, the new closed loop bandwidth can be calculated as such:

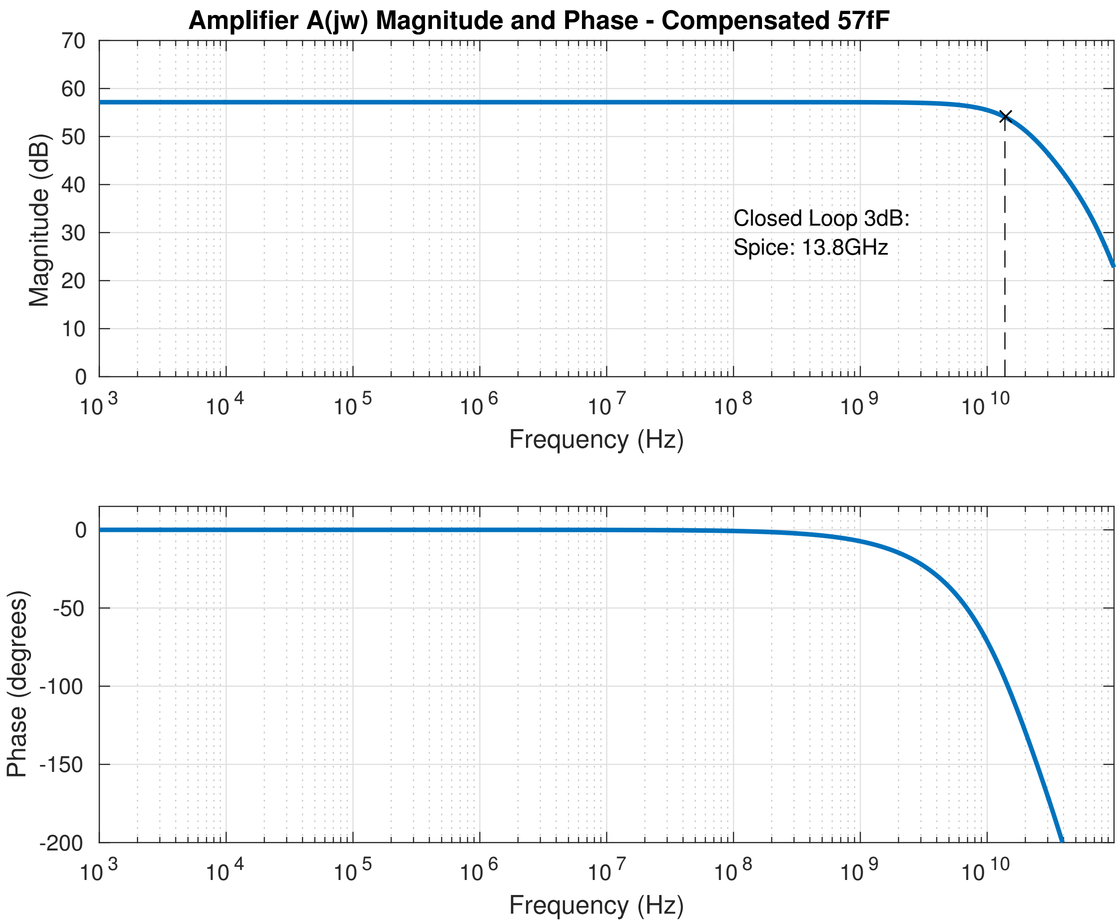
$$C_{in,C_F} = C_{in} + C_F \tag{27}$$

$$k = \frac{R_{in} * Q1_{gm} * R_x * A_{V3}}{R_F} \tag{28}$$

$$BW_{CL,C_F} = \frac{\sqrt{1+k}}{2\pi R_{in} C_{in} R_x C_x} = 19.2Ghz \tag{29}$$

5 Bode Plots and PZ Outputs - Part I(j)






```
*****************************************************
   ******    pole/zero analysis


   input =   0:is          output = v(vo)

   poles (rad/sec)                  poles ( hertz)
   real              imag           real              imag
   -33.1562m         0.             -5.27698m         0.
   -102.336g         -49.5561g      -16.2872g         -7.88710g
   -102.336g         49.5561g       -16.2872g         7.88710g
   -321.575g         358.533g       -51.1803g         57.0622g
   -321.575g         -358.533g      -51.1803g         -57.0622g
   -1.11894t         0.             -178.085g         0.
   -1.35128t         0.             -215.063g         0.
   -1.88412t         0.             -299.868g         0.

   zeros (rad/sec)                  zeros ( hertz)
   real              imag           real              imag
   0.                0.             0.                0.
   -1.09418t         0.             -174.144g         0.
```

Bias Generator	Hand calc	Spice	%Error	Reason for error
V_{BiasN}	-1.300V	-1.279V	-1.6%	Startup circuit bias
V_{BiasP}	1.300V	1.319V	1.5%	Startup circuit bias
Stage1	Hand calc	Spice	%Error	Reason for error
Id_1	18.3μA	20.9μA	14.2%	Bias generator error
Vx	1.300V	1.275V	-1.9%	
A_X	10kΩ	9.86kΩ	-1.4%	Finite MN_1 and MP_3 output resistance
gm_2	210μS	268μS	27.6%	Bias generator error
τ_{IN}	1.11ns			
τ_X	420ps			
Stage2	Hand calc	Spice	%Error	Reason for error
Id_4	36.75μA	43.5μA	18.4%	
V_W	1.496V	1.450V	-3.2%	
V_Y	-1.550V	-1.418V	-8.5%	Imbalance between MP_4 and MN_6 current
gm_4	105μS	120μS	14.3%	Error in V_Y
A_Y	-3.0	-3.25	8.3%	Error estimating gm_4
τ_Y	306ps			
Stage3	Hand calc	Spice	%Error	Reason for error
Id_7	10.25μA	22.9μA	123%	Error in V_Y plus finite output resistance
V_Z	1.364	1.102V	-19.2%	Error in V_Y
gm_7	45μS	79μS	75.5%	Error in Id_7
gm_8	31.2μS	51μS	63.5%	Error in Id_7
A_Z	1.414	1.440	1.8%	The benefit of ratiometric design
τ_Z	1.92ns			Error in estimating gm_8
Stage4	Hand calc	Spice	%Error	Reason for error
Id_{10}	2.96μA	30.43μA	928%	MN_{10}'s large width is a big error amplifier
V_{OUT}	0.299	-0.117V	-139%	
Vt_{10}	0.999	1.034V	3.5%	
gm_{10}	91.1μS	327μS	258%	
gmb_{10}	13.0μS	55.1μS	323%	
A_{OUT}	0.71	0.75	5.6%	
τ_{OUT}	1.63ns			Error in estimating gm_{10}
Total Power	578μW	1.065mW	84%	Not accounting for bias gen
Total Gain	30.04kΩ	34.66kΩ	15.5%	Error in estimating gm