DESIGN PROJECT

Part I due on Monday, February 29, 2016, 5pm

Part II due on Wednesday, March 9, 2016, noon

Overview

In this project, you will work on the design of the wideband transimpedance amplifier shown in Figure 1. A more elaborate version of this circuit is described in the following publication:

C. Knochenhauer et al., "40 Gbit/s transimpedance amplifier with high linearity range in 0.13 μm SiGe BiCMOS," Electronics Letters, vol. 47, no. 10, pp. 605-606, May 12, 2011.
URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5767249&isnumber=5767225

Your project work will consist of two parts:

I. Analysis and simulation of a SiGe BJT baseline design (in Figure 1)
II. Analysis and implementation of an alternative design in CMOS

You may work alone or in teams of two. Each team must submit one project report as specified below. You are encouraged to discuss the design problem with other teams, but your design must be unique. Under no circumstances should you exchange computer files with other teams; this would constitute a gross violation of the honor code.

For simplicity in this short project, you are not required to verify your designs across process, voltage and temperature variations. In practice, this would be the next step after getting your "nominal" designs to work.

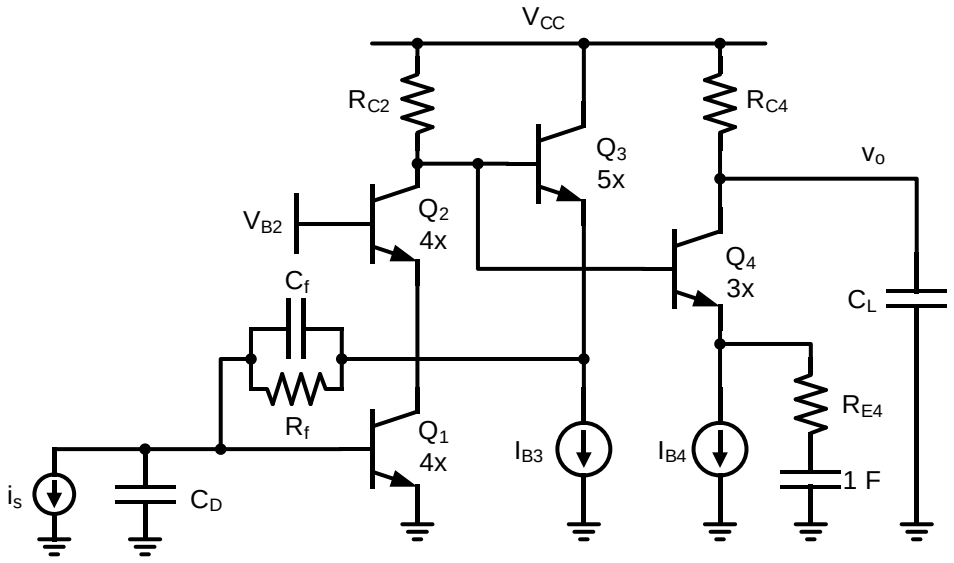

Figure 1. Baseline design.

Note: Each transistor consists of multiple unit elements. E.g., 4x refers to 4 devices in parallel.

Part I: Baseline design

As a first part of this project, you will analyze and complete the circuit of Figure 1 assuming the following parameters:

Table 1

Parameter	Value
Technology	EE214 SiGe Bipolar
Operating temperature	25°C
V_{CC}	2.5 V
V_{B2}	1.6 V
I_{B3}	4.5 mA
I_{B4}	2 mA
R_f	220 Ω
R_{C2}	250 Ω
R_{C4}	100 Ω
R_{E4}	15 Ω
C_L	20 fF
C_f	To be computed
C_D	200 fF
Peak input amplitude	150 μA

Proceed with the analysis as indicated below. In each step, use appropriate engineering approximations to simplify your analysis. **For parts (a) – (h) assume $C_f = 0$**.

a) Estimate g_m and r_π of all transistors and the bias point voltages of all circuit nodes. Assume $V_{BE(on)} = 0.8V$.

b) Run a .op analysis in HSpice to check the calculations of (a).

c) Estimate, by hand, the mid-band (low-frequency) loop gain (T_0), and the mid-band transresistance of the overall amplifier. Neglect r_π where appropriate.

d) Hand-calculate the two most significant poles of the amplifier loop gain T(jω) using a two-port model of the circuit. Model the input capacitance of the second and third stage (Q_3, Q_4) using the Miller approximation. I.e., compute the input capacitance by applying the appropriate (and constant) Miller gain term to $C_{\pi 3}$, $C_{\pi 4}$, $C_{\mu 1}$ and $C_{\mu 4}$. Ignore the poles contributed at the emitters of Q_2 and Q_3. You may use the simulated component values from part (b). Neglect r_π where appropriate. Feel free to make assumptions to simply the answers.

e) Based on the calculated value of T_0 and the two dominant loop-gain poles estimated in part (d), sketch a bode plot of T(j□) and estimate the phase margin and unity gain frequency. Do you expect to see peaking in the amplifier's closed-loop frequency response?

f) Calculate the closed-loop transimpedance(v_{E3}/i_s, where v_{E3} is the emitter of Q3) and pole locations (real and imaginary parts in the s-plane) based on your result from (e), assuming a two-pole loop response. What are ω_0 and Q?

g) Use a .LSTB analysis in HSpice to plot the magnitude and phase of the loop gain. As discussed in class, insert a 0V voltage source (vx) to the right of R_f and C_f or at the base

of Q_1. Compute the percent errors in the hand-calculated low frequency loop gain, the loop's unity gain frequency and phase margin.

h) Use HSpice to plot the magnitude and phase of the closed-loop transresistance $A(j\omega) = v_o/i_s$ as a function of frequency. Also run a .pz analysis on the closed-loop circuit and compare the obtained poles with your calculations from part (e). In order for this analysis to work properly, set ".option ITLPZ=1000 FMAX=2E12". The .pz output may contain several poles and zeros that are identical (except for small numerical errors); these must be discarded when interpreting the result. Also, ignore low frequency poles and zeros due to the decoupling capacitance. Calculate the error in your closed-loop pole calculation from part (f).

i) The capacitor C_f can be used to introduce a feedback zero. Estimate the value of C_f that yields a maximally flat response. What is the expected closed-loop bandwidth of the circuit?

j) For the calculated value of C_f, use HSpice to plot the magnitude and phase for both the loop gain, $T(j\omega)$, and the closed-loop gain, $A(j\omega)$, as functions of frequency. Tweak C_f until the magnitude response is flat, if needed. What is the phase margin? What is the closed-loop bandwidth? Compute the error in your closed-loop bandwidth estimate from part (i).

k) Estimate, by hand, the mid-band (low-frequency) input referred current noise spectral density of the circuit. Express your answer in pA/rt-Hz.

l) Use a .noise simulation in HSpice to check your result from part (k) and compute the percent error in the hand calculation. What is the spectral density at the closed-loop 3-dB frequency of the circuit?

m) Run a transient analysis using a 1-GHz sinusoidal input with the maximum signal amplitude specified in Table 1. Verify that the output is a "clean" sinusoid without any clipping. This test is also needed to make sure that the circuit remains stable when a large signal is applied.

Part II: Alternative design in CMOS

In this part of the project, you will explore a transimpedance amplifier topology of your choice to accomplish similar specifications as in part I. To make this task more interesting, you are permitted to use only MOSFETs of the 0.18-μm EE214B CMOS technology (no BJTs). The input and output must be single-ended. The following constraints and parameters apply:

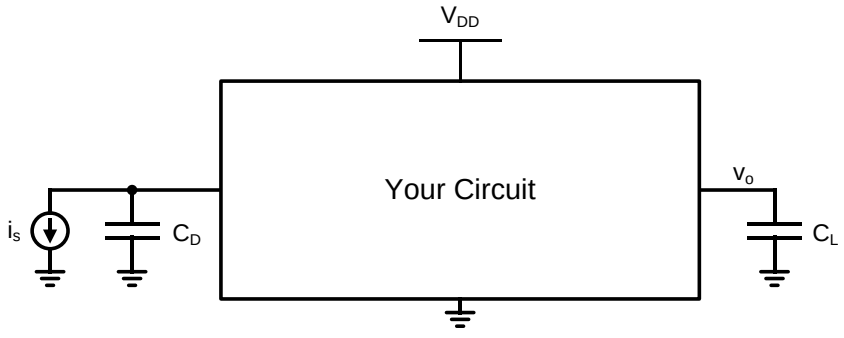

Figure 2. Alternative design.

Table 2

Parameter/Aspect	Value/Comment
Supply voltage, V_{DD}	1.8V
Closed-loop low frequency transimpedance gain $A_0 = v_o/i_s$	$\geq A_{0,partI}$ (from the simulation result announced after Part I is due)
C_L	$\geq$ 20 fF
Total supply current	$\leq I_{CC,partI}$ (To be announced)
Bandwidth, f_{3dB}	Maximize
Magnitude response	The overall response should ideally be maximally flat. No more than 1dB of peaking relative to the low-frequency closed-loop gain is allowed.
Input noise density at f_{3dB}	$\leq$ Noise density of part I circuit simulation (at f_{3dB}) (To be announced)
Ideal sources	Only one ideal supply voltage source (e.g. V_{DD}) and one ideal bias current source are allowed. All other voltages and currents must be derived from these sources (using current mirrors, etc.). One side of the current source must be connected to the supply or ground. Also, the current source must be placed outside the signal path. It would be nice to have a current source with zero parasitics in the signal path, but real life is just not that nice. Use reasonable ratios for current mirrors, less than 20:1. You are not going to impress us with huge ratios that help you save a few percent of power in exchange for a very impractical circuit.
Resistors	You can use ideal resistors in your design. We will grant 2% extra credit for anyone who includes realistic estimates for the parasitic capacitances associated with the resistors. Use the link below[1] to access typical process information. You may assume poly resistors with a capacitance of 100 aF/μm^2 to ground. Assume the resistor width is such that the current density is no larger than 1 mA/μm. Assume simple model that splits the capacitance 50/50 between the two terminals.
Inductors	Unavailable
Capacitors	Assume an ideal model for small capacitors such as C_f in Figure 1. If you use any capacitors >500 fF connected to signal path nodes, you must include a stray cap of 10% on one side, and 1% on the other. We will in general not be impressed by the creative exploitation of non-physical components.
Bypass capacitors	Two large ideal decoupling caps are available (for simplicity, assume 1 Farad). The caps can be used similar to the one used in Figure 1, i.e. one terminal must connect to ground or V_{DD}. You are not allowed to use these caps for AC coupling in the signal path. Your stages must be DC coupled.
Source-bulk Ties	D_{WELL} must be included manually for PMOS source bulk ties: Area = (W+2μm)·(L+3μm). The bulk of NMOS devices must be connected to ground; no source-bulk ties for NMOS.

[1] https://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/tsmc-018/t92y_mm_non_epi_thk_mtl-params.txt

The most basic idea you can follow in this part of the project is to maintain the same (or similar) circuit topology as in part I, and replace the BJTs with properly sized MOSFETS. The key questions to answer in this case are how much bandwidth you can extract under the given constraints, and how one would go about "optimally" sizing the MOSFETs. Another idea is to explore a different transimpedance amplifier topology, found e.g. through a literature survey. It is up to you decide how about how to split the overall gain among the various stages of your design.

What matters most in this part of the project is that you deliver a clear description and analysis of what you have done, and what you identified as the performance limiting issues in the chosen circuit. A well-executed project will provide a thorough hand analysis and/or Matlab optimization script that clearly show how you arrived at your final design. A circuit whose specs were optimized through pure "spice-monkeying" will not impress us much, as we must assume that you do not know how the circuit works.

Be sure to approach this project using a "divide and conquer" approach. For example, you can use ideal biasing circuits in the beginning while exploring different topologies. Once you have found a topology you like, you can replace the ideal components step by step while ensuring that the circuit still works. Proper biasing often appears to be a challenge for inexperienced designers. When your circuit does not work as expected, do not panic and carefully inspect the operating point output. In 90% of all cases, the problem is obvious from the bias point information alone (for example a typo in the netlist). There is no point in running AC simulations unless your bias point is as expected.

When designing current mirrors, be aware that they will not work as accurately as you may expect from your past experience with long channel models. In a mirror that uses short channels, an error of several tens of percent can easily occur due to V_{DS} differences. These errors may be just fine, depending on what you are trying to accomplish. It is OK to "tweak" width ratios somewhat to lower such errors, but keep in mind that you should not create a circuit that is overly sensitive and tries to "balance a marble on the tip of a cone." Again, we will not be impressed by such solutions that have no chance to work in reality.

Project Reports

Your team is required to prepare reports for each part using the format outlined below (hand-written (and scanned) reports are just fine). Submit your reports in the same manner you submitted your homework, promptly by the stated deadlines. We will not grant any extensions.

In case you decide to submit computer generated reports, make sure to use font sizes ≥ 10. Be sure to follow the format instructions below ***EXACTLY***. Part of the exercise in this project is to learn how to document your work in a clean and concise manner. We will deduct points for reports that exceed the allocated number of pages.

Part I report:

Pages(s)	**Content**
1	Cover page. Clearly indicate the names of the team members.
2	Bias point calculations for part I (a). Include a comparison with SPICE results from part (b) by providing a table that states the percentage deviations in the

	calculated voltages, g_m and r_π.
3-6	Calculations and plots for part I (c) through (f).
7-8	Bode plot and pz outputs for parts I (g) and (h). Be sure to include proper annotations, and comparisons to hand calculated values.
9	Calculations for part I (i).
10-11	Bode plots and pz outputs for part I (j). Be sure to include proper annotations, and comparisons to hand calculated values.
12	Calculations and simulation plot (with proper annotation) for parts I (k) and (l).
13	Plot for part I (m).

Part II report:

Pages(s)	**Content**
1	Cover page. Clearly indicate the names of the team members.
2	Performance summary table (See Table 2.) and the circuit schematic
3-11	Describe your design for part II. Your write-up for this part should contain some of the same basic elements that you have provided for part I. Specifically, include relevant bias point and ac calculations, as well as simulation outputs that document the bandwidth and noise performance of the circuit. As mentioned previously, it is very important to provide proper hand calculations that justify your final design point. End this portion of your report with a summary of your findings. Time permitting, and if you are interested, include a simulation of the circuit's THD (as explained later in this course).
Appendix	Include any information that does not fit onto pages 1-11. It is unlikely that we will read the appendix.

Project Report Submission

For part I, submit a hardcopy of your write-up in the same way you did this for all homework assignments. For part II, we will require:

1) A hard copy of your report, submitted to the homework collection box (or SCPD).
2) A soft copy of your report, submitted to the dropbox on the course website. (Coursework)
3) The final version of your circuit netlist, to be submitted to the dropbox on the course website. (Coursework)

Grading

Part I: 30%
Part II: 70%

Part II Grading Rubric

Aspect	**Percentage**	
Report	10%	• Are the diagrams and plots readable? • Have all the critical design choices and achieved specs been documented (examples: size of all components, bias currents, etc.)
Design flow	20%	• Did the team establish a logical design flow or mostly spice-moneyed the design toward the specs? • Is there a reasonably good match between hand analysis and simulation results? Are there any simulation results that seem to come "out of nowhere?"
Creativity	20%	• Did the team try out an interesting or new amplifier topology? • Are there any creative and potentially new ideas in the design flow/methodology?
Performance	20%	• Are all the specifications met? • How does this design rank in terms of bandwidth?