Front-end CMOS Chipset for 10 Gb/s Communication

Anders K. Petersen, Kürşad Kızıloğlu, Ty Yoon, Freddie Williams, Jr., Martin R. Sandor

Intel Corporation, Optical Components Division, Calabasas Design Center, 26610 Agoura Road, Calabasas, CA 91302, Tel: (818) 449 1535, Fax: (818) 449 1635, E-mail: kursad.kiziloglu@intel.com

Abstract **- A 10 Gb/s communication chipset is realized for the first time in 0.18 μm generic CMOS. It comprises (all fully differential):**

(i) a transimpedance amplifier: gain=1300 Ω, bandwidth = 9 GHz optical.

(ii) a limiting amplifier: t_{rise}, t_{fall} < 23 ps; sensitivity = 5 mV at BER = 10^{-12}.

(iii) a laser driver: adjustable I_{bias} (up to 40 mA) and I_{mod} (up to 35 mA), driving a laser module with Z_{in}=50 Ω.

I. INTRODUCTION

Advent of multimedia applications, which require data links with ever-increasing capacity, is necessitating high-speed optical communication systems. A variety of applications, including telecommunication (OC-192), data communication (10 Gb/s Ethernet) and Fibre Channel standards are demanding more transmission links at 10 Gb/s. An important consideration for applications to local and metropolitan area networks (LANs and MANs), however, is cost competitiveness. Although various solutions have been offered for these applications in SiGe [1], Si bipolar [2] and compound semiconductor technologies [3-4], the interest in using CMOS-based ICs for applications in optical communications has risen, particularly for LANs and MANs, where the use of low-cost and high-volume processes, such as CMOS, is desirable [5-11]. Figure 1 shows the system block diagram for an optoelectronic transceiver. In this manuscript, we report on the physical media dependent (PMD) layer chipset comprising the transimpedance amplifier (TIA), the limiting post-amplifier (LIA) and the laser driver amplifier (LDA). To the best of authors' knowledge, this report represents the first PMD layer chipset for 10 Gb/s communication, realized in standard digital 0.18 μm CMOS process. The following are some of the key design considerations that have enabled the successful implementation of highly analog front-end functions in a generic digital CMOS process:

(i) Choice of technology with sufficient performance margin: f_T > 45 GHz at the operating point for the transistors in the high-speed path.

(ii) Attention to detail in layout techniques: careful observation, minimization, and simulation of layout parasitics, particularly those in the high-speed path of the circuitry.

(iii) Fully differential implementation for best noise immunity, wideband operation and reduced sensitivity to external parasitics.

(iv) Careful modeling and creation of an active and passive component library.

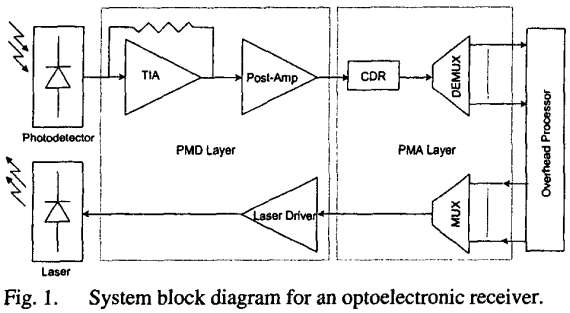

Fig. 1. System block diagram for an optoelectronic receiver.

II. TRANSIMPEDANCE AMPLIFIER

A. Design:

A critical part of an optical receiver is the TIA as its noise, gain and frequency performance largely determines the overall data rate and the sensitivity that can be achieved in an optical system. TIA designs present an additional challenge in that to be able to accommodate wideband data, the amplifier has to have a wideband frequency response, extending from dc to high

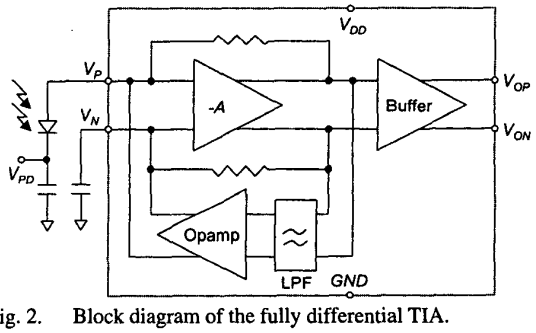

Fig. 2. Block diagram of the fully differential TIA.

0-7803-7246-8/02/$10.00 © 2002 IEEE

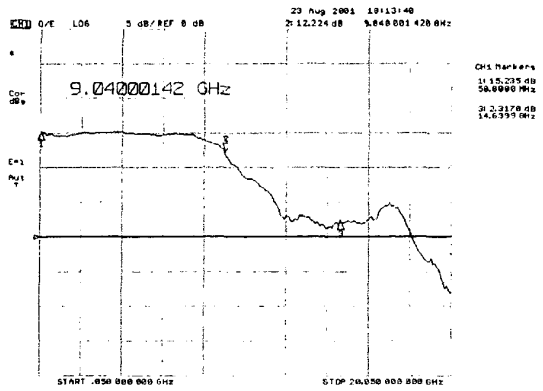

Fig. 3. Relative optoelectronic response of the photodetector and the TIA combination, indicating a 3-dB optical bandwidth in excess of 9 GHz.

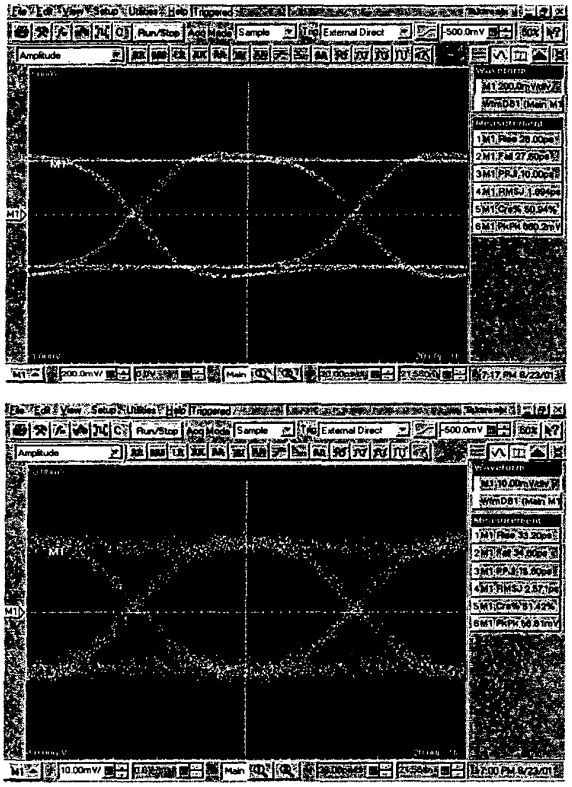

Fig. 4. 10 Gb/s optical eye diagrams of the TIA for 0 dBm (top) and -15 dBm (bottom) input optical power levels. The outputs were observed differentially. y-scale: 200 mV/div (top), 10 mV/div (bottom), x-scale: 20 ps/div.

frequencies, while maintaining minimum in-band ripple and phase distortion. We have implemented the TIA in a fully differential configuration for good noise immunity and wide-band operation [8] (Figure 2). A feedback loop comprising a high-gain opamp stage [9], which samples the TIA output and adjusts the input current drive, enables a wide optical input power range. An output buffer is designed with a 50 Ω output impedance for easy interfacing with subsequent amplification stages.

B. Measurements:

The TIAs were first measured on-wafer with an HP 8510B vector network analyzer (VNA) between 0.045 – 20 GHz. Differential microwave probes were utilized for signal input and output. Unused complementary ports were terminated in 50 Ω to preserve the balanced mode of operation. The TIA consumes 60 mA from a 1.8 V power supply. Its differential transimpedance, Z_T, into a 50 Ω load, which is calculated from its measured S-parameters, is 1300 Ω. The output of the TIA is well matched to 50 Ω ($|s22| < -10$ dB) in the entire measurement band. The performance of the operational amplifier feedback loop was also tested by feeding one of the inputs with a current source and by measuring the output offset. The TIA offset between the complementary outputs was maintained to less than 7 mV up to an input current drive of 3 mA. Next, a TIA and a high-speed photodetector were packaged together to characterize the TIA's optoelectronic (OE) response and eye diagrams. Unused input of the TIA was terminated in an on-chip capacitor for balanced loading of its input stage. An Agilent 8703B Lightwave Component Analyzer was utilized for measurements. A system OE bandwidth in excess of 9 GHz is obtained, which includes a photodetector with 150 fF capacitance (Figure 3). This bandwidth is sufficient for operation up to 12.5 Gb/s. Figure 4 demonstrates optical eye diagrams of the TIA at 10 Gb/s for two different input optical power levels.

II. LIMITING POST-AMPLIFIER

A. Design:

The output of the TIA in an optical receiver is generally small compared to the amplitude requirements for driving the succeeding clock and data recovery (CDR) and demultiplexer stages. The limiting post-amplifier (LIA), cascaded to the output of the TIA, performs the following functions: (i) provides additional voltage gain, (ii) cleans up the incoming signal, and (iii) presents a fixed output level independent of the input amplitude variations. The

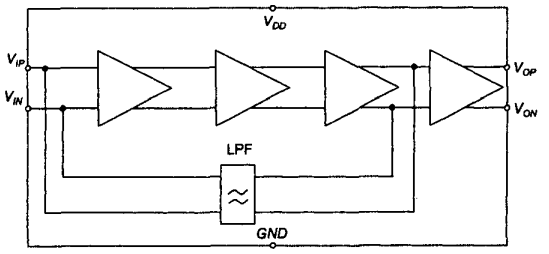

Fig. 5. Block diagram of the fully differential limiting post amplifier with offset cancellation.

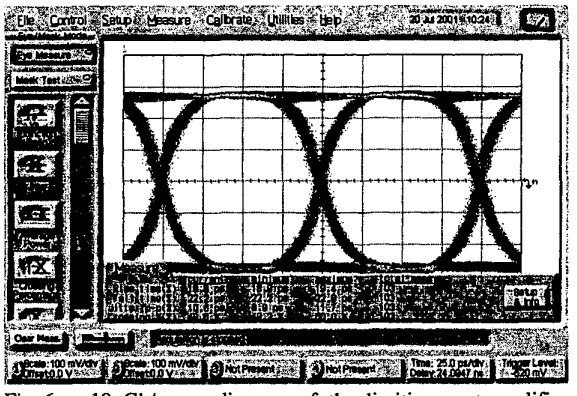

Fig. 6. 10 Gb/s eye diagram of the limiting post-amplifier with 15 mV peak-to-peak differential input signal. y-scale: 100 mV/div, x-scale: 25 ps/div.

LIA was implemented by cascading several fully differential wide-band stages to obtain the required gain-bandwidth product [10] (Figure 5). An offset cancellation scheme involving a low-pass filter was also utilized. The LIA has 50 Ω input and output impedances.

B. Measurements

On-wafer measurements of the LIA demonstrate a small-signal bandwidth and gain of 11.9 GHz and 40 dB, respectively. The chip draws a total of 200 mA from a 1.8 V power supply. Figure 6 demonstrates an eye diagram at the data rate of 10 Gb/s for a differential input signal amplitude of 15 mV peak-to- peak. For this measurement, the LIA output signal has a rise and fall time of better than 23 ps with a peak-to-peak jitter of better than 12 ps. The amplifier works at differential input signals up to 1.8 V peak-to-peak, with the same limited output amplitude of 600 mV differential peak-to-peak. A bit error rate (BER) of 10^{-12} has also been achieved with a differential input signal as low as 5 mV peak-to-peak. This signifies that the

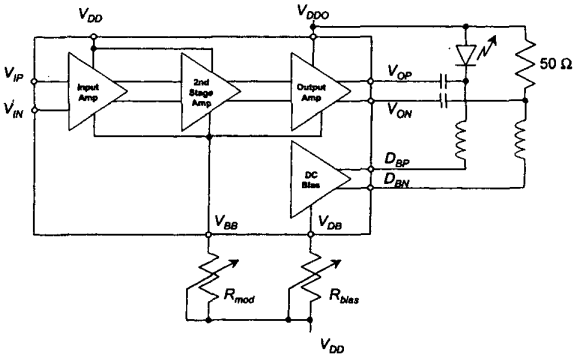

Fig. 7. Block diagram of the fully differential laser driver with laser bias current generator.

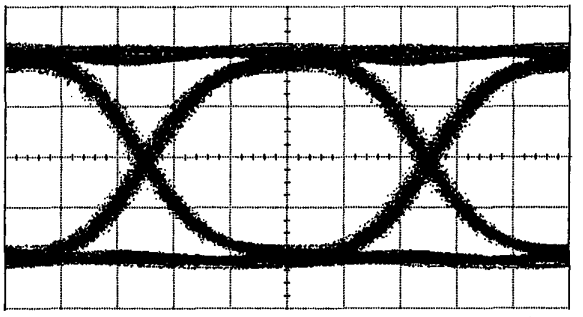

Fig. 8. 10 Gb/s output eye diagram of the laser driver amplifier with 500 mV peak-to-peak differential input signal. The modulation current setting was 30 mA peak-to-peak. y-scale: 375 mV/div, x-scale: 20 ps/div.

LIA successfully operates within an input signal dynamic range of 51 dB.

III. LASER DRIVER AMPLIFIER

A. Design:

The laser driver amplifier converts input signal coming from the digital multiplexer into a sufficiently large output current to modulate the laser in the optical transmitter. In addition to providing the modulation current drive, the LDA also supplies the dc bias current to keep the laser operation above threshold. The LDA comprises a wideband input gain stage, which is followed by an intermediate amplification stage. A final cascaded amplifier stage provides the large modulation current drive. The driver has 50 Ω on-chip input and output terminations for optimal interfacing with preceding amplification stages and a laser diode module with a 50 Ω input impedance [11] (Figure 7).

B. Measurements:

The LDA is able to supply modulation currents between 1.7 – 35 mA peak-to-peak into an external load of 50 Ω. At a modulation current drive of 30 mA peak-to-peak, the driver draws a current of 114 mA from the input power supply, V_{DD}, of 2.5 V and 63 mA from the output (laser diode) power supply, V_{DDO}, of 3.3 V. Figure 8 depicts the eye-diagram at 10 Gb/s of a packaged LDA, as observed by a high-speed digitizing oscilloscope (Z_{in} = 50 Ω). A 20% – 80% rise time, t_r, and a fall time, t_f, of 31 ps, and an rms jitter of 2.0 ps are measured respectively. The particular modulation current drive setting for this measurement was 30 mA peak-to-peak. Based on the measurements at this and other modulation current settings, it is inferred that an alternative output stage design with direct coupling into the laser diode (instead of the 50 Ω on-chip back termination) would be capable of supplying a modulation current drive of up to 70 mA peak-to-peak into a laser diode with 25 Ω input impedance.

IV. Conclusion

We have reported the first front-end chipset realized in 0.18 μm standard digital CMOS technology, suitable for 10 Gb/s communication. The chipset comprises a transimpedance amplifier (TIA), a limiting post-amplifier (LIA), and a laser driver amplifier (LDA), all in fully differential topology. The performance inherent in the chosen technology along with attention to detail in active and passive device modeling, layout techniques and the choice of fully differential architecture have enabled the successful implementation of these highly analog front-end functions in a generic digital CMOS process.

The TIA has a differential gain of 1300 Ω over an optical bandwidth in excess of 9 GHz, and can sustain a 3 mA (average) input current overload. The LIA accepts differential input voltages as small as 15 mV peak-to-peak and amplifies them to a differential output swing of 0.6 V peak-to-peak. The output signal level does not change for input levels as large as 1.8 V peak-to-peak. A BER of 10^{-12} has also been achieved at a differential input level of 5 mV peak-to-peak, signifying successful operation of the LIA within a 51 dB input signal dynamic range. The rise and fall times are better than 23 ps at 10 Gb/s operation. The LDA can drive a laser diode module with a 50 Ω input impedance. It has separately controllable laser pre-bias and modulation current outputs, which can be set up to 40 mA and up to 35 mA peak-peak, respectively. An alternative output stage design with direct coupling into the laser diode (instead of the 50 Ω on-chip back termination) is capable of supplying a modulation current drive of up to 70 mA peak-to-peak into a laser diode with 25 Ω input impedance.

References

[1] Y.M. Greshishchev, P. Schvan, J.L. Showell, M.-L. Xu, J.J. Ojha, J.E. Rogers, "A fully integrated SiGe receiver IC for 10 GB/s data rate," IEEE Journal of Solid-State Circuits, vol. 35, no. 12, December 2000, pp. 1949-1957.

[2] K. Kawai, H. Ichino, "A 0.6-W 10-Gb/s SONET/SDH bit-error-rate monitoring LSI," IEEE Journal of Solid-State Circuits, vol. 35, no. 12, December 2000, pp. 1988-1991.

[3] L.M. Lunardi, "InP-based monolithically integrated photoreceivers," Proceedings of International Conference on Indium Phosphide and Related Materials, Cape Cod, MA, USA, 11-15 May 1997, pp. 471-474.

[4] M. Yung, J. Jensen, R. Walden, M. Rodwell, G. Raghavan, K. Elliott, W. Stanchina, "Highly integrated InP HBT optical receivers," IEEE Journal of Solid-State Circuits, vol. 34, no.2, Feb. 1999, pp. 219-227.

[5] A. Tanabe, Y. Nakahara, A. Furukawa, T. Mogami, "A redundant multi-valued logic for 10 Gb/s CMOS demultiplexer IC," ISSCC 2001 Digest, pp. 220-221, 449.

[6] R. Nair, N.Y. Borkar, C.S. Browning, G.E. Dermer, V. Erraguntla, V. Govindarajulu, A. Pangal, J.D. Prijic, L. Rankin, E. Seligman, S. Vangal, H.A. Wilson, "A 28.5 GB/s CMOS non-blocking router for terabits/s connectivity between multiple processors and peripheral I/O nodes," ISSC 2001 Digest, pp. 224-225, 450.

[7] Y. Ohtomo, T. Yoshida, M. Nishisaka, K. Nishimura, M. Shimaya, "A single chip 3.5 Gb/s CMOS/SIMOX transceiver with automatic-gain-control and automatic-power-control circuits," ISSCC 2000 Digest, pp. 58-59.

[8] T. Yoon, B. Jalali, "Front-end CMOS chipset for fiber-based gigabit ethernet," Digest of Symposium on VLSI Circuits, Honolulu, HI, USA, 11-13 June 1998, pp. 188-191.

[9] K.-J. De Langen, J.H. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," IEEE Journal of Solid-State Circuits, Oct. 1998, vol.33, pp. 1482-1496.

[10] T. Yoon, B. Jalali, "622 MB/s CMOS limiting amplifier with 40 dB dynamic range," Electronics Letters, vol. 32, no. 20, 26 September 1996, pp. 1920-1921.

[11] K. Kiziloglu, T. Yoon, F. Williams, Jr., M.R. Sandor, A.K. Petersen, "A CMOS laser driver for 10 Gb/s communication," Technical Proceedings, National Fiber Optic Engineers Conference, July 2001, pp. 1237-1242.