

2016 EE214B Design Project - Part I

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1 Bias Calculations

Bias calculations go here.

2 Calculation of Key Design Parameters

Choice of L

- All devices used in current source have a minimum length of $2\mu\text{m}$.
- All other devices in the amplifier have minimum length of $1\mu\text{m}$. Minimum length is used as f_t is inversely proportional to L.
- All devices in bias generator circuit have length $\geq 2\mu\text{m}$.

Bias Generator circuit

- Constant gm reference based design is used as bias circuit to reduce mismatch errors.
- Transconductance of bias device (mn300) depends only on R2 and m (m is the ratio of MN300/MN400). Therefore gm can be set precisely.
- Start-up circuit is used to force the circuit to the desired operating point.

Approximations for hand calculations

For simpler hand calculations, following approximations are used.

1. $C_{db} = C_{sb} = 0.35C_{gs}$
2. $C_{gs} = (\frac{2}{3})WLCox + C_{ov}'W$
3. $C_{gd} = C_{ov}'W$
4. $g_{mb} = 0.2g_m$

Stage4

- As per the spec, common mode output voltage (v_{out}) has to be within -0.15v to 0.15v. Since the body is connected to vss, MN10 experiences back gate effect and the threshold voltage is given by:

$$\begin{aligned} V_t &= V_{t0} + \gamma(\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f}) \\ V_{t0} &= 0.5V, \gamma = 0.6, 2\phi_f = 0.8 \end{aligned} \quad (1)$$

- Stage 4 is a source follower which has a gain given by

$$A4 = \frac{g_{m_{10}}}{g_{m_{10}} + g_{mb_{10}} + (\frac{1}{R_L})} \quad (2)$$

- Gain of stage4 ($A4$) < 1 due to back gate effect and the output load.
- To achieve gain closer to 1 (0.6 - 0.7), it is important to size and bias MN10 such that $(g_{m_{10}} + g_{mb_{10}}) \gg (1/R_L)$.
- Transconductance of and drain current of MN_{10} is given by

$$g_{m_{10}} = \mu_n C_{ox} \left(\frac{W}{L} \right) v_{ov_{10}} \quad (3)$$

$$I_{d_{10}} = 0.5\mu_n C_{ox} \left(\frac{W_{10}}{L_{10}} \right) v_{ov_{10}}^2 (1 + \lambda(V_{dd} - V_{out})) \quad (4)$$

- MN_9 (bias device for source follower) is sized such that $Id_{10} + I_{R_L} = Id_9$ and the common mode output voltage does not fall out of range. This device is chosen to be of smaller size to reduce loading on V_{out} node.

$$\tau_{OUTPUT} = (R_L || \frac{1}{1.2gm_{10}})(C_L + Csb_{10} + Cgd_9 + Cdb_9) \quad (5)$$

- Cgs_{10} is assumed to be very small due to boot-strapping.

Stage 3

- Loading at node V_y increases with the increase in gain of stage 3 due to the miller effect. Hence gain of stage3 is kept low and is fixed at $\sqrt{2}$ to compensate for the gain lost in stage 4. Gain of stage3 (CS amplifier with diode connected load):

$$|A3| = \frac{gm_7}{gm_8} = \frac{V_{ov8}}{V_{ov7}} = \frac{V_{dd} - V_z - abs(V_{tp})}{V_y - V_{ss} - V_{tn}} = \sqrt{2} \quad (6)$$

- Choice of V_z from above (stage4) determines V_y .
- Minimum device sizes ($W=2\mu m$, $L=1\mu m$) are used for both MN_7 and MP_8 to reduce loading on V_y and V_z .

$$Id_7 = Id_8 = 0.5\mu n Cox(\frac{W_7}{L_7})v_{ov7}^2(1 + \lambda(V_z - V_{ss})) \quad (7)$$

$$\tau_Z = (\frac{1}{gm_8})(Cgs_8 + Cdb_8 + Cgd_{10} + Cgd_7(1 + \frac{1}{|A3|}) + Cdb_7) \quad (8)$$

Stage 2

- V_y from stage Z above determines the required ratio of R_3 and R_4 .

$$(\frac{R_4}{R_3}) = \frac{V_{ss}}{V_y} - 1 \quad (9)$$

- Gain of stage Y (Cascode amplifier) is set to 3.

$$|A2| = gm_4(R_3 || R_4) \quad (10)$$

- V_{ov4} and W_4 are optimized to reduce τ_X .
- MN_6 is sized such that current through MN_6 is same as the current through MP_4 and MP_5 .

$$Id_4 = Id_5 = Id_6 = 0.5\mu p Cox(\frac{W_4}{L_4})(V_{dd} - V_x - abs(V_{tp}))^2(1 + \lambda(V_{dd} - V_w)) \quad (11)$$

- Current through R_3 and R_4

$$I_{R3} + I_{R4} = V_{ss}/(R_3 + R_4) \quad (12)$$

$$\tau_Y = (R_3 || R_4)(Cgs_7 + Cgd_7(1 + |A3|) + Cgd_6 + Cdb_6 + Cgd_5 + Cdb_5) \quad (13)$$

Stage 1

- V_{ov4} from stage 2 sets V_X which in turn sets the ratio of R_1 and R_2 .

$$V_{ov4} = V_{dd} - V_x - |V_{tp}| \quad (14)$$

$$(\frac{R_1}{R_2}) = \frac{V_{dd}}{V_x} - 1 \quad (15)$$

- Gain of stage 1 (Common gate amplifier) is set to 10000.

$$|A1| = (R1||R2) \quad (16)$$

- MN1 and MP3 are sized such that $Id1 = Id3$.
- MN2 is sized to reduce τ_{IIN} node. τ_{IIN} is inversely proportional to gm_2 .

$$\tau_{IIN} = (\frac{1}{gm2})(Cin + Cgd_1 + Cdb_1 + Cgs_2 + Csb_2) \quad (17)$$

$$\tau_X = (R1||R2)(Cgd_2 + Cdb_2 + Cgd_3 + Cdb_3 + Cgs_4 + Cgd_4) \quad (18)$$

- Current through MN1, MN2 and MP3

$$Id_{1,2,3} = 0.5\mu pCox(\frac{W_3}{L_3})(Vdd - VbiasP - |Vtp|)^2(1 + \lambda(Vdd - Vx)) \quad (19)$$

- Current through R1 and R2

$$I_{R1} + I_{R2} = Vdd/(R1 + R2) \quad (20)$$

Vovn, Vovp

- Vovn and Vovp are chosen to achieve a reasonable balance between gain, Tau total and Power, and our choice was educated by the gm/Id technology plots.

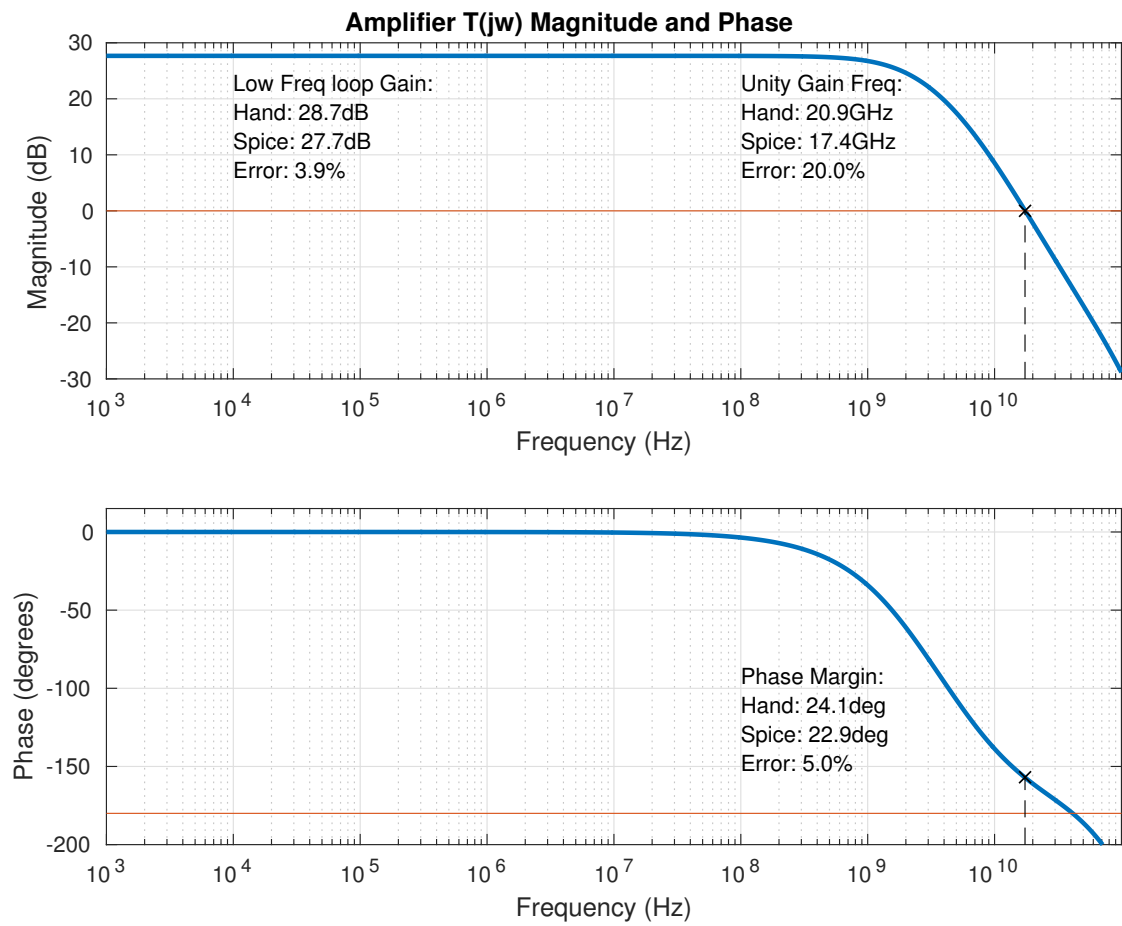
Total Design Performance

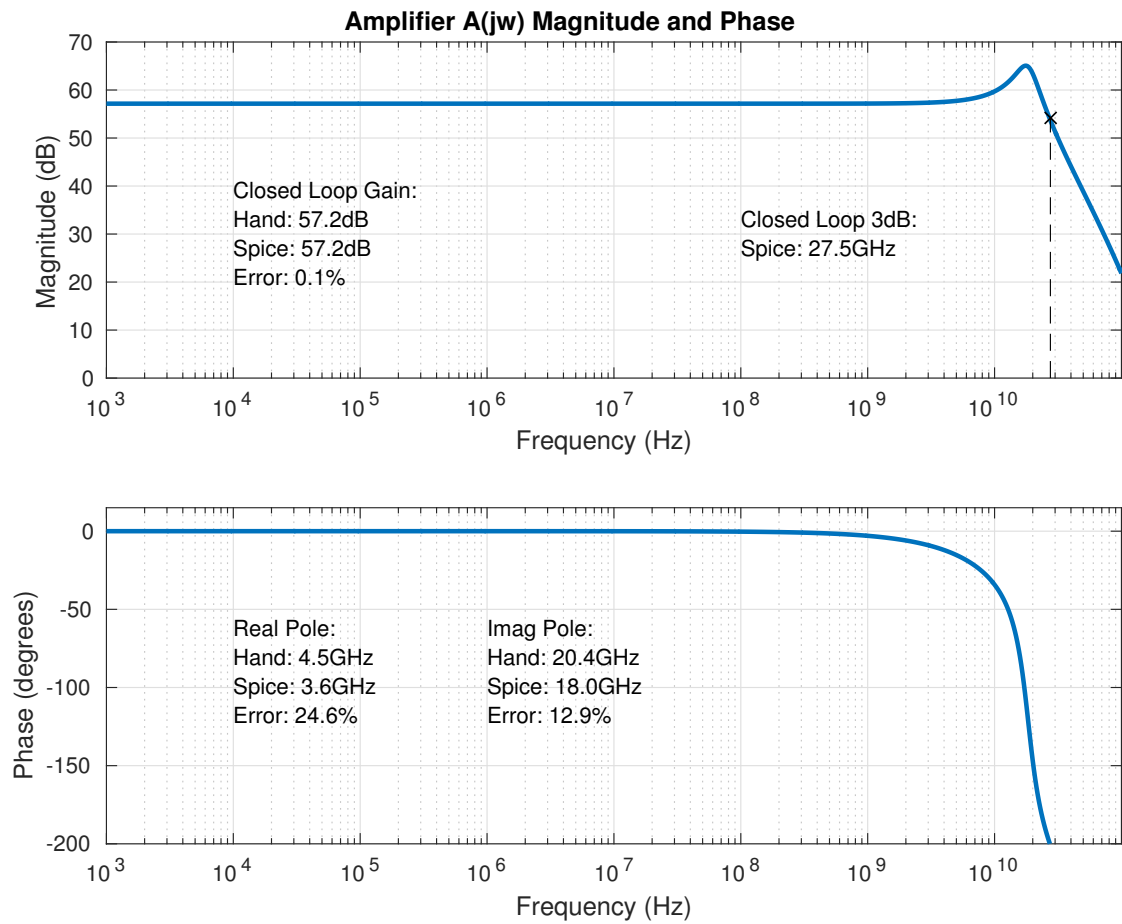
$$|A_{TOTAL}| = A1 * A2 * A3 * A4 \quad (21)$$

$$\tau_{TOTAL} = \tau_{IIN} + \tau_X + \tau_Y + \tau_Z + \tau_{OUTPUT} \quad (22)$$

$$Power = (Vdd - Vss)(Id_1 + Id_4 + Id_7 + Id_{10}) + (\frac{Vdd^2}{R1 + R2}) + (\frac{Vss^2}{R3 + R4}) \quad (23)$$

3 Bode Plots and PZ Outputs - Part I(g,h)





***** pole/zero analysis

input = 0:is output = v(vo)

poles (rad/sec) poles (hertz)

real	imag	real	imag
-33.1562m	0.	-5.27698m	0.
-22.9305g	113.319g	-3.64950g	18.0353g
-22.9305g	-113.319g	-3.64950g	-18.0353g
-473.782g	0.	-75.4048g	0.
-1.12800t	0.	-179.526g	0.
-1.18039t	0.	-187.865g	0.

zeros (rad/sec)

zeros (hertz)

real	imag	real	imag
0.	0.	0.	0.
-1.10418t	0.	-175.736g	0.

4 Calculations for Part I(i)

A feedback capacitor can be used to introduce a zero into the feedback loop in order to push the higher frequency pole out and flatten the response of the closed loop amplifier. The optimally flat response of the amplifier occurs when $Q = \sqrt{2}$. Hence:

$$\omega_0 = 1.09e11 rad/s \quad (24)$$

$$\omega_Z = \frac{\omega_0}{\sqrt{2} - \frac{\omega_{P1} + \omega_{P2}}{\omega_0}} \quad (25)$$

$$C_F = \frac{1}{\omega_Z R_F} = 57 fF \quad (26)$$

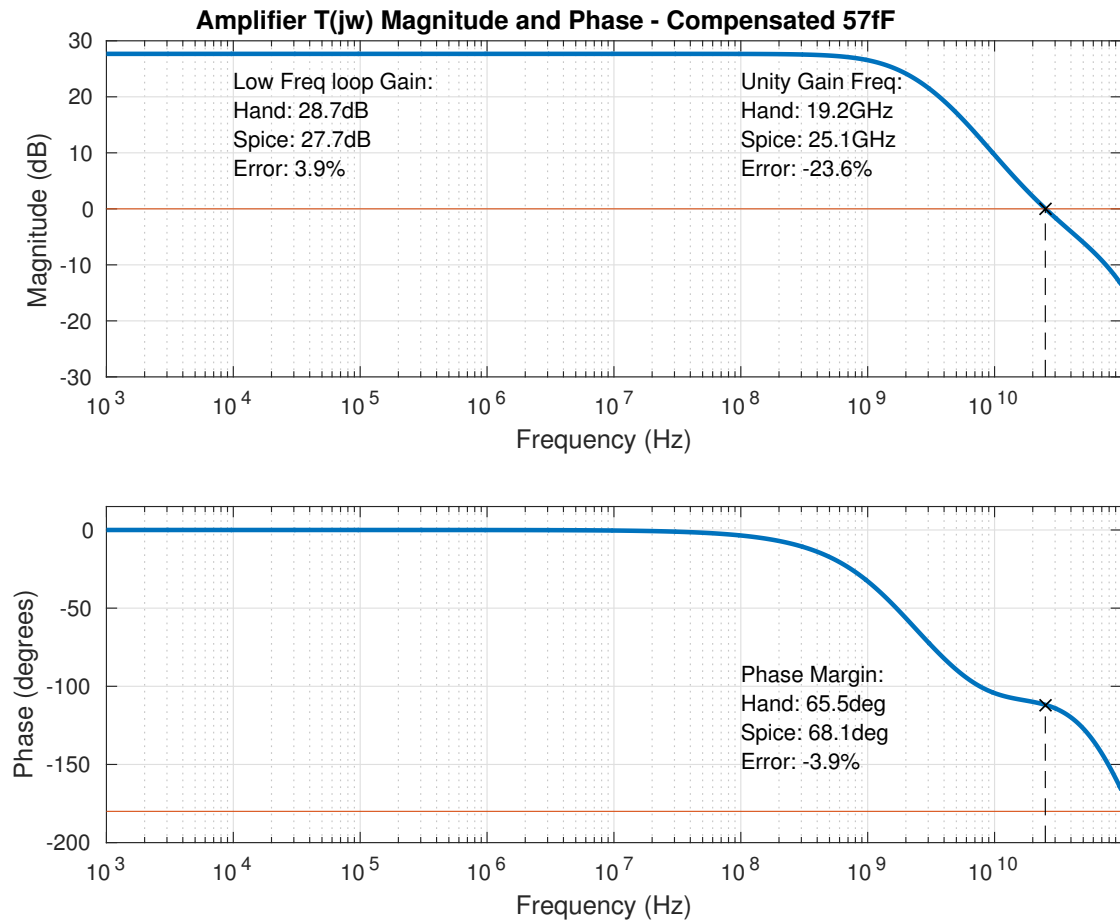
From this, the new closed loop bandwidth can be calculated as such:

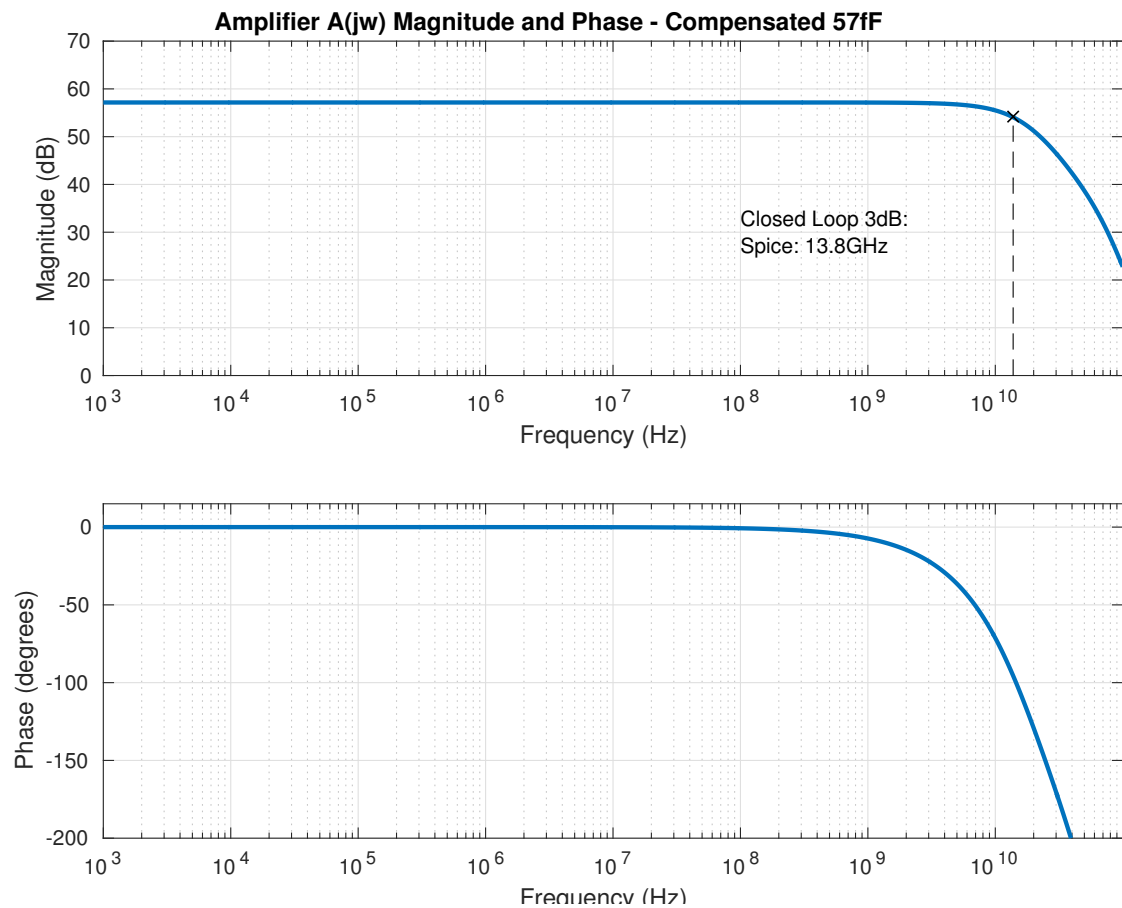
$$C_{in,C_F} = C_{in} + C_F \quad (27)$$

$$k = \frac{R_{in} * Q1_{gm} * R_x * A_{V3}}{R_F} \quad (28)$$

$$BW_{CL,C_F} = \frac{\sqrt{1+k}}{2\pi R_{in} C_{in} R_x C_x} = 19.2 GHz \quad (29)$$

5 Bode Plots and PZ Outputs - Part I(j)





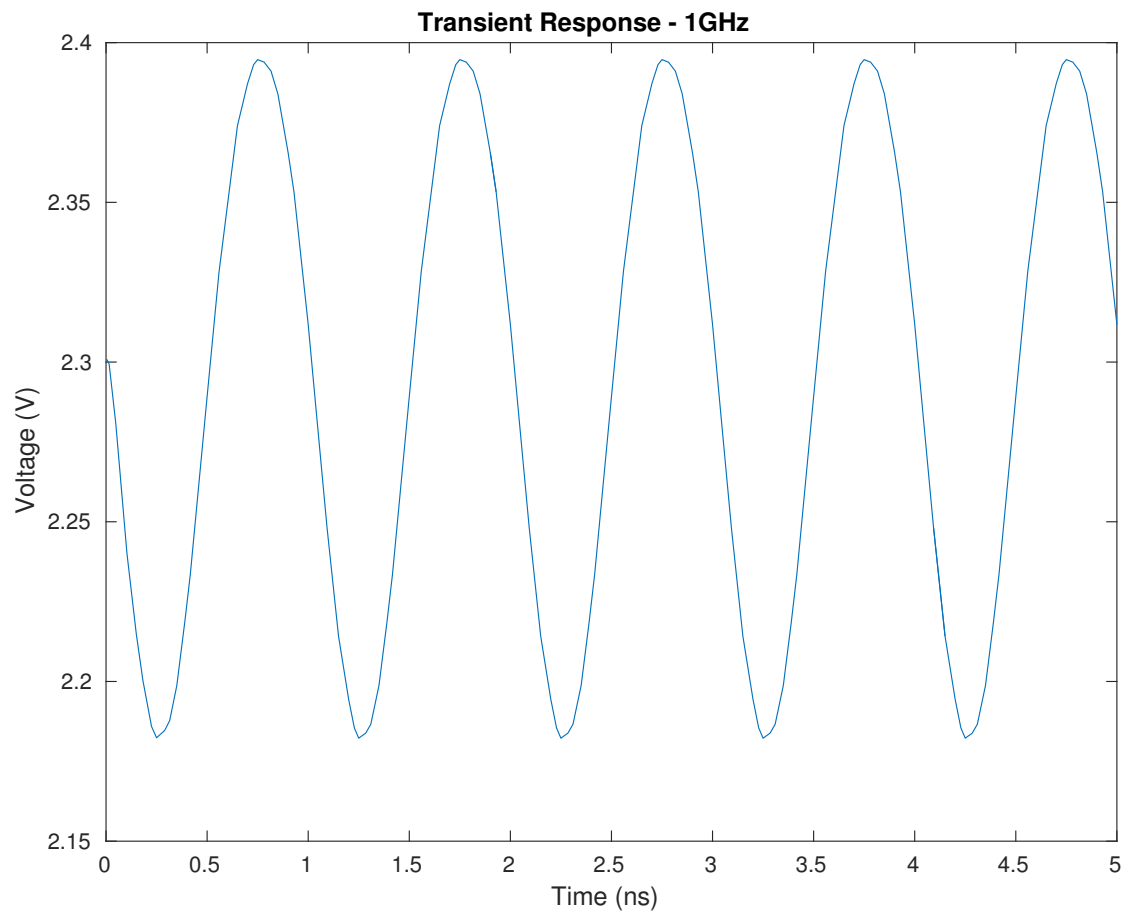
***** pole/zero analysis

input = 0:is output = v(vo)

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-33.1562m	0.	-5.27698m	0.
-102.336g	-49.5561g	-16.2872g	-7.88710g
-102.336g	49.5561g	-16.2872g	7.88710g
-321.575g	358.533g	-51.1803g	57.0622g
-321.575g	-358.533g	-51.1803g	-57.0622g
-1.11894t	0.	-178.085g	0.
-1.35128t	0.	-215.063g	0.
-1.88412t	0.	-299.868g	0.

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
0.	0.	0.	0.
-1.09418t	0.	-174.144g	0.

6 Transient Response - Part I(m)



Bias Generator	Hand calc	Spice	%Error	Reason for error
V_{BiasN}	-1.300V	-1.279V	-1.6%	Startup circuit bias
V_{BiasP}	1.300V	1.319V	1.5%	Startup circuit bias
Stage1	Hand calc	Spice	%Error	Reason for error
I_{d1}	$18.3\mu A$	$20.9\mu A$	14.2%	Bias generator error
V_X	1.300V	1.275V	-1.9%	
A_X	10k Ω	9.86k Ω	-1.4%	Finite MN_1 and MP_3 output resistance
gm_2	210 μS	268 μS	27.6%	Bias generator error
τ_{IN}	1.11ns			
τ_X	420ps			
Stage2	Hand calc	Spice	%Error	Reason for error
I_{d4}	$36.75\mu A$	$43.5\mu A$	18.4%	
V_W	1.496V	1.450V	-3.2%	
V_Y	-1.550V	-1.418V	-8.5%	Imbalance between MP_4 and MN_6 current
gm_4	105 μS	120 μS	14.3%	Error in V_Y
A_Y	-3.0	-3.25	8.3%	Error estimating gm_4
τ_Y	306ps			
Stage3	Hand calc	Spice	%Error	Reason for error
I_{d7}	$10.25\mu A$	$22.9\mu A$	123%	Error in V_Y plus finite output resistance
V_Z	1.364	1.102V	-19.2%	Error in V_Y
gm_7	45 μS	79 μS	75.5%	Error in I_{d7}
gm_8	31.2 μS	51 μS	63.5%	Error in I_{d7}
A_Z	1.414	1.440	1.8%	The benefit of ratiometric design
τ_Z	1.92ns			Error in estimating gm_8
Stage4	Hand calc	Spice	%Error	Reason for error
I_{d10}	$2.96\mu A$	$30.43\mu A$	928%	MN_{10} 's large width is a big error amplifier
V_{OUT}	0.299	-0.117V	-139%	
V_{t10}	0.999	1.034V	3.5%	
gm_{10}	91.1 μS	327 μS	258%	
gmb_{10}	13.0 μS	55.1 μS	323%	
A_{OUT}	0.71	0.75	5.6%	
τ_{OUT}	1.63ns			Error in estimating gm_{10}
Total Power	578 μW	1.065mW	84%	Not accounting for bias gen
Total Gain	30.04k Ω	34.66k Ω	15.5%	Error in estimating gm