

# Homework 1 Problem 3

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- 1)(a) [1]  
(b) 8 bit resolution, 28Gs/s, 280mW  
(c) 16nm FIN-FET, 2.8mm<sup>2</sup>  
(d) 32x interleaved SAR converters, used for implementing 56Gbps serial links over legacy 28Gbps backplanes.  
(e) 17.86 Hours
- 2)(a) [2]  
(b) 5 bit resolution, 500Ms/s, 1.62mW  
(c) 55nm CMOS, Area not stated  
(d) Digital Slope using Strongarm Comparator, Ultra wide-band wireless communications  
(e) 128.6 Days
- 3)(a) [3]  
(b) 10 bit resolution, 1.5Gs/s, 6.92mW  
(c) 14nm CMOS FIN-FET, 0.0016mm<sup>2</sup>  
(d) SAR architecture, application not specified  
(e) 722.5 Hours

## REFERENCES

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- [2] Y. Shu, F. Mei, Y. Yu, and J. Wu, "A 5-bit 500-ms/s asynchronous digital slope adc with two comparators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. PP, no. 99, pp. 1–1, 2017.
- [3] L. Kull, D. Luu, C. Menolfi, M. Braendli, P. A. Francese, T. Morf, M. Kossel, H. Yueksel, A. Cevrero, I. Ozkaya, and T. Toifl, "28.5 a 10b 1.5gs/s pipelined-sar adc with background second-stage common-mode regulation and offset calibration in 14nm cmos finfet," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 474–475.