1) a) F

b) T

c) F

2)

	Code Type	Code	Base 10	Analog Range
a)	Binary Mid Rise	10001	17	0.53125 0.5625
b)	Binary Mid Tread	10010	18	0.546875 - 0.578125
c)	Complementary Mid Tread	01011	20	0.609375 - 0.640625
d)	Gray Mid-Rise	01101	9	0.28125 - 0.3125

5 bits, 1V unipolar → 31.25 mV / bit

Homework 1 Problem 3

Samuel Lenius

1) (a) [1]
   (b) 8 bit resolution, 28Gs/s, 280mW
   (c) 16nm FIN-FET, 2.8mm^2
   (d) 32x interleaved SAR converters, used for implementing 56Gbps serial links over legacy 28Gbps backplanes.
   (e) 17.86 Hours
2) (a) [2]
   (b) 5 bit resolution, 500Ms/s, 1.62mW
   (c) 55nm CMOS, Area not stated
   (d) Digital Slope using Strongarm Comparator, Ultra wide-band wireless communications
   (e) 128.6 Days
3) (a) [3]
   (b) 10 bit resolution, 1.5Gs/s, 6.92mW
   (c) 14nm CMOS FIN-FET, 0.0016mm^2
   (d) SAR architecture, application not specified
   (e) 722.5 Hours

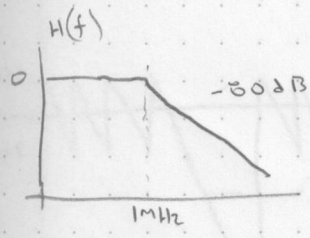
References

[1] Y. Frans, J. Shin, L. Zhou, P. Upadhyaya, J. Im, V. Kireev, M. Elzeftawi, H. Hedayati, T. Pham, S. Asuncion, C. Borrelli, G. Zhang, H. Zhang, and K. Chang, "A 56-gb/s pam4 wireline transceiver using a 32-way time-interleaved sar adc in 16-nm finfet," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1101–1110, April 2017.

[2] Y. Shu, F. Mei, Y. Yu, and J. Wu, "A 5-bit 500-ms/s asynchronous digital slope adc with two comparators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. PP, no. 99, pp. 1–1, 2017.

[3] L. Kull, D. Luu, C. Menolfi, M. Braendli, P. A. Francese, T. Morf, M. Kossel, H. Yueksel, A. Cevrero, I. Ozkaya, and T. Toifl, "28.5 a 10b 1.5gs/s pipelined-sar adc with background second-stage common-mode regulation and offset calibration in 14nm cmos finfet," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 474–475.

4) a) 50dB attenuation plot notell, slide 31



$50 = 80 \log_{10}(OSR)$

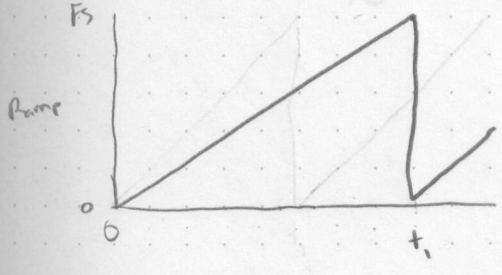
$OSR = 10^{50/80} = 4.216$

$f_s = 4.216 Ms/s$

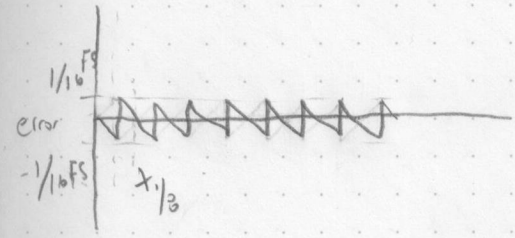
b) $50 = 60 \log_{10}(OSR)$

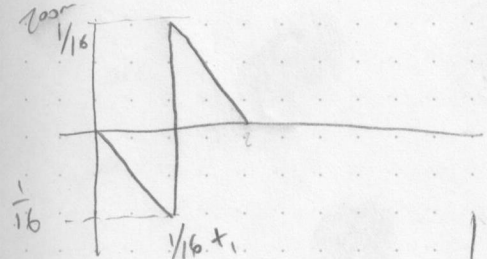
$OSR = 10^{50/60} = 6.81$

5) a) 3 bit mid-tread



error = 6 - Vramp





power = rms(error)^2

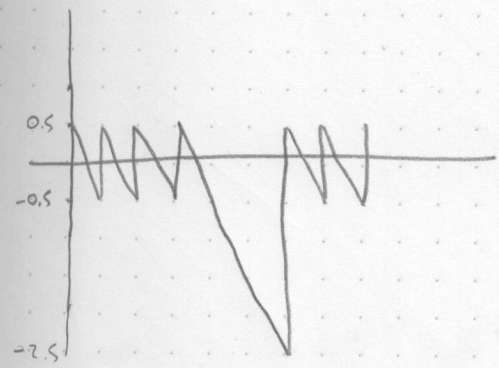
$= \frac{1}{T}\int_0^T u(t)^2 dt = \frac{1}{1/16\,t_1}\int_0^{1/16\,t_1}\left(\frac{t}{1/16\,t_1}\cdot\frac{Fs}{16}\right)^2 dt$

$t_x = 1/16\,t_1 = \frac{1}{t_x}\int_0^{t_x}\left(\frac{Fs}{16}\right)^2\cdot\left(\frac{t}{t_x}\right)^2 dt$

$= \frac{1}{t_x}\cdot\frac{Fs^2}{t_x^2\cdot 16^2}\cdot\frac{t^3}{3}\Big|_0^{t_x} = \frac{t_x^3}{3}\cdot\frac{Fs^2}{256\cdot 3}$

$power = \frac{Fs^2}{768}$ | $Fs=8$, $power = \frac{1}{12}$

5) b) Broken quantizer



By duty cycle inspection

① 11 cycles -0.5 to $+0.5$, $t = 1/16$

② 1 cycle 0.5 to 2.5 $t = 5/16$

① $\frac{1}{t_x}\int_0^{t_x}\left(0.5\cdot\frac{t}{t_x}\right)^2 dt = \frac{1}{4t_x^3}\cdot\frac{t^3}{3}\Big|_0^{t_x} = \boxed{\frac{1}{12}}$

$t_x = \frac{t_1}{16}$

② $\frac{1}{t_y}\int_0^{t_y}\left(2.5\cdot\frac{t}{t_y}\right)^2 dt = \frac{6.125}{t_y^3}\cdot\frac{t^3}{3}\Big|_0^{t_y} = \boxed{\frac{6.25}{3} \approx 2.083}$

$t_y = \frac{5t_1}{16}$

$$\text{Power} = \frac{\left(11\cdot\frac{1}{12} + 5\cdot\frac{6.25}{3}\right)}{16} = 0.7052$$

6) a) See next

b) sine wave deviation: $1.313\ e^{-3}$

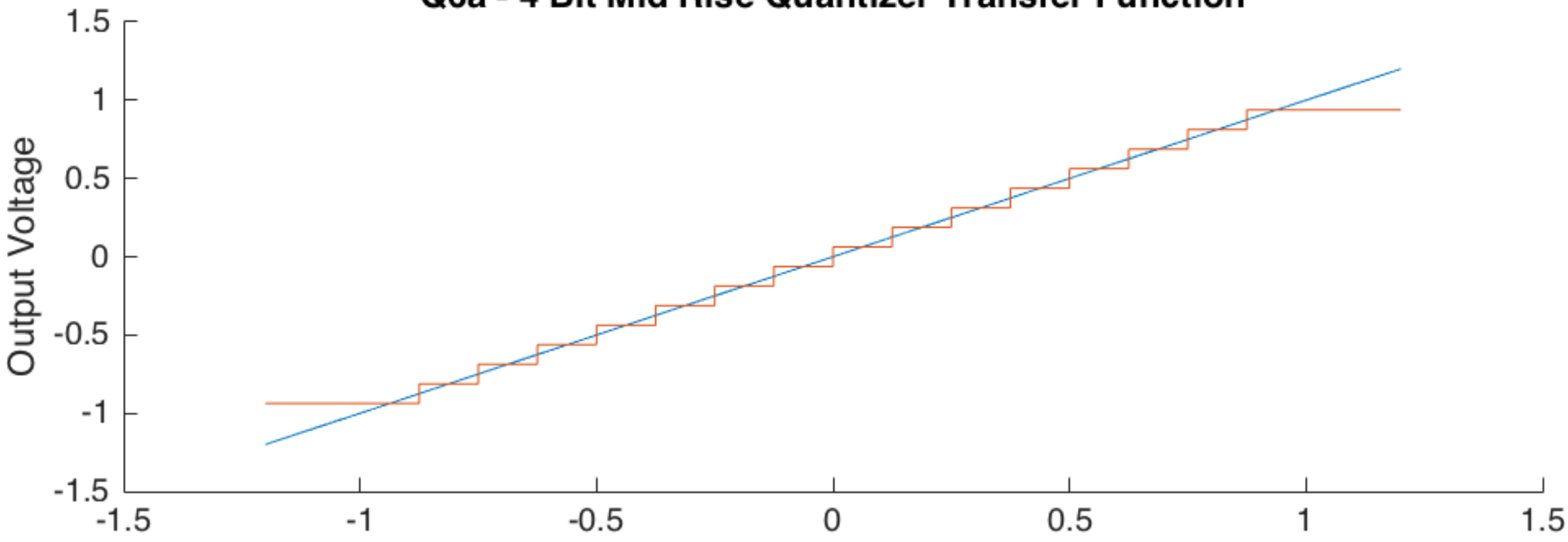
$\frac{\Delta^2}{12} = 1.302e^{-3}$

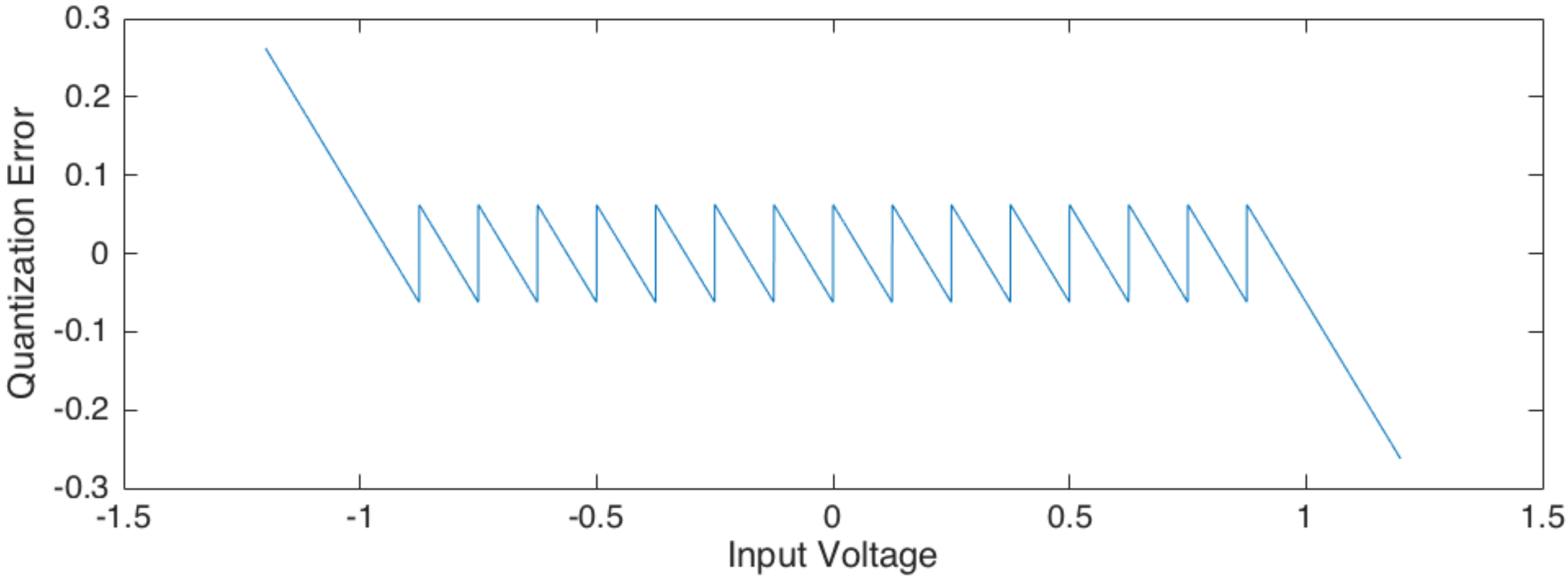
deviation: 0.820^{-}

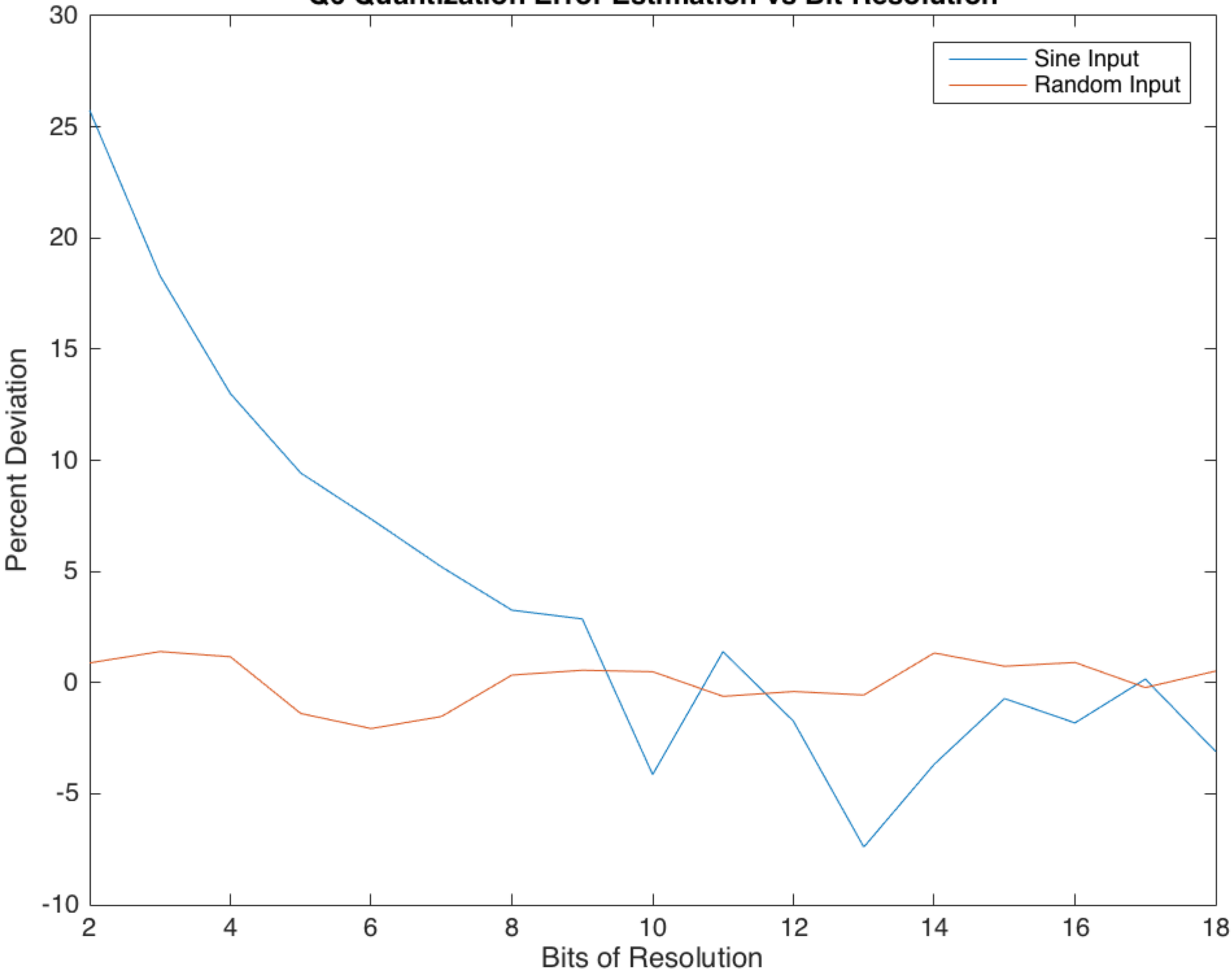
c) See next

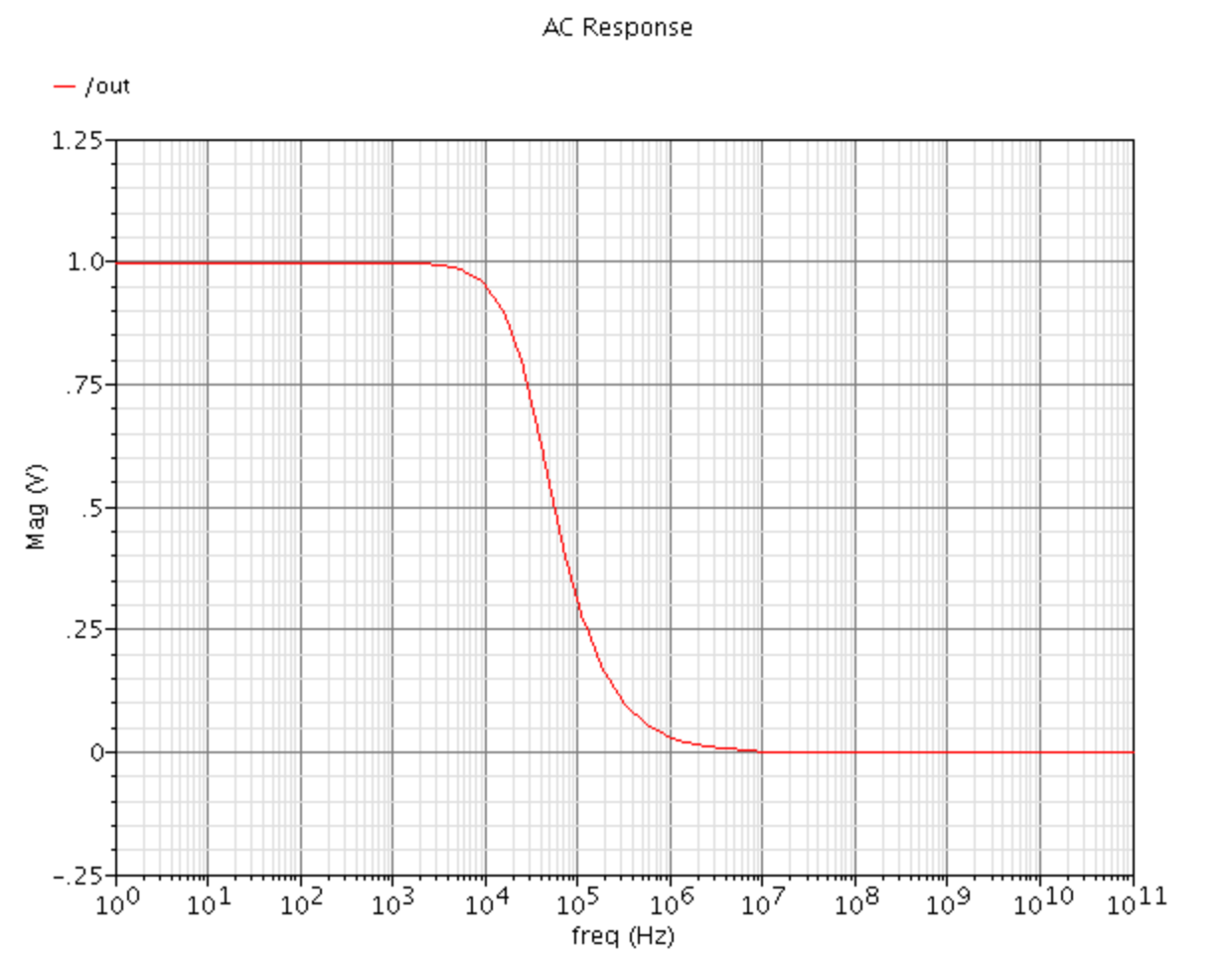
d) See next

e) At low resolutions, the deviation diverges significantly. I suspect this is due to the nonuniform distribution of voltage values of the sine wave.


Q6a - 4 Bit Mid Rise Quantizer Transfer Function
Output Voltage
1.5
1
0.5
0
-0.5
-1
-1.5
-1.5
-1
-0.5
0
0.5
1
1.5


Quantization Error
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-1.5
-1
-0.5
0
0.5
1
1.5
Input Voltage


Q6 Quantization Error Estimation vs Bit Resolution
Sine Input
Random Input
Percent Deviation
Bits of Resolution
30
25
20
15
10
5
0
-5
-10
2
4
6
8
10
12
14
16
18


AC Response
/out
1.25
1.0
.75
.5
.25
0
-.25
Mag (V)
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^{10}
10^{11}
freq (Hz)