5) -40.8mdB gain at 400MHz

6) a) See next

bi) See next for plot

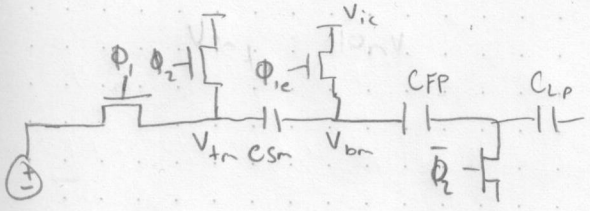
Immediately after Φ_1 rises, V_{cs} drops from 10mv to 9.386mV, an error of 0.614mV

V_{cs} is computed as $V_{cs} = (V_{tm} - V_{bm}) - (V_{tp} - V_{bp})$

The disturbances on the capacitors are equal in magnitude and not dependant on the input voltage, hence the difference in voltage across them is not affected. The bottom plate sampling technique takes advantage of common mode rejection in the OTA combined with equal charge injection to null the resulting offset.

bii) See next.

biii) Charge injection error headed when Φ_{1e} opens



Φ_{1e} closed $\Rightarrow$ $V_{bm} = V_{ic} = 0.6V$

Φ_1 closed $\rightarrow$ $V_{tm} = V_{ic} + \frac{V_{id}}{2} = 0.605V$

Φ_{1e} mosfet channel = $30\mu/0.2\mu$ $Q_{ch} = -WLC_{ox}(V_{dd} - V_{in} - V_t) = 36fC$

$C_{SM} \,||\, C_{FP} = 200fF$

$\Delta V = \frac{Q_{ch}}{2C} = \frac{36fF}{2 \cdot 200f} = \boxed{90.0mV}$ $\boxed{113mV \text{ observed}}$