HOMEWORK #5

(Due: Thursday, November 2, 2017, 11:59 pm PT via Gradescope Online Submission)

1. **Quick Questions.** For each of the following statements, state "T" for true or "F" for false. No explanation necessary. Correct answers are worth +1 point, while incorrect answers yield -1 point. No points for unanswered questions. Your minimum total score on this problem is zero points.

a) Adding a (finite bandwidth) pre-amplifier to a latch comparator does not improve the metastability rate, since it takes time away from exponential regeneration.	
b) A noisy comparator has a lower metastability rate, since the noise helps push the circuit out of its metastable state..	
c) As long as the comparators used in a flash ADC resolve ½ LSB within the given decision time, the comparators will automatically achieve very low metastability rates.	

2. In this problem you will examine the behavior of a comparator latch which has a simplified model provided in Figure 1 (H.-S. Lee, et al., JSSC, Dec 1984). This model represents the beginning of the comparison phase, so the PMOS switch from vom to vop (see full circuit in Figure 3) is off and is excluded from this model.

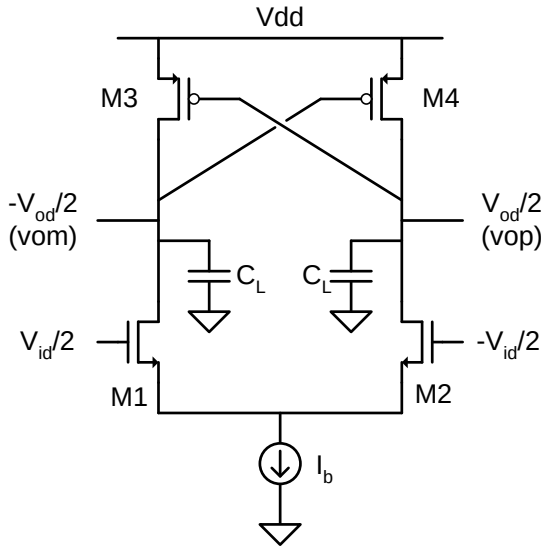

Figure 1

You can make the following assumptions:

- All relevant capacitances have been lumped into the load capacitors C_L.
- For the purposes of small-signal analysis, the small-signal differential input is assumed to step from 0 to V_{id} at the beginning of the comparison phase. In reality, V_{id} is set up and held before comparison begins.
- The gates of M1 and M2 are biased at a common-mode level, V_{cm}, that ensures both devices remain on during the comparison.

- Transistors M1-M4 can be modeled as a transconductor and output resistor, as shown in Figure 2.
- Assume that the circuit is fully symmetric with no offsets, i.e. $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$, $r_{o1} = r_{o2}$, and $r_{o3} = r_{o4}$.

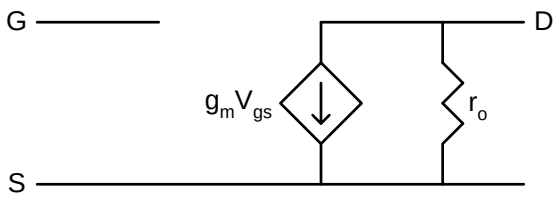

Figure 2

When the step input is applied, V_{od} initially changes at an exponential rate. This is the regeneration period which continues until one of the PMOS transistors turns off. Beyond that time, the V_{od} change is limited by the slew rate of the latch. We will examine both regeneration and slewing in this problem.

(a) Derive an expression for the differential output of the circuit, V_{od}, in the regeneration period as a function of time, for $t > 0$. Do not neglect the effect of finite output resistance. *Hint: start with s-domain analysis, then take the inverse Laplace transform to obtain the time-domain response.*

(b) Find the value of V_{op} when M3 turns off. Find the slewing rate at V_{om} at this point. Assume V_{id} is small such that M1 and M2 split the tail current equally.

(c) Now, you will run some Spectre simulations for the latch with the parameters given in Figure 3. The ratios are listed as W/L in microns. Assume that the n-wells for the PMOS transistors are tied to $V_{DD} = 1.8V$, while the NMOS bulks are tied to $V_{SS} = 0V$. First, perform a transient simulation with $V_{id} = 1mV$ and $V_{cm} = 0.9V$. Initially hold the STROBE low for 5ns and then measure the transition time after the STROBE goes high. The rise time for the STROBE is 0.2ns.

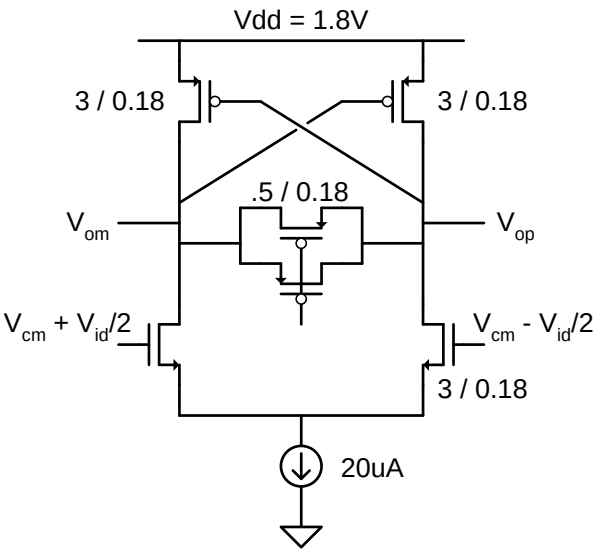

Figure 3

Copy the comparator_tb schematic (located in the ee315 library), which is a testbench to run the comparator shown below, to your own library. In ADE, run a transient analysis with the following settings:

Stop Time	15ns (conservative)
Vdd	1.8V
Vic	0.9V
Vid	1mV (for part c)

For part c and part d below, turn in transient plots showing str, vop, vom, and vod.

(d) Now we change V_{id} and compare the transient result to part (c).

i. Which region, regeneration or slewing, is affected the most (in duration) by decreasing the differential input from 1mV to 100μV?

ii. Which region is affected the most by increasing the differential input from 1mV to 100mV?

(e) Use your simulation set-up from above to extract the latch time constant (plot the differential output on a log scale as done in lecture notes)

(f) As a designer, you will typically be interested in finding out which components set or limit the regeneration time constant, so that you can work on informed improvements (rather than random schematic hacks). Run a DC operating point analysis for the circuit to find g_m and tabulate the most significant capacitances that are hanging on the regenerative node. To find the total capacitance (C_L), use the option "CAPTAB" from the DC analysis options window to report node capacitances, then look for the capacitance table in the Spectre output log after you simulate it. How close is C_L/g_m to the time constant value you found in part (e)?

(g) Estimate the (static) input offset voltage standard deviation of the comparator assuming A_{VT} = 4 mVμm. Consider only threshold voltage mismatch, and use the small-signal model of the comparator. For g_m and r_o values, you can use DC operating point analysis results from part (f).

3. Strong ARM Latch.

(a) Read the following paper:
B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," IEEE Solid-State Circuits Magazine, vol. 7, no. 2, pp. 12-17, Spring 2015.
http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7130773

(b) Do V_P and V_Q go all the way to ground at the end of regeneration?

(c) What would be the input common mode requirements for the modified StrongARM latch to function properly?

(d) In figure 4, explain if we can use an RS latch with PMOS input pair?

(e) Suggest a method to measure the offset of the StrongARM latch (assume to be a static offset).

Explain your design choices in the following cases in 1-2 sentences:

(f) How should we size the input pair to reduce kick-back?

(g) How should we size the input pair to reduce noise?

4. **ADC DNL and INL**.

a) Consider a monotonic ADC with output codes 0, 1, 2, …M. Show that

$$INL(j) = \sum_{i=1}^{j-1} DNL(i) .$$

b) Using (a), verify that

$$\sum_{i=1}^{M-1} DNL(i) = 0 .$$

c) Your friend at MIT just received his Nyquist-rate 12-bit prototype ADC back from the fab and tells you about his measurement results:

i. The SQNR (measured using a full-scale sine wave) seems to be excellent, at least 85 dB.

ii. For one of his chips, the DNL is not so great, he measured DNL = +0.1/-2.3 LSB.

iii. For yet another chip he measured: DNL = +0.3/-0.3 LSB, and INL = +0.1/-0.1 LSB.

What is wrong with the above statements? Explain briefly. Consider all statements separately, e.g., there is no connection to be made between (i) and (ii).

d) An otherwise perfect ADC has a missing code, i.e. DNL = -1. What is the INL of this converter? Justify your result with a sketch.

e) The table below shows DNL/INL data for an ADC. Complete the four empty fields in this table based on known properties and relationships between DNL and INL.

Code	0	1	2	3	4	5	6	7
DNL	undef.	0.1	-0.5	0.2	0.4			undef.
INL	undef.	0	0.1		-0.2	0.2	-0.1	

5. Consider a 6-bit flash ADC with an ideal reference resistor string and V_{ref} = 1.8V. Assume that the comparators have an offset voltage with standard deviation σ_{OS} = 2mV. What is the standard deviation of the converter's DNL and INL? (For simplicity, assume that the first and last comparator have zero offset.) Note that DNL and INL need to be expressed in terms of LSB.