HOMEWORK #4

(Due: Thursday, October 26, 2017, 11:59 pm PT via Gradescope Online Submission)

1. **Quick Questions.** For each of the following statements, state "T" for true or "F" for false. No explanation necessary. Correct answers are worth +1 point, while incorrect answers yield -1 point. No points for unanswered questions. Your minimum total score on this problem is zero points.

a) In a chopped amplifier, the chopping frequency should be set far below the signal bandwidth, so that the signal does not get disturbed.	
b) Autozeroing becomes more effective at rejecting flicker noise as the clock frequency is increased.	
c) The input offset drift (in µV/K) of a CMOS differential pair is proportional to the absolute offset caused by current factor mismatch ($\Delta\beta/\beta$).	

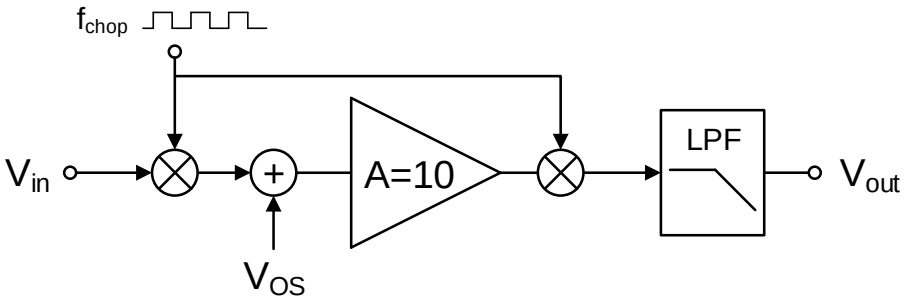
2. Boxcar Sampling. Read the first four pages of this paper:

   H. Gao, R.M. Walker, P. Nuyujukian, K.A.A. Makinwa, K.V. Shenoy, B. Murmann and T.H. Meng, "HermesE: A 96-Channel Full Data Rate Direct Neural Interface in 0.13 µm CMOS," IEEE J. Solid-State Circuits, pp. 1043-1055, Apr. 2012. http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6158616

   a) Derive equation (2).
   b) Verify the 3.4x advantage in the effective noise bandwidth, claimed by the authors.

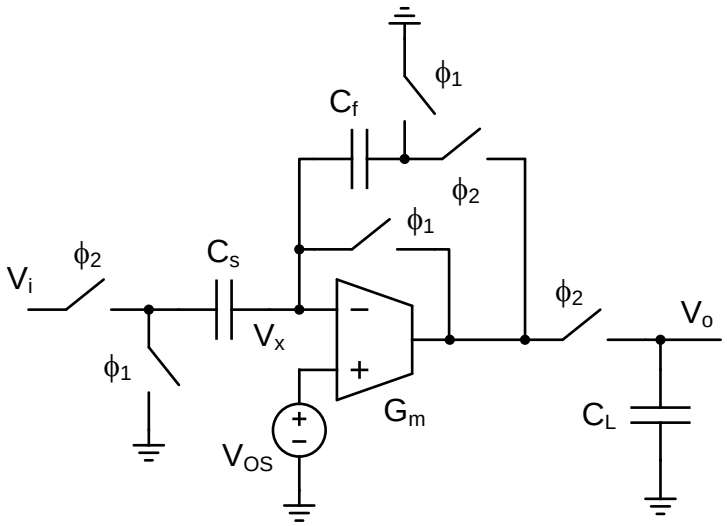
3. Shown below is a chopper-stabilized sensor interface circuit. The amplifier block "A" is an ideal amplifier block with gain of 10 and infinite bandwidth. It suffers from an input referred offset of V_{OS} = 20 mV. The circuit is chopped with a perfect 50% duty cycle at 1 MHz and the LPF block is a first order filter with a corner frequency of 50 kHz. In your solution to this problem, do not go overboard with math and instead think about proper engineering approximations. Hint: What does the step response of the filter look like on the time scale of the ½ chopping period? You can assume the filter to be as an integrator for frequencies above it cut off.

   a) Sketch the waveform of V_{out} versus time, assuming V_{in} = 0 and assuming that the waveform has reached steady-state.
   b) Calculate the peak-to-peak ripple of the output waveform using the same assumptions as in part (a).



4. Consider the CDS circuit shown below. Assume that the output is sampled at the end of ϕ_2. Parameters: $f_{clk} = 10\text{MHz}, T_{\phi 1} = T_{\phi 2} = \frac{T_{clk}}{2}$, $C_s = C_L = 2\text{pF}$, $C_f = 1\text{pF}$, $G_m = 1\text{mS}$, $\gamma = 1$, $\alpha = 3$ (noise parameters of the OTA). $C_{in} = 0$ (OTA input capacitance). Assume infinite DC voltage gain for the OTA unless otherwise stated.

   a) What is the voltage gain from V_i to V_o?
   b) Assuming $V_{OS} = 10\text{mV}$, what is the input referred residual offset at ϕ_2? Assume that the OTA has a DC voltage gain of 100 and infinite bandwidth for this part.
   c) Suppose V_{OS} contains a slow drift component modeled as a 1-Hz sinusoid with amplitude of 1mV. What is the input referred amplitude of this drift (assuming infinite OTA gain)?
   d) Calculate the noise charge at node V_x during ϕ_1. Ignore the noise from the switches and consider only the thermal noise of the OTA.
   e) Calculate the thermal noise contributed to V_o during ϕ_2. Again, ignore the noise from the switches and consider only the thermal noise of the OTA.
   f) Calculate the total thermal noise contained in the output samples. Explain why the CDS operation of the circuit plays no role in this calculation.

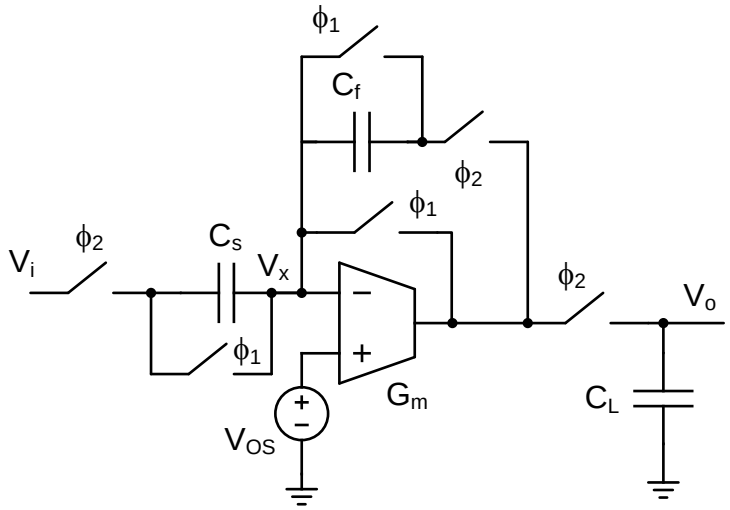


5. Considering the same CDS circuit, we will now run some simulations.
   a) First we want to validate the noise analysis results from the previous problem in Cadence. For that purpose, copy the starter schematic "hw4_cds_starter" along with the provided simulation state into your working directory.

      1. Run the NOISE analysis in ϕ_1 to find the total integrated noise charge at V_x. This is done via an auxiliary circuit that translates voltages into charge (mode q_x). To do this, set the parameter t0_phase to 1; this puts the circuit into phase 1 during the noise analysis. At which frequency does the noise integral reach 98% of its final value?
      2. Repeat part (i) with the switch noise turned off (set the parameter "swnoise = 0"). By how many percent does the noise charge drop? This number is expected to be small, since the switches in the circuit are sized to be roughly "10x faster" than the OTA time constant.
      3. Run the NOISE analysis in ϕ_2 to find the total integrated noise voltage at V_o. To do this, set the parameter t0_phase to 2; this puts the circuit into phase 2 during the noise analysis. Also, click on the noise analysis itself to change the node at which the noise is measured from q_x to v_o.
      4. Combine the results from (i) and (iii) to compute the total output noise. What is the difference (in %) relative to your hand calculation from problem 2?

   b) Now we will simulate flicker noise reduction from CDS. Since this occurs due to correlation between noise during the two clock phases, we need to use pnoise to see this effect. Copy the starter schematic "hw4_cds_flicker" along with the provided simulation states into your working directory. Open the "pnoise" state ("noise" is a copy of the state used in part (a); we won't use it). There are two changes from the previous parts of this problem. First, we have added the ability to disable CDS. Second, we have added a flicker noise source to the OTA.

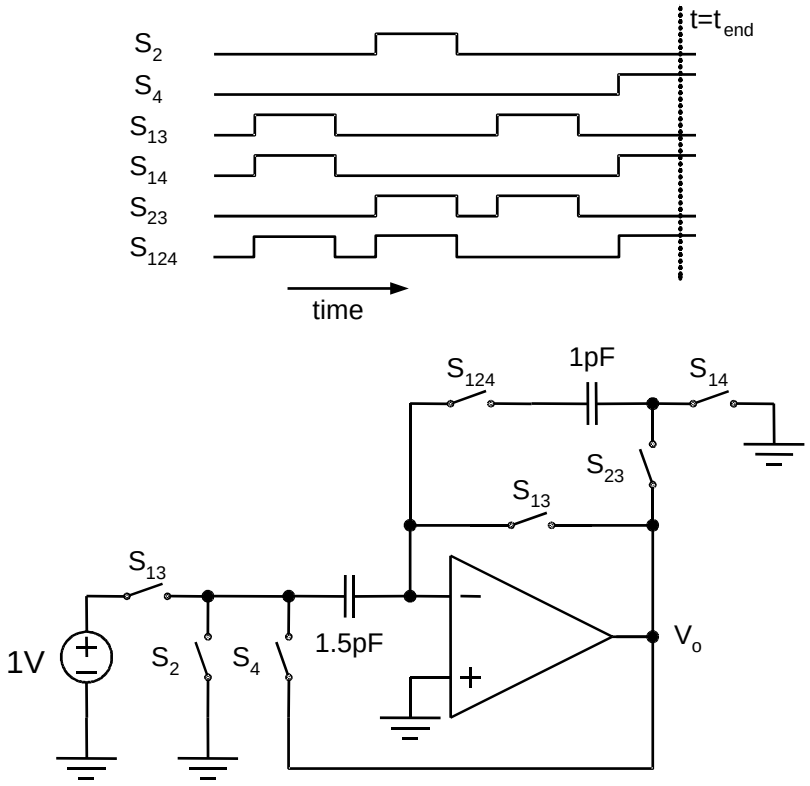
      With CDS enabled, in ϕ_1 the capacitors are grounded on one side and they sample the low-frequency noise (or offset) so that it can be rejected. With CDS disabled, in ϕ_1 the capacitor plates are shorted as seen in the schematic below. (Careful observers may notice that two switches could be removed – one a short and one an open – without changing the circuit's operation. We will ignore that for now.)



1. Make sure the parameters are set to flicker_on=0 and cds_en=1, and run the pnoise simulation. To confirm that your simulation makes sense, compare the total integrated noise to what you found in part (a)(iv). What is the % difference? Also, look at the PSD and notice that there is no flicker noise.
2. Now set flicker_on=1 and keep cds_en=1 and run the simulation again. Do you see any flicker noise yet?
3. Now keep flicker_on=1 and set cds_en=0 to turn off the CDS action. Hand in a plot of Vo from this simulation on top of Vo from the part (ii) simulation.
4. You probably noticed two things in the previous plot: CDS removes the flicker noise and it has higher thermal noise. You can run a simulation with flicker_on=0 and cds_en=0 to confirm that CDS off has lower thermal noise (it does). Can you explain why this is the case?

   Hint: Go through hand analysis for ϕ_1 noise charge at node Vx with CDS disabled and compare to your part 2d answer. No need to work through the algebra beyond this because ϕ_2 noise is unchanged.

6. In the courses notes we have seen simple circuit examples where charge conservation is used to compute the gain of a circuit. You will now look the "slightly" more complex example below, which will allow you to practice the important skill of keeping track of clock phases and charges in an SC circuit. In the circuit below, calculate the output voltage (V_o) at $t=t_{end}$. Assume that the amplifier has infinite gain and that all switches are ideal. Assume that all clock phases are long enough so that all transients settle completely. You may find it useful to redraw the circuit in its various phases. Does the result surprise you? (It should…).


t=t_end
S2
S4
S13
S14
S23
S124
time
S124
1pF
S14
S23
S13
S13
1V
S2
S4
1.5pF
Vo