6) d)

i) SDR = 85.4 dB

ii) SDR = 88.6 dB

maxstep is the maximum timestep that the simulator solver will take when computing the node states of the circuit.

iii) SDR = 60.2 dB

iv) SDR = 67.7 dB with ideal switches for Φ_{1e} and ϕ_2

The effect is strong but it does not dominate.

v) SDR = -1.11 dB - this doesnt make sense I think I messed something up.