Virtuoso Tutorial

This document provides a tutorial on how to use the Cadence Virtuoso tool suite for simulating circuits in EE315. In the first step, you will open an existing circuit from the EE315 library to test drive the entire system. As a second step, you will enter a small circuit and learn how to set up your own simulation.

At this point, we assume that you are sitting in front of a properly configured graphics interface, which could be either a terminal in an on-campus computer lab or your home PC configured for remote access (see handout “remote connection”). We have tested the software on the “corn” computer cluster.

Preparation

All new FarmShare accounts use the bash shell by default, but for this class you must use tcsh. Each time you log on, you should type “tcsh” to switch to the correct shell. Alternatively, you can contact FarmShare support to have your default shell changed to tcsh. See the following webpage for details: https://web.stanford.edu/group/farmshare/cgi-bin/wiki/index.php/FAQ

If you haven't done this already, do:

```
source /usr/class/ee315/DOT.cshrc
```

Decide on your working directory for EE315. By default, it's "~/ee315" (defined by the variable $EE315_WORKDIR in /usr/class/ee315/DOT.cshrc). If you don't like it, you can override it by:

```
setenv EE315_WORKDIR <your_EE315_DIR>
```

It's best if you include the source statement and the definition for EE315_WORKDIR in your ~/.cshrc file. Otherwise, you'll have to type these commands every time. If the directory doesn't exist already, create it:

```
mkdir -p $EE315_WORKDIR
```

Now setup the Virtuoso directory (opus is the old name for Virtuoso)

```
mkdir -p $EE315_WORKDIR/opus
cp $EE315_HOME/opus/cds.lib $EE315_WORKDIR/opus/
ln -s $EE315_HOME/opus/DOT.cdsinit $EE315_WORKDIR/opus/.cdsinit
ln -s $EE315_HOME/opus/DOT.cdsplotinit $EE315_WORKDIR/opus/.cdsplotinit
```

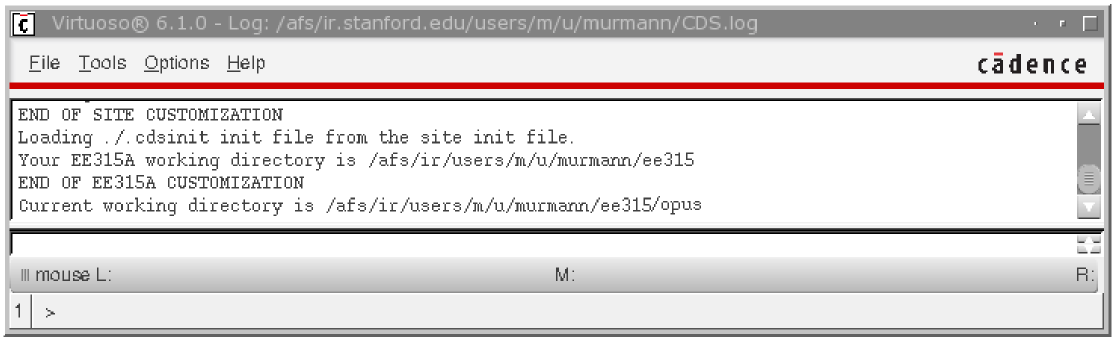
To start a virtuoso session:

```
cd $EE315_WORKDIR/opus
virtuoso &
```

Note: directories under EE315_WORKDIR:
opus: virtuoso library directory
simulation: virtuoso ADE directory (created automatically when you run your first simulation)

You will have to follow the steps outlined above only once. Afterwards, you will always begin by simply launching the “virtuoso &” command from the opus folder in your working directory ($EE315_WORKDIR/opus). An important tip: In order to prevent the VNC connection to time out, it typically helps to leave the “top” command running at an xterm prompt inside your VNC window and also in the secure CRT session from which you executed the vncserver command.

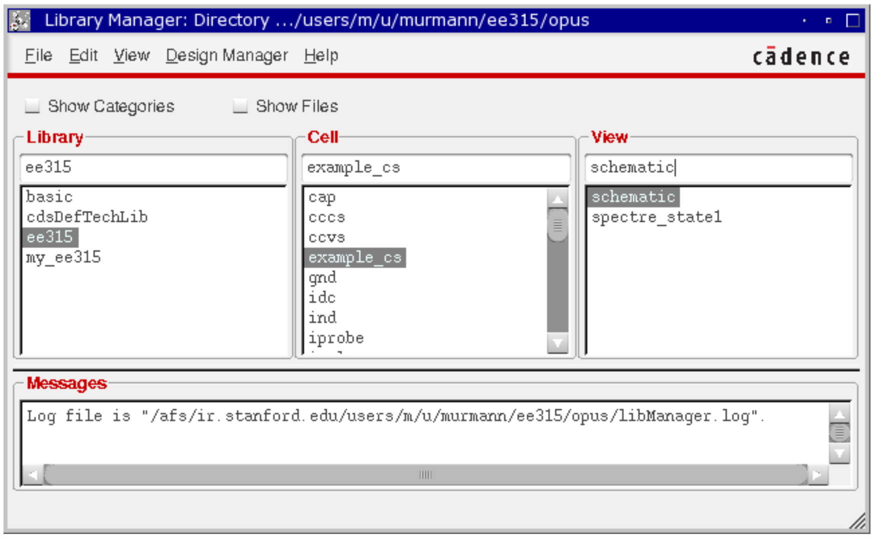
Assuming that you have completed the setup and launched virtuoso, you should now see the following window on your screen:


Virtuoso® 6.1.0 - Log: /afs/ir.stanford.edu/users/m/u/murmann/CDS.log
File Tools Options Help
cadence
mouse L:
M:
R:
1 >

```
END OF SITE CUSTOMIZATION
Loading ./.cdsinit init file from the site init file.
Your EE315A working directory is /afs/ir/users/m/u/murmann/ee315
END OF EE315A CUSTOMIZATION
Current working directory is /afs/ir/users/m/u/murmann/ee315/opus
```

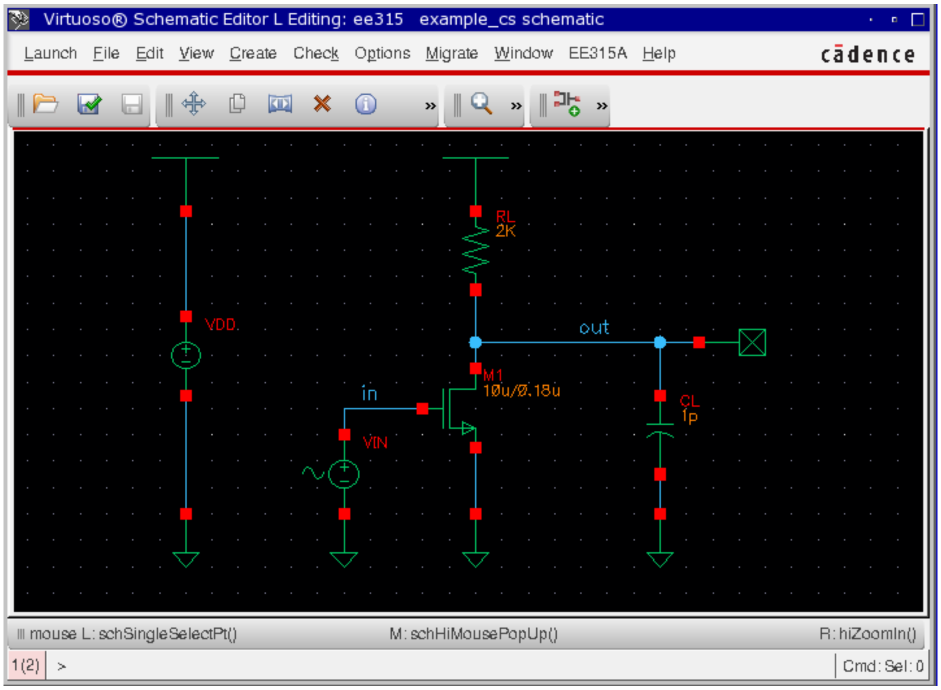
Part I: Opening an Existing Design

1. Click Tool → Library Manager. The library manager window will appear.

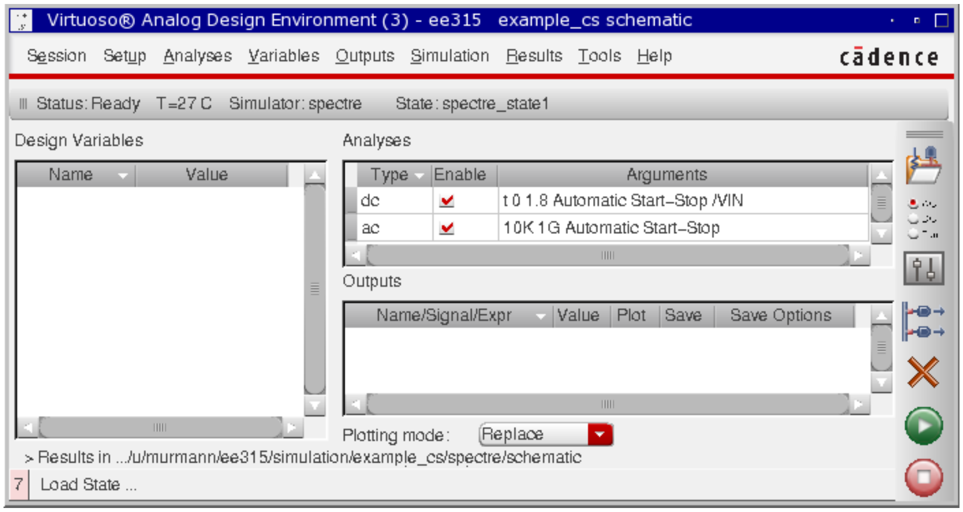


```
Log file is "/afs/ir.stanford.edu/users/m/u/murmann/ee315/opus/libManager.log".
```

In this window, the left column is a list of the available libraries. The ee315 library contains all the components that we will use for this class. Any library that you will create later on will also appear in this list (e.g. my_ee315). Left-click the ee315 library and the cell “example_cs” in the middle column. In the right column you will now see the various “views” of this cell. Double-click the “schematic” view and confirm that you will open the cell “read only”. A schematic window showing a common source amplifier will appear as shown below. **Note:** At this point you may receive a licensing error message and may be asked if you want to try to get a higher tiered license, click ‘always.’


Virtuoso® Schematic Editor L Editing: ee315 example_cs schematic
Launch File Edit View Create Check Options Migrate Window EE315A Help
cādence
RL
2K
VDD
out
M1
10u/0.18u
in
CL
1p
VIN
mouse L: schSingleSelectPt()
M: schHiMousePopUp()
R: hiZoomIn()
1(2)
>
Cmd: Sel: 0

2. Click Launch → ADE L. The Analog Design Environment window will now appear (click 'always' if you receive a licensing message). In this window, click Session → Load State. In the pop-up window that now appears, click "Cellview" (near the top) and select "spectre_state1" from the State dropdown menu. Click OK to confirm. The ADE window should now look as follows:


Virtuoso® Analog Design Environment (3) - ee315 example_cs schematic
Session Setup Analyses Variables Outputs Simulation Results Tools Help
cādence
Design Variables
Name
Value
Analyses
Outputs
Plotting mode:

Status: Ready T=27 C Simulator: spectre State: spectre_state1

Type	Enable	Arguments
dc	✓	t 0 1.8 Automatic Start-Stop /VIN
ac	✓	10K 1G Automatic Start-Stop

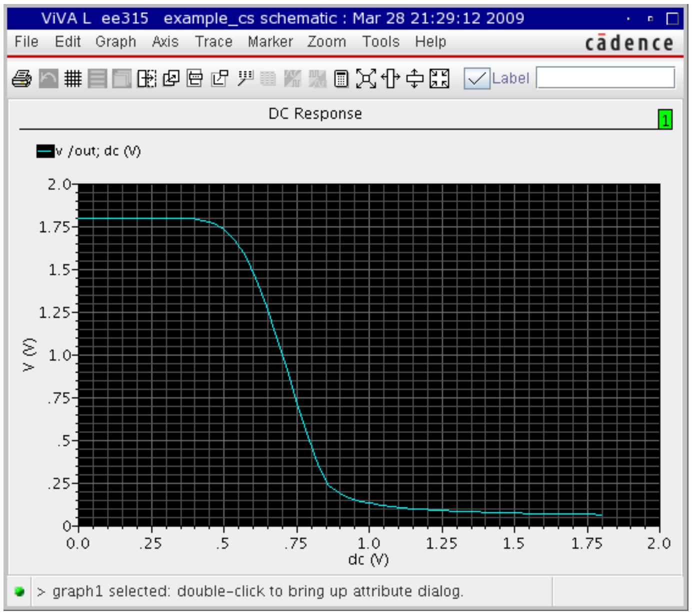
Name/Signal/Expr	Value	Plot	Save	Save Options

Plotting mode: Replace

```
> Results in .../u/murmann/ee315/simulation/example_cs/spectre/schematic
7  Load State ...
```

3. Press the green "play" button – this will start a set of simulations. When complete, you should see the message "Ready" reappear in the Status field of the main Virtuoso window. In order to display the circuit's operating point, click Result → Annotate → DC Node Voltages and Result → Annotate → DC Operating Points. The schematic in the editor window will now have annotations for all node voltages, element currents and g_m, and g_m/I_D of the MOSFET.

4. Click Results → Direct Plot → Main Form. Select "dc" and "Voltage" and subsequently click on the "out" net in the schematic window (note that the bottom of the direct form prompts you to ">Select net on schematic…"). You should now see a plot of the circuit's dc transfer characteristic:


ViVA L ee315 example_cs schematic : Mar 28 21:29:12 2009

> graph1 selected: double-click to bring up attribute dialog.

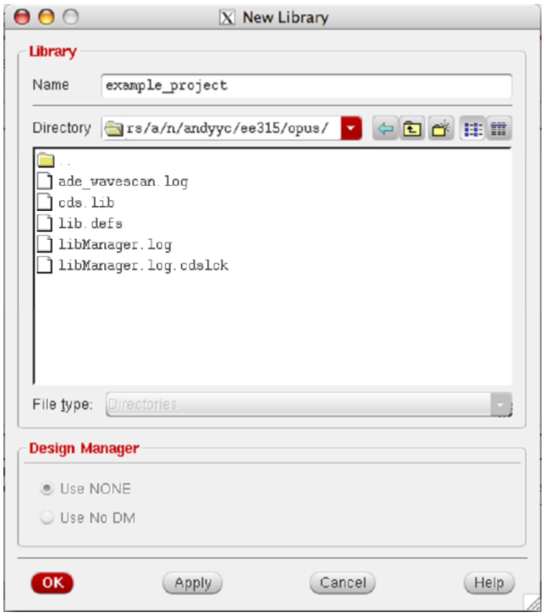
5. In the direct plot form, select “ac”, “Voltage”, and “dB20” and again click on the ‘out’ net in the schematic window. You should now see a plot of the circuit’s ac response.

Part II: Entering and Simulating a New Design

Now that you have a basic feel for the functionality of our tools, we will guide you to create your own schematic and simulation setup. For simplicity, we will focus on the ac simulation of a simple RC circuit. Along the way, feel free to explore the environment by clicking through the various related menus, etc.

Creating a new library

To create your own schematics, the first step is to create a new library that will hold them. In the Library Manager click: **File -> New-> Library**. A dialog box should appear and you should fill the appropriate boxes as shown in the picture below.


New Library

Library

Name: example_project

Directory: rs/a/n/andyyc/ee315/opus/

```
..
ade_wavescan.log
cds.lib
lib.defs
libManager.log
libManager.log.cdslck
```

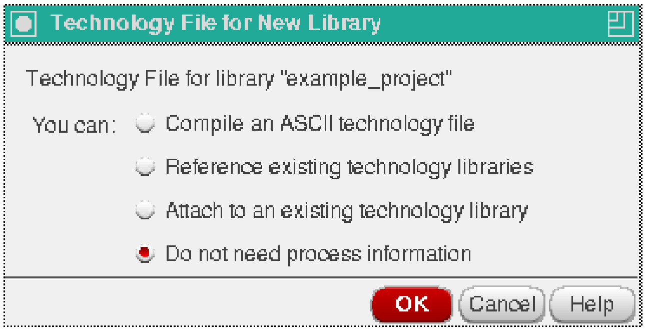
File type: Directories

Design Manager

● Use NONE
○ Use No DM

You can choose any name for the library. In this case we have chosen **example_project** for the library name. Cadence will automatically create a subdirectory named **example_project**. Press the **OK** button.

Next you will see the "**Technology File for New Library**" window. This window allows you to specify the technology you will use for your IC design. Since many of us will be using Virtuoso just to draw schematics and run simulations, we need not add a technology file for the library (it's required if you draw layouts). So as shown below, click on the **"Do not need process information"** and click **OK.**



Technology File for New Library

Technology File for library "example_project"

You can: ○ Compile an ASCII technology file

○ Reference existing technology libraries

○ Attach to an existing technology library

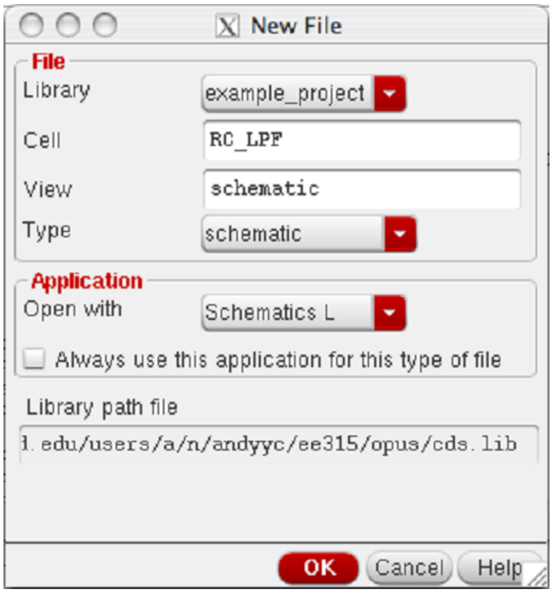
● Do not need process information

A new library named **project** has been created in the directory that was specified above. This step is performed only once. In this library, new cells will be designed such as RC_LPF (see below).

Creating a new schematic: RC Low Pass Filter

In the Library Manager, Click: **File -> New -> Cell View**

The 'New file' form should appear as shown below. We will be making an RC low pass filter, so type **RC_LPF** in the 'Cell' block. In the 'View' block type schematic or from the 'Type' pull-down menu choose *schematic* and the 'View' block will be automatically filled. In the *Application* section, select the following: Open with: *Schematic L* and check the box next to *Always use this application for this type of file*. Once you make these two selections, in the future they will be automatically selected.



New File

File

Library: example_project

Cell: RC_LPF

View: schematic

Type: schematic

Application

Open with: Schematics L

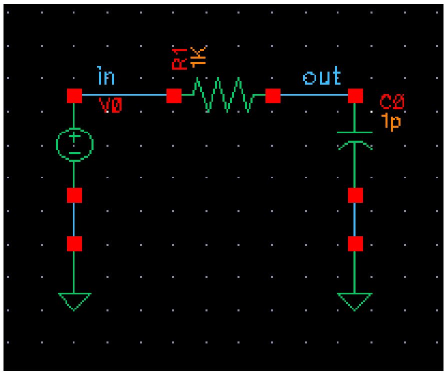
□ Always use this application for this type of file

Library path file

l.edu/users/a/n/andyyc/ee315/opus/cds.lib

Left click the **OK** button. The Virtuoso-Schematic Editing window should now open on your screen.

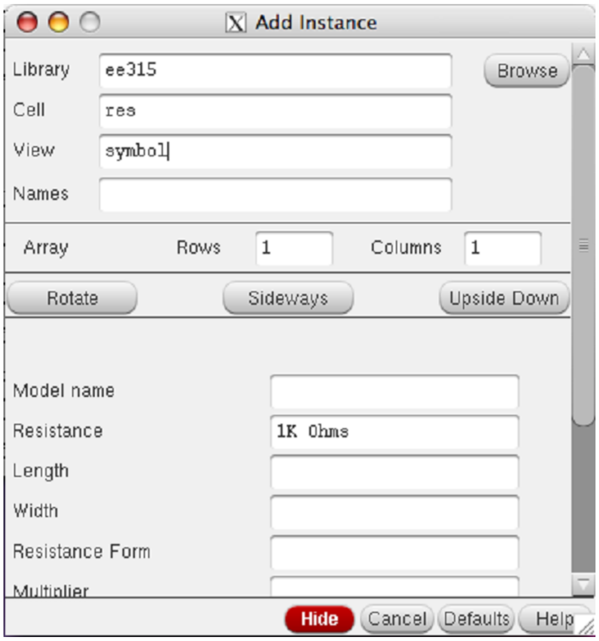
The circuit that we create will look like this:



Left click in the window: **Create -> Instance...**

Shortcuts: You may notice letters by some of these menu choices. Rather than clicking through all the menus, you can just hit that button on the keyboard to the same effect. These are called hot-keys. In the future, you can press **i** in order to insert an instance.

A Command Browser window appears. We will first lay a resistor. In this window, type **ee315** in the 'Library' block and **res** in the 'Cell' block and hit the tab key. The window should now look as shown in the figure below.



Library	ee315
Cell	res
View	symbol
Names	
Array Rows	1
Columns	1
Model name	
Resistance	1K Ohms
Length	
Width	
Resistance Form	
Multiplier	

Note that you can use the 'Browse' button in order to browse through the libraries and find the cell you want. You can edit the parameters of the **res** cell, such as resistance, width, length, etc. For this exercise, keep the default parameters (1 kOhms).

Move the cursor into the editing window. Notice that there is a resistor instead of the normal cursor. Position it where you want to put the resistor, and left click to place it. You can press 'r' to rotate the resistor if you want it to face a different direction (this is especially useful with pins). Press <Esc> to return to a normal cursor after you have finished placing the resistor.

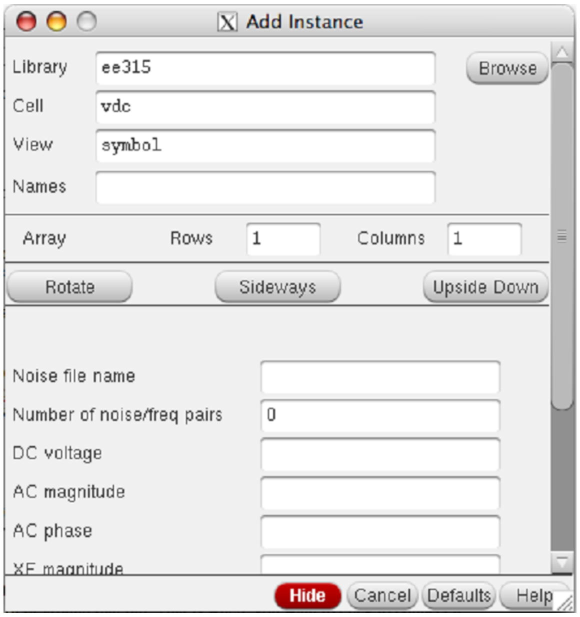
Click **Create -> Instance**

Follow the same steps as before, but choose a **capacitor (cap)**. Use the default values for its capacitance.

Before trying to place a component, you can left click the **Hide** button on the Add Component window. This will move it into the background so it's out of your way.

Repeat the same procedure as above and add the **gnd** pin. Place the **gnd** symbol below the capacitor.

To add the voltage source select the **vdc** cell. In the library, you will see many types of voltage sources, iie.g. vpulse, vpwl, vsin. They each have different purposes and will be used for different types of simulations. For now, leave the default settings for the vdc instance; we will modify this later.


Add Instance

Library: ee315
Cell: vdc
View: symbol
Names:

Array Rows: 1 Columns: 1

Noise file name:
Number of noise/freq pairs: 0
DC voltage:
AC magnitude:
AC phase:
XF magnitude:

Now, we'll add all the wires to connect the various components. Click **Create -> Wire**. The shortcut is '**w**'. You can refer to the figure above to see how everything is connected together.

Notice that as you get closer to one pin than another (including those on devices), a small diamond will show up inside of or around that pin. That is where you want to click to connect a wire. For the first wire, left click on the positive terminal of the voltage source and connect it to one end of the resistor.

If you put a wire where you don't want it to go, you can delete the wire by left clicking **Edit -> Delete** (shortcut is '**del**') and then left click on the object you want to delete (wire, pin, component, etc).

The lower left portion of the schematic entry window tells you what command mode you're in (e.g. "Point at object to delete" if you are in the delete mode). You can quit the current command mode by pressing the escape key.

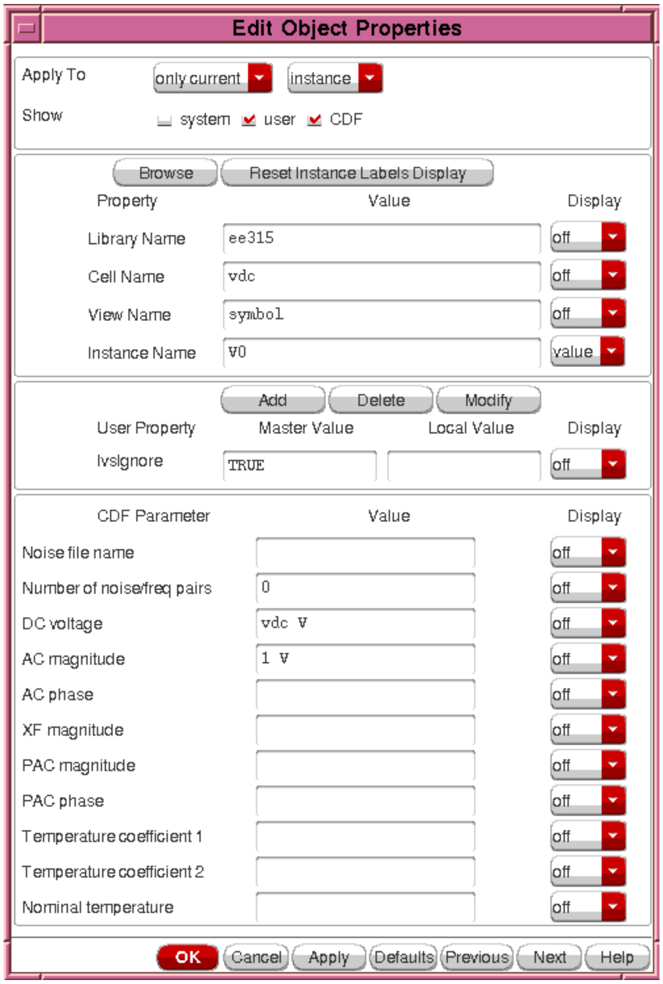
We can label the wires by selecting **Create -> Wire Name**, or pressing **l**. Label the wire above the voltage source **in** and the wire above the capacitor **out**.

Once you are done editing, left click **File -> Check and Save**. This will check your work for connection errors and will save your work in the library.

After making all the connections, the schematic should look similar to the one shown above.

Running an AC simulation: RC Low Pass Filter

First, we need to setup our voltage source from before. Select the voltage source and go to **Edit -> Properties -> Objects**, or use the shortcut '**q**'. Let's modify the voltage source so that its DC voltage is a design variable, vdc, we will define this later. The DC voltage will set the circuit's operating point. Let's arbitrarily make the AC voltage 1 V, as usual.



Edit Object Properties

Apply To: only current, instance

Show: □ system ☑ user ☑ CDF

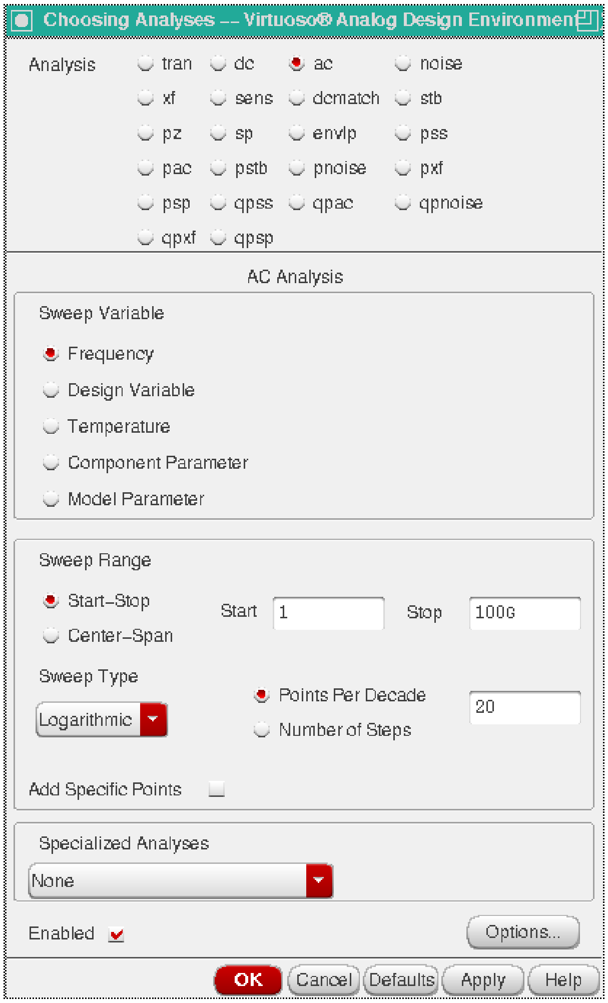
Property	Value	Display
Library Name	ee315	off
Cell Name	vdc	off
View Name	symbol	off
Instance Name	V0	value

User Property	Master Value	Local Value	Display
lvsIgnore	TRUE		off

CDF Parameter	Value	Display
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage	vdc V	off
AC magnitude	1 V	off
AC phase		off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off

Like before, we will want to launch the Analog Design Environment (Launch -> ADE L). The session menu has options that allow you to save and load states. Saving your state allows you to save your simulations so that you don't have to set them up each time you open ADE. The Setup menu selects the circuit you are simulating, the type of simulator, the model libraries, and environment related variables. This is already setup for you.

To run an AC simulation, select Analyses->Choose and select the AC button. We will want to sweep frequency from 1Hz to 100GHz, so enter that into the Sweep Range as shown below. For the Sweep Type, automatic will work, but we can specify points manually by selecting Logarithmic and 20 points per decade. Click OK. **Note:** The AC simulation will sweep the frequency of all voltage sources in your circuit.



Analysis ○ tran ○ dc ● ac ○ noise ○ xf ○ sens ○ dcmatch ○ stb ○ pz ○ sp ○ envlp ○ pss ○ pac ○ pstb ○ pnoise ○ pxf ○ psp ○ qpss ○ qpac ○ qpnoise ○ qpxf ○ qpsp

AC Analysis

Sweep Variable

● Frequency
○ Design Variable
○ Temperature
○ Component Parameter
○ Model Parameter

Sweep Range

● Start-Stop Start 1 Stop 100G
○ Center-Span

Sweep Type

Logarithmic

● Points Per Decade 20
○ Number of Steps

Add Specific Points □

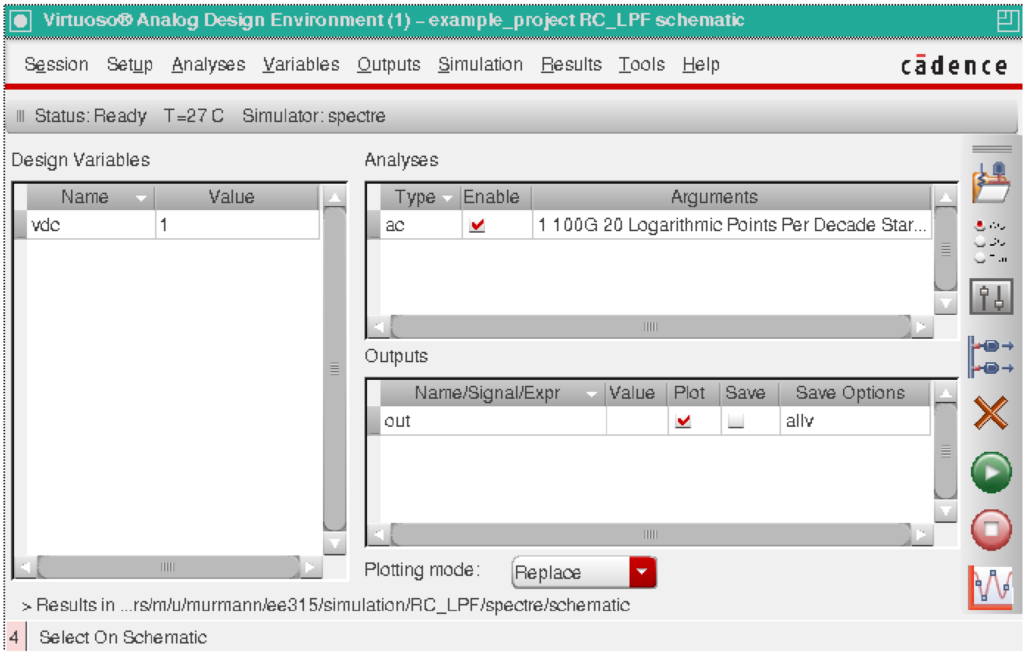
Specialized Analyses

None

Enabled ☑

Since we used a variable for our DC voltage, we will need to define it now. Select **Variables -> Copy from Cell View**. You should see vdc appear in the Design Variables window. Double click on vdc and enter **1** for its value and click OK. Design variables are useful because you can sweep these variables when you are running a simulation. For example, in the AC simulation above, we can sweep a design variable rather than frequency. We won't be sweeping the vdc variable in this simulation though.

To select an output to plot, go to **Outputs -> To Be Plotted -> Select on Schematic**, and click on the wire labeled **out** and then hit Escape to stop selecting nodes. Your ADE window should look like this:


Virtuoso® Analog Design Environment (1) - example_project RC_LPF schematic

Status: Ready T=27 C Simulator: spectre

Design Variables

Name	Value
vdc	1

Analyses

Type	Enable	Arguments
ac	✓	1 100G 20 Logarithmic Points Per Decade Star...

Outputs

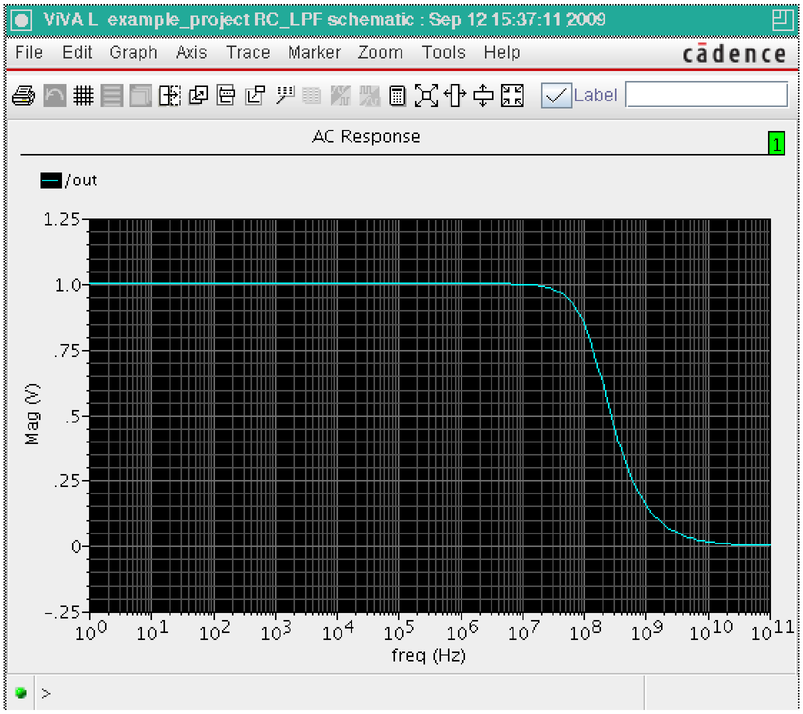
Name/Signal/Expr	Value	Plot	Save	Save Options
out		✓	□	allv

Plotting mode: Replace

> Results in ...rs/m/u/murmann/ee315/simulation/RC_LPF/spectre/schematic

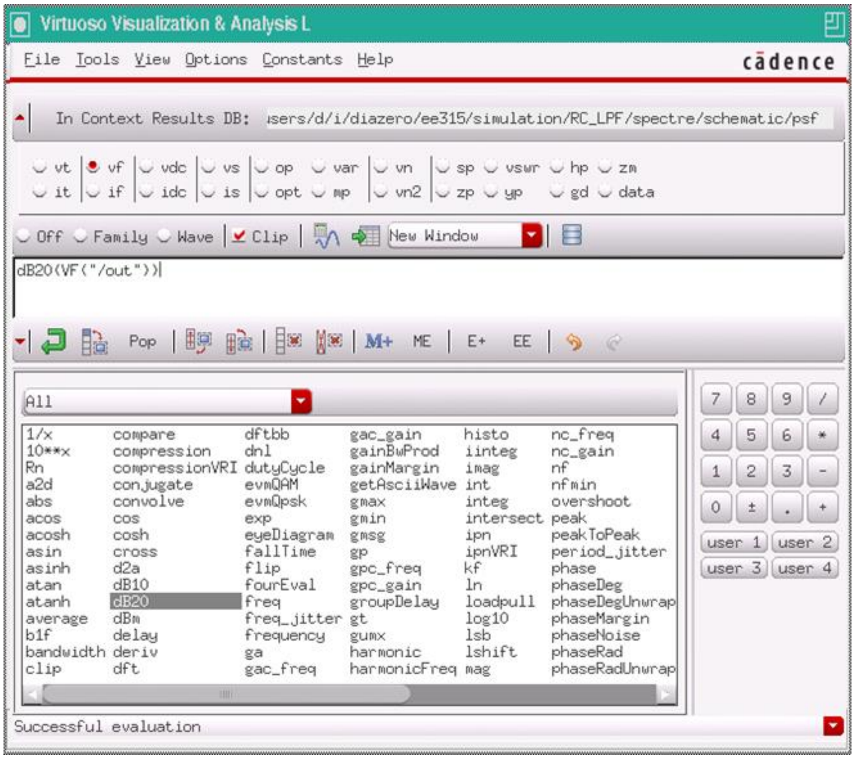
4 Select On Schematic

Run the simulation by clicking the green button on the right (Netlist and Run). You should get a plot of the AC voltage at the output like the one below.



What if you wanted to plot the y-axis in dB? Click the calculator icon in the toolbar of the waveform editor. The calculator works like some HP calculators because it uses a stack. This means you first input the operands (waveforms) and then select the operation you want to perform on them.

Click the vf button. Then select the wire labeled **out**, so that **VF("/out")** appears in the buffer for your calculator. In the window on the below, there are many built in functions. Change the category to "All" and select db20. Your calculator should look something like this:



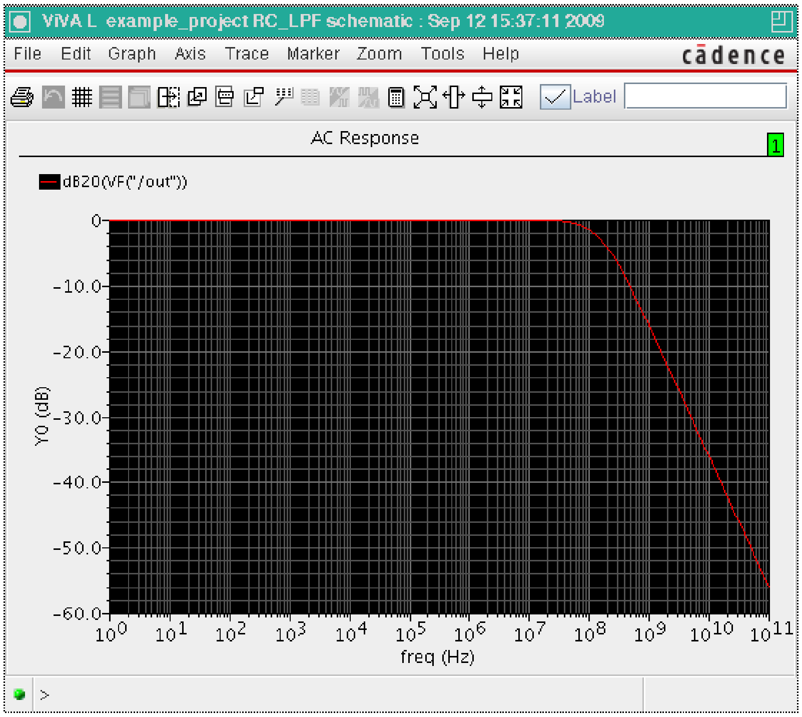
In Context Results DB: users/d/i/diazero/ee315/simulation/RC_LPF/spectre/schematic/psf

```
dB20(VF("/out"))
```

Successful evaluation

Virtuoso Visualization & Analysis L
File Tools View Options Constants Help
cādence
vt vf vdc vs op var vn sp vswr hp zm
it if idc is opt mp vn2 zp yp gd data
Off Family Wave Clip
New Window
Pop M+ ME E+ EE
All
1/x 10**x Rn a2d abs acos acosh asin asinh atan atanh average b1f bandwidth clip
compare compression compressionVRI conjugate convolve cos cosh cross d2a dB10 dB20 dBm delay deriv dft
dftbb dnl dutyCycle evmQAM evmQpsk exp eyeDiagram fallTime flip fourEval freq freq_jitter frequency ga gac_freq
gac_gain gainBwProd gainMargin getAsciiWave gmax gmin gmsg gp gpc_freq gpc_gain groupDelay gt gumx harmonic harmonicFreq
histo integ imag int integ intersect ipn ipnVRI kf ln loadpull log10 lsb lshift mag
nc_freq nc_gain nf nfmin overshoot peak peakToPeak period_jitter phase phaseDeg phaseDegUnwrap phaseMargin phaseNoise phaseRad phaseRadUnwrap
7 8 9 /
4 5 6 *
1 2 3 -
0 ± . +
user 1 user 2
user 3 user 4

Change the drop down menu from Append to New Win and click the plot icon. Your final plot should look like the one below.



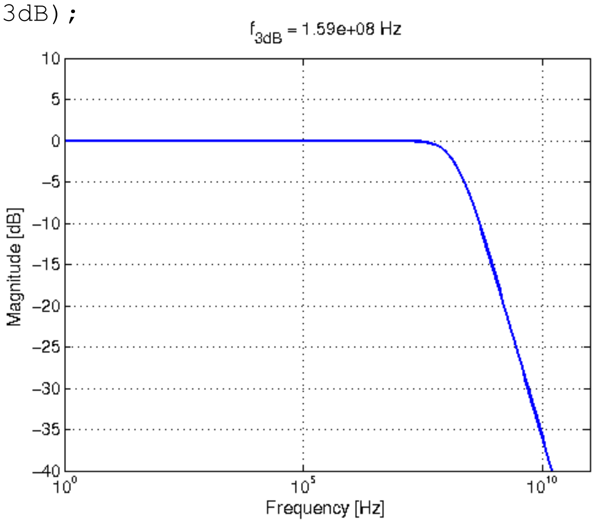
Part 3: Plotting Results in Matlab

Even though the Virtuoso tool suite provides many options for plotting and post-processing of simulation data, it is sometimes convenient to export the data to Matlab. Below is an example Matlab script that shows how the AC simulation data from the above RC filter example data can be accessed and plotted.

```
clear all;
% read simulation result (AC simulation, signal 'out')
s = cds_srr('../simulation/RC_LPF/spectre/schematic/psf','ac-ac','out')
f = s.freq;
mag = 20*log10(abs(s.V));

% find 3-dB frequency
idx = find(f > 1e7);
f3dB = interp1(mag(idx), f(idx), mag(1)-3)
str = sprintf('f_3_d_B = %2.2d Hz', f3dB);

% plot magnitude versus frequency
figure(1)
semilogx(f, mag, 'linewidth', 2);
title(str);
set(gca, 'fontsize', 14);
xlabel('Frequency [Hz]');
ylabel('Magnitude [dB]');
axis([min(f) max(f) -40 10]);
grid;
```



In this example, simulation data is accessed via the cds_srr function provided in the SpectreRF MATLAB Toolbox. The function has up to three inputs: directory, dataset, and signal. Depending on the number of inputs, the cds_srr function can perform three different functions:

- cds_srr(directory) will print out the available simulation results within that folder. Following the same example from above, if you call cds_srr('../simulation/RC_LPF/spectre/schematic/psf') you will see that there are 8 datasets available.
- cds_srr(directory,dataset) will show available signals. In the above example, you will see that the input and output voltages as well as the current through the voltage source are available.
- cds_srr(directory,dataset,signal) returns the requested data in a struct. In the example above, it contains frequency and voltage vectors.

You can look also view these datasets and signals via Tools → Results Browser in ADE L. The (directory,dataset) function does not always show all available signals, in which case you'll need to check the Results Browser for signal names. For more info on the Matlab interface, consult the SpectreRF MATLAB Toolbox Documentation on the course website under CAD.

Unrelated note: The default keyboard shortcuts in Matlab are different on Linux compared to Windows. If you'd like, you can go to Preferences -> Keyboard -> Shortcuts and choose "Windows Default Set"