HOMEWORK #3

(Due: Thursday, October 19, 2017, 11:59 pm PT via Gradescope Online Submission)

1. **Quick Questions.** For each of the following statements, state "T" for true or "F" for false. No explanation necessary. Correct answers are worth +1 point, while incorrect answers yield -1 point. No points for unanswered questions. Your minimum total score on this problem is zero points.

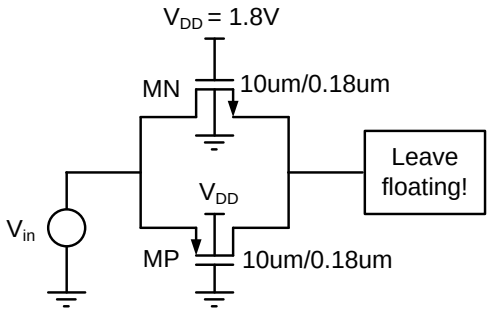
a) Under idealized slow-gating conditions, a MOS sampling switch does not inject any channel charge during turn-off.	
b) Bottom plate sampling reduces the impact of clock jitter in sampled data circuits.	
c) Practical sampling circuits can typically achieve a jitter performance better than 1fsrms.	

2. **Spectral performance metrics.** Download the file hw3_adc_out.mat. It contains the output of an ADC with a sampling frequency f_s = 100 MS/s. The input was a full-scale sinusoidal signal. The ADC has a 10 bit mid-rise quantizer whose full scale range is [-1, +1].
   a) Plot the spectrum from 0 to $f_s/2$. The y axis should be in dBFS while the x axis should be scaled in MHz.
   b) What was the frequency of the sinusoidal signal at the input of the ADC, f_{in}?
   c) Compute the following metrics (using Matlab): SNR, SNDR, ENOB, THD, and SFDR. Please do not use the built-in Matlab functions, and instead write the few lines of code yourself.
   d) Which nonideality determines the SFDR in this measurement?
   e) Estimate the standard deviation of the thermal noise, normalized to the (known) standard deviation of the quantization noise.

3. **Switch on resistance**. Shown below is the schematic of a CMOS sampling switch in its "ON" state.
   a) Run a DC sweep in Cadence to plot the on-resistance of MN, MP, and MN||MP as a function of V_{in} in one diagram. Sweep V_{in} from 0 to V_{DD} and scale your Y-axis to a maximum of 1kΩ. Use your simulation results to complete the table below the schematic diagram. Note: The node indicated as **"Leave floating!"** should be left floating as stated; in particular, it should not be connected to ground!
   b) Using the data from part a, find the optimum width ratio $k = W_P/W_N$ that minimizes the relative on-resistance variation in the range of $V_{IN} = 0 \ldots V_{DD}$.
   c) Consider a case where this switch drives a capacitance of C = 1 pF. Size the switch such that the circuit transients are guaranteed to settle to within 0.1% in one half clock cycle at 100 MHz clock frequency. For this calculation, assume the worst case on-resistance near the center of the input voltage range. No need to simulate this, just turn in your hand calculation.

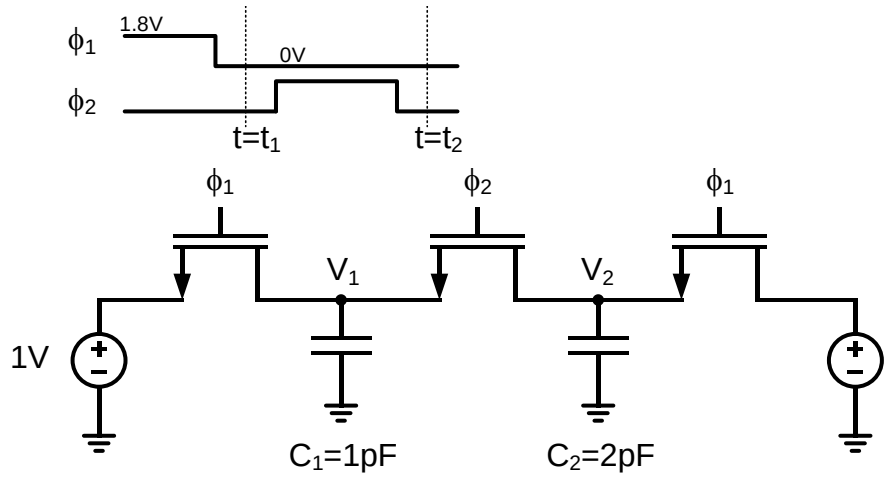
Cadence Tips:

- Use devices 'nmos' and 'pmos4' from the ee315 library. Make sure the devices are named MN and MP, respectively (instance name in device properties).
- Copy the file "hw3_save_op.scs" file from /usr/class/ee315/opus to your local opus directory. Before running the DC sweep simulation, add this file as a model library by going to "*Setup → Model Libraries → add model file*" in ADE L (Analog Design Environment). When this file is added as model library, Cadence will save the DC simulation output for MN and MP for each value of V_{in}.
- If you want to plot the data in Matlab, here is an example for reading in $r_{on}=1/g_{ds}$ of the NMOS transistor (here the cell name is chosen to be hw3_q2):
  Gds=cds_srr('../simulation/hw3_q2/spectre/schematic/psf','dc-dc','MN:gds')
  Ron = 1./Gds.S



r_{on}(MN) @ V_{in}=0V	
r_{on}(MN||MP) @ V_{in}=0V	
r_{on}(MP) @ V_{in}=V_{DD}	
r_{on}(MN||MP) @ V_{in}=V_{DD}	
Maximum r_{on}(MN||MP) within V_{in}=0…V_{DD}	

4. **Switch nonidealities.** In the circuit below, all switches are identical NMOS devices with W=10µm, L=0.2µm, C_{ox}=10fF/µm^2, V_t=0.4V, C_{ol}=0.1fF/µm. Ignore settling dynamics time in this problem (assume that the clock period is much longer than the settling time for each transition) and assume fast gating.



a) Calculate the standard deviation of V_1 at times t_1 and t_2. Express your answer in µVrms.
b) Calculate the value of V_1 at time t_1, taking only charge injection into account (neglect clock feed-through).
c) Calculate the value of V_1 at time t_1, taking only clock feed-through into account.

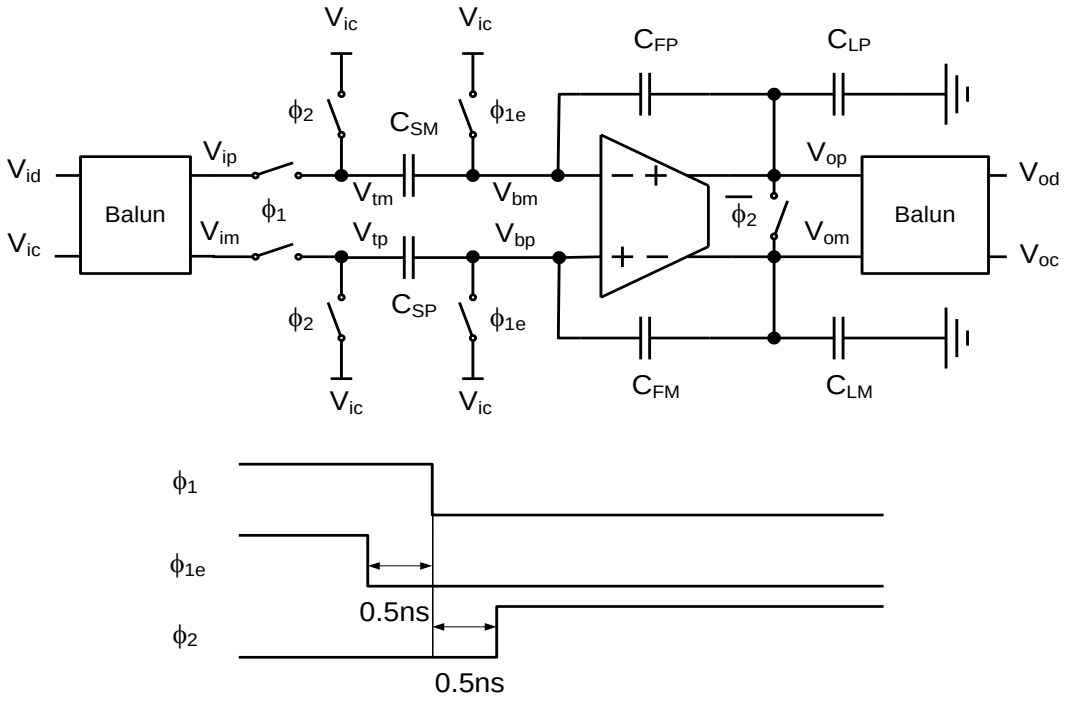
5. **SpectreRF warm-up.**

   You should now be familiar with the Cadence Virtuoso software. In this problem, you will use some of the more advanced SpectreRF simulator modes which we will make use of in this course. Work through the "SpectreRF Tutorial" handout available on the course website under "CAD". For N=4.6, what is the gain for a 400 MHz input signal in dB assuming 1 GHz sampling?

   Hint: You can get this from a plot similar to Figure 5 from the handout. You may want to use Marker → Place → Trace Marker, click anywhere on the trace, then double click on the marker and set the X position to 400M.

6. **Bottom plate sampling T/H circuit**. In this problem, we will study charge injection and distortion effects caused by MOS switches. The fully differential, single-stage OTA used in this problem is implemented using an idealized macro model.

   The circuit schematic: **"switch_cap_ckt"** is in the ee315 cadence library and will be used as a **starter schematic** for the simulations in this problem. Please copy this schematic (with all its views and states) to your working library (which you created in homework 1). The schematic consists of a fully differential OTA ("diff_ota1"), a clock generator ("clock_gen_e"), switches and ideal baluns.



Each of the switches has a fixed on resistance "R_{on}" which has been set to a default value of 10Ω. Ideal baluns are used for differential to single ended conversion and vice-versa.

The given parameters for the simulations are: G_m=1mS, A_{vo}=1e6, g_m/I_D=10S/A, f_T=20GHz, $C_{SP,M}$= $C_{FP,M}$=100fF, $C_{LP,M}$=500fF, V_{ic}=0.6V, V_{oc}=0.9V, V_{DD}=1.8V, α=2, γ =1. These parameter values are already stored/set up for you in the schematic and the provided simulation states.

a) Open the schematic and the simulation state "state_a." Run a transient simulation for the provided circuit and plot the differential output voltage for V_{id} = 10mV. Observe that the differential output settles to a value that is very close to the sampled input. Submit a plot showing ϕ1, ϕ1e, ϕ2, V_{od}.

b) Charge injection

   i. Replace the ideal switches in the starter schematic with 30μm/0.18μm NMOS devices (except for the switch at the OTA output). Use the cell 'switch_nmos' in the ee315 library. Re-run the transient simulation from the previous part of this problem with V_{id}=10mV. Generate a plot that shows the total differential voltage across the sampling capacitors V_{cs}=[V_{tm}-V_{bm}]-[V_{tp}-V_{bp}]) and V_{od}. What is the error of V_{cs} after the falling edge of ϕ1 in mV? Why is the final output voltage close to the ideal value of 10mV despite the large voltage disturbance across the sampling capacitor? Explain briefly.

ii. In a separate diagram, plot the voltage across a single capacitor, e.g. V_{tm}-V_{bm}. Explain the various transients on this waveform.

iii. Estimate (via hand calculation) the charge injection error you expect to see on C_{SM} after the opening of switch ϕ_{1e}. Compare this number with the observed value in simulation.

c) Noise

i. Calculate the output-referred differential sampled noise at the output. What is the total output noise? How much of this comes from the switches versus from the OTA? Express your answer in units of V^2.

For your hand calculations, you can assume that the parasitic source/drain capacitance of each transistor is 80 fF the device is turned on and 40 fF if the device is off, and the input-referred voltage noise of the OTA can be expressed as $\alpha 4kT\gamma/G_m$. The OTA has no input capacitance. You may want to work with a single-ended circuit and then double the noise to get the differential output noise.

ii. Now we will simulate this circuit and compare with our hand calculations. We will use pss/pnoise simulations. For this, you will create a new ADE L state. Copy all of the design variables from 'state_a', but change fs to 50M. For the pss simulation, set the errpreset to conservative and under Options set maxacfreq to 25G. For pnoise, sweep the output to fs/2 (25M) and set maxsidebands to 500. The output is a voltage from /vop to /vom and noisetype is timedomain with a specific point at 9n. You should still be using nmos devices for all of the switches (except the one at the OTA output).

Use the noise summary window (Results → Print → Noise Summary) to see how much each noise source contributes to the total integrated noise. Under "Truncate & Sort", set it to 9 since we want to see the contributions from all 9 noise sources in this circuit. Note that /I0/R0 and /I0/R2 are the OTA noise contributors.

What is the total output-referred noise? How much of this comes from the OTA, and how much comes from the sum of all switches? Compare these to your hand calculations from part I, and account for any disagreement. What could you have changed about your simulation to get a more accurate result?

d) Distortion

For this part we are going to consider the effects of distortion due to nonlinearities, thus we will be measuring the SDR (signal-to-distortion ratio, SDR=1/THD).

i. Run a transient analysis using ideal switches and the state 'state_d1.' This is mainly to "calibrate" the setup and to get a feel for how accurately we can determine distortion in the given circuit and for a differential input amplitude of 0.8V. Copy the file /usr/class/ee315/matlab/sim_fft.m to your working directory. Run this file in Matlab and submit a plot of the spectrum. What is the achieved SDR?

Important note: This is simulation is set up such that the simulator produces only discrete time points every 20ns ("strobeperiod" is set to 20ns). When you plot V_{od} (or any other time domain waveform), you will therefore see only a few discrete time points.

ii. Keeping everything same as the above, change maxstep to 0.01ns (to change this parameter, in the ADE L window, go to analysis→choose→Options). What is the SDR now? What is the purpose of the simulation parameter 'maxstep'? Explain why and how it affects the SDR estimate of the circuit.

iii. Replace the ideal switches in the starter schematic with 30μm/0.18μm NMOS devices (except for the switch at the OTA output) and re-run the analysis. What is the achieved SDR? Submit a plot of the output spectrum.

iv. The poor SDR you see in the previous simulation may come from two effects: (1) Track mode distortion due to nonlinear R_{on}, and (2) signal dependent charge injection from the bottom plate switches due impedance changes in the sampling top plate switches. To see if one of the two effects may dominate, run a simulation with all switches ideal, except for the ones connected to $V_{ip,m}$ (30μm/0.18μm NMOS devices). What is the resulting SDR? Can you conclude that either one of the two mechanisms dominates? Hint: we say that one mechanism dominates if its effect is at least one order of magnitude (ie 10 times higher) than the other. If one of the mechanisms is dominant, you should see significant changes in the resulting SDR of 10 dB or more when its effect is removed.

v. Using the same setup as in (iv), re-run the simulation with a reduced input frequency of 5/64 f_s (use 'state_d2'). What is the SDR now? How do you explain the change?