Review Session 3

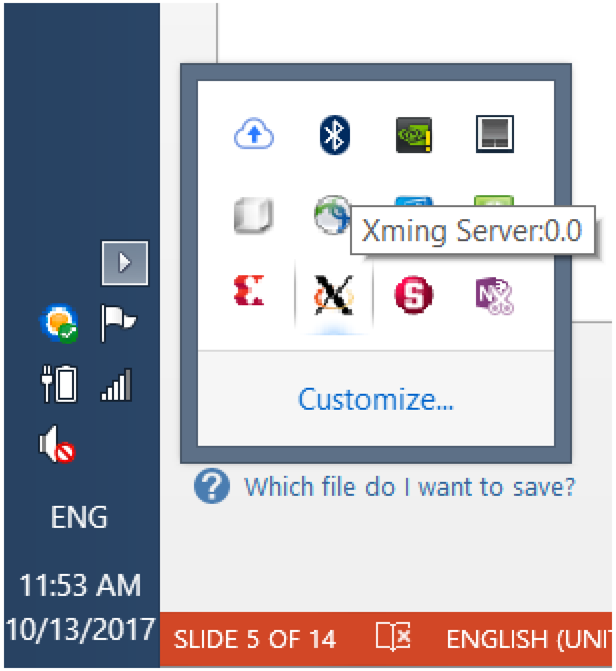
10/13/2017

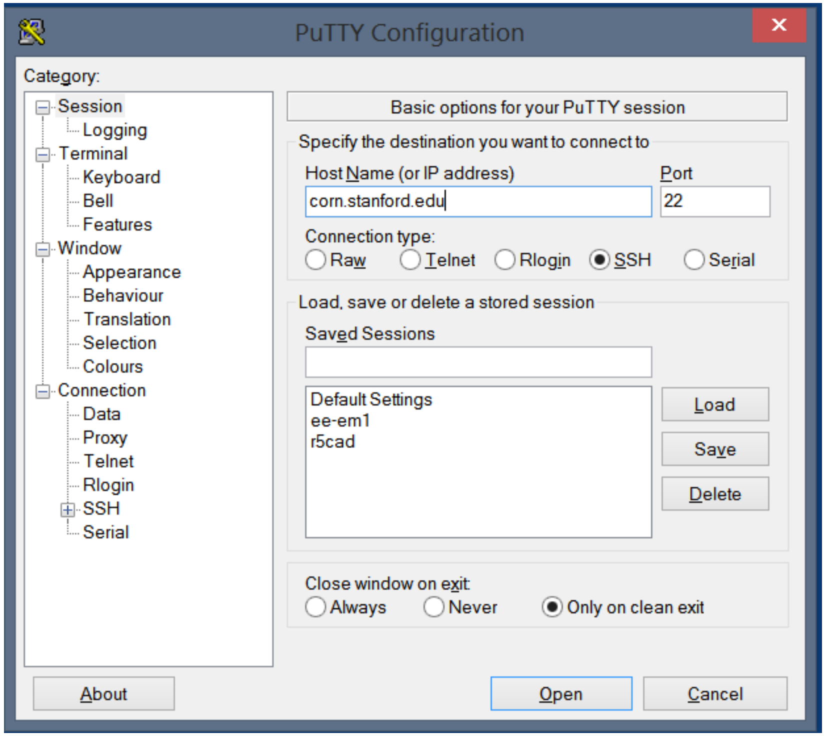
Corn Remote Connections

- VNC Issues?
- Try X11 Forwarding
  - Windows:
    - PuTTY: http://www.putty.org/
    - Xming: https://sourceforge.net/projects/xming/
  - MAC:
    - XQuartz: https://www.xquartz.org/

Windows: SSH with X11 Forwarding

- Run Xming, then connect to corn through PuTTY





Basic options for your PuTTY session

Specify the destination you want to connect to

Host Name (or IP address): corn.stanford.edu

Port: 22

Connection type: ○ Raw ○ Telnet ○ Rlogin ● SSH ○ Serial

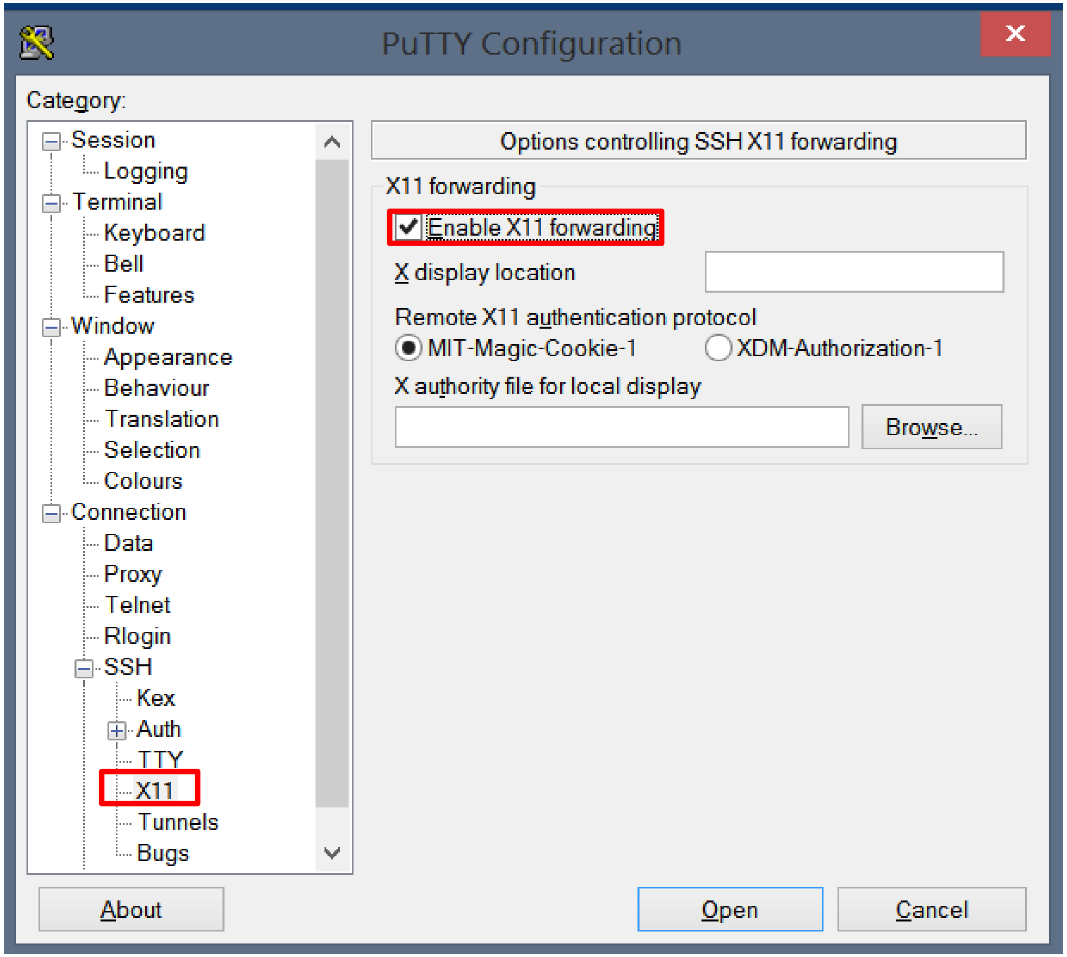
Load, save or delete a stored session

Saved Sessions

Default Settings
ee-em1
r5cad

Close window on exit: ○ Always ○ Never ● Only on clean exit

Windows: SSH with X11 Forwarding



Options controlling SSH X11 forwarding

X11 forwarding

☑ Enable X11 forwarding

X display location

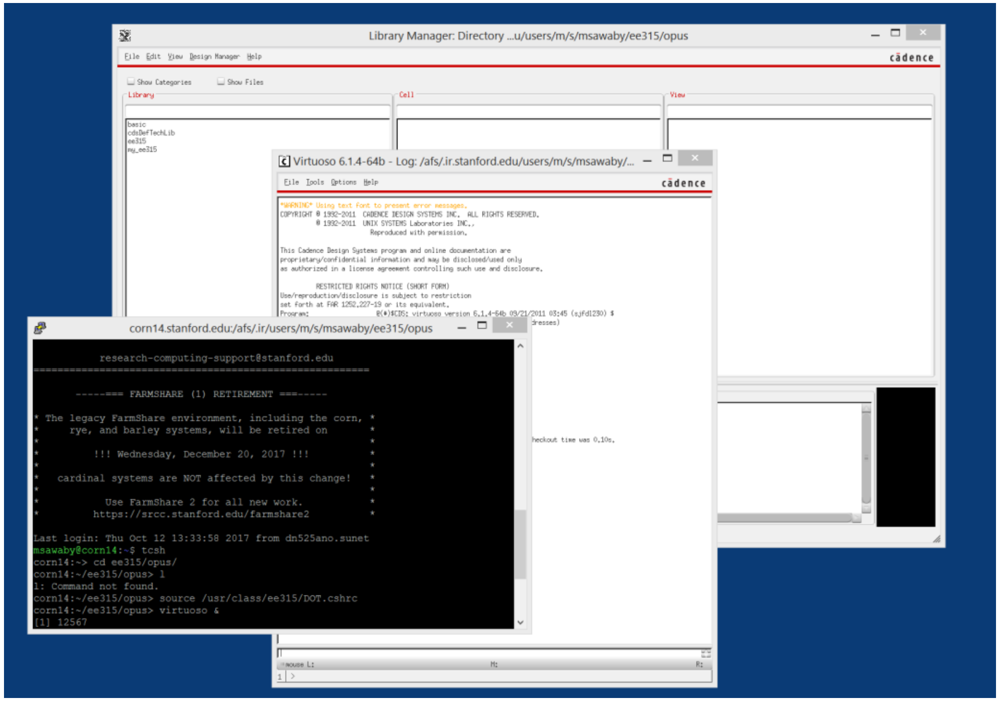
Remote X11 authentication protocol

● MIT-Magic-Cookie-1 ○ XDM-Authorization-1

X authority file for local display

Windows: SSH with X11 Forwarding

- In the shell that opens:
  - Log in.
  - Load virtuoso like usual (as if you are logging through corn.)


Library Manager: Directory ...u/users/m/s/msawaby/ee315/opus
File Edit View Design Manager Help
cādence
Show Categories
Show Files
Library
Cell
View
basic
cdsDefTechLib
ee315
my_ee315
Virtuoso 6.1.4-64b - Log: /afs/.ir.stanford.edu/users/m/s/msawaby/...
File Tools Options Help
cādence
corn14.stanford.edu:/afs/.ir/users/m/s/msawaby/ee315/opus
mouse L:
M:
R:

```
*WARNING* Using text font to present error messages.
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                       Reproduced with permission.

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          RESTRICTED RIGHTS NOTICE (SHORT FORM)
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set forth at FAR 1252.227-19 or its equivalent.
Program:                 @(#)$CDS: virtuoso version 6.1.4-64b 09/21/2011 03:45 (sjfdl230) $
```

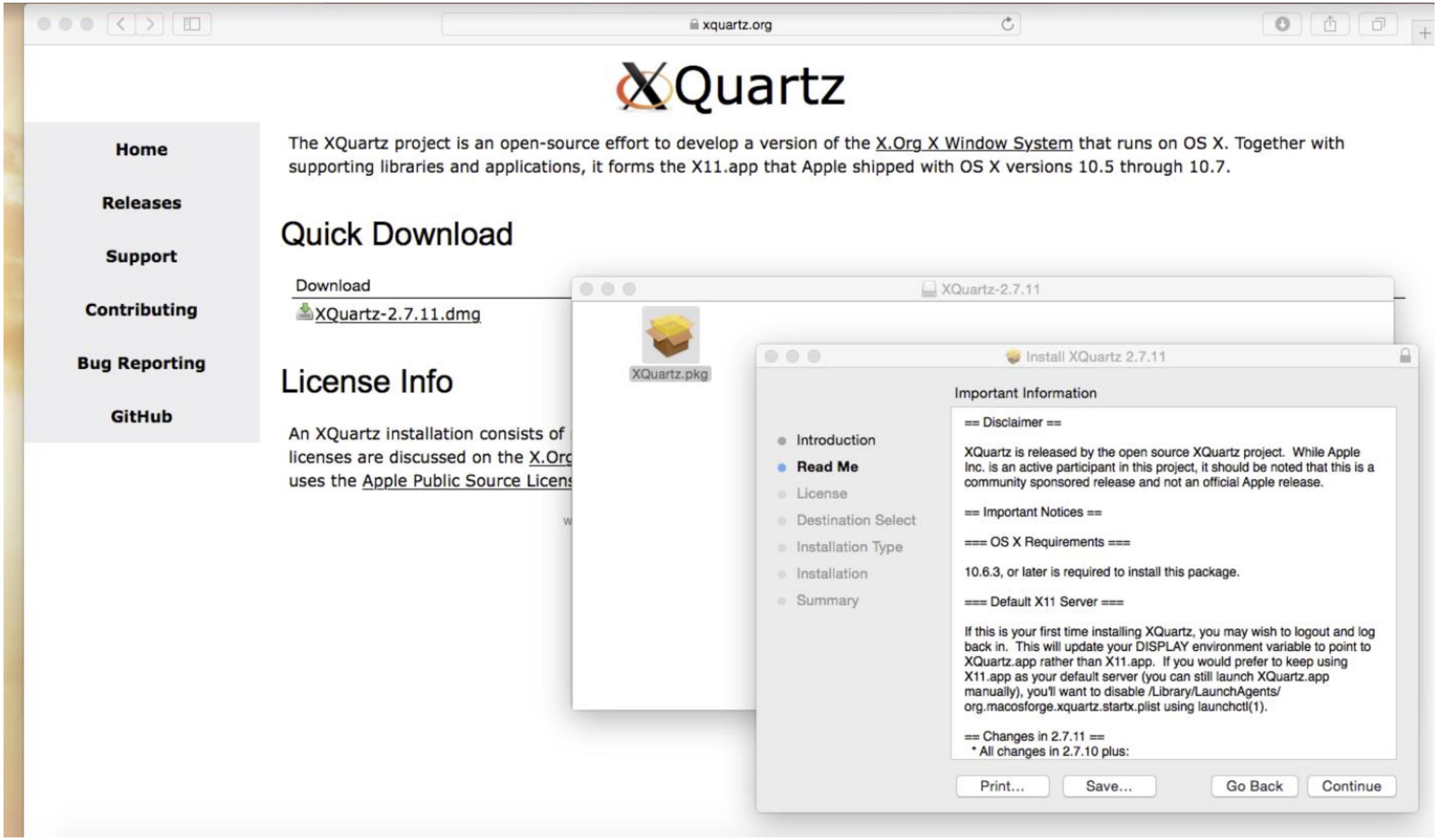
```
          research-computing-support@stanford.edu
========================================================

       -----=== FARMSHARE (1) RETIREMENT ===-----

* The legacy FarmShare environment, including the corn, *
*     rye, and barley systems, will be retired on        *
*                                                        *
*         !!! Wednesday, December 20, 2017 !!!           *
*                                                        *
*   cardinal systems are NOT affected by this change!   *
*                                                        *
*           Use FarmShare 2 for all new work.            *
*         https://srcc.stanford.edu/farmshare2           *

Last login: Thu Oct 12 13:33:58 2017 from dn525ano.sunet
msawaby@corn14:~$ tcsh
corn14:~> cd ee315/opus/
corn14:~/ee315/opus> l
l: Command not found.
corn14:~/ee315/opus> source /usr/class/ee315/DOT.cshrc
corn14:~/ee315/opus> virtuoso &
[1] 12567
```

MAC: X11 Forwarding



The XQuartz project is an open-source effort to develop a version of the X.Org X Window System that runs on OS X. Together with supporting libraries and applications, it forms the X11.app that Apple shipped with OS X versions 10.5 through 10.7.

Quick Download

Download

XQuartz-2.7.11.dmg

License Info

An XQuartz installation consists of
licenses are discussed on the X.Org
uses the Apple Public Source Licens

Important Information

== Disclaimer ==

XQuartz is released by the open source XQuartz project. While Apple Inc. is an active participant in this project, it should be noted that this is a community sponsored release and not an official Apple release.

== Important Notices ==

=== OS X Requirements ===

10.6.3, or later is required to install this package.

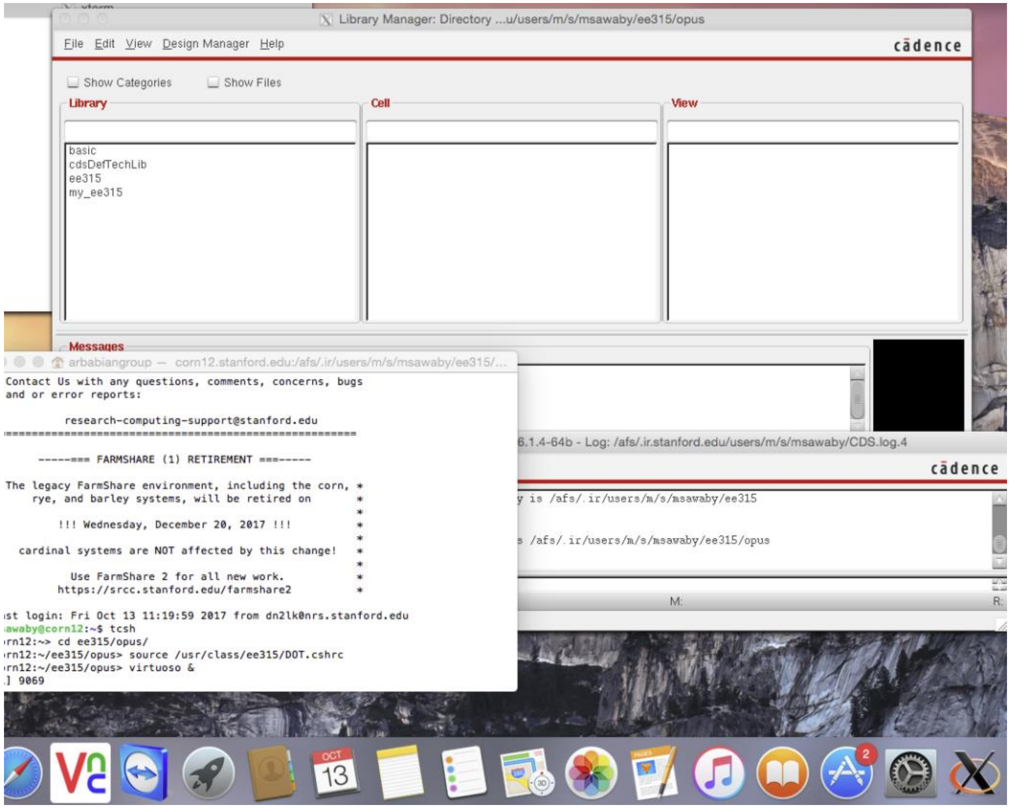
=== Default X11 Server ===

If this is your first time installing XQuartz, you may wish to logout and log back in. This will update your DISPLAY environment variable to point to XQuartz.app rather than X11.app. If you would prefer to keep using X11.app as your default server (you can still launch XQuartz.app manually), you'll want to disable /Library/LaunchAgents/org.macosforge.xquartz.startx.plist using launchctl(1).

== Changes in 2.7.11 ==
 * All changes in 2.7.10 plus:

MAC: X11 Forwarding

- Lunch XQuartz. In a terminal, type:
  - ssh -X corn.stanford.edu -l msawaby


Library Manager: Directory ...u/users/m/s/msawaby/ee315/opus
File Edit View Design Manager Help
cādence
□ Show Categories
□ Show Files
Library
Cell
View
basic
cdsDefTechLib
ee315
my_ee315
Messages
arbabiangroup — corn12.stanford.edu:/afs/.ir/users/m/s/msawaby/ee315/...
6.1.4-64b - Log: /afs/.ir.stanford.edu/users/m/s/msawaby/CDS.log.4
cādence
M:
R:

```
Contact Us with any questions, comments, concerns, bugs
and or error reports:

         research-computing-support@stanford.edu
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     -----=== FARMSHARE (1) RETIREMENT ===-----

The legacy FarmShare environment, including the corn, *
    rye, and barley systems, will be retired on       *
                                                      *
       !!! Wednesday, December 20, 2017 !!!           *
                                                      *
  cardinal systems are NOT affected by this change!   *
                                                      *
        Use FarmShare 2 for all new work.             *
       https://srcc.stanford.edu/farmshare2           *

ıst login: Fri Oct 13 11:19:59 2017 from dn2lk0nrs.stanford.edu
awaby@corn12:~$ tcsh
ırn12:~> cd ee315/opus/
ırn12:~/ee315/opus> source /usr/class/ee315/DOT.cshrc
ırn12:~/ee315/opus> virtuoso &
.] 9069
```

```
y is /afs/.ir/users/m/s/msawaby/ee315

s /afs/.ir/users/m/s/msawaby/ee315/opus
```

HW3

Submission through Gradescope

Q1: T/F

Q2: ADC Performance

Q3: Switch ON Resistance

Q4: Switch Non-Idealities

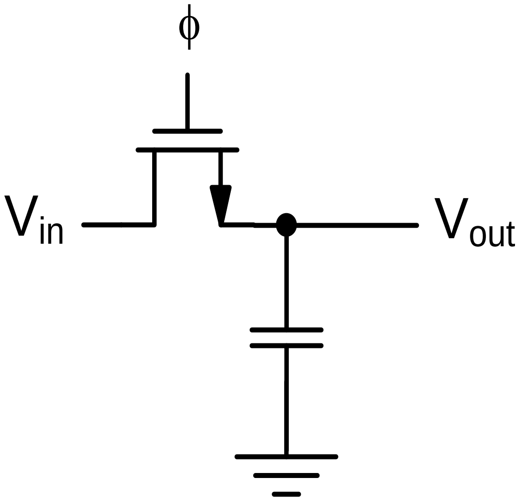
Q5: CAD

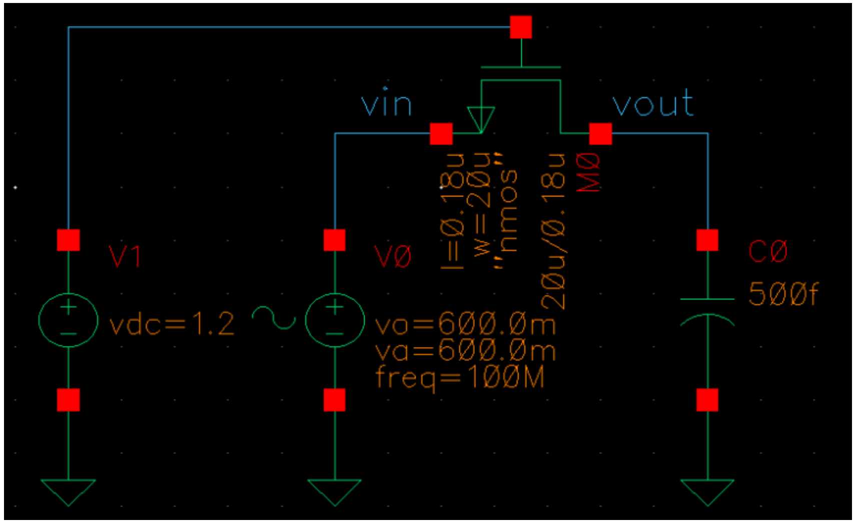
Q6: Bottom-Plate Sampling

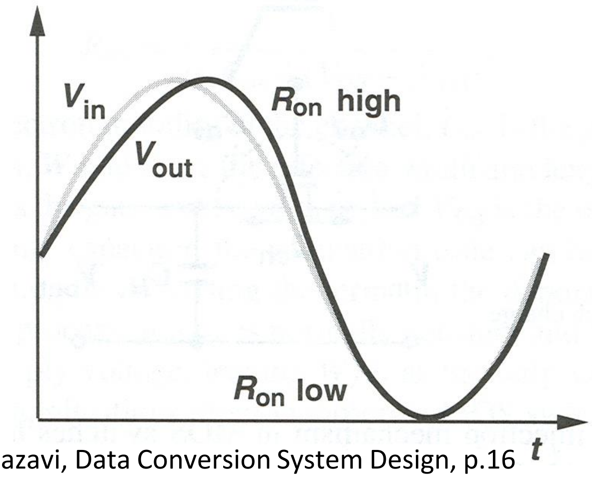
Q2 Hint

- Plot spectrum, get input freq.
- Calculate SNR, SNDR, ENOB, THD: write your own code!
- Part e) the ADC has ideal $\Delta^2/12$ quantization noise. Noise sources are thermal and quantization.

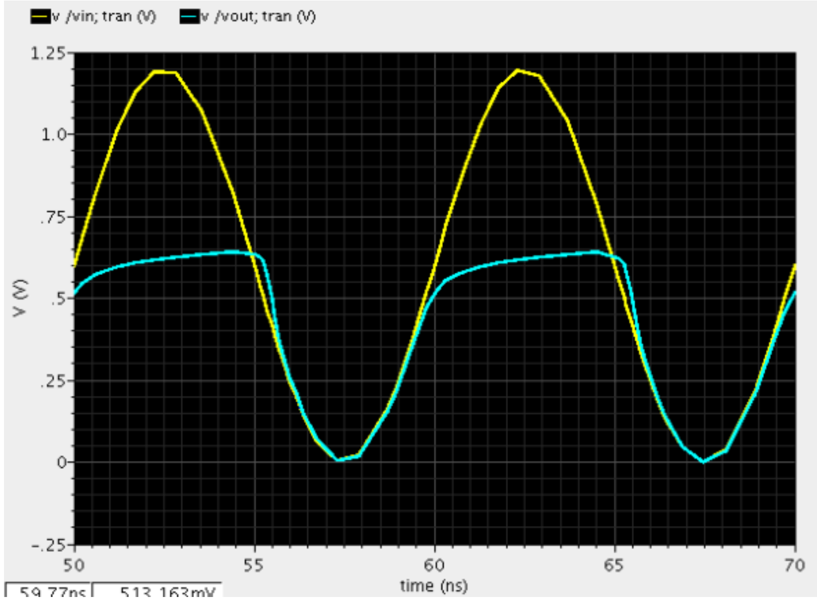
Q3 Review: Tracking Nonlinearity







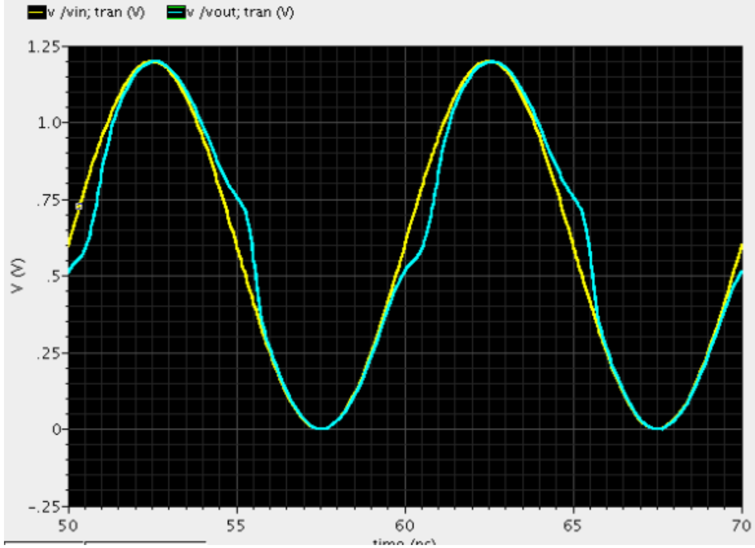
Razavi, Data Conversion System Design, p.16



Q3 Review: Tracking Nonlinearity

- Transmission gate

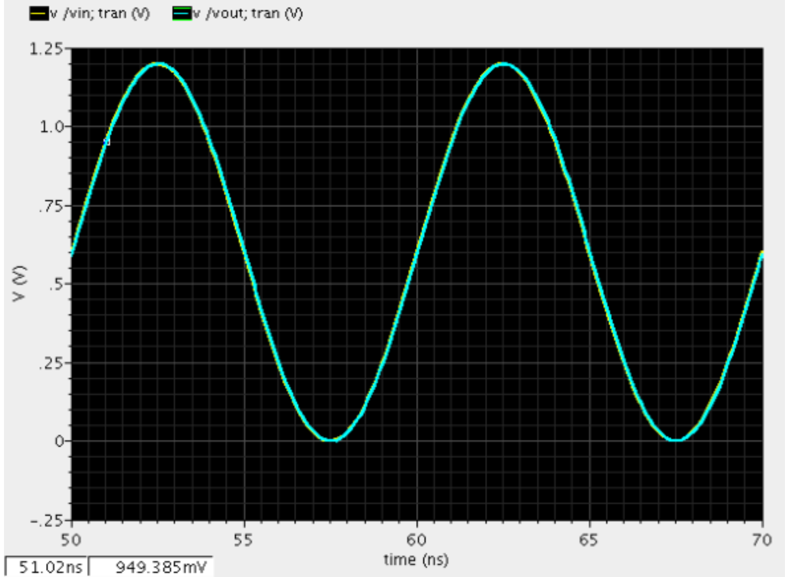
  added pmos, same dimensions as nmos



- Bootstrapped NMOS

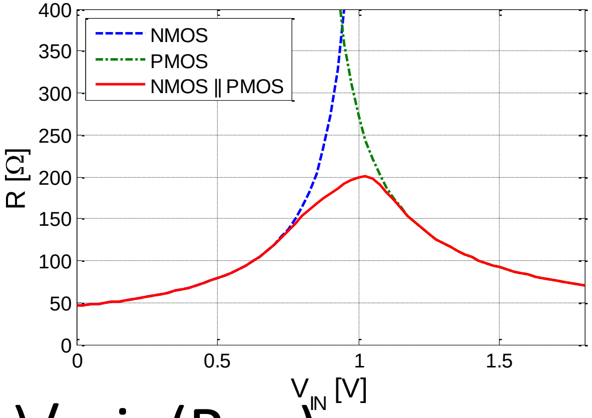
  added vdc to

  set Vgs=Vdd



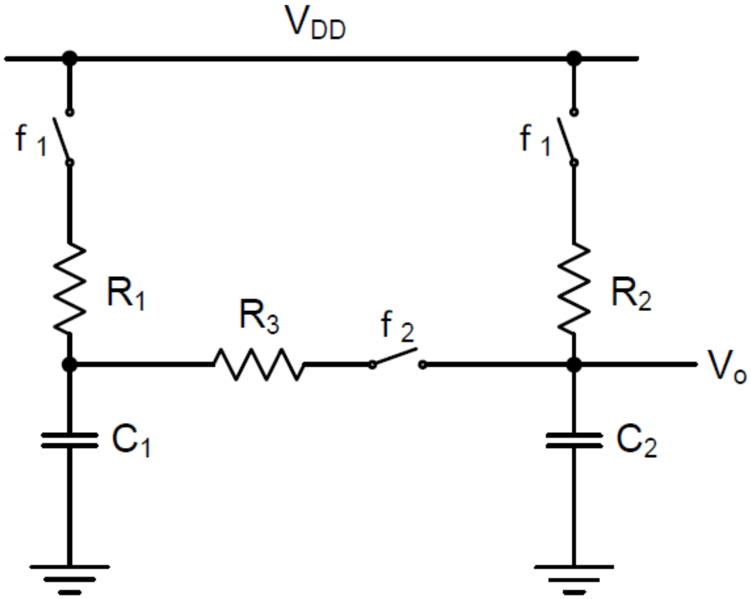
Q3 Hint

- Simulation using Cadence
- Recall how t-gate works (lecture 5-6, slide 31)
- Recommend to start this problem early in case corn goes down
- Suggestion: plot using Matlab
- Condition to minimize variation?
  - Theory
  - From sims: Ron variation = max(Ron)/min(Ron) (use ron = 1/gds and not ron directly!)
  - No need to re-simulate: scale Ron!



Q4 Review

- Calculate Noise (std deviation of signal), charge injection and clock feedthrough.
- Let’s solve this example:



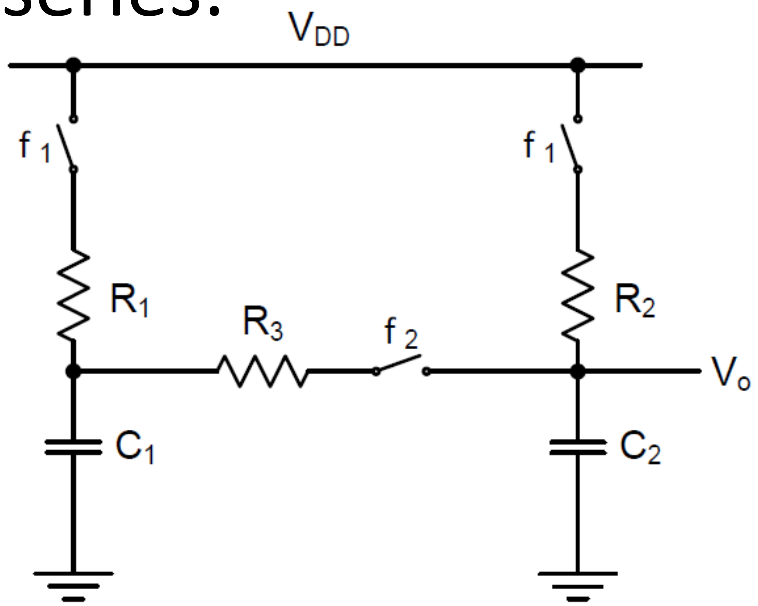
Switched Cap Noise Example

- During Φ_1 after redistribution in Φ_2 :

$$-\frac{kT}{C_1}\left(\frac{C_1}{C_1+C_2}\right)^2+\frac{kT}{C_2}\left(\frac{C_2}{C_1+C_2}\right)^2$$

- During Φ_2, C_1 and C_2 are in series:

$$-\frac{kT}{\frac{C_1C_2}{C_1+C_2}}\left(\frac{C_1}{C_1+C_2}\right)^2$$



- Adding all we get:

$$-\frac{kT}{C_2}$$

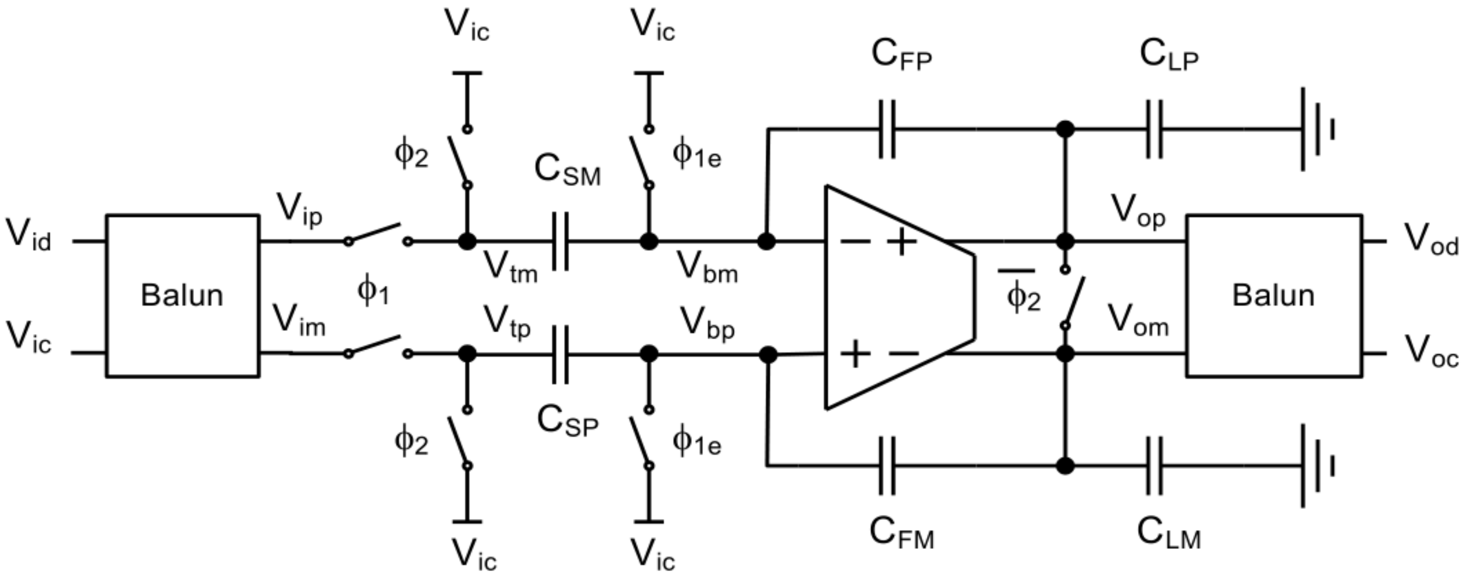
Problem 6

- Hand calculate, then simulate bottom plate sampling circuit
  - Charge injection, Noise, Distortion
  - For NMOS parameters, run DC simulation then plot DC op through (results -> print -> DC Operating Points) then click on the transistor. (or assume: Cox=10fF/µm^2, Vt=0.6V)
- Noise simulation: pss, pnoise
  - Models as LPTV circuit, gets a result using a single simulation
  - Downside: simulation is slow, because you need so many sidebands (due to high N)

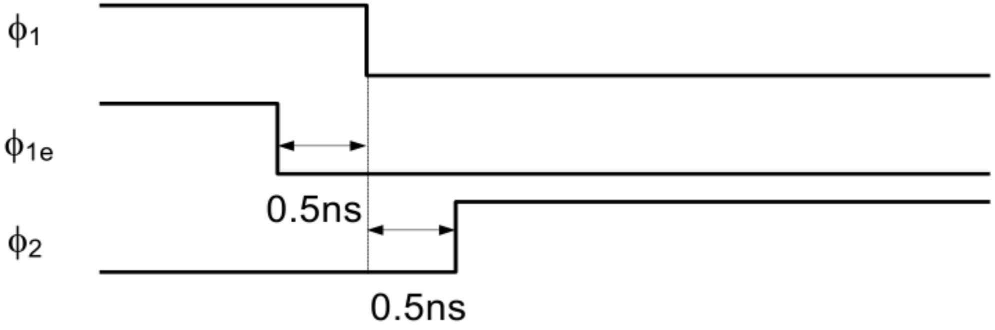
Problem 6

- Can also simulate using .noise
  - One simulation for each phase; add up the powers
  - Simulation files are switch_cap_ckt_noise in ee315 library
- Different capacitances and OTA input-referred noise so these numbers differ from your homework

Schematic

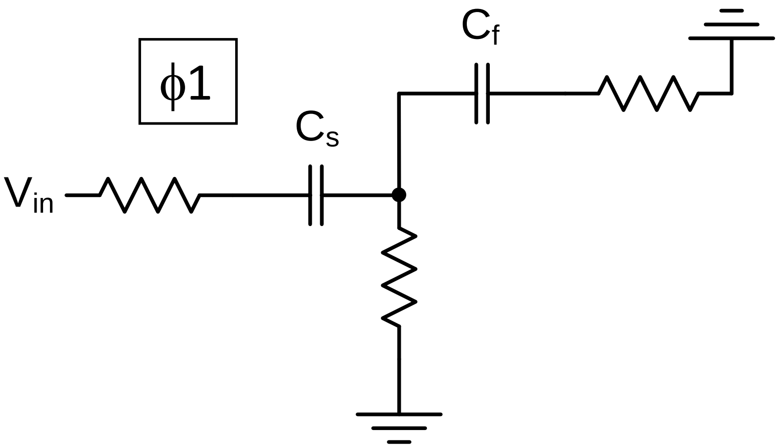


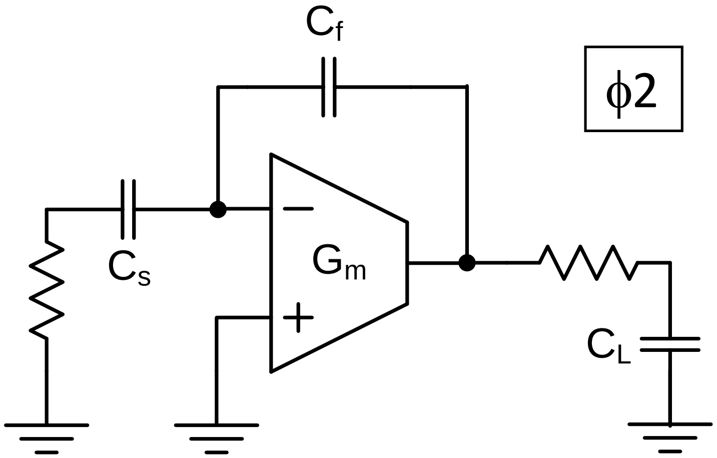
V_ic
V_ic
C_FP
C_LP
φ2
C_SM
φ1e
V_ip
V_op
V_id
Balun
V_tm
V_bm
V_od
φ1
φ2
V_om
Balun
V_ic
V_im
V_tp
V_bp
V_oc
C_SP
φ2
φ1e
C_FM
C_LM
V_ic
V_ic



φ1
φ1e
0.5ns
φ2
0.5ns

Two Phases





Noise due to switches

Noise due to amplifier and switches

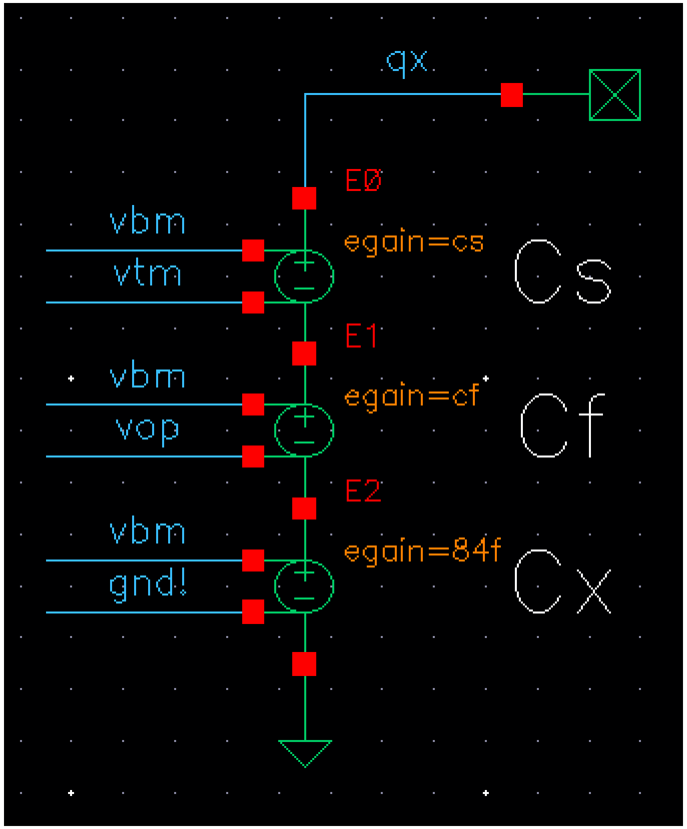
Reference: Murmann, Solid-State Circuits Magazine, 6/2012

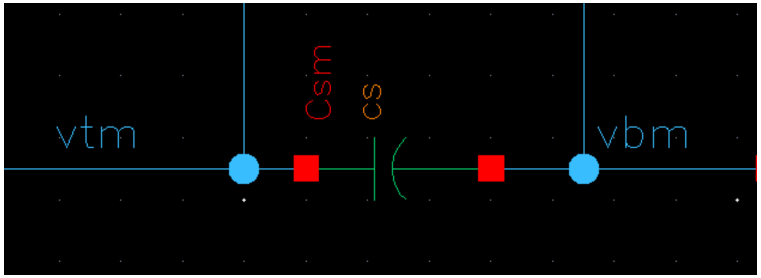
Phase 1: Tracking

- Interested in the total noise charge at input to the OTA
- What do we know?
  - Capacitance
  - Voltage
- We will have to calculate the charge ourselves with voltage-controlled voltage sources (VCVS)
- Qtot = Cs*Vs + Cx*Vx + Cf*Vf
  - Vs = voltage across capacitor Cs
  - Cx adds to the total noise charge (Also affects feedback factor!)
- Note: we'll find single-ended noise, then double it to get differential noise

Phase 1: How to measure Qx

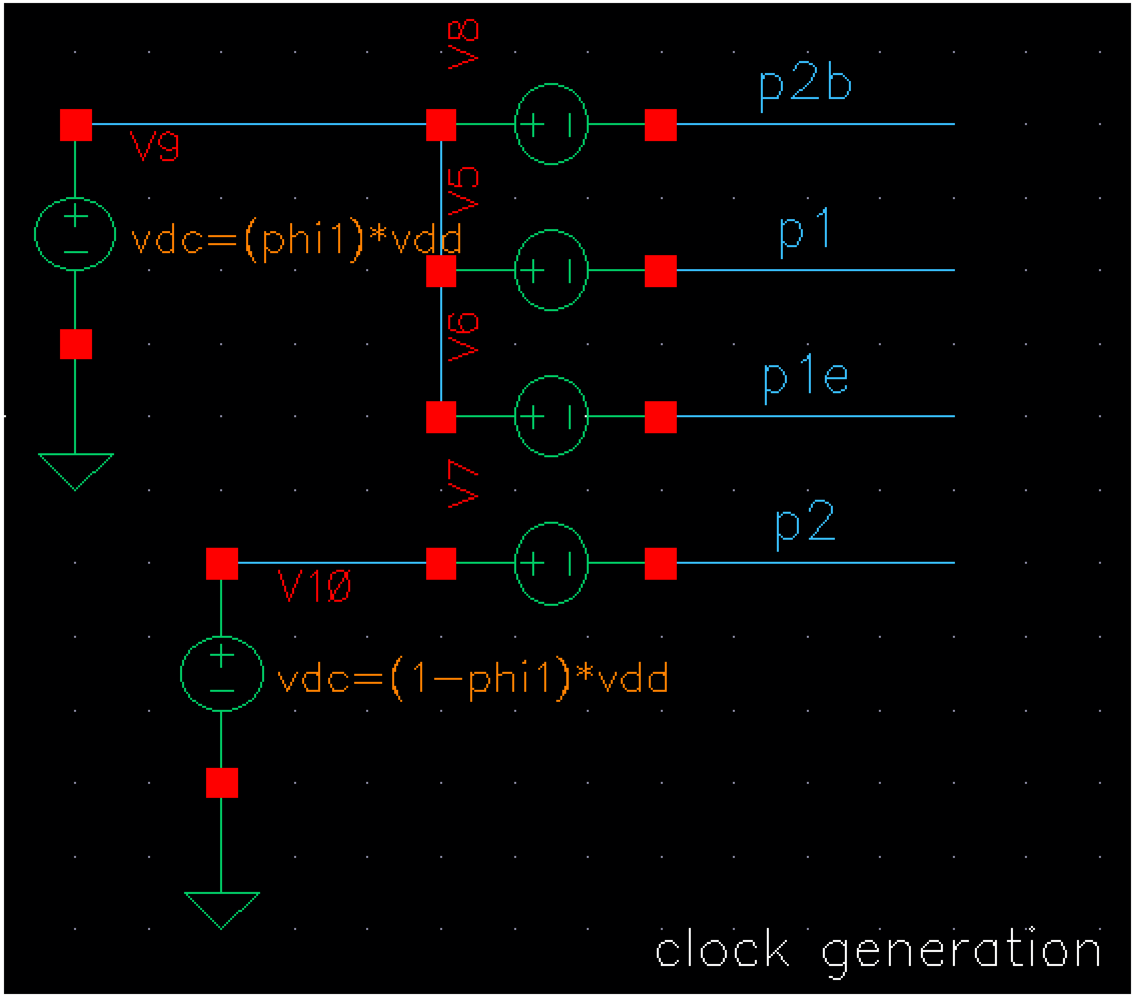
- VCVS produces an output equal to:
  - Vout = egain*(V+ - V-)
- With egain=C, the output “voltage” is really representing the charge
- Example: voltage across Cs will be vbm-vtm





Phase 1: Switch configuration

- Easily change clock phases from ADE L window

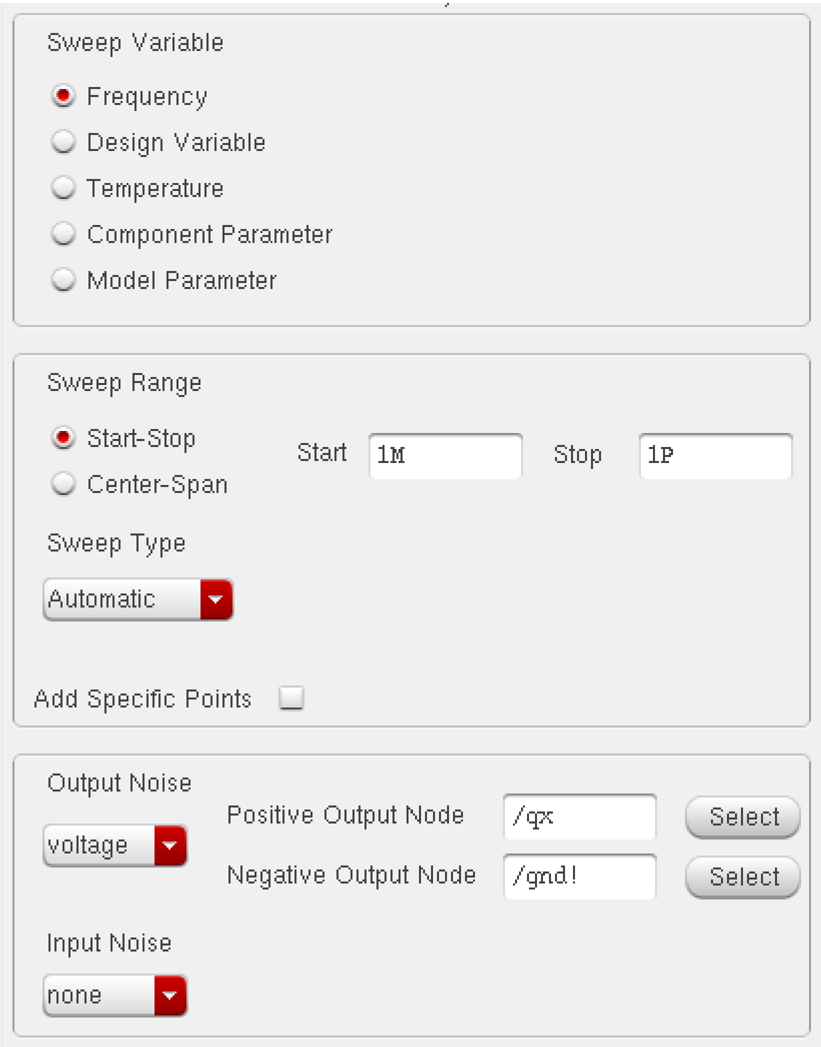


Phase 1: Schematic summary

- Summary so far…
  - We want to sum up the charge at node X
  - To do this, we use VCVS to measure the voltage across each capacitor, and use Q=CV to calculate the charge across that capacitor
- Next
  - Set up the .noise analysis

Phase 1: Tracking

- Design variables copied from the pss/pnoise analysis from before
  - Add “phi1 = 1”
- Noise analysis:
  - Sweep freq 1M-10T
  - Output from /qx to /gnd!
  - No input source



Sweep Variable

● Frequency
○ Design Variable
○ Temperature
○ Component Parameter
○ Model Parameter

Sweep Range

● Start-Stop
○ Center-Span

Start: 1M
Stop: 1P

Sweep Type: Automatic

Add Specific Points □

Output Noise: voltage
Positive Output Node: /qx
Negative Output Node: /gnd!

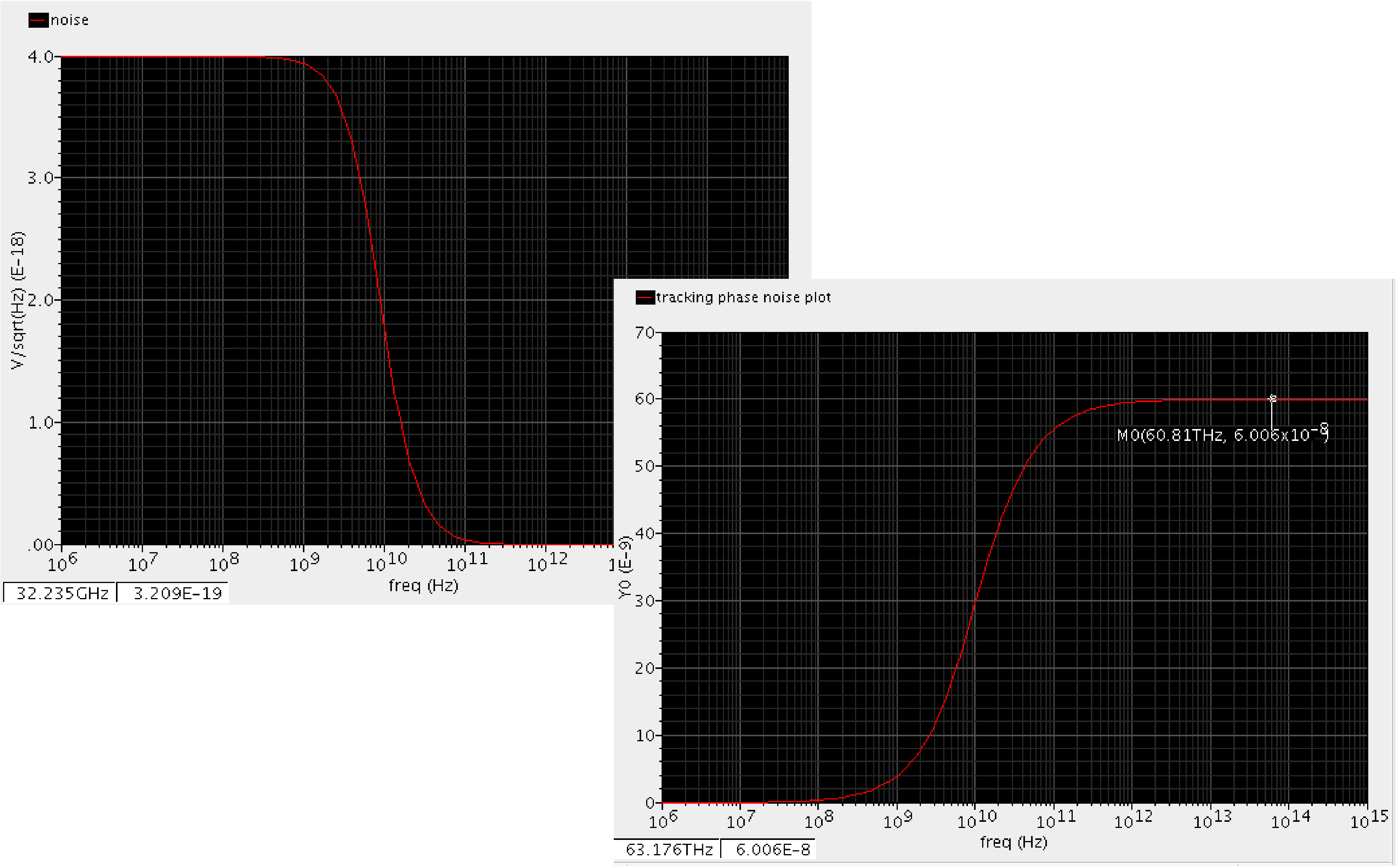
Input Noise: none

Phase 1: Calculating output noise

- The output from .noise is the charge noise power at node X (units are Coulomb^2/Hz)
  - Cadence thinks the units are V^2/Hz, but it’s wrong. Recall we scaled the capacitor voltages by capacitance, so it’s really charge noise that we’re getting
- V^2 = Q^2 / C^2, so we get output-referred voltage noise using

```
VN2() / pow(VAR(“cf”) 2)
```

Phase 1: Plotting output noise



Phase 1: Hand calcs

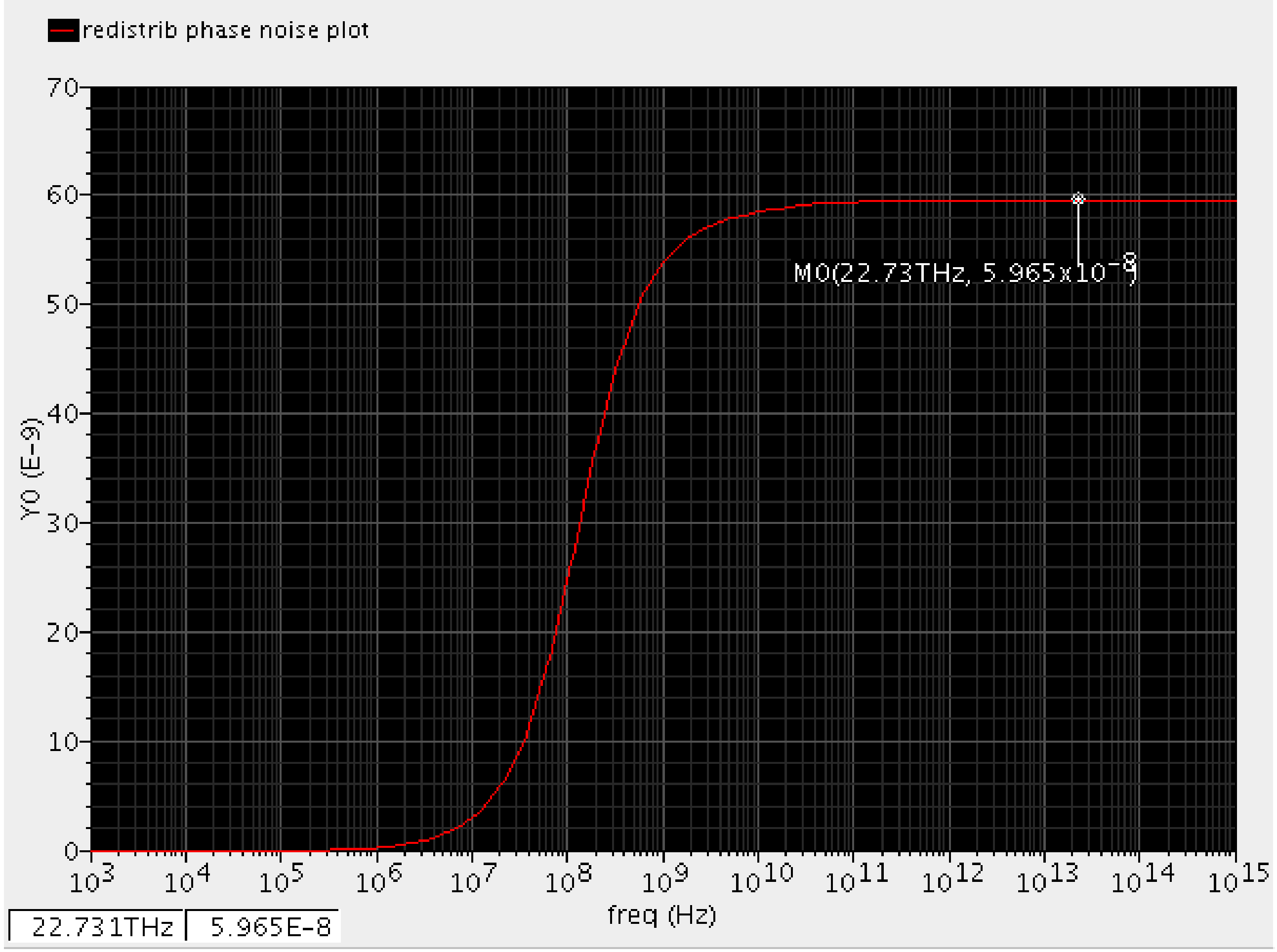
- Recall factor of 2 to get differential noise
- Hand calculation: 1.14 * 10^-7 V^2
- Simulation: 1.20 * 10^-7 V^2

Phase 2: Configuration

- Change variable phi1=0 to put us in phase 2
- Change .noise output to /vod to /gnd! (differential noise)
- Output no longer needs scaling by Cf^2

```
    iinteg(VN2())
```

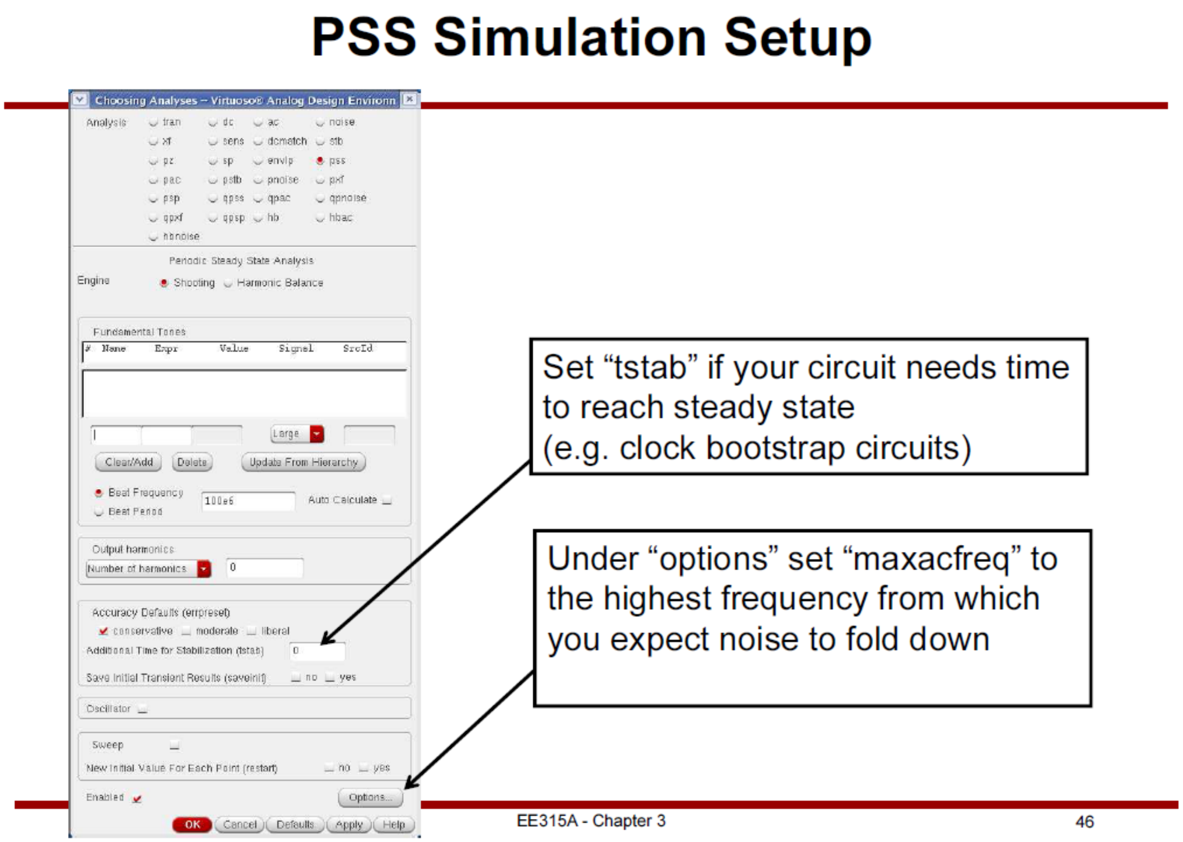
Phase 2: Plotting



Phase 2: Hand calcs

- Hand calculation: 6.6 * 10^-8 V^2
- Simulation: 5.9 * 10^-8 V^2

PSS Simulation



PSS Simulation Setup

Choosing Analyses – Virtuoso® Analog Design Environm

Analysis ○ tran ○ dc ○ ac ○ noise ○ xf ○ sens ○ dcmatch ○ stb ○ pz ○ sp ○ envlp ● pss ○ pac ○ pstb ○ pnoise ○ pxf ○ psp ○ qpss ○ qpac ○ qpnoise ○ qpxf ○ qpsp ○ hb ○ hbac ○ hbnoise

Periodic Steady State Analysis

Engine ● Shooting ○ Harmonic Balance

Fundamental Tones

#	Name	Expr	Value	Signal	SrcId

● Beat Frequency 100e6 Auto Calculate □

○ Beat Period

Output harmonics

Number of harmonics 0

Accuracy Defaults (errpreset)

☑ conservative □ moderate □ liberal

Additional Time for Stabilization (tstab) 0

Save Initial Transient Results (saveinit) □ no □ yes

Oscillator □

Sweep □

New Initial Value For Each Point (restart) □ no □ yes

Enabled ☑

Set "tstab" if your circuit needs time to reach steady state
(e.g. clock bootstrap circuits)

Under "options" set "maxacfreq" to the highest frequency from which you expect noise to fold down

Comparison

	Phase 1 noise	Phase 2 noise	Total noise
Hand calculation	1.14e-7	6.6e-8	1.80e-7
Simulation .noise	1.20e-7	5.9e-8	1.79e-7
Simulation .pnoise (500 sidebands)	1.07e-7	5.6e-8	1.63e-7
Simulation .pnoise (2000 sidebands)	1.15E-7	5.6e-8	1.71e-7