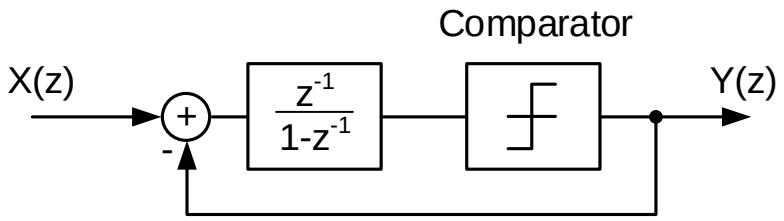
HOMEWORK #2

(Due: Thursday, October 12, 2017, 11:59 pm PT via Gradescope Online Submission)

1. **Quick Questions.** For each of the following statements, state "T" for true or "F" for false. No explanation necessary. Correct answers are worth +1 point, while incorrect answers yield -1 point. No points for unanswered questions. Your minimum total score on this problem is zero points.

a) In a D/A interface, the images from first-order hold reconstruction can be removed using an appropriate digital filter at the DAC input.	
b) A D/A interface that is built using an oversampling delta-sigma loop does not require a DAC in its feedback path.	
c) It is not possible to have DNL = –1.5 LSB in a thermometer D/A converter.	

2. **Matlab simulation of a basic delta-sigma converter.** Consider the first-order, single-bit delta-sigma modulator shown below.



   a) Download the starter file "hw2_ds.m" from the course website (under "homework"). This program is meant to simulate the system with a DC input and compute the average of the digital output. Complete the code and try a number of different DC inputs: 0.5, 0.8, –0.2. Verify that the cumulative average of the output converges to the DC input over time. Submit the Matlab plot for X = 0.8.
   b) What happens when you have a DC input larger than 1? Explain the observed behavior (The output Y(z) and well as the internal output of the integrator).
   c) Modify the Matlab program to simulate the converter with a sine-wave input. Use a half-scale sine wave with 5 cycles in 4096 points and then take the FFT of the output. What is the oversampling ratio assuming that the sinusoid frequency corresponds to the signal band edge (f_B)? Plot the magnitude FFT in dBFS, where the full scale range is defined by the +1/-1 feedback levels. Scale the x-axis of the plot to reflect the normalized frequency f/f_s. Verify the existence of noise-shaping and submit your FFT plot.
   d) From the FFT output, extract the quantization noise power in the band from 0 to $0.05f_s$ (do not include the signal bin!). What is the value you would expect from first order theory? Comment on the potential discrepancies.

3. A segmented DAC consists of a thermometer encoded MSB DAC with 6 bits. The standard deviation of the elements from their nominal value is 3%. The number of bits in the binary weighted LSB DAC is 6 bits and the standard deviation of the elements is 4%. What is the standard deviation of the DNL for the worst code?

4. Read the following paper: C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," IEEE J. Solid-State Circuits, vol. 33, pp. 1948-1958, Dec. 1998. What application is this DAC intended for?

5. In the above reference, it was found that for the given objectives, a thermometer/ binary partition of 8/2 is most suitable. Your task in this problem is to re-optimize this DAC for a 65-nm technology with a different set of process parameters, without altering its basic structure. The design variables to be optimized are:

Parameter	Description
B_t	Number of bits in thermometer section
A_{unit}	Area of unit current source

Your target specs and process parameters are:

Parameter	Description	Value
B	Resolution	12 bits
INL_{spec}	Worst case integral nonlinearity	< 0.5 LSB
DNL_{spec}	Worst case differential nonlinearity	< 0.5 LSB
Y	Target yield	95%
A_{decode}	Approximate decoder and routing area	$2^{Bt}\cdot 2000\ \mu m^2$
A_{total}	Total DAC area (to be minimized)	$2^B\cdot A_{unit}+ A_{decode}$
k_u	Unit element matching parameter	6%μm
σ_u	Standard deviation of unit element mismatch	$k_u/sqrt(A_{unit})$

a) Following the procedure outlined in the reference, answer the following **using only hand calculations** (After the equations are written by hand, it is ok to use Matlab/ Excel to perform a sweep across **integer** values of B_t):

   i. What values of A_{unit} and B_t actually minimize the total area defined above in the table? What is the minimum total area (in mm^2)?
   ii. What values of A_{unit} and B_t give the "optimal point" described by the paper? What is the total area (in mm^2) in this case

b) Create a plot similar to Fig. 9 of the reference paper to illustrate the "minimum area" design. In this diagram, plot the total DAC area in mm^2 (log scale) versus the design parameter B_t (linear scale in bits).

6. Use Matlab to simulate your "minimum area" design from problem 5 part (a) i, and make appropriate modifications to achieve the targeted yield.

a) Download the starter file "hw2_dac.m" from the "Homework" section of the course website. This file contains code for a 100-run Monte Carlo simulation that generates an INL envelope and RMS plot (see Fig. 7 and Fig. 8 of the paper). Below the line "Your code goes here," add additional code to generate the respective plots also for DNL. Turn in a printout of the code you added to the file (no need to submit a printout of the given code).

b) Generate and turn in envelope and RMS plots for both DNL and INL using the parameters you calculated in your hand analysis. Note that you should use the A_{unit} and B_t values calculated above in problem 4.
c) Does your initial design meet the yield spec? Explain why it does or why it doesn't. Note that meeting the yield spec requires that "on average" no more than 5 out of the 100 runs lie outside the specified DNL or INL.
d) If your hand design does not meet the yield spec, make appropriate adjustments (OK to iterate in Matlab) to A_{unit} without changing anything else. What is the value of A_{unit} that achieves the desired yield? What is the final total area of your design?