A Fast Bootstrapped Switch for High-Speed High-Resolution A/D Converter

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***Abstract*— This paper introduces new charge and discharge paths to speed up the turn-on and turn-off process of bootstrapped switch. In the mean time, linearity is improved without increasing capacitance or area. The proposed switch is designed in SMIC 65nm CMOS process and the results indicate that total harmonic distortion (THD) of 95dB is acquired when 103MHz input signal is sampled at 1Gsps.**

***Keywords*— bootstrapped switch, high speed, high linearity**

I. INTRODUCTION

A sample-and-hold (S/H) network is an essential part in analog-to-digital converters (ADCs), and its switches have a great deal in determining the overall performance. The signal-dependent on-resistance of the switch is the main error source in the S/H. To address this issue, Abo and Gray introduced a bootstrapped switch [1]. This innovated structure makes Vgs relatively as a constant, which in turn increases S/H's linearity considerably. However, due to a variety of non-ideal factors, such as charge injection, bulk effect, clock feed through etc, there are some practical techniques to reduce the distortion. These approaches include employing bottom plate sampling plus differential signal paths, increasing the size of devices, and introducing a dummy switch.

With increased demand of the high-speed high-resolution pipeline ADCs, the conventional bootstrapped switch has found limitations in terms of the linearity as well as turn-on and turn-off time under the low-voltage condition in deep submicron CMOS process technology.

Several methods have been proposed to further improve the linearity [2] [3] [4] [5] [6]. Although these ideas and above mentioned techniques can be helpful, clearly increasing of design complexity is to trade for performance. As a result, the bootstrapped switch has become a large area consumed component in the switched capacitor circuits.

Bottom plate sampling in the frequency range of several mega hertz demands a short turn-off time, because a bootstrapped switch at the summing node has to turn off completely before the one on the other plate starting turn on. In addition, widely used sampling network without sample-and-hold amplifier requires fast bootstrapped switch to track the input moving signal.

This work presents an improved bootstrapped switch. The structure speeds up turn-on and turn-off process and increases the linearity. And this approach has no increasing in circuit complexity or the chip die size corresponding to the traditional design. After this introduction, conventional circuit and its limitations are analysed in section II. And section III describes proposed solution followed by simulation results in section IV. At last, a conclusion comes in section V.

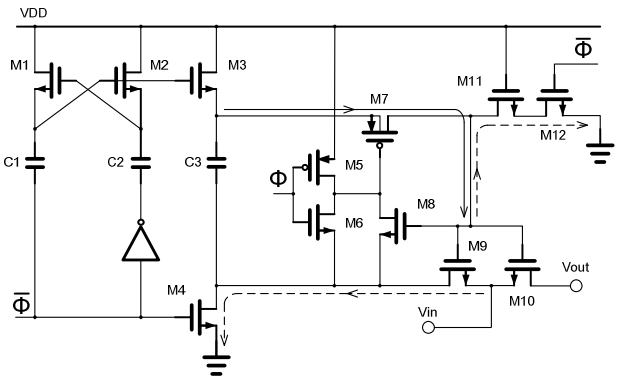

Fig. 1 Conventional bootstrapped switch

II. CONVENTIONAL STRUCTURE

The conventional bootstrapped switch introduced by Abo and Gray is shown in Fig. 1. During ON phase, a clock booster, made up of M1, M2, C1, C2 and an inverter, charges C3 to VDD. Then M7 and M9 connect C3 between gate and source of M10 in OFF phase. In this way, Vgs of M10 is kept VDD to maintain relatively constant on-resistance regardless of the input signal. However, parasitic capacitance of M7, M8, M9, M11 and M12 share the charge from C3, which makes Vgs less than VDD.

When Φ goes high, M6 is ON and the gate voltage of M7 is pulled down to ground. Consequently, M7 begins to turn on and brings up the gate voltage of M8, M9 and M10 (the charge path is shown as solid curve in Fig. 1). The single charge path is not open directly, causing delay in tracking the input signal.

When Φ goes low, M5 pulls up the gate voltage of M7 to VDD to turn it off. Therefore, C3 is isolated from M10, whose gate and source are discharged to ground through M11, M12 and M4 (the discharge paths are shown as dashed curves in Fig. 1). Between these two paths, the one through M11 and M12 is more important, so larger transistor size in this path is required.

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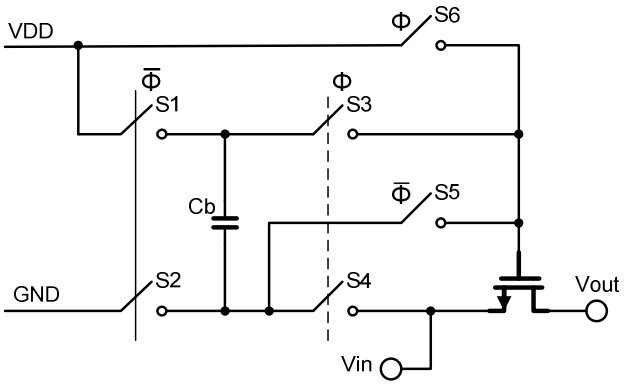


Fig. 2 Prototype structure

For reliability consideration [1], M11 is added to relax voltage pressure over M12 during OFF phase, since gate voltage of M10 can reach as much as 2*VDD. Besides, M11 is on in both phases, and has to be designed as a high voltage device. As a result, non-minimum channel length of these two NMOS provides a substantial portion of parasitic capacitance which limits Vgs of M10.

In the conventional structure, the width of M7, M9, M11 and M12 must be made large to minimize turn-on and turn-off time. Consequently, Vgs of M10 goes down, which magnifies the variation of its on-resistance, thus makes its linearity performance get worse. This basic trade-off leaves few choices but increasing C3, yet adding a few pico farads to C3 will occupy a good sum of chip area.

III. Proposed Bootstrapped Switch

A. Prototype design

The overview of the proposed topology is given in Fig. 2. During the OFF phase, S5 connects the gate of the NMOS to ground, while Cb is charged to VDD via S1 and S2. When it comes to ON phase, S3 and S4 connect Cb to the gate and source of the NMOS respectively, then Vgs is slightly less than VDD due to parasitic capacitance of the NMOS.

In this structure, S3 and S4 are not directly driven by clock. As a result, a delay in both turn-on and turn-off slows down bootstrapped switching behaviour. During this transition, these two switches somehow keep their previous state even the rising edge of clock has already arrived. In order to accelerate the process, S5 and S6 take charge during this delay: S5 shorts the gate and source of the NMOS; S6 connects the gate to VDD. After the delay, S3 closes completely and S6 is disconnected automatically.

B. Circuit implementation

Fig. 3 shows the proposed bootstrapped switch in transistor level. Comparing with the conventional circuit, M11 and M12 are replaced by M13 and M14 in the grey solid line box. M13 is added for fast turn-on while M14 is for fast turn-off. The other transistors and capacitors are the same as the conventional structure, so that the area has no change in the proposed structure.

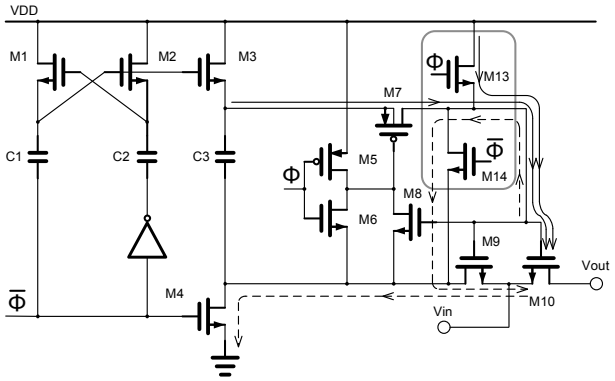


Fig. 3 Proposed bootstrapped switch

ON phase - M6 and M13 is on simultaneously, therefore the gate of M8, M9 and M10 is charged before M7 turns on. This amount of charge comes from voltage source instead of C3, which leads to higher Vgs as well as earlier turn-on of M8, M9, and then M7. So adding up the extra charge path speeds up turn-on of M10 (dual charge paths is shown as solid curves in Fig. 3). M13 is disabled when its source reaches less than one threshold than VDD, which happens not long before M7 turns on completely.

OFF phase - M14 shorts the gate and source of M10 before M9 turns off and is grounded by M4. Putting gate and source together at first place is a more straight way to turn off M10. M4 also guarantees they come to ground in the end (new discharge paths are shown as dashed curves in Fig. 3). As a result, Vgs of M10 goes low before the gate and source are grounded; therefore it provides a faster turn off mechanism.

When an input signal is large, Vgs of M14 may not be sufficient to turn it on immediately. However, after M4 brings down the source voltage of M14, the discharge path between the gate and source of M10 clears up. So increasing M4 can shorten turn-off time visibly and its parasitic capacitors almost do not share charge from C3. In addition, voltage drop between the source and drain of M14 is less than VDD, since parasitic capacitance due to M14 are much smaller than that of M11 plus M12, so a high voltage transistor is no longer necessary.

IV. Simulation Results

The proposed bootstrapped switch has been simulated using with Spectre under SMIC 65nm CMOS technology. The power supply voltage is 1.2V. A sine-wave of 30MHz with 1V peak-to-peak swing in single-ended is applied to both conventional and proposed bootstrapped switch. The capacitive load is set at 2pF each. As shown in Fig. 4, the solid line is Vgs of M10 of the proposed switch, while the dashed one is that of conventional. According to this waveform, the proposed switch is faster in both turn-on and turn-off than its conventional counterpart. The details are given in Table I. Furthermore, proposed structure yields a higher Vgs, about 50mV, which reduces variation of on-resistance of M10.

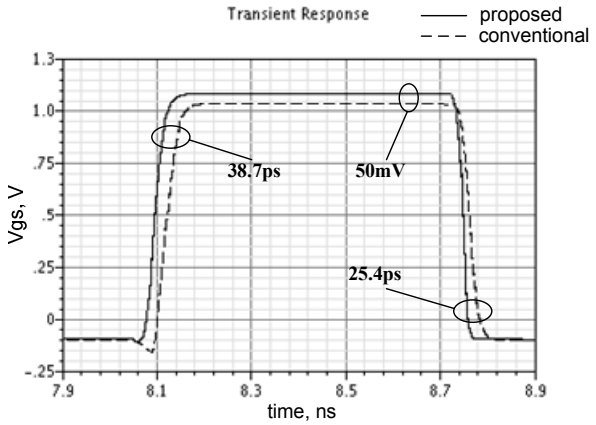


Fig. 4 Vgs of M10 of both conventional and proposed

TABLE I
Turn-on and turn-off time of conventional and proposed

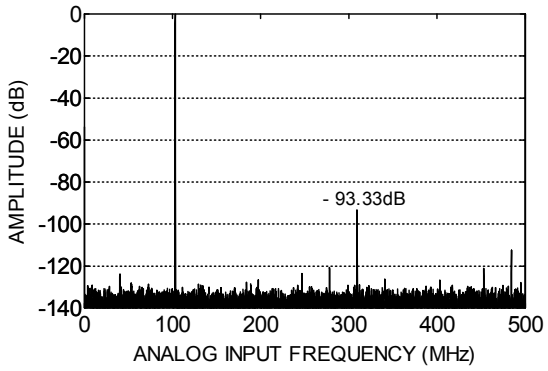
	turn-on time (ps)		turn-off time (ps)	
	min	**max**	**min**	**max**
conventional	112.45	182.85	84.35	87.60
proposed	73.98	114.43	57.58	65.73

TABLE II
Harmonic distortion in single-ended

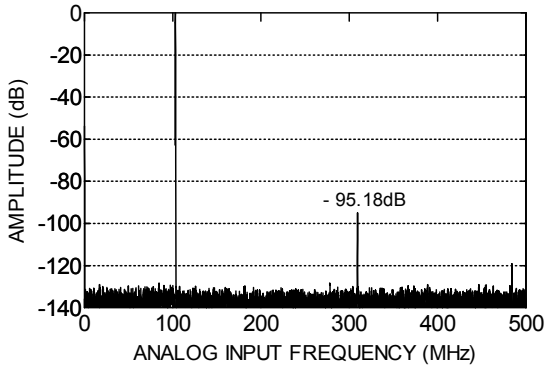
	THD	**HD2**	**HD3**
ref [2] @ fin=91MHz, fs=1GHz	N/A	-64dB	-85.5dB
conventional @ fin=103MHz, fs=1GHz	-68.8dB	-68.8dB	-94.6dB
proposed @ fin=103MHz, fs=1GHz	-74.1dB	-74.1dB	-98.1dB

Bootstrapped switches are utilized to sample a 103MHz sine wave with 0.8V peak-to-peak swing in single-ended and also loaded with 2pF capacitor each. Table II shows the total distortion, HD2 and HD3 as well as comparison with previous work.

Simple single-ended sampling network suffers from charge-injection and clock feed through and is seldom used in high performance AD converter. Therefore, bottom plate sampling and differential signal paths are introduced to overcome these issues. A 103MHz 1.6V peak-to-peak differential sine wave is sampled by 1GHz clock. The output performed using FFT is shown in Fig. 5. Differential sampling circuit cancels even order harmonic distortion naturally; therefore third order tone dominates the overall performance. Table III summarizes harmonic distortions in differential-ended sampling network and compare them with reference design as well as



(a) Conventional bootstrapped switch



(b) Proposed bootstrapped switch

Fig. 5 FFT of the output of conventional and proposed switch

TABLE III
Harmonic distortion in differential-ended

	THD	**HD3**
ref [5] @ fin=10MHz, fs=100MHz	-101dB	-115.4dB
conventional @ fin=103MHz, fs=1GHz	-93.3dB	-93.3dB
proposed @ fin=103MHz, fs=1GHz	-95.2dB	-95.2dB

conventional one. The sampling network maintains over 12 bit linearity even if the input frequency goes up to 400MHz.

V. CONCLUSION

A fast bootstrapped switch used in high-speed and high-resolution A/D converter is presented. This new technique accelerates the turn-on and turn-off process by introducing two new charge or discharge path and improves the linearity. The better result is achieved with no additional capacitance and no extra area. Finally, this structure relaxes voltage stress over transistor and increases circuit reliability.

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