Optimizing SAR ADC

Thomas Flores

(Dated: November 19, 2017)

I. DETERMINING TIME CONSTANT

We will begin our design targeting a sample speed of $100\,\mathrm{MS\,s^{-1}}$. We will be using a 10-bit asynchronous approach, and so we need to figure out what the best and worst case settling times will be. We start from PAPER and use equations

$$T_{async} = \sum_{i=0}^{N-1} K \cdot \log \frac{V_{FS}}{V + res[i]} \tag{1}$$

We see that

$$\frac{T_{async}}{T_{sync}}_{min} \approx \frac{1}{2} \tag{2}$$

So we design a synchronous SAR ADC with half the speed of our target asynchronous design and assume it will be twice as fast after asynchronous implementation. Therefore, our new target design is $50\,\mathrm{MS\,s^{-1}}$. Given our metastability rate $P = 10^{-7}$, we find that we need

$$N_\tau = \log\left(\frac{N_{codes}}{P_{meta}}\right) \approx 20 \tag{3}$$

Therefore,

$$\tau = \frac{1}{2F_s N_\tau N_{ck,conf}} \tag{4}$$

This means $\tau = 41.67\,\mathrm{ps}$

We then see how we must size the input pair to provide the necessary gain for our minimum signal. We use the relationship for the exponential gain

$$v_{od}(t) = v_{id}(t) A_{v0} e^{\frac{1}{2\tau f cmax}} \tag{5}$$

where here we have $v_{id}(t) = 997\,\mathrm{pV}$, and $v_{od}(t) = V_{DD} - V_{th,n} \approx 950\,\mathrm{mV}$. We solve for the only unknown, giving

$$A_{v0} = \frac{v_{od}(t)}{v_{id}(t)} e^{-\frac{1}{2\tau f cmax}} \tag{6}$$

We begin our design using a comparator design with reasonable values. We will extract the regeneration time for this design, and sweep over some transistor widths to find times that are within the required τ spec calculated above. Values closest to this τ will be assumed maximum due to minimal power consumption to meet spec (faster τ = higher power consumption).

- Simulate using the "hw_comparator_testbench"
- Reasonable starting values: $W_{input} = 1\,\mu m$, $W_{current} = 3\,\mu m$, $W_{latch,n} = 1.5\,\mu m$, $W_{latch,p} = 2W_{latch,n} 3\,\mu m$, $W_{reset} = 3\,\mu m$