An 8-bit 450-MS/s Single-Bit/Cycle SAR ADC in 65-nm CMOS

Vaibhav Tripathi and Boris Murmann
Department of Electrical Engineering
Stanford University
Stanford, USA
vaibhavt@stanford.edu, murmann@stanford.edu

***Abstract*— A low-energy 8-bit 450-MS/s single-bit/cycle SAR ADC is presented. The design combines top-plate sampling, small unit capacitances (0.75 fF), symmetric DAC switching, and judicious delay optimization around a single high-speed comparator to achieve an ENOB of 7.6 at Nyquist, translating into an FOM of 76 fJ/conversion-step. The converter occupies an active area of 0.035 mm^2 in 65-nm CMOS.**

I. Introduction

Successive approximation ADCs are known for their outstanding power efficiency at low to moderate conversion rates. However, at high speeds (>100 MS/s) this advantage deteriorates as the constituent blocks are pushed against the speed limits of the process technology; this is an effect that is particularly pronounced in SAR ADCs due to the sequential nature of the conversion. Here, we report a single-channel, single-bit/cycle SAR ADC that was designed to advance the attainable throughput of the conventional SAR architecture while maintaining attractive power efficiency. To our knowledge, the design described this paper is the fastest SAR ADC containing only a single comparator reported to date.

The proposed converter combines a variety of design techniques: (1) judicious optimization of DAC settling and logic delay with asynchronous timing, (2) a comparator designed for the optimum tradeoff between its regeneration and reset delays, and (3) a symmetrically switched DAC using top-plate sampling and small unit capacitors. A potential application for this converter is within a time-interleaved array, where the combination of high-speed (leading to low channel count), low complexity (minimum number of offset-prone comparators) and small input capacitance (~160 fF) is highly valued.

This paper is organized as follows. Section II describes the overall ADC architecture along with the symmetrical DAC switching scheme. Section III presents circuit details including the optimization of the SAR loop, the comparator and the data capture latch. Section IV summarizes the measurement results along with a comparison to the current state-of-the-art.

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II. ADC Architecture and DAC Switching

Fig. 1 shows the ADC block diagram along with its 7-bit binary weighted capacitive DAC, which acquires the input via top plate sampling [1]. This allows us to resolve the first bit without redistributing any charge, which saves energy and improves speed. The capacitor C_{DIV} attenuates the DAC signal and sets the converter's full-scale range to 0.7 V peak-differential. This choice is preferred over a rail-to-rail input range to maintain linear input sampling up to high frequencies. The DAC reference voltage V_{REF} is generated off-chip and is decoupled with an internal 500 pF gate oxide capacitor. The decoupling capacitance is sized such that it supplies the dynamic currents with a maximum transient glitch of 1/3 LSB. As a result, the external voltage supplies only the relatively small average reference current. The input tracking begins with the positive edge of the incoming clock and its length is set to approximately 0.3 ns (13.5% duty cycle) via an on-chip delay line. The delay line is sized such that its jitter does not deteriorate the overall performance. Once the input is acquired, the SAR loop runs asynchronously until all bits are resolved. The asynchronous operation obviates the need for a fast external clock.

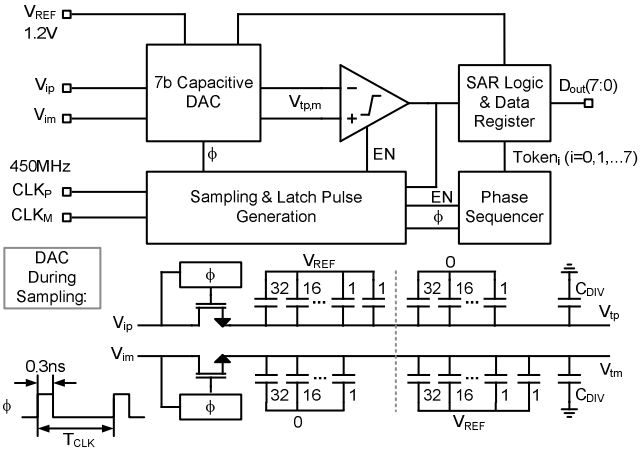

Fig. 1. ADC block diagram and DAC during sampling.

Using the original top plate sampling scheme of [1] requires a comparator with good common-mode (CM) rejection, since large CM jumps occur during charge redistribution. Capacitor splitting can be used to alleviate this issue [2]. The improved splitting used here achieves (nearly) symmetric switching and constant common mode. The MSB capacitance, which is usually formed by 64 unit elements, is split into 2x32 units that see opposite bottom plate voltages in the track phase (one set is charged against V_{REF}, the other against GND; see Fig. 1). This split is applied to all capacitances in the DAC, except for the LSB, which is minimum-size. As shown in Fig. 2 (using the MSB as an example), for every capacitance switching on the positive half of the circuit, there is an equal capacitance switching on the opposite side making the DAC transitions symmetric. The only exception occurs for the LSB transition, which is asymmetric but has almost no effect on the input common mode due to the inherently small step size.

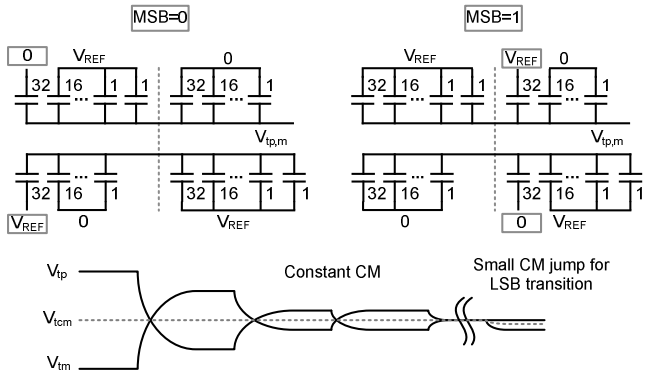

Fig. 2. DAC switching.

III. Circuit Design and Optimization

A. SAR Loop

The speed of a SAR ADC is limited by the sum of the delays through its main blocks (see Fig. 3): DAC settling (T_{DAC}), comparator decision time (T_C) and SAR logic delay (T_L). Maximizing the speed therefore boils down to a joint minimization of all three components. To illustrate the tradeoffs explored in this design, consider the DAC MSB circuit slice shown in Fig. 4. The DAC uses an inverter circuit to drive the bottom plates of the capacitors and the size of the PMOS device is defined by the required on-resistance during sampling. The optimum size for the NMOS follows from a more complex consideration that includes the loading of the SAR logic. Widening the NMOS improves the DAC settling time (T_{DAC}) during redistribution, but increases the logic delay (T_L). Consequently, there exists an optimum sizing that minimizes $T_L + T_{DAC}$ as shown. The optimum is shallow, but the reward for proper optimization is high, since the time savings multiply with the number of conversion cycles.

B. Comparator

Fig. 5 shows the comparator. It employs two pre-amplifiers to attenuate kickback to the input and to optimize reset and regeneration speed. The first stage provides a voltage gain of 8 dB while the second acts as a near unity gain buffer (when EN = 0). The loads of this buffer perform the reset of the latch and obviate the need for explicit reset switches, which would add capacitance that slows the regeneration. On the other hand, accurate and fast reset is needed due to the high effective clock rate of the loop (~4 GHz). Increasing the size of the PMOS load (W_P in Fig. 5) reduces the comparator reset time (T_R). However, it this also reduces the gain of the second preamp and increases the parasitic load at the latch's regenerative nodes. As a result, the comparator's regeneration time steadily increases with W_P and there exists an optimum that minimizes $T_C + T_R$ as shown in Fig. 6. With the described optimizations, the comparator achieves a regeneration time constant of approximately 6 ps (measured through post-layout simulations).

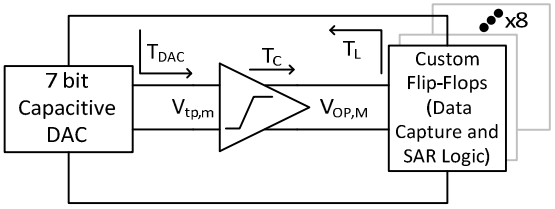

Fig. 3. Delays in the SAR loop.

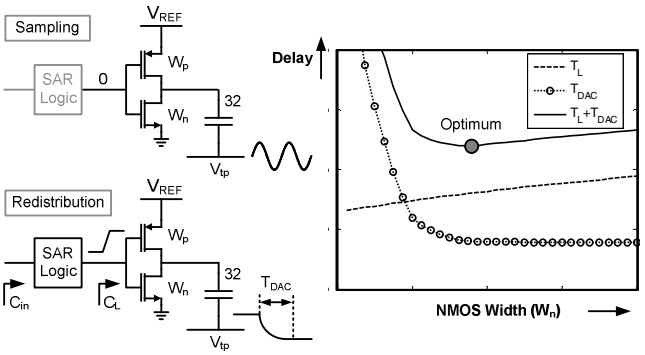

Fig. 4. Optimization of logic and DAC delay ($T_L + T_{DAC}$).

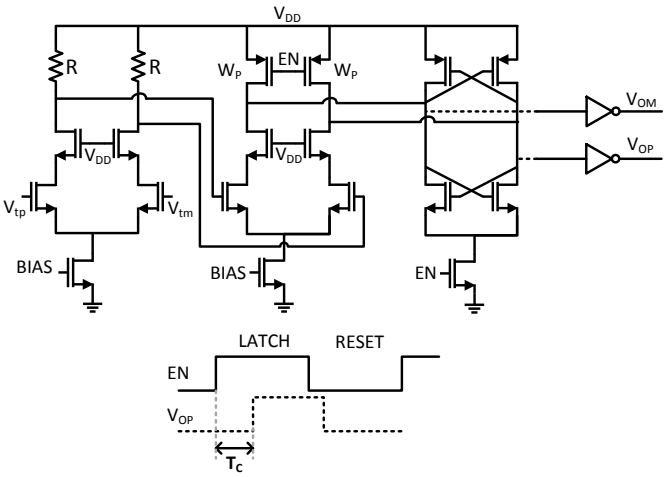

Fig. 5. Comparator schematic and timing.

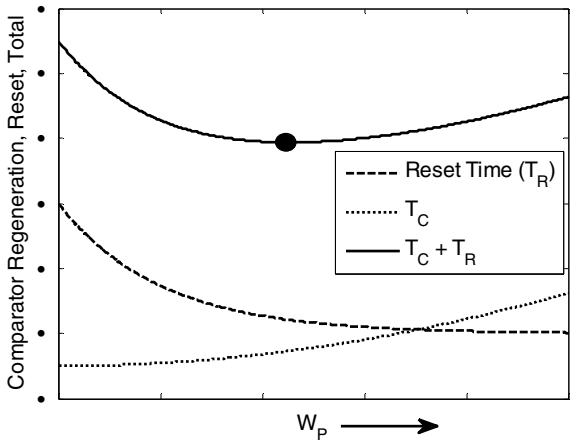

Fig. 6. Comparator optimization.

C. Data Capture Latch

During the conversion phase, the outputs of the comparator are captured by the data capture latch, which needs to perform the following two tasks: (1) Store the comparator decision (digital output) until the latch is reset for the next conversion cycle. (2) Feed back the comparator decision as quickly as possible to the capacitive DAC. This delay is part of the SAR loop delay and minimizing it is critical to achieve high conversion speed. In our design, we employ a custom designed latch (modified from [3]) for each of the 8 output bits (see Fig. 7). Transistors $M_{1A, B}$ are added and a delay is incorporated between the start of the sampling phase ($\phi \rightarrow 1$) and the latch reset phase ($\overline{RST} \rightarrow 0$) shown as 'Bit Out' time in Fig. 7. This allows us to store the latch state (D) and buffer it off-chip during sampling (without eating into the SAR conversion time) together with resetting both feedback nodes (FBP, FBM) to ground.

At the end of ADC sampling and latch reset ($\overline{RST} \rightarrow 1$) phase, the output nodes D/D' are pre-charged to V_{DD}, the comparator outputs $V_{OP, M}$ are reset to ground and the latch is ready for evaluation. This phase begins with the rising edge of $Token_i$, which enables the PMOS cross-coupled pair to resolve and store the corresponding comparator decision at nodes D/D'. This result is also fed back to the DAC via FBP and FBM. The PMOS cross-coupled devices are sized just large enough to latch nodes D/D' in the available time. This allows lower power dissipation and fast latch reset, but also results in smaller gain, which may cause incorrect DAC feedback if $Token_i$ is asserted during the comparator decision time. In this design, we added an NMOS cross-coupled pair ($M_{2A, B}$) across FBP/FBM to provide additional gain, thereby ensuring fast and correct feedback to the DAC. The clock to feedback delay ($Token_i$ to FBP/FBM) of the latch is 22 ps (measured through post layout simulation).

D. SAR Clock Generation

The required eight clock edges are generated asynchronously during the SAR operation in order to capture the output bits and also time the feedback to the DAC. Domino logic is used with its evaluation triggered by the comparator enable signal EN (see Fig. 8) so that the clock generation path stays out of the critical SAR loop delay (and does not limit the conversion speed).

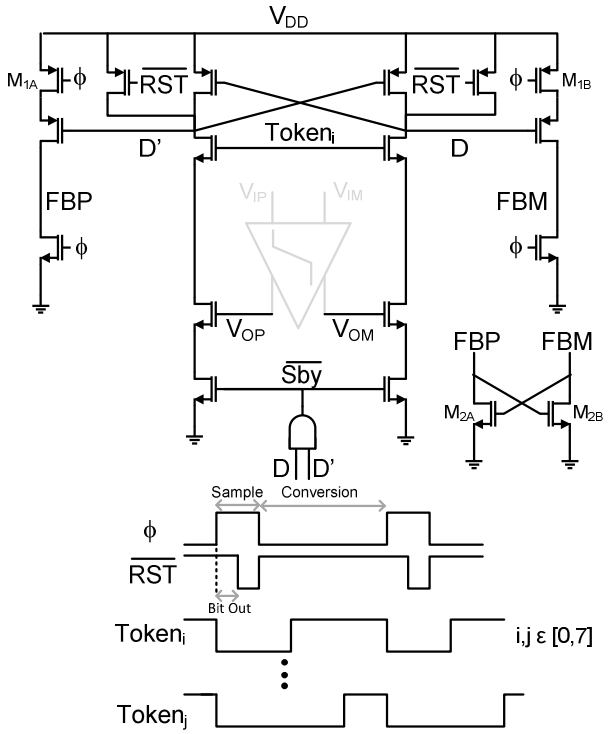

Fig. 7. Data capture latch and its timing diagram

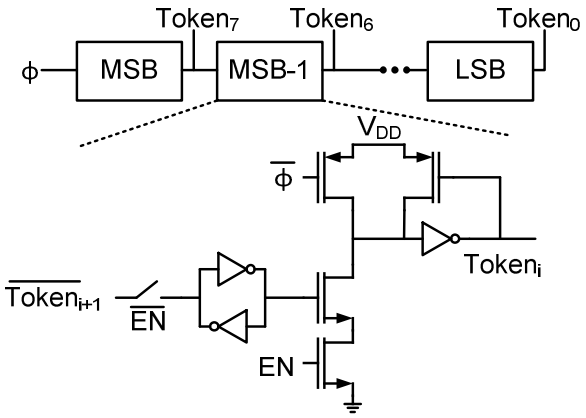

Fig. 8. SAR clock generation.

IV. Measurement Results and Conclusion

The prototype ADC is fabricated in a 1P9M 65-nm CMOS process with a core chip area of 0.035mm^2. The die micrograph with the corresponding layout is shown in Fig. 9. The output data is captured at full speed and fed to a PC for performance evaluation. Figs. 10 and 11 summarize the measurement results obtained at f_s = 450 MHz. The DNL and INL are within ±1 LSB, which indicates good matching of the small unit capacitors. The measured SNDR is nearly flat with input frequency (f_{in}) and the ADC achieves SNDR = 47.3 dB at Nyquist. It consumes 5.4 mA (including sampling clock generation, token generation, bias generation, and external reference current, but excluding digital I/O) from a supply

voltage of 1.2 V, with a dynamic contribution of approximately 57%. This translates into a FOM ($P/(f_s 2^{ENOB})$) of 76.1 fJ/conversion-step (at Nyquist). To our knowledge, this is the fastest (non-interleaved) SAR ADC containing a single comparator reported to date. It achieves approximately the same ratio of sampling rate to process f_T as [4], without the need for a second comparator and offset-calibration. Table I compares our prototype ADC to the current state-of-the-art and an FOM comparison is shown in Fig. 12 [8].

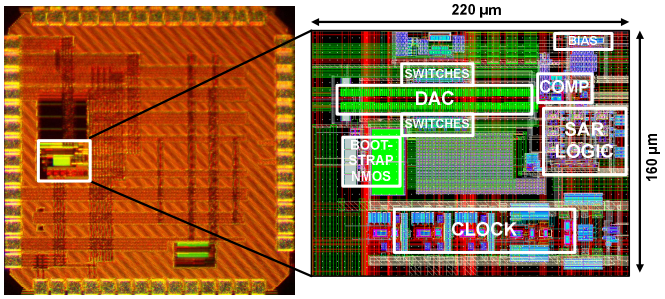

Fig. 9. Chip photo and layout.

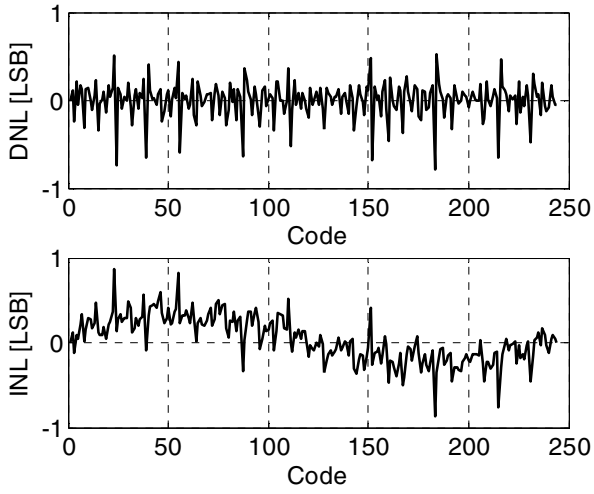

Fig. 10. Measured DNL and INL.

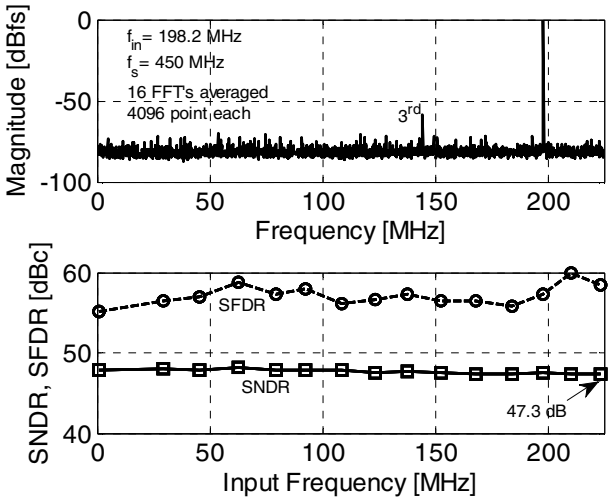

Fig. 11. Measured output spectrum, SFDR and SNDR.

TABLE I. PERFORMANCE COMPARISON

	[5]	[6]	[7]	[4]	This work
Architecture	**2b/cycle**	**1b/cycle**	**2b/cycle**	**1b/cycle (2 cmp)**	**1b/cycle (1 cmp)**
Technology [nm]	65	65	28	32	**65**
Supply Voltage [V]	1.2	1.2	1	1.0	**1.2**
Resolution [bits]	8	10	8	8	**8**
f_s [MS/s]	400	100	750	1200	**450**
SNDR (@Nyq) [dB]	40.4	56	43.3	37.8	**47.3**
FOM [fJ/conv-step]	116.9	21.9	50.2	32.9	**76**

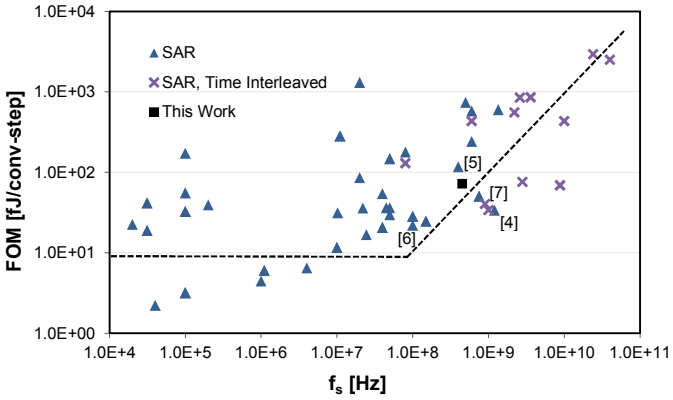

Fig. 12. FOM comparison

ACKNOWLEDGEMENTS

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