UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

Jan M. Rabaey | *Homework #6* | *EECS 141*

Due Monday, March 16, 5pm, box in 240 Cory

In last homework we have learned how to calculate the equivalent capacitance and resistance of a logic gate from basic device parameters. In this homework we will learn an alternative approach to extracting capacitance and resistance. We will do so through simulation.

1. Use the unit size inverter from homework #1 and construct a simulation schematic as shown in Fig. 1 below. V_{DD} is 1V. Specify the pulsating input source same as in homework #1 (500MHz, 10ps rise/fall time, V1=0V and V2=1V). Simulate the propagation delay in two loading cases: C_L=2fF and C_L=4fF. *(8 pts)*

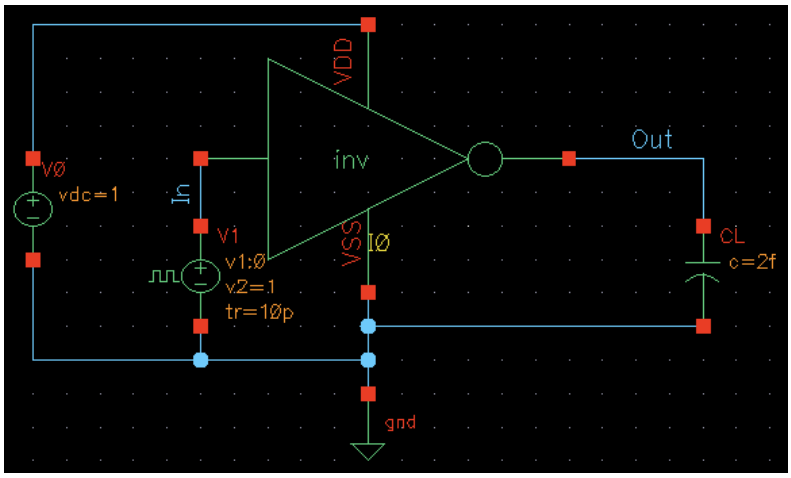


Figure 1 Simulation Schematic to Extract Inverter Resistance and Output Capacitance.

C_L	2fF	4fF
t_{pHL}	20.1ps	33.7ps
t_{pLH}	22.7ps	38.3ps

2. Next we will extract the equivalent capacitance and resistance of this inverter, assuming that propagation delay of an inverter can be approximated by

$$t_p = 0.69 \times R_{eq} \times C_{eq}$$

Use the results from Part 1 and estimate the equivalent resistance (R_{eq}) and total drain diffusion capacitance (C_d) of the inverter. To simplify the problem, assume that PMOS and NMOS have approximately equal on-resistance so that we can use the averaged delay instead of using separate high-to-low and low-to-high delay data. *(8 pts)*

$$\begin{cases} \dfrac{20.1ps + 22.7ps}{2} = 0.69 \times R_{eq} \times \left(C_d + 2fF\right) \\ \dfrac{33.7ps + 38.3ps}{2} = 0.69 \times R_{eq} \times \left(C_d + 4fF\right) \end{cases}$$

Therefore

$$\begin{cases} R_{eq} = 10.6k\Omega \\ C_d = 0.93fF \end{cases}$$

3. To estimate input capacitance of the inverter, replace the load capacitor in Fig. 1 with another unit-size inverter. Remember to load the additional inverter with a 2fF capacitor (Fig. 2). Simulate the propagation delay of the original inverter and estimate its input capacitance (C_g). *(8 pts)*

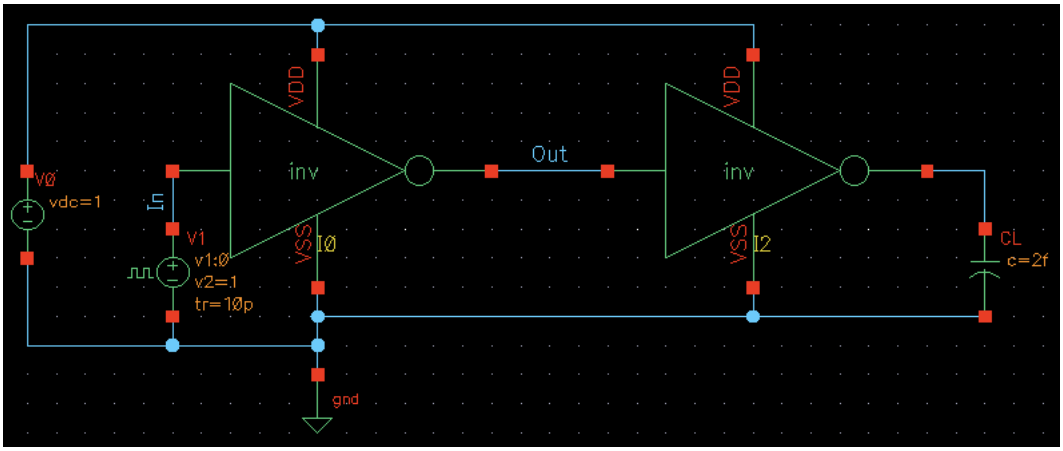


Figure 2 Simulation Schematic to Extract Inverter Input Capacitance.

From simulation:

$$\begin{cases} t_{pHL} = 10.2ps \\ t_{pLH} = 11.7ps \end{cases}$$

Therefore

$$\frac{10.2ps + 11.7ps}{2} = 0.69 \times 10.6k\Omega \times \left(C_g + 0.93fF\right)$$
$$C_g = 0.57fF$$

4. Now that we have the equivalent resistance and capacitance extracted, let us put them to use and compute the propagation delay of the FanOut-4 inverter in homework #1 (Fig. 3). Recall that your simulated result in homework #1 was

$$\frac{t_{pHL} + t_{pLH}}{2} = \frac{32.5ps + 39.5ps}{2} = 36ps$$

Explain why the discrepancy between calculation and simulation is within or beyond your expectation. *(10 pts)*

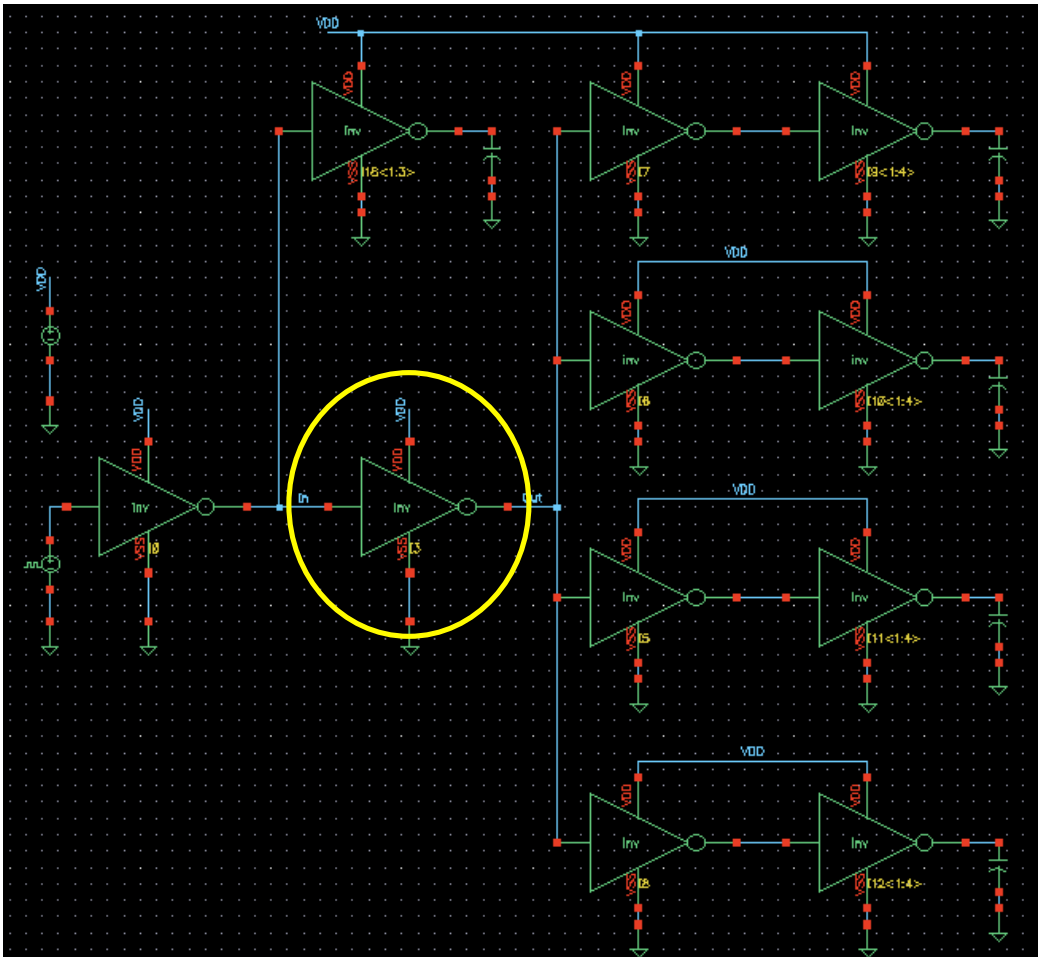


Figure 3 Simulation Schematic from Homework #1.

Hand calculation:

$$t_p = 0.69 \times R_{eq} \times \left(C_d + 4C_g\right) = 0.69 \times 10.6k\Omega \times \left(0.93fF + 4 \times 0.57fF\right)$$

$$t_p = 23.5ps$$

There is apparently large discrepancy between calculation and simulation, owing to several factors (model approximation, un-equal pull-up and pull-down, etc.). But the biggest factor is the finite rise and fall time at the inverter's input. The 0.69×R×C equation assumes step input. Actual input to the inverter however has finite slope. The simulated result is hence the sum of its step response time and the ramp time of input. As a matter of fact propagation delay at the inverter's input in Fig. 3 is

$$\frac{t_{pHL} + t_{pLH}}{2} = \frac{22.8ps + 27.4ps}{2} = 25.1ps$$

A more appropriate equation that calculates the delay with ramped input is

$$t_{p,ramp} = t_{p,step} + \frac{V_T^*}{V_{DD}} \times t_{p,in}$$

Or

$$36ps = 23.5ps + \frac{V_T^*}{1V} \times 25.1ps$$

$$V_T^* \approx 0.5V$$

5. Next we will research on another important aspect of digital circuit design: energy. Use the capacitance estimated in Parts 2 and 3, calculate dynamic power dissipation of the inverter circled in Fig. 3, then compare it with simulated average power dissipation. To isolate the inverter from rest of the circuit, a simple method is to insert an arbitrarily small resistor in series with the inverter's supply (Fig. 4). *(6 pts)*

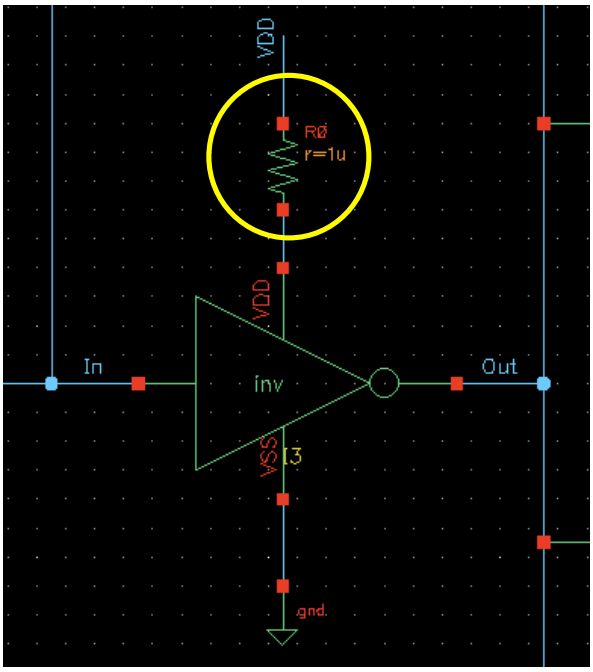


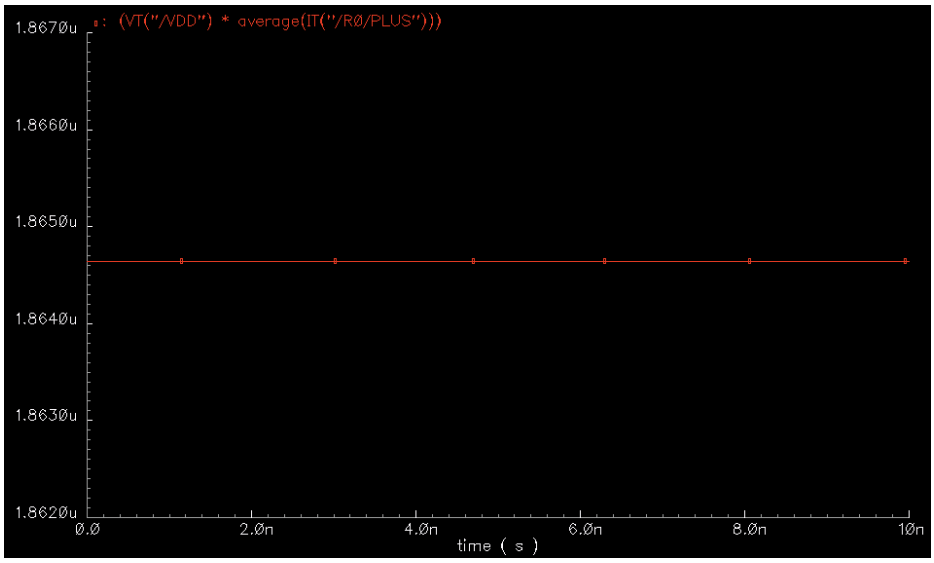
Figure 4 Adding a Small Resistor to the Inverter's Supply.

Hand calculation:

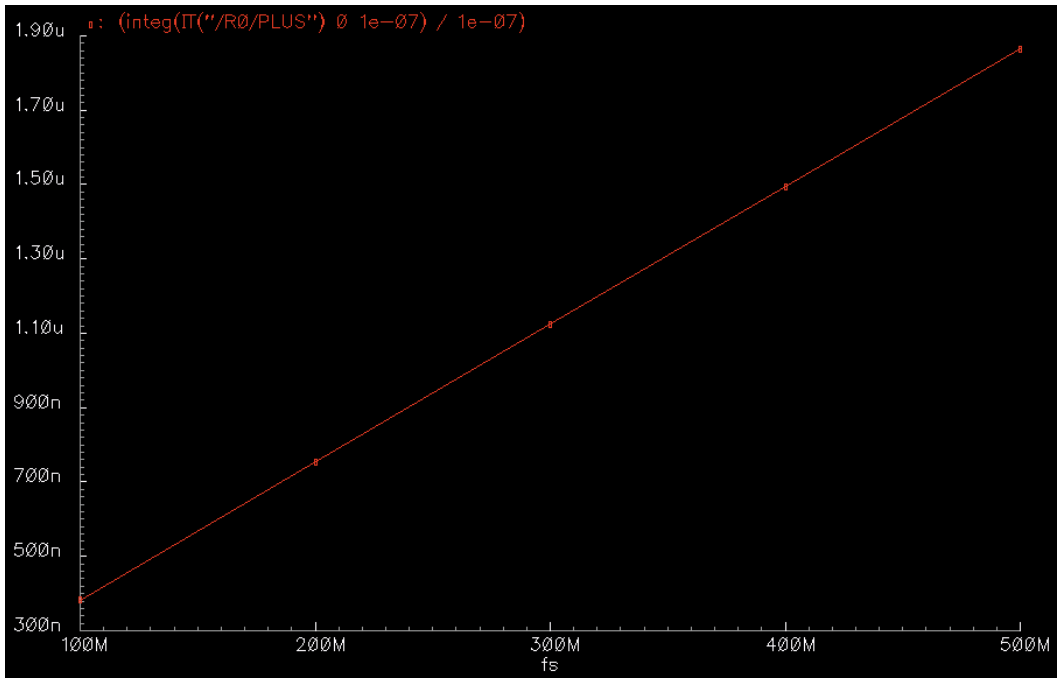
$$P = CV^2 f = \left(C_d + 4C_g\right) \times V_{DD}^2 \times f$$

$$P = \left(0.93f + 4 \times 0.57f\right) \times 1^2 \times 500M = 1.6\mu W$$

The simulated result is 1.86μW.



6. You may have noticed that the simulated power is higher than the calculated in Part 5. To explore the reasons, simulate the power dissipation at different clock frequencies (100MHz, 200MHz, 300MHz, … 500MHz) and plot power versus frequency. Does power extrapolate to 0 at DC? Why doesn't it? *(10 pts)*



Linear fit to above curve yields:

$$P = 3.7 \times 10^{-15} \times f + 12.6nW$$

Apparently when frequency (*f*) is 0, power is not. The extra 12.6nW can be considered the leakage power of this inverter.

7. You have learned from recent lectures that the dynamic power of an inverter actually consists of two parts: power due to charging and discharging load capacitance, and power due to short circuit conduction. Can you design an experiment in simulation that can separate these two parts in the total power dissipation? *(0 pts.* ***This part of the homework is optional and will not be graded. It is here to entertain your curiosity and creativity!****)*