EE 315
Project Milestone

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(Dated: November 9, 2017)

I. INVERTER CHAIN

We design an inverter chain to buffer the comparator outputs and drive a load capacitance of 50 fF. Using a FO4 approach, we can write the total necessary number of stages as

$$N = \log_4\left(\frac{C_{load}}{C_{inv}}\right) \tag{1}$$

where C_{inv} is the input capacitance for the unit inverter. Our unit inverter is sized using minimum sized nmos transistors such that $W_n = 180\,\text{nm}$ and $L_n = 90\,\text{nm}$. To reduce on resistance variation but to also minimize delay, the pmos is sized such that $W_p = 2 * W_n$ and $L_n = L_p$. To determine the input capacitance for our unit inverter, we set up the test bench as show in Figure 1. Here, we input a step response into a chain of inverters and probe the output at

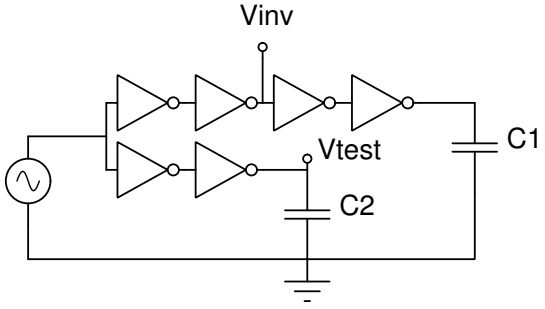

FIG. 1. Test bench for extracting the input capacitance of the unit inverter.

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two points. At V_{test} we probe the output into C_2 and sweep C_2 from 0.3 fF to 0.6 fF. We extract the rise and fall time from 0.1 to $0.9 \cdot V_{DD}$ and match to the rise and fall time at V_{inv}. Using this approach, we find that $C_{inv} = 0.52\,\text{fF}$. Therefore, our inverter chain with FO4 will have

$$N = \log_4\left(\frac{50\,\text{fF}}{0.52\,\text{fF}}\right) \approx 3 \tag{2}$$

and is shown below in Figure 2.

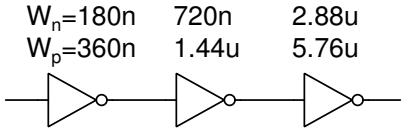

FIG. 2. Inverter chain design to drive a capacitive load of 50 fF. All lengths are minimum length = 90 nm

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II. DC ANALYSIS

We performed DC operating point analysis on the comparator design to extract transconductance for device M_0 and node capacitance at nodes *vop* and *vom* using CAPTAB.

We measured a transconductance of 151.1 µS and a capacitance of 14.4 fF.

III. REGENERATION TIME CONSTANT

The time constant for the comparator's positive feedback regeneration phase can be computed as

$$\tau = \frac{gm_0}{C_{vop}} = \frac{151.1 \times 10^{10}\,\mu\text{S}}{14.4\,\text{fF}} = 95.3\,\text{ps} \tag{3}$$

IV. SAMPLE RATE

The sample rate is fundamentally limited by the τ of the comparator combined with the desired reliability, here the probability of experiencing a metastable state on a given conversion - P_{meta}

Here, we can directly compute the minimum resolvable voltage at the input as

$$v_{id,min} = \frac{1}{2} P_{meta} LSB = 997\,\text{pV} \tag{4}$$

Where LSB is

$$LSB = \frac{V_{fullscale}}{2^{bits}} = 1.953\,\text{mV} \tag{5}$$

We can compute the number of time constants that we are required to wait for the output to resolve this voltage as

$$N_{taus} = ln\left(\frac{N_{codes}}{P_{meta}}\right) = 20.7 \tag{6}$$

With a clock duty cycle of 50% this allows us to define what the clock period is, as half of the clock cycle is devoted to waiting for the comparator to resolve.

$$T_{clk} = 2N_{taus} \cdot \tau = 3.954\,\text{ns} \tag{7}$$

$$F_{clk,max} = \frac{1}{T_{clk}} = 252.9\,\text{MHz} \tag{8}$$

As each conversion requires two cycles for sample and hold, and 10 cycles to perform the conversion, the sample frequency from this clock frequency is

$$T_{sample,max} = 12 \cdot T_{clk} = 47.448\,\text{ns} \tag{9}$$

$$F_{sample,max} = \frac{1}{T_{sample}} = 21.075\,\text{MS}\,\text{s}^{-1} \tag{10}$$

V. THERMAL NOISE VOLTAGE - HAND ANALYSIS

Prior to analyzing the circuit, we know we must extract the transistor γ. To do so, we create the test bench as shown in Figure 3. Here, we set the gate voltage equal to the V_{gs} extracted from the DC bias point (425.6 mV) and simulate the noise by creating a current controlled voltage source. The resulting gamma from the simulation is shown in Figure 4, for which we find $\gamma \approx 0.84$.

We can model the circuit using the small signal model. We therefore have a gain of

$$A_v = -\frac{g_{m_n}}{g_{ds_n} + g_{ds_p} - g_{m_p}} \tag{11}$$

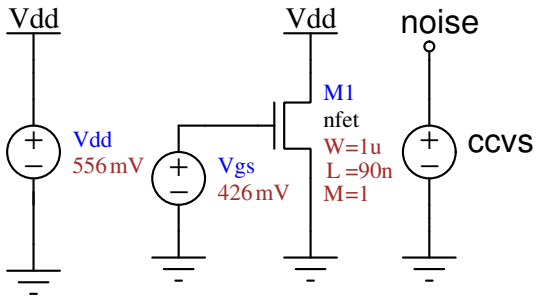

FIG. 3. Test bench for extracting γ for our technology.

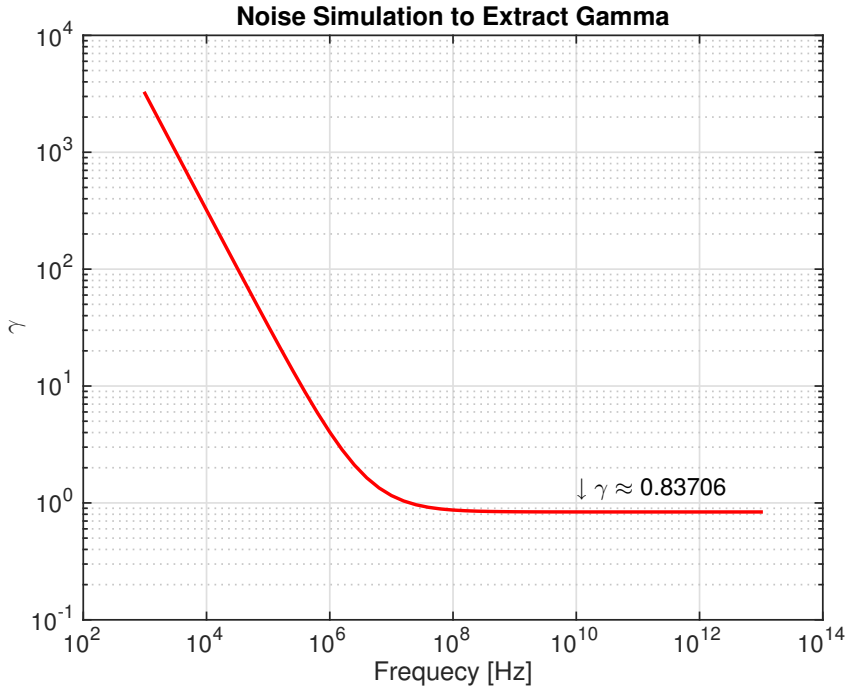

FIG. 4. Extracting γ for our technology.

The total thermal noise from the nmos and pmos transistors can be written at the output as

$$\overline{V_{out}^2} = 2\left(\overline{i_{d_n}^2} + \overline{i_{d_p}^2}\right) Z_{eq}^2 = 8kT\gamma\left(g_{m_n} + g_{m_p}\right) R_{eq}^2 \left|\frac{1}{1 + sR_{eq}C_L}\right|^2 \Delta f \tag{12}$$

where $R_{eq} = (r_{o,n}||r_{o,p})$ and where we multiply by two to consider the complete differential noise after the single ended equivalent analysis. Integrating over frequency gives

$$\overline{V_{out,tot}^2} = 2\gamma R_{eq}\left(g_{m_n} + g_{m_p}\right)\frac{kT}{C_L} \rightarrow \overline{V_{out,tot}} = 2.86\,\mathrm{mV_{RMS}} \tag{13}$$

We can then refer this to the input using the previously derived gain equation to find

$$\overline{V_{in,tot}^2} = \frac{\overline{V_{out,tot}^2}}{|A_v|^2} = \left(2\gamma\left(g_{m_n} + g_{m_p}\right) R_{eq}\frac{kT}{C_L}\right)\left(\frac{g_{ds_n} + g_{ds_p} - g_{m_p}}{g_{m_n}}\right)^2 \rightarrow = \overline{V_{in,tot}} = 2.68\,\mathrm{mV_{RMS}} \tag{14}$$

VI. THERMAL NOISE VOLTAGE - SIMULATION

We run the .noise simulation for the comparator test bench and find

$$\overline{V_{out,tot}} = 1.03\,\mathrm{mV_{RMS}} \tag{15}$$

Referring this back to the input using the gain derived from the previous section ($A_V = 1.0678$), we find

$$\overline{V_{in,tot}} = 0.96\,\mathrm{mV_{RMS}} \tag{16}$$

The output and input referred noise give a percent error of -64.08% with respect to the hand analysis.

VII. TRANSIENT NOISE SIMULATION

We run the transient noise simulation of the comparator setting FMAX such that

$$FMAX = \frac{10}{2\pi\tau} \approx 16.7\,\mathrm{GHz} \tag{17}$$

where τ is the regenerative time constant derived in section III. The simulation results and associated error function fit are shown in Figure 5. From the fit, we find that the associated input referred noise is $0.72\,\mathrm{mV_{RMS}}$, giving a percent error of -73.02% and -24.90% with respect to hand analysis and the .noise simulation.

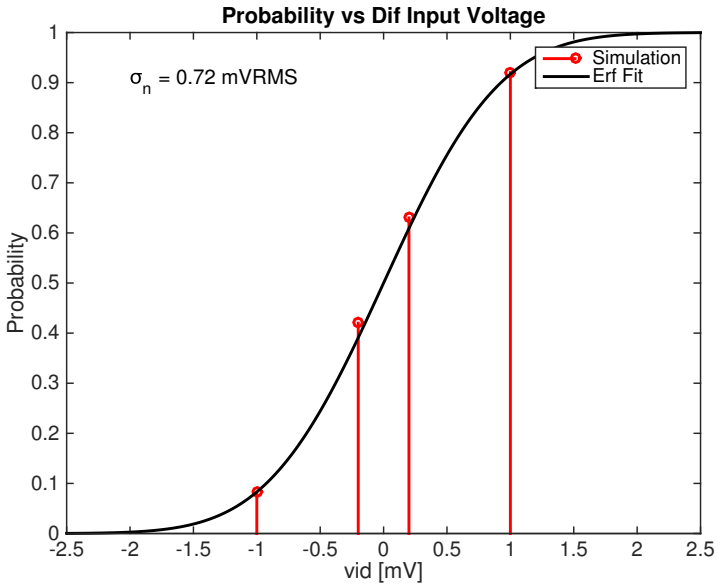

FIG. 5. Results from transient noise simulation at $-1\,\mathrm{mV}$,$-200\,\mu\mathrm{V}$,$-200\,\mu\mathrm{V}$, and $1\,\mathrm{mV}$

VIII. TOTAL DAC CAPACITANCE

The total DAC capacitance is simply the sum of all the DAC capacitors. In each DAC, there are 9 capacitors, with unit capacitor multipliers ($C_u = 2.5\,\mathrm{fF}$) of 1, 1, 2, 4, 8, 16, 32, 64, and 128. This gives

$$C_{DAC_{single}} = 256C_u = 0.64\,\mathrm{pF} \tag{18}$$

Therefore, the total DAC capacitance for the two DAC configuration is $1.28\,\mathrm{pF}$.

The total sampling noise is simply

$$\overline{v_{n,samp}^2} = \frac{2kT}{C_{DAC_{single}}} \rightarrow \overline{v_{n,samp}} = 0.11\,\mathrm{mV_{RMS}} \tag{19}$$

IX. SNR

To calculate the SNR, we must first find the total noise, which we write as

$$\overline{v_{n,total}^2} = \overline{v_{n,quant}^2} + \overline{v_{n,samp}^2} + \overline{v_{n,comp}^2} \tag{20}$$

where $\overline{v_{n,samp}^2}$ and $\overline{v_{n,comp}^2}$ were previously calculated. To calculte the sampling noise, we write

$$\overline{v_{n,quant}^2} = \frac{\Delta^2}{12} = \frac{\left(\frac{2V_{ref}}{2^B}\right)^2}{12} \rightarrow \overline{v_{n,quant}} = 0.5638\,\mathrm{mV_{RMS}} \tag{21}$$

where $V_{ref} = 1\,\mathrm{V}$. the total noise is then

$$\overline{v_{n,total}} = 0.92\,\mathrm{mV_{RMS}} \tag{22}$$

The SNR can be written as

$$SNR = 10\log_{10}\left(\frac{P_{sig}}{P_{noise}}\right) \tag{23}$$

Assuming a full scale signal from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$, we find

$$SNR = 57.68\,\mathrm{dB} \tag{24}$$

$$SQNR = 10\log_{10}\left(\frac{P_{sig}}{P_{n,quant}}\right) 61.97\,\mathrm{dB} \tag{25}$$

X. FINAL TRANSIENT SIMULATIONS

We first replace he ideal comparator with our comparator, including the inverter chain designed in Section I. The resulting simulation and associated FFT are shown in Figures 6 and 7. As our inverter chain solution has an odd count od inverters, we crossed the connection between the comparator and the SAR logic such that the VOP of the comparator through the buffer drives the complement input of the SAR logic, and vice-versa.

The input signal here is $\frac{3}{64} * F_{sample} = 984\,\text{kHz}$ with an amplitude of $2\,\text{V}p-p$. The output signal is referenced to $\pm 0.5\,\text{V}$, so for the sake of clear plotting for the transient plots, here we have doubled it.

To compute the signal to noise ratio, we compute a discrete fourier transform. Next we ratio the power of the fundamental tone to the power of the remainder of the transform, subtracting out the DC, along with first, third and fifth harmonics.

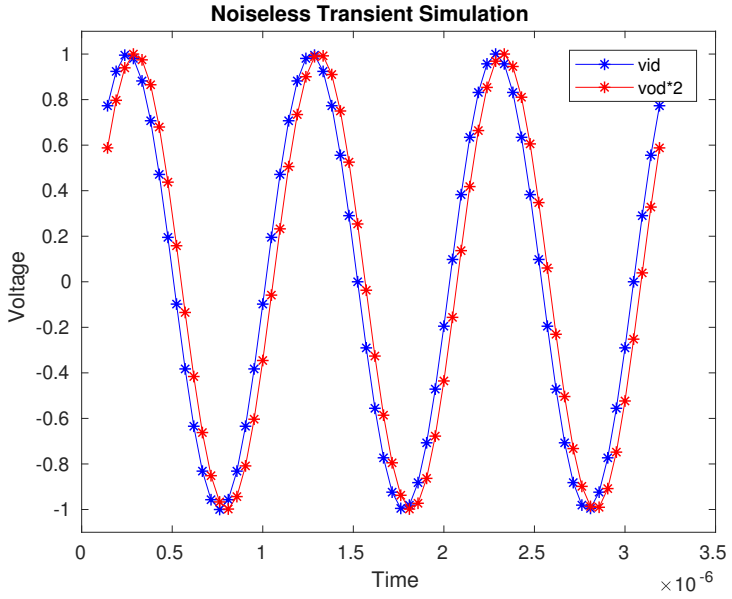

FIG. 6. Noiseless transient simulation.

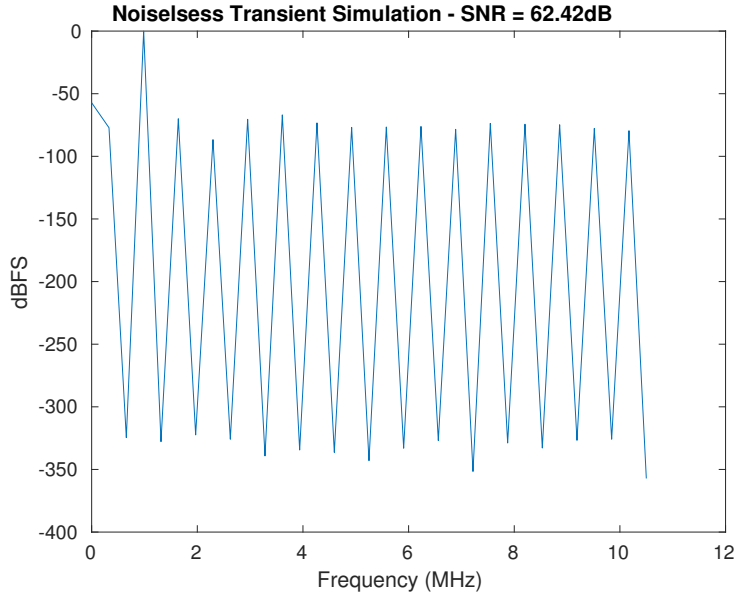

FIG. 7. Noiseless transient simulation FFT.

Here, we see that the SQNR for our simulation with no noise is 62.42 dB. This value closely matches the approximate ideal SQNR for a 10 bit ADC $SQNR_{ideal} = 6.02\,\text{dB} \cdot B + 1.76\,\text{dB} \approx 62\,\text{dB}$.

Finally, we simulate for and extract the SNR. For this, we run a transient noise simulation, the results of which are shown in Figure 8 and 9. From our simulations, we find $SNR = 60.77\,\text{dB}$.

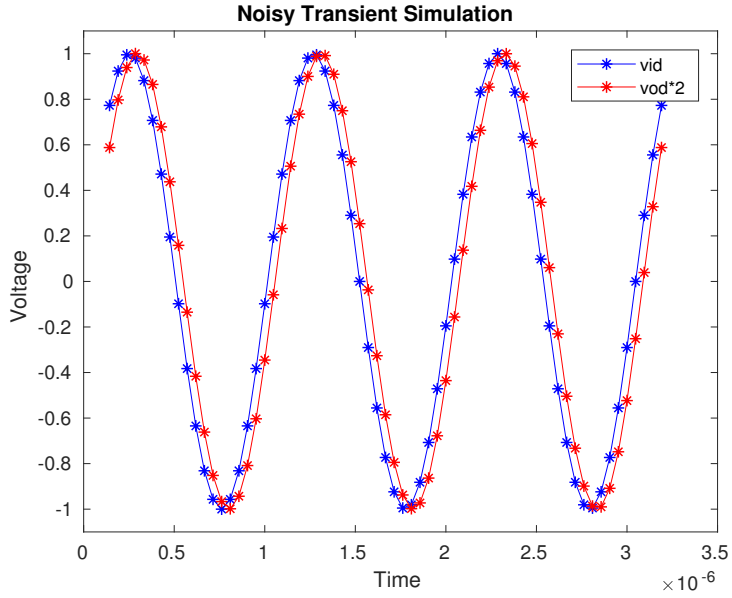

FIG. 8. Noisy transient simulation.

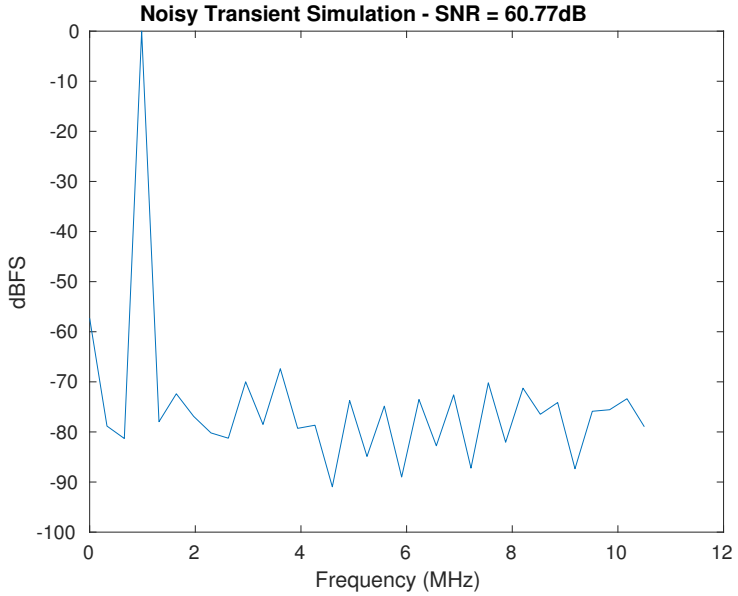

FIG. 9. Noisy transient simulation FFT.