EE 315
Final Project

Thomas Flores and Samuel Lenius

***Abstract*—Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Ut purus elit, vestibulum ut, placerat ac, adipiscing vitae, felis. Curabitur dictum gravida mauris. Nam arcu libero, nonummy eget, consectetuer id, vulputate a, magna. Donec vehicula augue eu neque. Pellentesque habitant morbi tristique senectus et netus et malesuada fames ac turpis egestas. Mauris ut leo. Cras viverra metus rhoncus sem. Nulla et lectus vestibulum urna fringilla ultrices. Phasellus eu tellus sit amet tortor gravida placerat. Integer sapien est, iaculis in, pretium quis, viverra ac, nunc. Praesent eget sem vel leo ultrices bibendum. Aenean faucibus. Morbi dolor nulla, malesuada eu, pulvinar at, mollis ac, nulla. Curabitur auctor semper nulla. Donec varius orci eget risus. Duis nibh mi, congue eu, accumsan eleifend, sagittis quis, diam. Duis eget orci sit amet orci dignissim rutrum.**

I. Introduction

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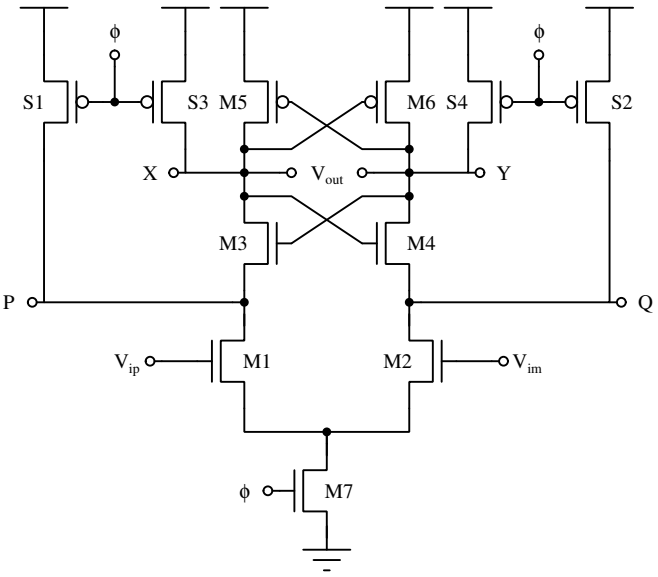

Fig. 1. Circuit topology for the strong arm latch comparator.

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II. Comparator

Proper optimization of the comparator element in the SAR ADC will provide the greatest improvement in our figure of merit, as it will ultimately set the maximum speed of our design. Given that our figure of merit is proportional to the power consumed for each decision, the ideal design includes a dynamic comparator which only draws current during the decision time. For this reason, we choose the Strong Arm Latch [1] for its energy efficiency and simple design.

To size our comparator to first order, we begin by considering the required noise specification of the total SAR ADC. We can derive the maximum noise power for our full-scale signal power as

$$\sigma_{n,in}^2 = \frac{P_{sig}}{10^{SNR_{spec}/10}} = \frac{\frac{(0.5V_{FS})^2}{2}}{10^{\frac{SNR_{spec}}{10}}} \tag{1}$$

Because we are designing to first order and expect some noise contribution from the other blocks, we impose a slightly higher noise spec of $60\,\mathrm{dB}$. This gives an input referred noise requirement of $\sigma_{n,in} = 707.11\,\mu\mathrm{V_{RMS}}$ for $V_{FS} = 2\,\mathrm{V}$.

We approximate the input referred noise for the strong arm latch as

$$\sigma_{n,in}^2 \approx \frac{8\gamma}{A_v}\frac{kT}{C_{P,Q}} \tag{2}$$

where the gain A_v during the amplification phase can be approximated as

$$A_v \approx \frac{g_{m1,2}}{I_D}V_{tn} \tag{3}$$

We select $\frac{g_m}{I_D} = 15$ as this provides a reasonable tradeoff between speed and power of the transistor (SHOW CURVE?). From simulations, we find that the approximate threshold voltage $V_{tn} \approx 250\,\mathrm{mV}$ for our nmos devices. We can then solve for the minimum capacitance necessary nodes P and Q using Equations 2, 3, and $\sigma_{n,in} = 707\,\mu\mathrm{V_{RMS}}$

$$C_{P,Q} \geq \frac{8\gamma}{A_v}\frac{kT}{\sigma_{n,in}^2} \rightarrow C_{P,Q} \geq 14.79\,\mathrm{fF} \tag{4}$$

To begin our design, we create a unit comparator constructed from some reasonable design choices. To maximize speed in the cross coupled inverters, we assume that pmos elements M5,6 should be twice the width of the nmos elements M3,4. To size M3,4, we must limit the widths so they do not signficantly contribute to the mismatch at the input. For our design with $A_v \approx 3.5$, this means that $W3,4 \geq \frac{1}{3.5}W1,2$ due to the offset referral to the input.

TABLE I
WIDTHS FOR COMPARATORS. ALL LENGTHS MINIMUM LENGTH $L = 90\,\mathrm{nm}$

Transistor	Unit	First Order Design	Optimized
M1,2	$1\,\mu\mathrm{m}$	?	?
M3,4	$\alpha W_{M1,2}$	?	?
M5,6	$2W_{M3,4}$	?	?
M7	?	?	?
S1,2	?	?	?
S3,4	?	?	?

III. Track and Hold

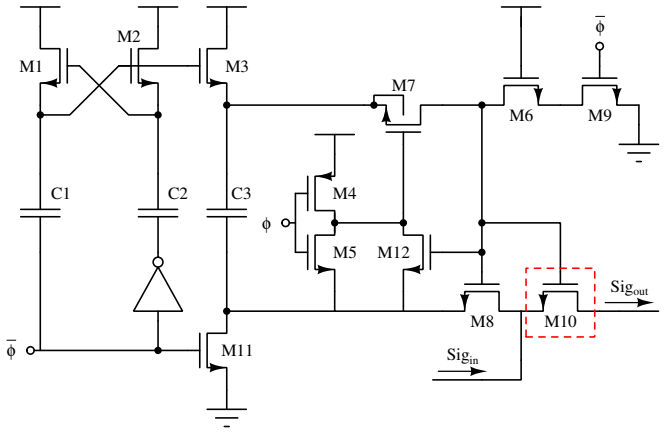

Fig. 2. Circuit topology for the bootstrapped switch for improved linearity.

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IV. 9 Bit Capacitive DAC

Here we implement a 9 bit capacitive constant common mode top plate sampling DAC as in [2013 Tripathi].

Each bit of the DAC is binary weighted with a single dummy value in the sequence 1, 1, 2, 4, 8, 16, 32, 64, 128. For each bit there is both the top plate sampled capacitor and the corresponding inverter cell.

In order to have equal time constants between capacitors and inverter cells, equal scaling parameters are applied to each, hence the device widths of the cells follow the same sequence as the capacitors.

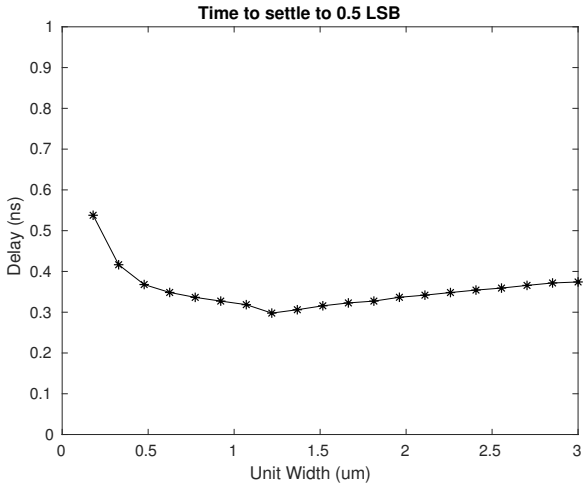

Fig. 3. Optimization of settling time vs device unit width.

One complication of this approach is that the electrical effort to drive the inverters scales with this same sequence. Hence as the driver inverters scale up, the sequence of gate drive buffers must as well for optimal delay and power consumption. This leads to each DAC inverter cell being designed individually for the expected range of electrical effort of that cell across optimization.

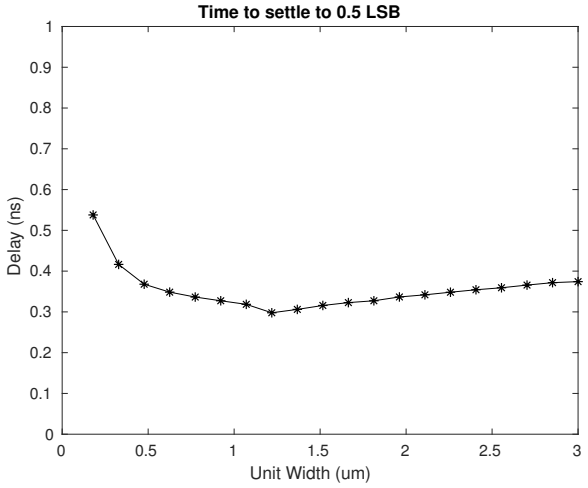

Fig. 4. DAC inverter unit cells.

Our initial implementation of the inverter cell followed [2013 Tripathi] however we found that by using an inverter and a pair of N-channel devices we were able to achieve lower total delay and settling time.

The specific issue with a standard inverter cell was that as the DAC switched it's MSB or MSB-1 bits, the dV/dT induced currents through the P-channel devices of the MSB-1 and MSB-2 cells caused a disturbance that reduced the gate overvoltage, hence increasing channel resistance and lengthening the duration of the glitch.

By using a pair of N-channel devices we have applied a much higher gate overvoltage, and additionally the switching glitches now increase the gate overvoltage, improving the recovery time for glitches. The use of two N channel devices here reduces the total gate capacitance to drive by a factor of two while reducing the output node parasitic capacitance, hence reducing DAC power overall.

Using a criterion of settling to within 1/2 LSB our optimized design has a delay of 370ps. Accounting for the 1% parasitic capacitance to ground on the top plate of the DAC capciators, our DAC reference voltage is 606mV in this design.

V. Asynchronous Reset Logic

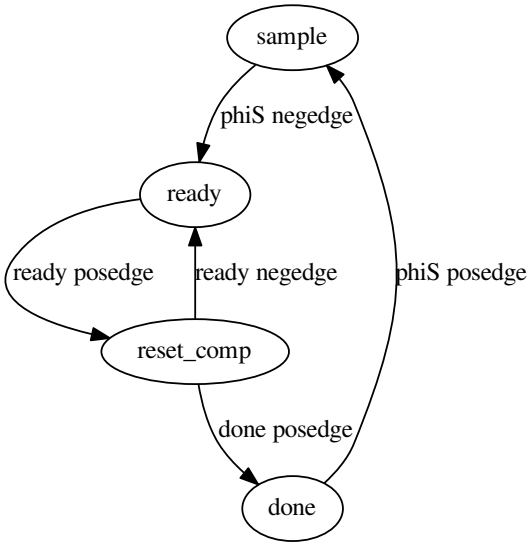

Fig. 5. State transition diagram for asynchronous reset logic.

In this ADC we implement asynchronous reset logic as in [2006 Chen]. The state machine that our asynchronous logic implements is as follows.

First the sampling clock edge rises, this opens the sampling gates and resets the internal state of the logic.

Second, the sampling clock drops and the asynchronous clock rises, enabling the dynamic comparator.

Third, the comparator makes a decision an one of it's two output lines drops. The outputs of the comparator are tied to the inputs of NAND gate as well as a buffer chain to drive the logic. The reset state of the comparator has both lines high, hence the output of the NAND is low. Once the comparator has made a decision, the output of the NAND is high, we call this signal 'Ready'. When Ready rises, we sample and shift one bit, and drop the asynchronous clock.

Fourth, after the bit is sampled, we reset the comparator. Here again we use the Ready signal to indicate that this step is finished. Once both of the comparator's output lines rise, the NAND's output will go to zero and we're prepared to convert

the next bit. The Ready signal dropping will cause the clock to rise again, reenabling the comparator.

Fifth, once all 10 bits are shiftd out, we assert the done signal internally to the logic and the comparator is held in low power reset, ready for when the next sample comes in.

REFERENCES

[1] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17. [Online]. Available: http://ieeexplore.ieee.org/document/7130773/