EE 315
Project Milestone

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I. INVERTER CHAIN

We design an inverter chain to buffer the comparator outputs and drive a load capacitance of 50 fF. Using a FO4 approach, we can write the total necessary number of stages as

$$N = \log_4\left(\frac{C_{load}}{C_{inv}}\right) \tag{1}$$

where C_{inv} is the input capacitance for the unit inverter. Our unit inverter is sized using minimum sized nmos transistors such that $W_n = 180\,\text{nm}$ and $L_n = 90\,\text{nm}$. To reduce on resistance variation but to also minimize delay, the pmos is sized such that $W_p = 2 * W_n$ and $L_n = L_p$. To determine the input capacitance for our unit inverter, we set up the test bench as show in Figure 1. Here, we input a step response into a chain of inverters and probe the output at

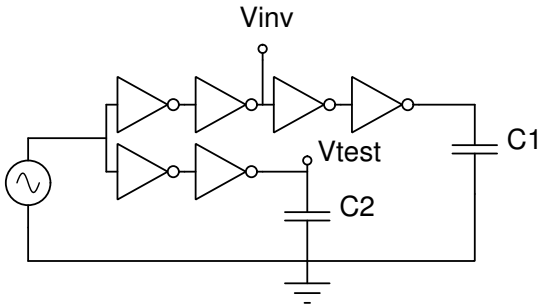

FIG. 1. Test bench for extracting the input capacitance of the unit inverter.

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two points. At V_{test} we probe the output into C_2 and sweep C_2 from 0.3 fF to 0.6 fF. We extract the rise and fall time from 0.1 to $0.9 \cdot V_{DD}$ and match to the rise and fall time at V_{inv}. Using this approach, we find that $C_{inv} = 0.52\,\text{fF}$. Therefore, our inverter chain with FO4 will have

$$N = \log_4\left(\frac{50\,\text{fF}}{0.52\,\text{fF}}\right) \approx 3 \tag{2}$$

and is shown below in Figure 2.

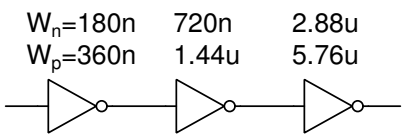

FIG. 2. Inverter chain design to drive a capacitive load of 50 fF. All lengths are minimum length = 90 nm

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II. DC ANALYSIS

III. REGENERATION TIME CONSTANT

IV. SAMPLE RATE

V. THERMAL NOISE VOLTAGE

We can model the circuit using the small signal model. We therefore have a gain of

$$A_v = -\frac{g_{m_n}}{g_{ds_n} + g_{ds_p} - g_{m_p}} \tag{3}$$

The thermal noise sources from the nmos and pmos transistors can be written at the output as

$$\overline{V_{out,tot}^2} = 2 \cdot \left(\frac{4kT\gamma}{g_{m_p}} + \gamma g_{m_n} \left(r_{o,n} || r_{o,p} \right) \frac{kT}{C_L} \right) \tag{4}$$

$$\overline{i_d^2} = 4kT\gamma g_{m_{n,p}} \Delta f \tag{5}$$

where we will assume $\gamma = \frac{2}{3}$. This noise current will be dropped into the output, which sees

$$Z_{out} = \frac{1}{sC_L} || R_{out} = \frac{R_{out}}{1 + sC_L R_{out}} \tag{6}$$

. where $R_{out} = r_{o,n} || r_{o,p}$. This gives

$$\overline{V_{out,tot}^2} = \int_0^\infty 4kT\gamma (g_{m_n} + g_{m_p}) \left(r_{o,n} || r_{o,p} \right)^2 \left| \frac{1}{1 + \left(r_{o,n} || r_{o,p} \right) (2\pi f C_L)} \right|^2 df = \gamma \left(g_{m_n} + g_{m_p} \right) \left(r_{o,n} || r_{o,p} \right) \frac{kT}{C_L} \tag{7}$$

We can then refer this to the input using the previously derived gain equation to find

$$\overline{V_{in,tot}^2} = \frac{\overline{V_{out,tot}^2}}{|A_v|^2} \left(\gamma \left(g_{m_n} + g_{m_p} \right) \left(r_{o,n} || r_{o,p} \right) \frac{kT}{C_L} \right) \left(\frac{g_{ds_n} + g_{ds_p} - g_{m_p}}{g_{m_n}} \right)^2 \tag{8}$$