EE 315
Project Milestone

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I. INVERTER CHAIN

We design an inverter chain to buffer the comparator outputs and drive a load capacitance of 50 fF. Using a FO4 approach, we can write the total necessary number of stages as

$$N = \log_4\left(\frac{C_{load}}{C_{inv}}\right) \tag{1}$$

where C_{inv} is the input capacitance for the unit inverter. Our unit inverter is sized using minimum sized nmos transistors such that $W_n = 180\,\text{nm}$ and $L_n = 90\,\text{nm}$. To reduce on resistance variation but to also minimize delay, the pmos is sized such that $W_p = 2 * W_n$ and $L_n = L_p$. To determine the input capacitance for our unit inverter, we set up the test bench as show in Figure 1. Here, we input a step response into a chain of inverters and probe the output at

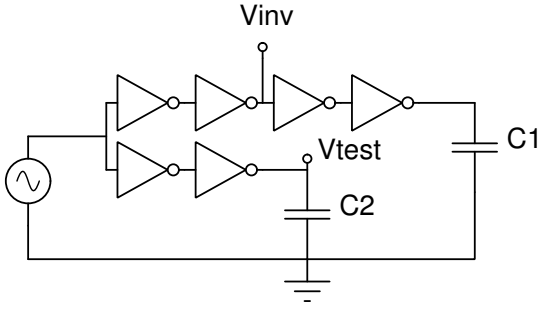

FIG. 1. Test bench for extracting the input capacitance of the unit inverter.

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two points. At V_{test} we probe the output into C_2 and sweep C_2 from 0.3 fF to 0.6 fF. We extract the rise and fall time from 0.1 to $0.9 \cdot V_{DD}$ and match to the rise and fall time at V_{inv}. Using this approach, we find that $C_{inv} = 0.52\,\text{fF}$. Therefore, our inverter chain with FO4 will have

$$N = \log_4\left(\frac{50\,\text{fF}}{0.52\,\text{fF}}\right) \approx 3 \tag{2}$$

and is shown below in Figure 2.

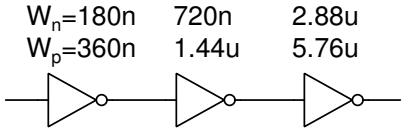

FIG. 2. Inverter chain design to drive a capacitive load of 50 fF. All lengths are minimum length = 90 nm

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II. DC ANALYSIS

We performed DC operating point analysis on the comparator design to extract transconductance for device M_0 and node capacitance at nodes *vop* and *vom* using CAPTAB.

We measured a transconductance of $151.1\mu S$ and a capacitance of 14.4fF.

III. REGENERATION TIME CONSTANT

The time constant for the comparator's positive feedback regeneration phase can be computed as

$$\tau = \frac{gm_0}{C_{vop}} = \frac{151.1 \times 10^{10}\,\mu\text{S}}{14.4fF} = 95.3ps \tag{3}$$

IV. SAMPLE RATE

The sample rate is fundamentally limited by the τ of the comparator combined with the desired reliability, here the probability of experiencing a metastable state on a given conversion - P_{meta}

Here, we can directly compute the minimum resolvable voltage at the input as

$$v_{id,min} = 0.5 * P_{meta} * LSB = 997pV \tag{4}$$

Where LSB is

$$LSB = \frac{V_{fullscale}}{2^{bits}} = 1.953mV \tag{5}$$

We can compute the number of time constants that we are required to wait for the output to resolve this voltage as

$$N_{taus} = ln(\frac{N_{codes}}{P_{meta}}) = 20.7 \tag{6}$$

With a clock duty cycle of 50% this allows us to define what the clock period is, as half of the clock cycle is devoted to waiting for the comparator to resolve.

$$T_{clk} = 2 * N_{taus} * \tau = 3.954ns \tag{7}$$

$$F_{clk,max} = \frac{1}{T_{clk}} = 252.9MHz \tag{8}$$

As each conversion requires two cycles for sample and hold, and 10 cycles to perform the conversion, the sample frequency from this clock frequency is

$$T_{sample,max} = 12 * T_{clk} = 47.448ns \tag{9}$$

$$F_{sample,max} = \frac{1}{T_{sample}} = 21.075MS/s \tag{10}$$

V. THERMAL NOISE VOLTAGE

We can model the circuit using the small signal model. We therefore have a gain of

$$A_v = -\frac{g_{m_n}}{g_{ds_n} + g_{ds_p} - g_{m_p}} \tag{11}$$

The thermal noise sources from the nmos and pmos transistors can be written at the output as

$$\overline{V_{out,tot}^2} = 2 \cdot \left(\frac{4kT\gamma}{g_{m_p}} + \gamma g_{m_n} \left(r_{o,n} || r_{o,p}\right) \frac{kT}{C_L} \right) \tag{12}$$

We can then refer this to the input using the previously derived gain equation to find

$$\overline{V_{in,tot}^2} = \frac{\overline{V_{out,tot}^2}}{|A_v|^2} \left(\gamma \left(g_{m_n} + g_{m_p}\right) \left(r_{o,n} || r_{o,p}\right) \frac{kT}{C_L} \right) \left(\frac{g_{ds_n} + g_{ds_p} - g_{m_p}}{g_{m_n}} \right)^2 \tag{13}$$