EE 315
Final Project

Thomas Flores and Samuel Lenius

***Abstract*—Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Ut purus elit, vestibulum ut, placerat ac, adipiscing vitae, felis. Curabitur dictum gravida mauris. Nam arcu libero, nonummy eget, consectetuer id, vulputate a, magna. Donec vehicula augue eu neque. Pellentesque habitant morbi tristique senectus et netus et malesuada fames ac turpis egestas. Mauris ut leo. Cras viverra metus rhoncus sem. Nulla et lectus vestibulum urna fringilla ultrices. Phasellus eu tellus sit amet tortor gravida placerat. Integer sapien est, iaculis in, pretium quis, viverra ac, nunc. Praesent eget sem vel leo ultrices bibendum. Aenean faucibus. Morbi dolor nulla, malesuada eu, pulvinar at, mollis ac, nulla. Curabitur auctor semper nulla. Donec varius orci eget risus. Duis nibh mi, congue eu, accumsan eleifend, sagittis quis, diam. Duis eget orci sit amet orci dignissim rutrum.**

I. INTRODUCTION

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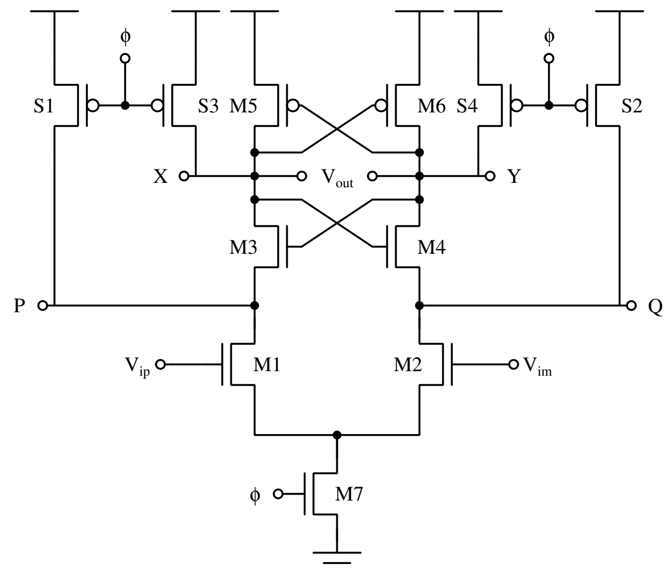

Fig. 1. Circuit topology for the strong arm latch comparator.

II. COMPARATOR

Proper optimization of the comparator element in the SAR ADC will provide the greatest improvement in our figure of merit, as it will ultimately set the maximum speed of our design. Given that our figure of merit is proportional to the power consumed for each decision, the ideal design includes a dynamic comparator which only draws current during the decision time. For this reason, we choose the Strong Arm Latch [1] for its energy efficiency and simple design.

To size our comparator to first order, we begin by considering the required noise specification of the total SAR ADC. We can derive the maximum noise power for our full-scale signal power as

$$\sigma_{n,in}^2 = \frac{P_{sig}}{10^{SNR_{spec}/10}} = \frac{\frac{(0.5V_{FS})^2}{2}}{10^{\frac{SNR_{spec}}{10}}} \tag{1}$$

Because we are designing to first order and expect some noise contribution from the other blocks, we impose a slightly higher noise spec of $60\,\mathrm{dB}$. This gives an input referred noise requirement of $\sigma_{n,in} = 707.11\,\mu\mathrm{V_{RMS}}$ for $V_{FS} = 2\,\mathrm{V}$.

We approximate the input referred noise for the strong arm latch as

$$\sigma_{n,in}^2 \approx \frac{8\gamma}{A_v} \frac{kT}{C_{P,Q}} \tag{2}$$

where the gain A_v during the amplification phase can be approximated as

$$A_v \approx \frac{g_{m1,2}}{I_D} V_{tn} \tag{3}$$

We select $\frac{g_m}{I_D} = 15$ as this provides a reasonable tradeoff between speed and power of the transistor (SHOW CURVE?). From simulations, we find that the approximate threshold voltage $V_{tn} \approx 250\,\mathrm{mV}$ for our nmos devices. We can then solve for the minimum capacitance necessary nodes P and Q using Equations 2, 3, and $\sigma_{n,in} = 707\,\mu\mathrm{V_{RMS}}$

$$C_{P,Q} \geq \frac{8\gamma}{A_v} \frac{kT}{\sigma_{n,in}^2} \rightarrow C_{P,Q} \geq 14.79\,\mathrm{fF} \tag{4}$$

To begin our design, we create a unit comparator constructed from some reasonable design choices. To maximize speed in the cross coupled inverters, we assume that pmos elements M5,6 should be twice the width of the nmos elements M3,4. To size M3,4, we must limit the widths so they do not signficantly contribute to the mismatch at the input. For our design with $A_v \approx 3.5$, this means that $W3,4 \geq \frac{1}{3.5} W1,2$ due to the offset referral to the input.

TABLE I
DEFAULT

test	test

III. Track and Hold

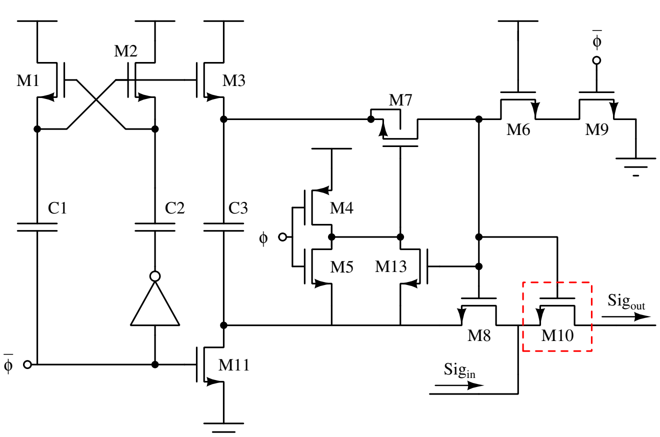

Fig. 2. Circuit topology for the bootstrapped switch for improved linearity.

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References

[1] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17. [Online]. Available: http://ieeexplore.ieee.org/document/7130773/