DESIGN OF HIGHLY LINEAR SAMPLING SWITCHES FOR CMOS TRACK-AND-HOLD CIRCUITS

Examensarbete utfört i Elektroniksystem

vid Linköpings Tekniska Högskola

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Muhammad Irfan Kazim

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Abstract

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Results indicate that for a specified supply of 3.3 Volts, bulk-effect compensation does not improve third-order harmonic distortion significantly which defines the upper most limit on linearity for a differential topology. However, for low-voltage operations bulk-effect compensation improves third-order harmonic noticeably.

Keywords
Switch non-linearities, Bootstrap switch, Bulk-effect compensation switch, Charge injection

ABSTRACT

This thesis discusses non-linearities associated with a sampling switch and compares transmission gate, bootstrapping and bulk-effect compensation architectures at a circuit level from linearity point of view for 0.35υm n-well CMOS process. All the switch architectures have been discussed and designed with an additional constraint of switch reliability.

Results indicate that for a specified supply voltage of 3.3 volts, bulk-effect compensation does not improve third order harmonic distortion significantly which defines the upper most limit on linearity for a differential topology. However, for low voltage operations bulk-effect compensation improves third-order harmonic distortion noticeably.

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TABLE OF CONTENTS

1

INTRODUCTION

Sampling of the time-varying input signal is the first step in any type of Analog to Digital (A/D) conversion. For high-resolution and high-speed A/D converter, a high-performance Sample and Hold (S/H) circuit is needed as its frontend component. Linearity of the frontend Sample and Hold circuit directly impacts the linearity of the consequent stages of A/D converter. High- performance sample and hold circuits are usually implemented as discrete-time circuits, often as Switched Capacitor (SC) circuits. The high linearity of SC S/H circuits is limited by the input sampling switch and the signal dependent amplifier non-linearity. [6]

Sampling switch non-linearity is mainly attributed to non-linear on resistance and associated parasitic capacitance which produce harmonic distortion when sampling high-frequency signals. This limits not only SINAD (Signal to Noise and Distortion Ratio) but also SFDR (Spurious Free Dynamic Range) and THD (Total Harmonic Distortion) which are fundamental metrics to measure linearity.

In this thesis transmission gate and three different bootstrapping switch architectures with and without bulk-effect compensation have been analyzed. The objective is to achieve maximum linearity with rail to rail swing when used in a differential topology at an input signal frequency of 50 MHz and sampling clock of 100 MHz. Out of these architectures, the gate-source signal dependent bootstrapping switch without bulk effect compensation [6] has been found the best to achieve linearity of more than 87 DB with rail to rail swing at an intended input and sampling clock frequencies. It approaches to equivalent 14-bit linearity. All these switches have been additionally designed with con-

straints of device reliability and implementation in 0.35um standard n-well CMOS (Complimentary Metal Oxide Semiconductor) technology for reduced process costs.

1.1 SOURCES OF NON-LINEARITY IN A SAMPLING SWITCH

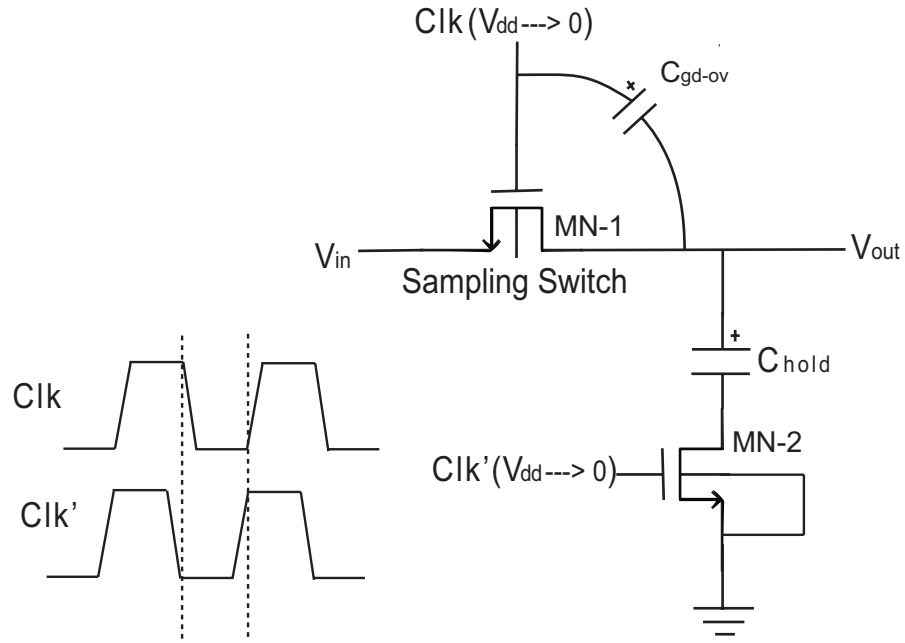

Figure 1.1: Bottom-plate sampling in the simplest track and hold circuit

Figure 1.1 shows the simplest track-and-hold circuit. When Clk is high, the switch is turned on and charge is stored on the capacitor to V_{in}. When Clk is low, the switch turns off and the capacitor will hold the sampled voltage. The on-resistance of this switch is given by

$$R_{on}(t) = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs}(t) - V_t(t))} \tag{1.1}$$

Where

$$V_{gs}(t) = V_g - V_{in}(t) \tag{1.2}$$

$$V_t(t) = V_{t0} + \Upsilon(\sqrt{2|\Phi_F| + V_{SB}(t)} - \sqrt{2|\Phi_F|}) \tag{1.3}$$

$$V_{SB}(t) = V_{in}(t) - V_B \tag{1.4}$$

The time-varying input signal $V_{in}(t)$ dependence of $R_{on}(t)$ in $V_{gs}(t)$ and $V_t(t)$ in Eq. (1.1) is the cause of the non-linearity and harmonic distortion in the sampling switch. Bootstrapping technique is used to make $V_{gs}(t)$ constant and thus free from input signal dependence. This reduces non-linearity in on-resistance to a great extent. Bulk effect-compensation further reduces non-linearity in on-resistance by connecting source terminal directly to bulk terminal.

The on-resistance R_{on} together with the sampling capacitor C_{hold} forms the RC time-constant that defines the -3 dB bandwidth during track mode. It is defined as follows.

$$f_{-3dB} = \frac{1}{2\pi R_{on} C_{hold}} = \frac{1}{2\pi} \cdot \frac{u_n C_{ox} \frac{W}{L}(V_{gs}(t) - V_t(t))}{C_{hold}} \tag{1.5}$$

From Eq. (1.5), it is clear that to achieve high input bandwidth for a fixed sampling capacitor, the on-resistance R_{on} needs to be small. Also for a given switch size and supply voltage, -3 dB frequency increases with increasing C_{ox} by improving technology and by reducing L (technology scaling). Equation (1.5) also suggest that low voltage operation of these sampling switches comes at the cost of reduced -3 dB frequency.

Input signal dependence of charge injection is another source of non-linearity in sampling switches. Charge injection can be made independent of input signal and constant to some extent by bootstrapping technique as shown in Eq. (3.3). Charge injection due to gate-drain overlap capacitance is still input signal dependent as shown by Eq. (3.6) and a source of non-linearity. This problem can be addressed by using bottom-plate sampling technique as shown in Fig. 1.1. This technique requires an additional switch MN-2 which defines the sampling instance by turning off before sampling switch MN-1. Charge Injection is constant in this case because MN-2 is always connected to ac ground or input common mode.

1.2 NON-NEGOTIABLE SWITCH SPECIFICATIONS

Table 1.1 summarizes the non-negotiable specifications for the switch.

Switch Non-Negotiable Specifications
Implementation in 0.35 um N-well CMOS Technology
Switch Reliability
Differential Topology
Rail-to-Rail Swing of Input Signal
Maximum Input Signal Frequency = 50 MHz
Sampling Clock Frequency = 100 MHz

Table 1.1. Switch non-negotiable specifications

1.3 PERFORMANCE METRICS AND THEIR ORDER OF PRECEDENCE

The order of precedence for switch performance which has been observed during this thesis is summarized in Table 1.2. These performance metrics along with their test set up are described in detail in Section 3.3.9 of chapter 3.

Performance Metrics and Order of Precedence
SINAD, SFDR and THD - [Linearity Matrix]
On-Resistance during Track mode
Sample-to-Hold Step Size during Hold mode
Low Voltage Operation
Power Consumption
Area constraints

Table 1.2. Switch performance metrics and order of precedence

2

CMOS IC PROCESSES AND RELIABILITY

2.1 CMOS SINGLE-WELL AND TWIN-WELL IC PROCESSES

The cross sections of n-well, p-well and twin-well CMOS technologies are shown in the Fig. 2.1.

Both PMOS and NMOS devices are fabricated in CMOS Technology. These devices require substrate material of opposite type of doping for their fabrication. The meaning of the terms substrate, bulk, well, native transistors and well transistors is necessary to clarify here for understanding the CMOS process technology. The substrate is the material underneath the gate. For example in an n-well CMOS technology, the NMOS transistor is located directly on the p-substrate material but the PMOS transistor is located in a deep, lowly doped n-well that is the substrate for the PMOS. The opposite is true for p-well CMOS technology. In a twin-well process both transistors are located in separate wells. The term bulk (B) is used for substrate to avoid confusion with the use of S to denote source. Native transistors are the transistors that lie directly in the substrate whereas well transistors are the transistors that lie in wells. For example in an n-well CMOS technology, the wells are n-type. The native transistors have n-type sources and drains, and the well transistors have p-type sources and drains as shown in the above figure. The channels formed by the native transistors in the p-type substrate are n-channels.

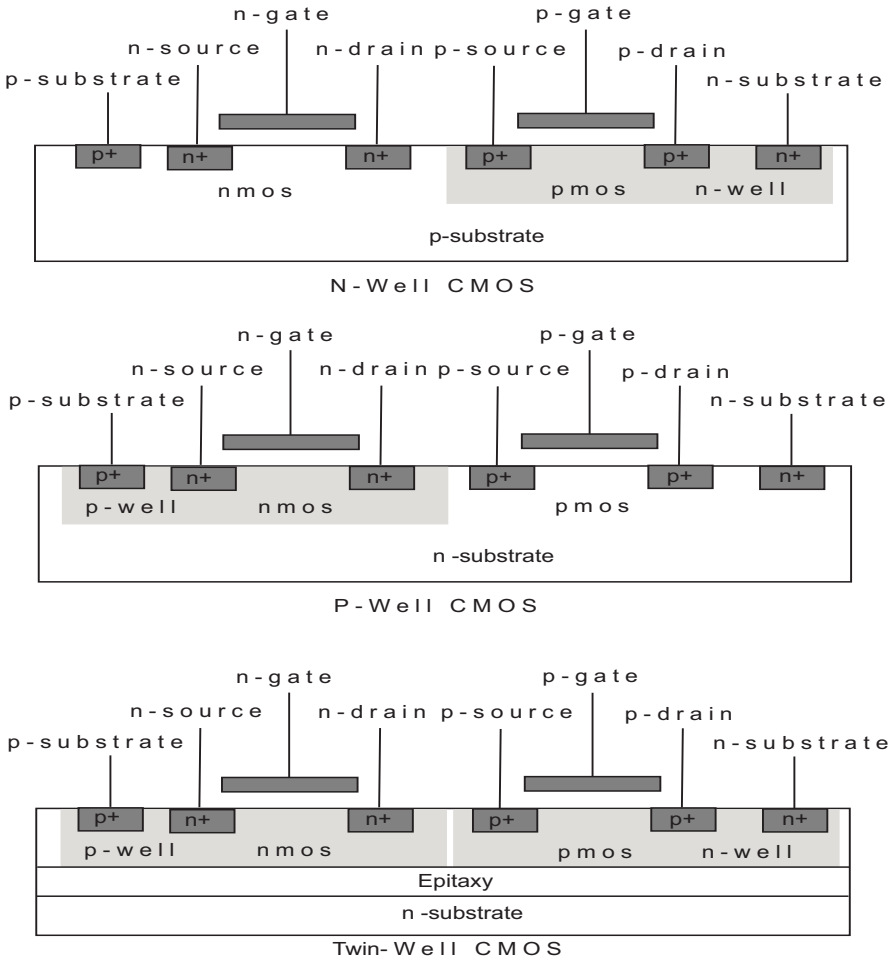

Figure 2.1: N-Well, P-Well and Twin-Well CMOS IC Processes

An important difference between p-well and n-well CMOS technologies is the doping levels of the substrate and well. Since the wells are realized by means of diffusion, they are doped at a higher level than the substrate itself. As a result, the bulk doping level of an NMOS in a p-well CMOS technology is much higher than in an n-well CMOS technology. Typically this ratio is 10 to 50. These two values of bulk doping levels will give different values of transistor parameters.

For an n-well CMOS process, the bulk of the PMOS is the n-well. It is isolated from the substrate and thus can be connected to the source. On the other

hand, the bulk of the NMOS is the substrate itself and thus the bulk of the NMOS can not be connected to the source. If we try doing this, all the sources of the different NMOS transistors will be connected to each other. The opposite is true for p-well CMOS technology. This is the reason that why NMOS can not be bulk-effect compensated in standard n-well CMOS technology. If we want bulk-effect compensation of the input sampling switch in an n-well CMOS technology then we need to implement this switch as a PMOS device so that bulk can be tied to the source. On the other hand, twin-well technology makes it possible to tune threshold voltage, body effect and the channel transconductance of both NMOS and PMOS transistors independently. This is done by growing NMOS and PMOS transistors in separate p and n-well respectively on the lightly doped epitaxy layer over a n+ or p+ substrate.

2.2 CMOS IC RELIABILITY CONSTRAINTS

ASIC foundries define different supply voltage and current density limits for different CMOS technologies to maintain the reliability performance of the Integrated Circuits (IC). Any ASIC device operated at voltages and/or current densities in excess of these reliability limits can be subject to device failure.

The low-distortion CMOS switch described in this thesis exploits the reliable limits by operating at twice voltage levels than the specified rated supply voltage of 3.3 Volts (V) for the 0.35um CMOS process. It is therefore important for ASIC designers to understand some of the very common CMOS device breakdown mechanisms and their interdependence on transistor terminal voltages. Some of the common CMOS circuit failures are gate-oxide breakdown, gate-induced drain leakage, hot carrier effects and punch-through. These have been discussed below with respect to the reliability limits which they impose over transistor terminal voltages. It shall be shown later on that the low distortion CMOS switch is designed without violation of these reliability limits.

2.2.1 GATE-OXIDE BREAKDOWN

There has been a debate for some time over whether the lifetime of gate-oxide breakdown is related to E (Electric Field), or 1/E, or just the applied gate voltage. Presently, simple models of calculating lifetime have been observed valid over certain ranges of gate oxide thickness. Moderately thick oxides seem to have a lifetime related to 1/E at high electric field or E at low

electric field while for very thin oxides (thinner than 5nm) the lifetime appears to be related to applied voltage. [1] [2]

The gate-oxide breakdown phenomenon is discussed here for moderately thick oxides (> 5nm) and time-to-breakdown lifetime t_{bd} related to 1/E at high electric field (electric field > 5MV/cm is taken as high). This explanation is suitable for gate oxide thicknesses of 7-9 nm for single-well 0.35 um processes designed for Electric Field between 5-7 MV/cm. In [5] Abo discusses gate-oxide breakdown and its relation with oxide voltage with respect to the above relation.

Time-dependent gate-oxide breakdown is the formation of a conducting path through the oxide to substrate due to electron tunneling current when CMOS devices are operated beyond foundry specified operating voltages. The Fowler-Nordhiem equation for oxide current density explains this phenomenon of electron tunneling current. Once electrons have breached the oxide potential barrier they are accelerated through the oxide by the electric field which is determined by the oxide voltage V_{ox} and the oxide thickness t_{ox} given by the relationship.

$$V_{ox} < E_{bd} \cdot t_{ox} \tag{2.1}$$

where E_{bd} is the breakdown electric field of gate-oxide.

Gate-source and gate-drain are voltages across gate-oxide during transistor operation [5]. In this manner time-dependent gate-oxide breakdown limits gate-source and gate-drain potential differences which are the points of concern for ASIC Designers [3].

Time-to-breakdown lifetime t_{bd} for Intrinsic (defect free) silicon dioxide is shown following a reciprocal electric field dependence, expressed as [4]

$$t_{bd} = \tau_0(T)\exp\left(\frac{G(T)t_{ox}}{V_{ox}}\right) \tag{2.2}$$

For $\tau_0(T) \approx 10^{-11}s$, $G(T) = 350$ MV/cm for a 20 year lifetime at $125^{\circ}C$, Eq. 1.2 becomes

$$\frac{V_{ox}}{t_{ox}} < 7 \qquad MV/cm \tag{2.3}$$

For oxide defects the practical limit is taken as 5 MV/cm [5]. As V_{ox} increases beyond E_{ox} the lifetime of the oxide decreases exponential from Equation 1.2.

2.2.2 GATE-INDUCED DRAIN LEAKAGE (GIDL)

GIDL imposes the following limit on gate-drain voltage due to tunneling current.

$$V_{dd} \leq V_{gd} \leq E_{gidl} \times t_{ox} + 1.2V - V_{FB}M \tag{2.4}$$

where E_{gidl} is the electric filed (typical value 4MV/cm) that induces tunneling current, 1.2V is the band gap voltage and V_{FB} is the flat-band voltage of the MOSFET.

2.2.3 HOT CARRIER EFFECTS

Hot carrier damage rate is the highest in a transistor with a minimum channel length and when the drain-source voltage is the maximum permitted voltage while the gate-source voltage is around half of the drain-source voltage. The following Equations describe this constraint

$$V_{dd} < V_{ds} \leq V_{dsat}(L) + E_c \cdot (l_2 + l_{LDD}) \tag{2.5}$$

$$l_2 = 0.2{t_{ox}}^{1/3}{X_j}^{1/2} \tag{2.6}$$

where E_c is the critical field, l_{LDD} is the effective length of the lightly doped drain and X_j is the drain/source junction depth.

2.2.4 PUNCH-THROUGH

Punch-through is the breakdown phenomenon caused by the overlap of source and drain junction depletion regions during the device off-condition. It limits the magnitude of V_{ds} as described by the following Equation.

$$V_{dd} \approx V_{ds} < V_p \propto \frac{N_{sub}L^3}{X_j + 3t_{ox}} \tag{2.7}$$

where N_{sub} is the substrate doping concentration.

2.2.5 CONCLUSION

All the above equations from Equations (2.1) to (2.7) suggest that the transistor terminal voltages V_{gs},V_{gd},V_{ds} should be with in the specified rated supply voltage V_{dd} for the reliable operation. This means that a transistor will be with in the reliable limits even if for example, the gate voltage V_g with respect to ground is greater than V_{dd} provided that V_{gs} is less than V_{dd}. The low-distortion bootstrapped switch described in the next chapter also exploits this condition. The source-to-substrate and drain-to-substrate voltages should not exceed the reverse breakdown voltages which are typically much larger than V_{dd}.

3

TRANSMISSION GATE AND RELIABLE LOW-DISTORTION MOS SAMPLING SWITCH

3.1 TERMINOLOGIES - TRACK AND HOLD

All the switch designs which have been discussed ahead have two modes of operation. One is track mode and the other one is hold mode. Track mode is basically the ‘ON’ phase of the sampling switch irrespective of the switching state of the rest of the transistors in the design. During this phase the output of the sampling switch is able to track the input.

Hold mode is basically the ‘OFF’ phase of the Sampling Switch irrespective of the switching state of the rest of the transistors in the design. During this phase the output of the sampling switch is held to a constant fixed value.
The performance of all the switches has been discussed for a differential topology.

3.2 LINEARITY OF TRANSMISSION GATE

NMOS transistors can not conduct for source voltages beyond $V_{dd} - V_{t,n}$ for normal clock signals, where $V_{t,n}$ is the threshold voltage of NMOS transistor. Their on-resistance is relatively non-linear for high voltages near $V_{dd} - V_{t,n}$. Conversely, PMOS transistor can not conduct for voltages below

$V_{t,p}$ where $V_{t,p}$ is the threshold voltage of PMOS transistor. Their on-resistance is also relatively non-linear for low voltages near $V_{t,p}$. A Transmission gate consists of both NMOS and PMOS transistors connected in parallel. Its on-resistance is much more linear as compared to individual NMOS and PMOS switches. Therefore, it serves as a good reference switch for comparing the linearity of the other switches in this thesis. The design strategy used for sizing the two transistors is now described so that switch is linear enough.

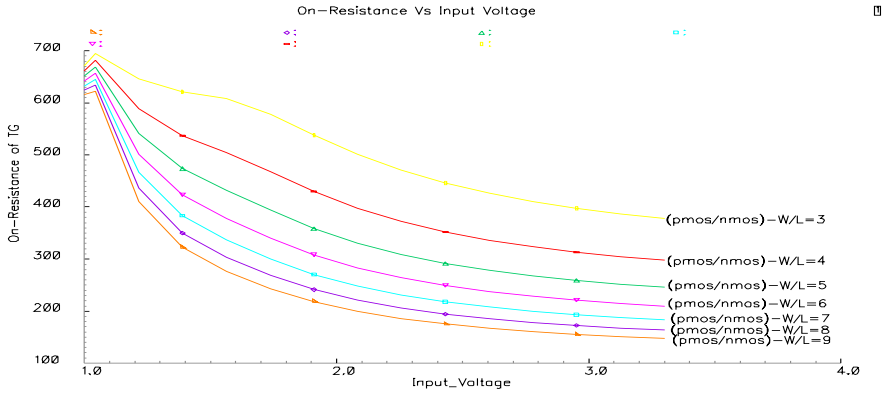

Figure 3.1: On-resistance for a transmission gate as a function of Input Voltage for relative $[W/L]$ ratios

The on-resistance R_{on} of transmission gate sampling switch is measured in a special test-bench in Cadence. It involves ac analysis with one frequency spot and dc analysis with bias voltage sweeping. This linearizes bias point and R_{on} is measured around that value for a single frequency. R_{on} curve is plotted for transmission gate at 49MHz. For this purpose special function ‘value’ of calculator has been used.

Using the above test-bench first of all the on-resistance of the transmission gate is swept across the entire input voltage range to determine relative

$[W/L]$ ratio between PMOS and NMOS transistors. The curves in Fig. 3.1 show that for the value of relative $[W/L]$ ratio around four, the on-resistance starts looking fairly linear

After fixing the relative $[W/L]$ ratio to four, on-resistance is swept again across the entire range of input voltage for the individual $[W/L]$ ratio of NMOS transistor. The on-resistance is shown for different $[W/L]$ ratios of NMOS transistor in Fig. 3.2.

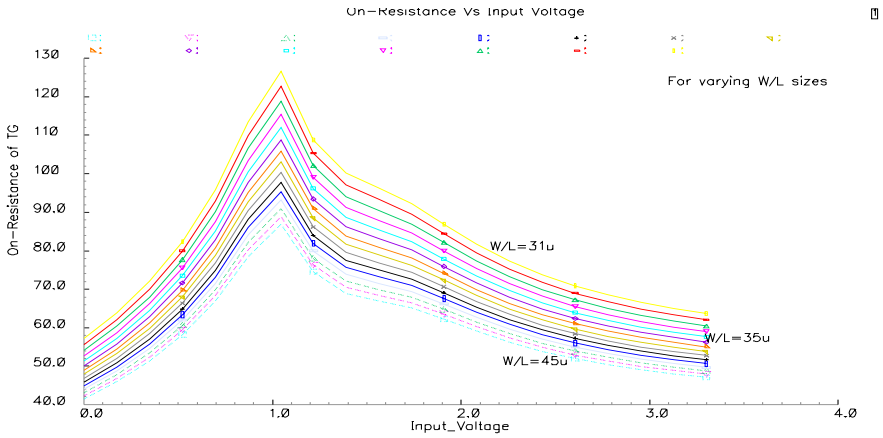

Figure 3.2: On-resistance as a function of input voltage for NMOS $[W/L]$ ratio

The final switch sizes for NMOS and PMOS transistors are shown in the Table 3.1.

	NMOS	PMOS
Width	35um	140um
Length	0.35um	0.35um

Table 3.1. Sizes of NMOS and PMOS transistors in transmission gate

This transmission gate is used in a differential topology to measure SINAD, SFDR and THD with a hold capacitance C_h of 800 fF. The results are summed up in Table 3.2.

	Transmission Gate
Input Signal Frequency, f_{in}	49 MHz
Sampling Clock Frequency, f_{clk}	100 MHz
Signal to Noise and Distortion Ratio, SINAD	47.9841 dB
Spurious Free Dynamic Range, SFDR	48.3598 dB
Total Harmonic Distortion, THD	-46.389 dB

Table 3.2. Performance of transmission gate

3.3 LOW DISTORTION BOOTSTRAPPED SWITCH

3.3.1 BASIC BOOT STRAP CONCEPT

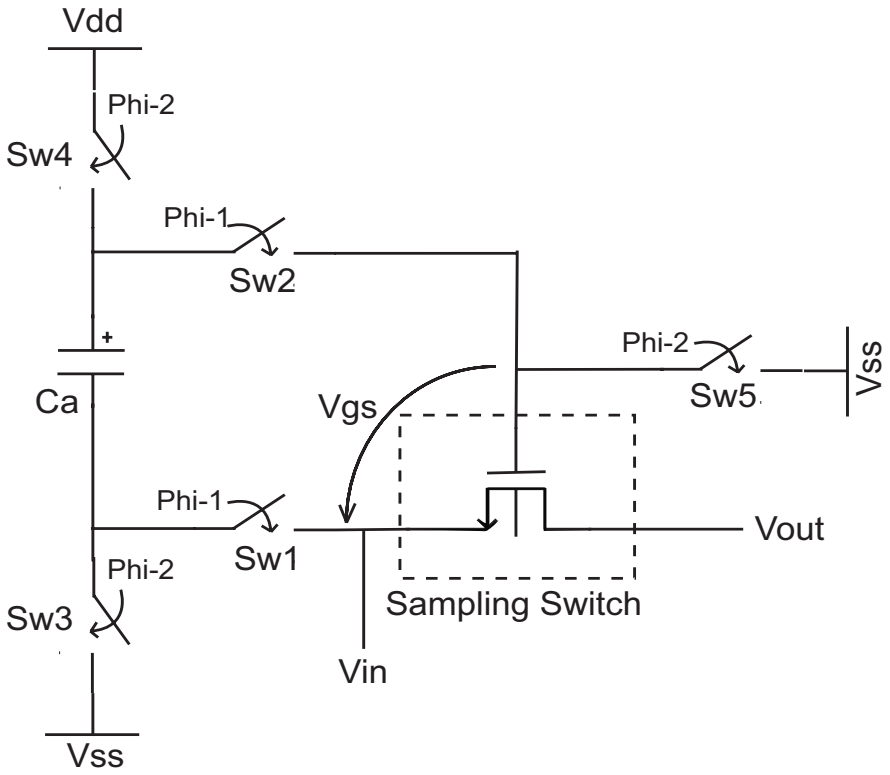

Figure 3.3: Basic bootstrap circuit

Figure 3.3 shows the conceptual circuit of gate-source bootstrapping technique which has been implemented in this thesis. It shows the main sampling switch along with five additional switches (Sw1-Sw5) and a bootstrap capacitor. Although in the actual circuit there are more than five switches for specific reasons which shall be described later on.

This bootstrapping topology works with two phases of non-overlapping clocks Phi-1 and Phi-2. The term non-overlapping clocks mean that the two clock phases have the same frequency but they are not high simultaneously at any instant of time. The generation of two non overlapping clocks is an essential requirement because it greatly enhances performance by guaranteeing that charge is not advertently lost. It actually prevents the capacitor Ca from

being partially discharged during the transition phase of the clock. Switches Sw3 and Sw4 charge the capacitor Ca to V_{dd} during Phi-2 phase of the Clock. The charged capacitor is then connected in series with the input voltage Vin during phase Phi-1 of the clock through switches Sw1 and Sw2. This results in the gate-source voltage of the sampling transistor approximately equal to V_{dd} which is the voltage across capacitor Ca. Switch Sw5 makes sure that the sampling switch is not conducting by connecting it to V_{ss} during phase Phi-2 of the clock when capacitor Ca is being charged to V_{dd}.

The advantage of this scheme is that switch conductance becomes independent of the time varying input voltage which linearizes the sampling switch.

3.3.2 TRANSISTOR-LEVEL IMPLEMENTATION

The bootstrap circuit implemented in this thesis adopted from [6] as shown in Fig. 3.5 is a modified form of Abo's bootstrap switch [5]. This bootstrap circuit differs from Abo's bootstrap circuit in the design of the clock-doubling/ boosting circuit. The rest of the design is the same. Before discussing the transistor level implementation of this circuit, the two different clock-boosting schemes are worth discussing.

3.3.3 CLOCK DOUBLING IN ABO'S ARCHITECTURE

Abo uses a classical charge pump type of clock multiplier comprising of MN-1, MN-2, C1 and C2 as shown in Fig. 3.4 to drive transistor MN-3 of Fig. 3.5. The disadvantage of this design is that transistors MN-1 and MN-2 in Fig. 3.4 are free from the reliability as their gate-source voltage is approximately twice as much as the specified supply voltage (3.3 V for 0.35um process). The cross-coupled NMOS transistors self-charge the capacitors C1 and C2 to 3.3 Volts when Phi-1 is applied. Double clock signals between V_{dd} and $2V_{dd}$ are obtained at the gates of MN-1 and MN-2 at alternative clock cycles Phi-1 and Phi-2 respectively in Fig. 3.4.

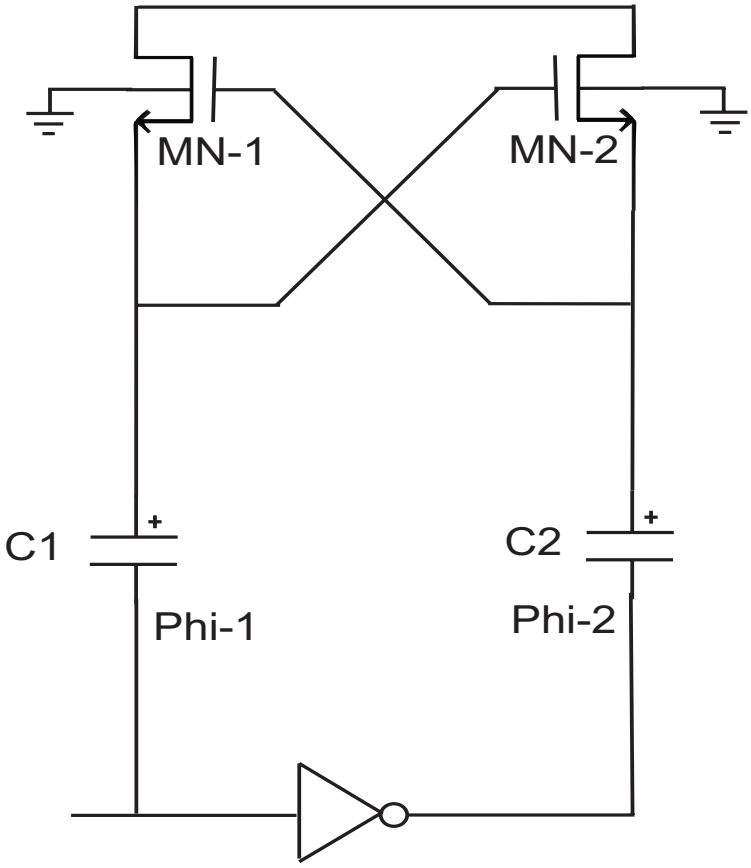

Figure 3.4: Charge pump for clock doubling in Abo's architecture

3.3.4 CLOCK DOUBLING IN IMPLEMENTED BOOTSTRAP ARCHITECTURE

Transistors MN-1, MN-2, MP-1 and capacitor Ca1 shown in a dotted box in Figure 3.5 form the clock-doubling circuitry to drive transistor MN-3. This solution provides clock doubling by ensuring the reliability constraint. None of the transistors in this scheme have terminal voltages V_{gs}, V_{ds} and V_{gd} exceeding the specified supply voltage of 3.3 V.

During phase Phi-1 of the clock, capacitor Ca1 is pre-charged to a fixed value of $V_{dd} - V_t$, where V_t is the voltage drop across diode connected transistor

MN-1. During the next phase of Phi-1, MP1 transistor connects the the bottom plate of the capacitor Ca1 to V_{dd}. As a result the top plate of the capacitor Ca1 rises to $2V_{dd} - V_t$. The gate voltage of transistor MN-3 toggles between $V_{dd} - V_t$ and $2V_{dd} - V_t$.

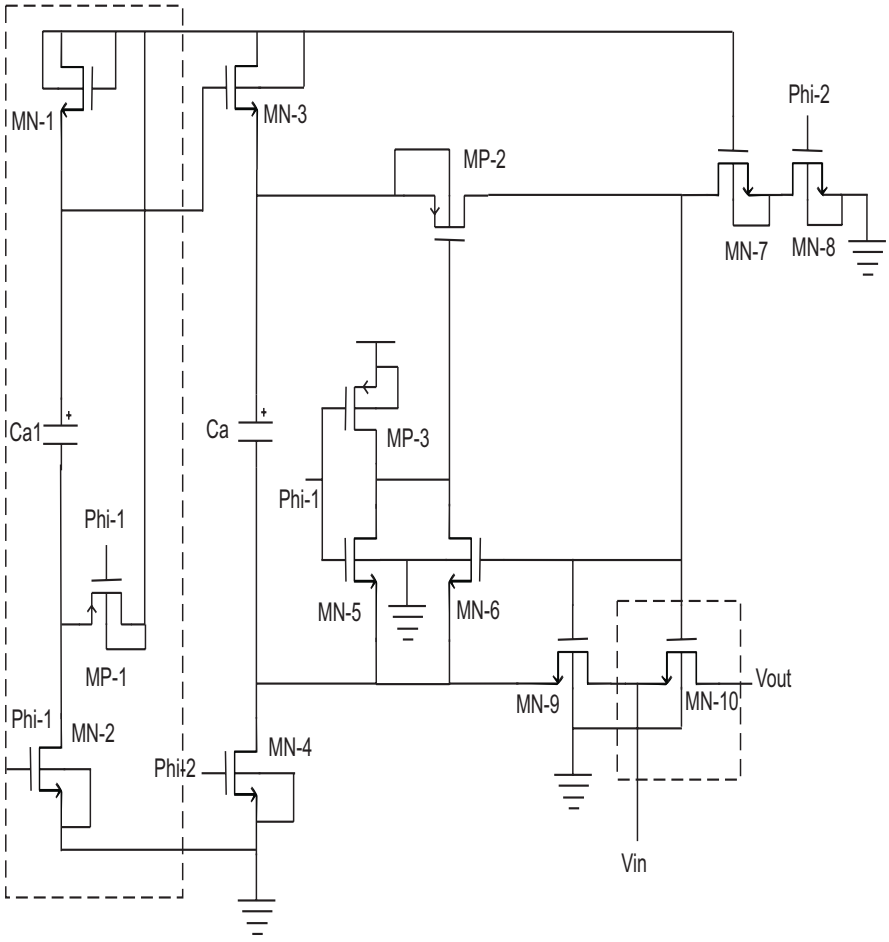

Figure 3.5: Transistor level implementation of bootstrap circuit

In both designs a clock-boosting circuit is used to drive transistor MN-3. It is important to see that if MN-3 has been driven from a normal clock which toggles between V_{dd} and 0, then what disadvantage would have been there.

Firstly an NMOS transistor is a weak switch for switching V_{dd} with V_{dd} at it's gate voltage.

Secondly during the off-state with 0 at the gate voltage, the drain of MN-3 could be exposed to a voltage greater than V_{dd} $(V_{dd} - V_t - V_{on} + V_{in})$ if the input voltage $V_{in} > V_t + V_{on}$, where V_t is the threshold voltage of MN-3 and V_{on} is the voltage drop across MN-9 during the on state. This will make MN-3 an unreliable switch.

Another option could have been to use PMOS instead of NMOS. In that case it would not have been possible to turn PMOS off during the other phase and it would have been a leaky switch.

The transistor operation shall now be discussed here for the worst case input signal equal to V_{dd}. In Fig. 3.5 transistors MN-9, MP-2, MN-4, MN-3 and MN-8 correspond to five ideal switches Sw1-Sw5 in Fig. 3.3, respectively. MN-10 is the main sampling switch whose gate is grounded through MN-7 and MN-8 during Phi-2 phase of the clock, hence, turning it off. During the same phase MN-1, MN-2, MP-1 and Ca1, forming a clock-boosting circuit, drive transistor MN-3 which unidirectionally charges capacitor Ca. Transistors MP-2 (connected to V_{dd} through MP-3) and MN-9 isolate the sampling switch MN-10 when the capacitor Ca is being charged to V_{dd}. The charged capacitor provides constant voltage of V_{dd} between gate and source of MN-10 during phase Phi-1 of the clock, thus also ensures a low on-resistance independent of the input signal. During this phase, MN-5 pulls down the gate of MP-2, turning it on and allowing the charge to flow from capacitor Ca to the gate of MN-6, MN-9 and MN-10. This turns all three transistors on. MN-9 also enables node N1 to follow the input voltage shifted by V_{dd}, keeping the gate-source voltage constant regardless of the input signal. MN-6 and MN-7 increase the reliability of the transistors MP-2 and MN-8. There is as such no other functionality of these switches. MN-7 reduces the V_{ds} and V_{gd} of MN-8 when Phi-2 is off and node N1 is at $2V_{dd}$ for the worst case input of V_{dd}. Equation 1.7 suggests that by increasing the channel length of MN-7, it's punch-through voltage V_{ds} can be increased. Transistor MN-6 ensures that the gate-source voltage across MP-2 does not exceed V_{dd} by allowing the input voltage to appear at node N3 during Phi-1 phase of the clock. The voltage at node N1 can be expressed as follows considering the parasitic capacitances C_p attached to the upper plate of Ca.

$$V_{N1} = V_{in} + \frac{Ca}{Ca + C_p} \cdot V_{dd} \tag{3.1}$$

For the worst case input voltage of V_{dd} MN-9, which is an NMOS transistor, is required to conduct. The gate of this transistor is for this reason connected to the gate of MN-10 for bootstrapped voltage to ensure high conductivity by maintaining V_{gs} of the transistor equal to V_{dd} during phase Phi-1 of the clock. The gate voltage falls to zero volts during phase Phi-2 to bring both transistors MN-9 and MN-10 in cutoff state. In this scheme MN-3 is a reliable switch. During on phase it charges capacitor Ca to V_{dd}. During off phase, MN-3 has $V_{dd} - V_t$ at the gate and $V_{dd} + V_{in}$ at the drain. Even for the worst case input voltage of $V_{in} = V_{dd}$, transistor MN-3 is off. The transistor reliability is also ensured during the off-state.

3.3.5 CHARGE INJECTION

The discussion of this bootstrapped switch is incomplete with out discussing charge injection phenomenon which occurs due to unwanted charges injected into the circuit by turning off some transistors slightly earlier in the overall circuit.

In this bootstrapped switch, the output node V_{out} is the most sensitive from charge injection point of view . The phenomenon of charge injection at V_{out} can be understood by considering the simplified model of the bootstrapped sampling switch as shown in Fig. 3.6.

There are two reasons of it. The first dominating reason is that when a transistor turns off, it's channel charge flows out to source and drain regions. If the clock Phi has fast turning off time then it is assumed that charge flows equally in both directions towards source and drain. This channel charge flowing to the output junction V_{out} for the bootstrapped voltage of $V_{dd} - V_{in}$ at gate terminal is given by

$$\Delta Q_{CH} = \frac{Q_{CH}}{2} = \frac{-WLC_{ox}(V_{dd} - V_t)}{2} \tag{3.2}$$

The change in voltage according to $Q = CV$ at the output node because of this channel charge is given as

$$\Delta V_{CH} = \frac{\Delta Q_{CH}}{2C_{hold}} = \frac{-WLC_{ox}(V_{dd} - V_t)}{2C_{hold}} \tag{3.3}$$

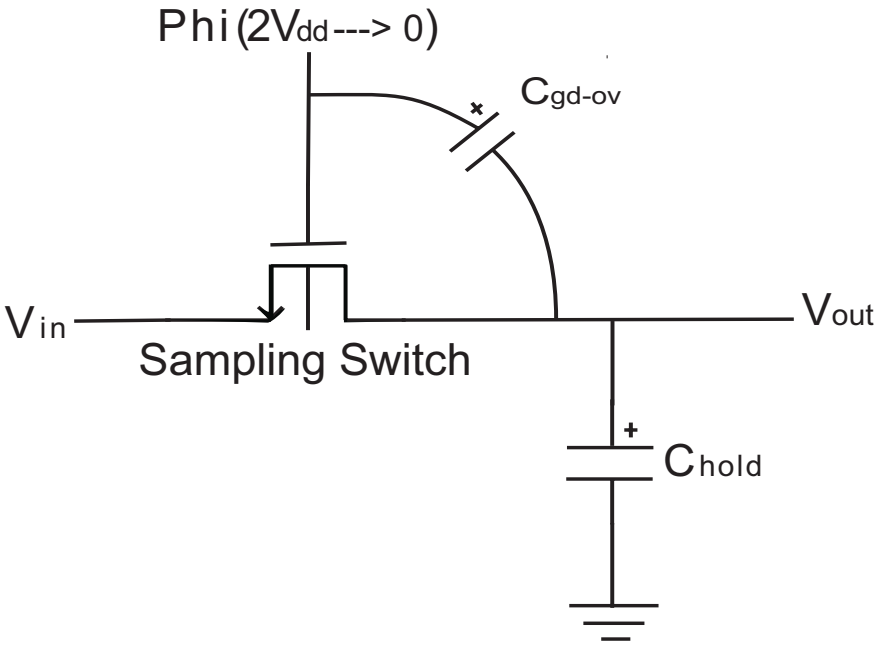

Figure 3.6: Charge injection in single ended application

From Eq. (3.3) it is evident that either the size of the sampling transistor should be small or the value of C_{hold} should be high in order to have a reduced charge injection at the output. The bootstrapped switch has also an improved input voltage dependent signal distortion by keeping $V_{gs} = V_{dd}$.

The second reason is the gate-drain overlap capacitance which introduces variation to the output voltage during the turn off-phase of the sampling switch. For normal switches operating between V_{dd} and 0 Volts this change is normally less as compared to the change caused by the channel charge at the output. But for the bootstrapped switch under discussion, this change is also pronounced because it is switching between $V_{in} + V_{dd}$ and 0 Volts. In particular when $V_{in} = V_{dd}$ the sampling transistor switches between $2V_{dd}$ and 0 Volts introducing maximum change in the output voltage. C_{eq} at the output node due to two capacitances is given by

$$C_{eq} = \frac{C_{hold} C_{gd-ov}}{C_{hold} + C_{gd-ov}} \tag{3.4}$$

When Phi changes from $V_{in} + V_{dd}$ to 0 Volts, the charge flow through C_{eq} is given by

$$\Delta Q_{eq} = -(V_{in} + V_{dd})C_{eq} = \frac{-(V_{in} + V_{dd})C_{hold}C_{gd-ov}}{C_{hold} + C_{gd-ov}} \tag{3.5}$$

The change in voltage at the output node as a result of this charge flow is

$$\Delta V_{ov} = \frac{\Delta Q_{eq}}{C_{hold}} = \frac{-(V_{in} + V_{dd})C_{gd-ov}}{C_{hold} + C_{gd-ov}} \tag{3.6}$$

The total charge injection at the output node is given by Equations (3.3) and (3.6).

The charge injection is corrected to the first order by introducing differential topology as it appears as a common-mode disturbance. The charges introduced by two switches in a differential topology do not exactly cancel each other because the two input differential signals are not equal to each other. The overall error is however suppressed for differential signals because this technique removes constant offset and lowers the non-linearity component.

3.3.6 KT/C NOISE AND ACQUISITION TIME CONSIDERATIONS FOR SAMPLING CAPACITOR SIZING

When a capacitor is connected to a transistor, the mean squared value of noise is equal to KT/C due to on-resistance of the transistor. In order to have smaller KT/C noise, the value of C_{hold} should be larger. For calculating the value of C_{hold} from this constraint, KT/C noise contribution has been included in the following SNR (signal-to-noise ratio) formula.

$$SNR = 10 \cdot \log\left[\frac{\left(\frac{V_{in,\,p-p}}{2\sqrt{2}}\right)^2}{\frac{\left(\frac{V_{in,\,p-p}}{2^N}\right)^2}{12} + \frac{KT}{C_{hold}}}\right] \tag{3.7}$$

For $V_{in,\,p-p}$ equal to 3.3V, SNR of 100 dB and N equal to 14, value of C_{hold} from equation (3.7) is calculated as follows,

$$C_{hold} \cong 4\,pF \tag{3.8}$$

Using the same formula, the value of C_{hold} for SNR of 88 DB, $V_{in,\,p-p}$ of 3.3V and N equal to 14, is calculated as

$$C_{hold} \cong 1.1\,pF \tag{3.9}$$

From Simulations the value of SFDR and THD has been found to be equal to 77.7312 dB and 77.68 dB respectively for C_{hold} equal to 2.5pF, 100 MHz sampling clock and 49 MHz input clock frequency. The reason for this discrepancy can be attributed to another factor called acquisition time. Acquisition time is the delay in time when a track-and-hold circuit enters the tracking mode and tracks an input signal with a certain accuracy. Ideally speaking the sample-and hold circuit should immediately start tracking the input signal as the clock phase Phi goes high or to $V_{in} + V_{dd}$ value as in this case of the boot strapped switch. Acquisition Time can be used as a measure of C_{hold} and R_{on} for maximum allowable sampling frequency. Acquisition time is given by

$$t_{acq} = (N+1) \cdot R_{on} \cdot C_{hold} \cdot \ln(2) \tag{3.10}$$

where N is the number of bits and R_{on} is on-resistance of the sampling transistor. It is clear from this relationship that the greater the value of C_{hold}, the greater is the acquistion time. For an acquisition time t_{acq} of 10ns which corresponds to 100 MHz clock, N equal to 14 bits and R_{on} equal to 1.5 k-Ohms, value of C_{hold} has been found to be

$$C_{hold} \cong 641\,fF \tag{3.11}$$

From simulations, the value of C_{hold} was taken to be 750fF for a reasonable SFDR and THD of above 87 dB and 90 dB respectively.

3.3.7 TRANSISTOR SIZING AND DESIGN STRATEGY

TRANSISTORS	W/L (um)	TRANSISTORS	W/L(um)
MN1	4.5/0.35	MN8	10/0.35
MN2	4.5/0.35	MN9	5/0.35
MN3	8/0.35	MN10	20/0.35
MN4	5/0.35	MP1	4.5/0.35
MN5	3/0.35	MP2	12.5/0.35
MN6	3/0.35	MP3	8/0.35
MN7	10/0.7		

Table 3.3. Transistor sizes for bulk-effect free switch

Some considerations for transistor sizing are discussed here.

The sampling switch MN10 transistor size is most critical from channel charge injection and low R_{on} point of view. If the size of the sampling transistor is large then it will result in an increased charge-injection at the output as could be seen from Eq. (3.3). On the other hand in order to have lower value of R_{on} the size of the sampling transistor should be larger. From simulations an optimum value of 20/0.35 um was selected as the sampling transistor W/L ratio for these trade-offs.

The next most important transistor in the design is MP-2 from sizing point of view. This transistor allows $V_{in} + V_{dd}$ to appear as gate voltage for the sampling transistor. So the propagation delay t_p of this transistor should be as small as possible. Secondly it is a PMOS device so it's width should naturally be larger as compared to NMOS devices to compensate for lower charge mobility and hence speed of the transistor. On the other hand by increasing the size of the transistor, parasitic capacitances associated with the upper plate of the boosting capacitor will reduce the gate voltage of sampling switch as described by Eq. (3.1)

All transistors in the design have a length of 0.35um except MN-7 whose length has been kept to 0.7um. This improves the punch-through voltage of MN-7 as described by Eq. (2.7) in Sec. 2.2.4.

It is important to mention here that different transistors in the circuit have different threshold values which causes unnecessary delays and distortions in the waveforms. The threshold voltage of transistor MP-2 should be low as

compared to the threshold voltages of MN-6, MN-9 and MN-10 so that it allows the gate voltages of these transistors to reach $V_{in} + V_{dd}$ quickly.

All other transistors in the circuit were designed to have less propagation delay and thus avoiding unnecessary leakage paths because of different turn on times.

The sizes of Ca and Ca1 have been kept to 5pF to have low KT/C noise which are not that much sensitive. The sizing strategy of C_{hold} has already been discussed above which is also quite critical from performance point of view.

3.3.8 GRAPHS SHOWING AFFECTS OF VARYING C_{hold} AND SAMPLING TRANSISTOR WIDTH DURING TRACK AND HOLD PHASES

In the following graphs values of C_{hold} are varied from 650fF to 1.8pF. The effect of these variations on charge injection during hold mode and on acquisition time during track-mode can be observed as explained above.

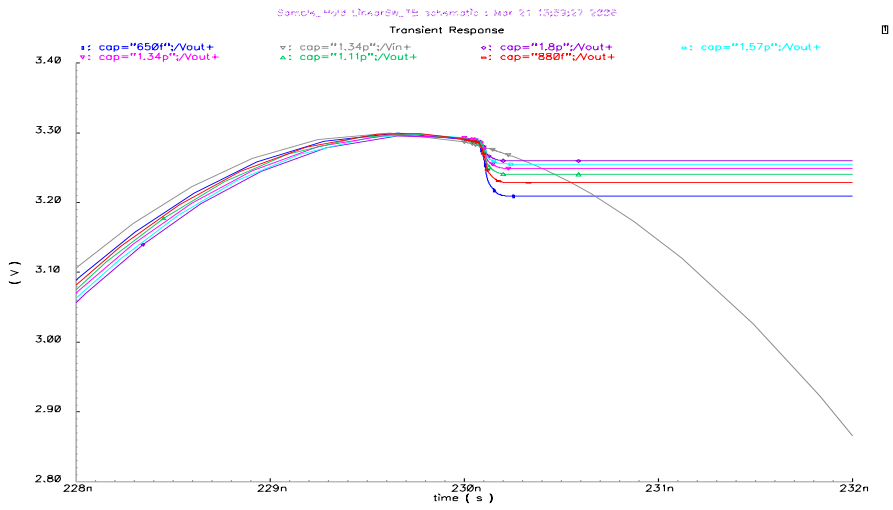

Figure 3.7: Charge injection during hold-mode for different C_{hold} values

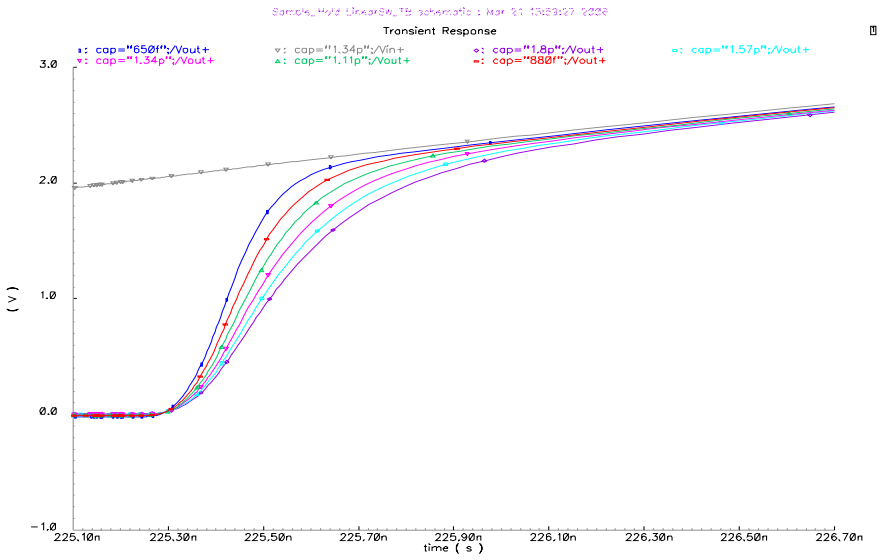

Figure 3.8: Acquisition time during track-mode for different C_{hold} values

Figures 3.9 and 3.10 show effects of varying sampling switch (MN-10 in figure 3.5) sizes from 10um to 20um on charge injection during hold mode and acquisition time during track mode respectively as explained above.

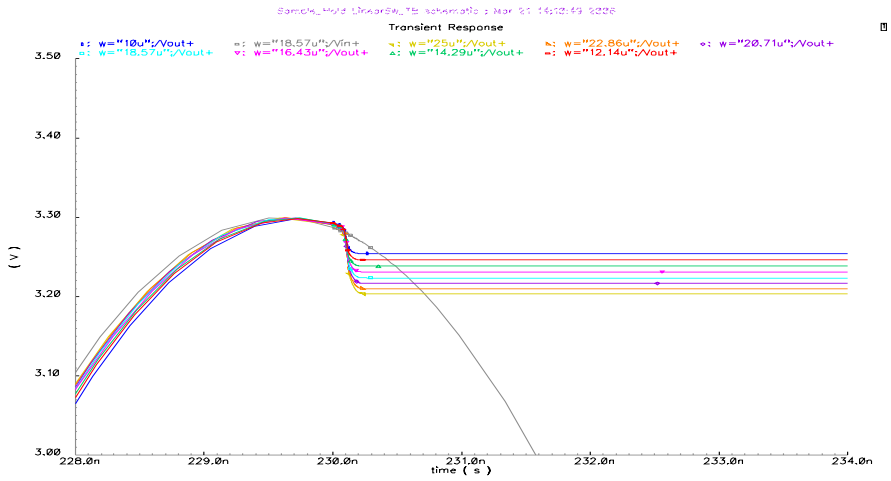

Figure 3.9: Charge injection during hold-mode for different widths of MN-10

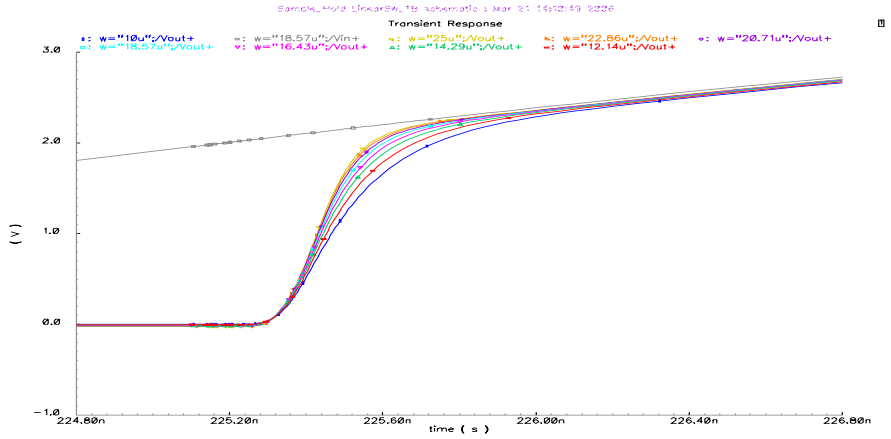

Figure 3.10: Acquisition time during track-mode for different widths of MN-10

3.3.9 PERFORMANCE METRICS AND TEST SETUP

The performance metrics for this bootstrapped switch are reliability, on-resistance R_{on} , SINAD, SFDR, THD and sample-to-hold step size which are described as follows.

RELIABILITY

As described in Sec. 2.2, the reliability constraint requires that all transistor terminal voltages V_{gs},V_{gd},V_{ds} are with in the specified rated supply voltage V_{dd}. This means that the transistor will be in the reliable limits even if e.g., the gate voltage V_g with respect to ground is greater than V_{dd} provided that V_{gs} is less than V_{dd}. This condition has been fulfilled for the bootstrapped transistor under discussion.

ON-RESISTANCE

When a MOS switch is turned on, an on-resistance is associated with it whose value depends on the switch size and gate driving capability. The on-resistance R_{on} together with the sampling capacitor C_{hold} forms the RC time-constant that defines the -3 dB bandwidth. It is given by

$$f_{-3DB} = \frac{1}{2\pi R_{on} C_{hold}} = \frac{1}{2\pi} \cdot \frac{u_n C_{ox} \frac{W}{L} (V_{dd} - V_t)}{C_{hold}} \tag{3.12}$$

From the above equation it is clear that in order to achieve high input bandwidth for a fixed sampling capacitor, the on-resistance R_{on} needs to be small. Also for a given switch size and supply voltage, -3 dB frequency increases with increasing C_{ox} by improving technology and by reducing L (technology scaling). A trade-off exists between -3 dB frequency and supply voltage for low-power design.

The bootstrapped sampling switch on-resistance R_{on} value is measured in a special test-bench in Cadence. The fundamental requirement for measuring R_{on} is that the sampling switch should be in track-mode i.e., on condition. It’s not trivial to keep the sampling switch MS on in the presence of so many other switches in Fig. 3.5. This was ensured by assigning capacitors Ca and Ca1 the initial voltage of 3.3 and 0 volts respectively. Further, Phi-1 and Phi-2 phases of clocks were connected to V_{dd} and 0 volts to make sure that MS

conducts and that the charging circuitry remains disabled. The drain of the sampling transistor MS is connected to ground instead of the hold capacitor in this test bench. R_{on} measurement involves AC analysis with one frequency spot and DC analysis with bias voltage sweeping. This linearizes the bias point and R_{on} is measured around that value for a single frequency. R_{on} is simulated from 1MHz to 50MHz. The R_{on} curve is then plotted at 49 MHz. For this purpose the special function 'value'of the calculator in Cadence has been used.

R_{on} is additionally swept against $[W/L]$ for plotting R_{on} curves for different PMOS and NMOS $[W/L]$ relative values of transmission gate in Figures 3.1 and 3.2.

SINAD

Signal-to-noise-and-distortion ratio SINAD is defined as

$$SINAD = 10\log\left(\frac{P_{signal}}{P_{noise} + P_{distortion}}\right)[dB] \tag{3.13}$$

On the other hand, the maximum signal-to-noise ratio, SNR, is equal to the ratio of the maximum sinusoidal power to the quantization noise. If oversampling is taken into account, then maximum achievable SNR for an A/D converter becomes

$$SNR_{max} = 6.02 \cdot N + 1.76 + 10\log(OSR)[dB] \tag{3.14}$$

where OSR = Oversampling Ratio = $\frac{f_s}{2f_0}$ where f_s and f_0 are sampling frequency and input signal bandwidth respectively, N is the number of bits.

The SINAD of this boot strapped switch is measured in Matlab by taking the samples of the output waveform at the instant immediately when sampling switch goes from the tracking phase to hold-phase. The SINAD estimation algorithm uses least squares method to fit one sinusoidal signal to every applied frequency from the output data. The amplitudes and phases of all sinusoidal signals are then estimated and the corresponding sinusoidal signal $\bar{y}(n)$ is subtracted from the output data $y(n)$ to get an estimation of the noise and distortion power. The estimated SINAD is given by

$$SINAD = 10\log\left[\frac{\frac{1}{N}\sum_{n=0}^{N-1}(\bar{y}(n)-A_3)^2}{\frac{1}{N}\sum_{n=0}^{N-1}(y(n)-\bar{y}(n))^2}\right] \quad (3.15)$$

The above calculation method has been taken from [9]. The matlab code is given in Appendix-A.

SFDR

Spurious free dynamic range (SFDR) is evaluated in Matlab by taking the DFT (Discrete Fourier Transform) of the sampled output signals for a known frequency and the ratio of the smallest desired signal amplitude to the largest undesired signal amplitude. SFDR is defined as

$$SFDR = 20\log\left(\frac{MaximumSignalAmplitude}{LagestUndesiredSignalAmplitude}\right) \quad (3.16)$$

The matlab code is given in Appendix-A.

THD

Total harmonic distortion (THD) is defined as the ratio of the power of second and higher order harmonics to the power of the fundamental signal. It is given by the following formula.

$$THD = 10\log\left(\frac{V_2^2 + V_3^2 + V_4^2}{V_f^2}\right) \quad (3.17)$$

The matlab code of THD is given in Appendix-A.

SAMPLE-TO-HOLD STEP SIZE

Sample-to-hold step or pedestal error is the difference between the real and ideal output voltage levels during hold-mode. This difference is caused by the storage of noise due to charge-injection and clock-feed through on the hold

capacitor. If the channel charge is assumed to be divided equally between the drain and source regions of the sampling switch, then the pedestal error is given by Eq. (3.3).

3.3.10 PLOTS AND RESULTS

The performance of gate-source boot strapping switch is compared with the transmission gate switch which is considered a very linear switch. The following table summarizes the performance results for input signal frequency of 49 MHz and Clock sampling frequency of 100 MHz for differential topology.

Ratio of $\frac{[W/L]_{PMOS}}{[W/L]_{NMOS}}$ is taken as 4 in these calculations.

	TG	Boot Strap Switch
SNR [dB]	47.9841	87.0092
SFDR [dB]	48.3598	87.1067
THD [dB]	-46.389	-87.102

Table 3.4. Performance comparison of TG and Bootstrap switch

An amplitude spectrum of the output signal for the bootstrapped switch is shown in Fig. 3.11 on next page.

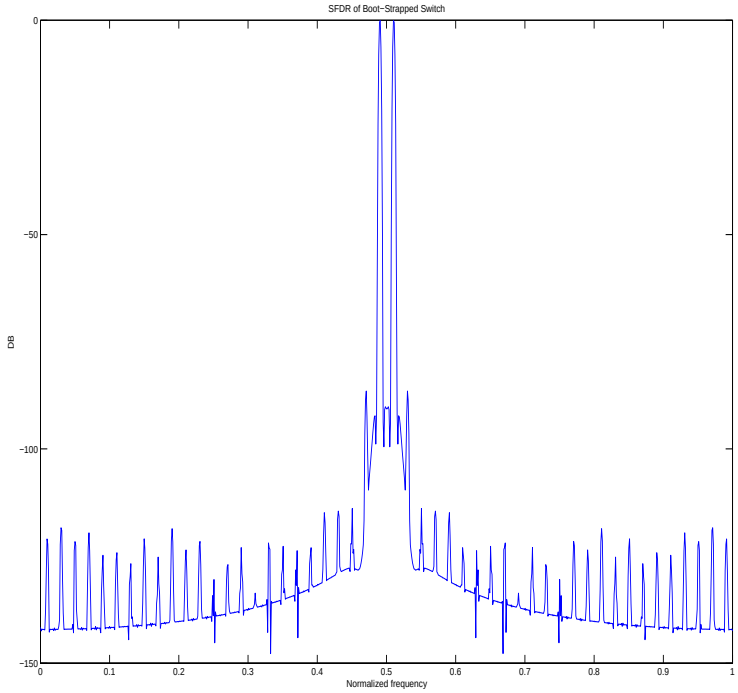

Figure 3.11: Amplitude spectrum of bootstrapped switch output signal

As it can be seen from this plot that the 3rd order harmonic is basically limiting the SFDR performance metric for the bootstrap switch. 2nd or even-order harmonics are greatly suppressed because of differential topology

An on-resistance plot of the bootstrap switch is shown in Fig. 3.12.

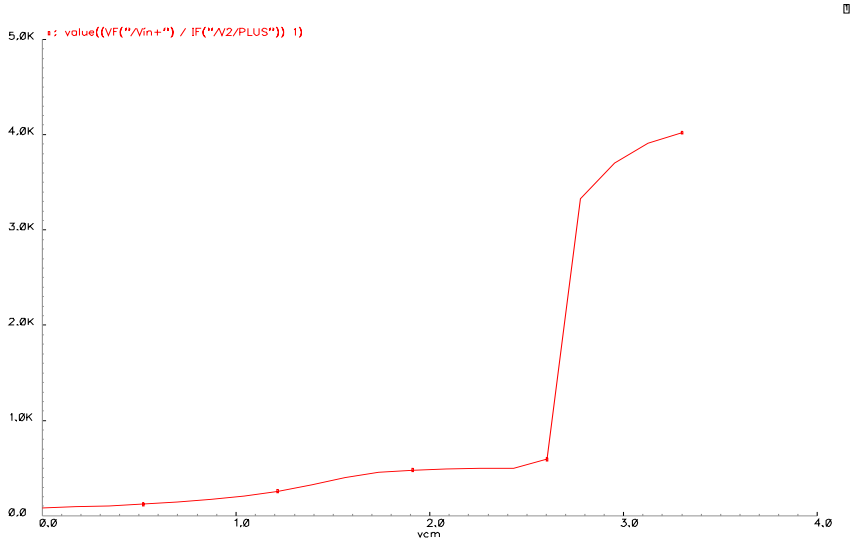

Figure 3.12: On-resistance of the bootstrapped switch

As it can be seen from this graph that the value of finite on-resistance for this bootstrap switch is quite linear and has low value until 2.6 Volts. After that there is a sudden rise in on-resistance value.

3.3.11 LOW-VOLTAGE OPERATION

Low-voltage operation of this switch is not a necessity but a must condition for shrinking technology when rail to rail switching operation is desired without the availability of low threshold MOSFETs. Figure 3.13 summarizes the performance of the bootstrap switch shown in Fig. 3.5 in terms of low on-resistance when supply voltage is varied from 0.9 Volts to 2.9 Volts.

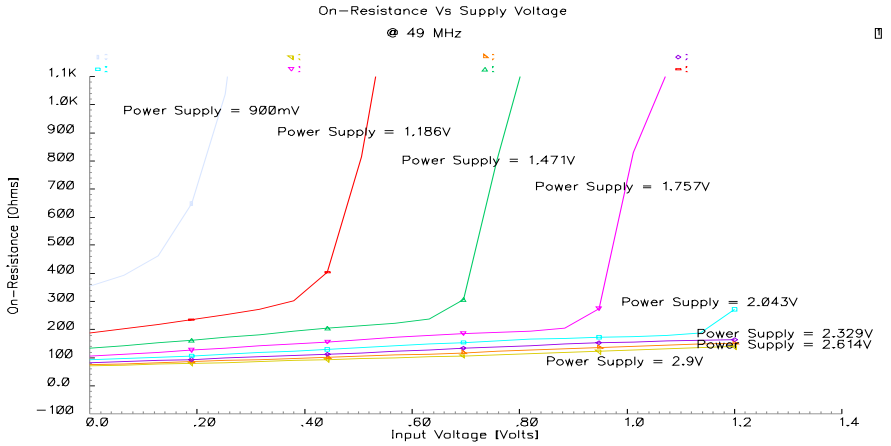

Figure 3.13: Plot of switch impedance vs supply voltage

Figure 3.14 shows that the gate to source voltage is quite linear and fairly signal independent when supply voltage is varied from 1.5 Volts to 3 Volts. This clearly illustrates that bootstrap capacitor Ca in Fig. 3.5 acts as a floating battery.

Figures 3.13 and 3.14 suggest that this switch can operate for voltages as low as 1.5 volts for input signal frequency of 49 MHz and sampling clock of 100 MHz.

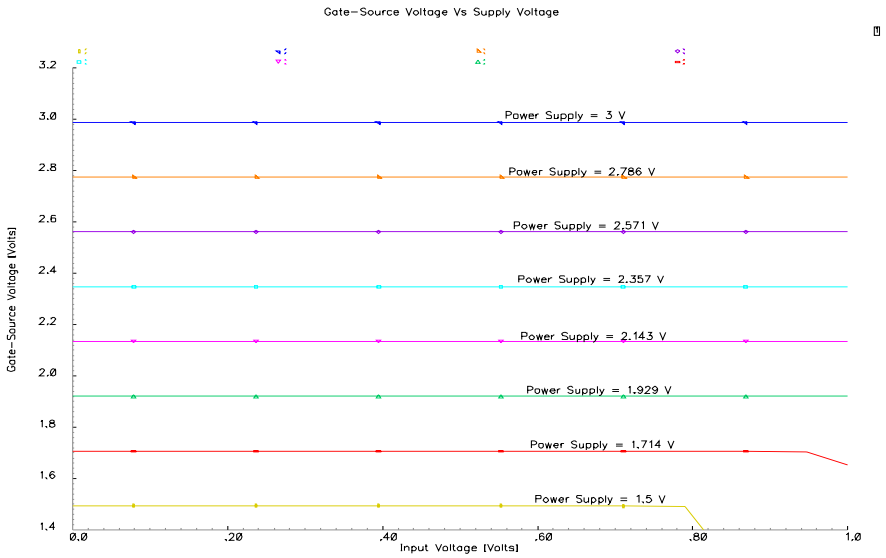

Figure 3.14: Plot of V_{gs} of sampling switch vs supply voltage

4

BULK-EFFECT COMPENSATED SWITCH ARCHITECTURE

4.1 INTRODUCTION

The bootstrapping switch described in the previous chapter reduces the non-linearities significantly by keeping the on-resistance or conductance of the sampling switch to almost a constant level. The on-resistance of this bootstrap switch is given by,

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{dd} - V_t)} \tag{4.1}$$

where V_t in the above expression is given by

$$V_t = V_{t0} + \gamma(\sqrt{2|\Phi_F| + V_{SB}} - \sqrt{2|\Phi_F|}) \tag{4.2}$$

The threshold voltage V_t is the still the cause of nonlinear harmonic distortion in the on-resistance in particular at low-power supply due to bulk-effect V_{SB}, (input signal voltage across source-bulk junction [7]). One way of getting around this problem is to connect the bulk terminal of the bootstrap sampling switch (described in chapter 3) directly to the source of the transistor. But this solution is not possible in standard n-well CMOS processes. This is because the bulk of the NMOS transistor is not isolated from the substrate in an n-well CMOS process. It therefore can not be connected with the source of

the sampling switch. If the same sampling switch is implemented as a PMOS device then the bulk can be connected to the source and it would be a bulk-effect free compensation. In both architectures discussed here, the sampling switch has been implemented as a PMOS device.

4.2 WALTARI BOOTSTRAP SWITCH ARCHITECTURE WITH BULK-EFFECT COMPENSATION

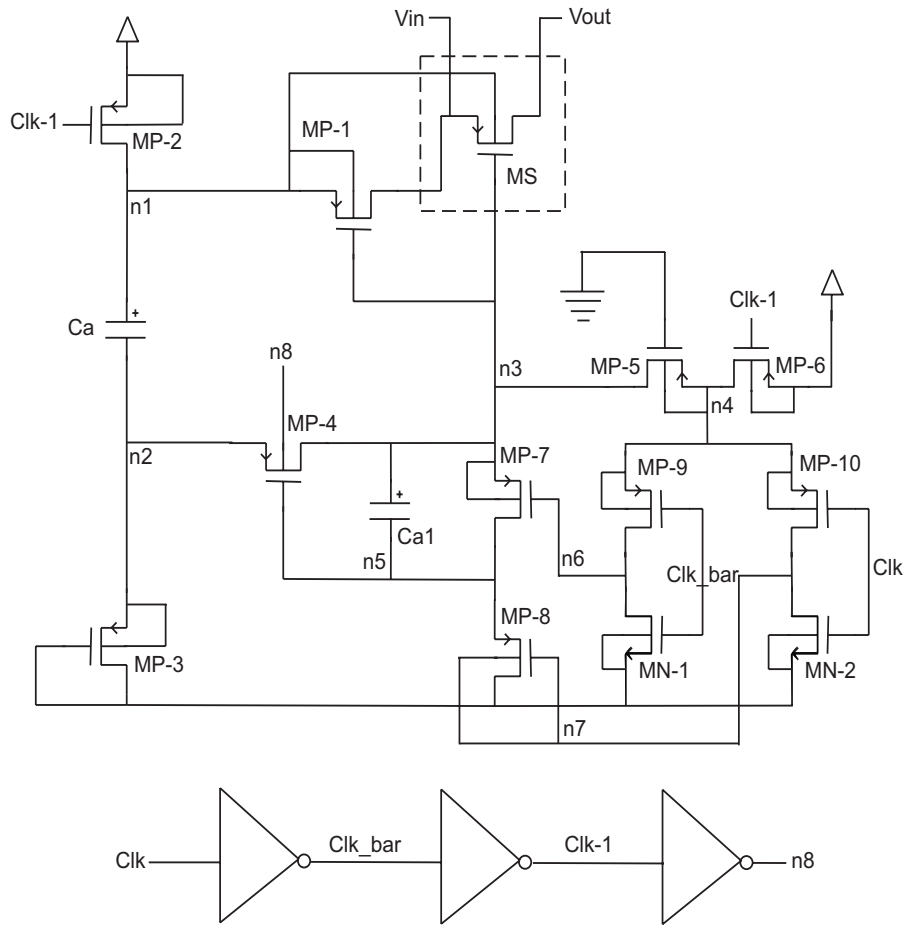

Figure 4.1: Waltari bulk-effect compensated bootstrap switch in n-well CMOS technology

4.2.1 RELIABILITY

The Waltari bootstrap switch works on the same bootstrapping principle as described in chapter 3 with an exception that no where in the circuit, clock doubling has been used. But this is not enough to ensure that the switch is operating with in reliability limits in the long term. Improper transistor connections could lead the gate-source or gate-drain voltages of nodes n2, n3 and n5 to exceed the rated supply voltage of V_{dd} and thus driving transistors out of reliability limits. Transistor MP4 has terminal voltages V_{gs}, V_{gd}, V_{ds} within supply voltage V_{dd} because it's gate voltage always follows node n3. The transistor MP6 drain-source voltage is reduced by the voltage drop across MP5. Transistors MP7 and MP8 are ensured to operate within the reliability limits by connecting their gates to n4 instead of V_{dd} during the off-state. This ensures that the switch is operating within device reliability limits all the time.

4.2.2 CIRCUIT OPERATION

The sampling switch MS is the PMOS transistor in this design which should conduct at voltage levels well below V_{ss}. It's gate voltage is bootstrapped to a more negative voltage by connecting the negative plate of the capacitor C1 to its gate during the tracking phase (Clk -> V_{dd}) through transistor MP4. Transistors MP1 and MP4 isolate the sampling switch MS during the hold phase (Clk -> 0V) while C1 is charged. The series transistor MP1 with sampling switch should also be a PMOS device with an ability to conduct at voltage levels well below V_{ss}. This is the reason that the gates of both the transistors MS and MP1 are connected together to be driven by the bootstrapped negative voltage.

During the hold-phase, node n3 is connected to V_{dd} through MP5 and MP6, thus turning off the sampling switch MS. MP9-MN2 and MP10-MN1 form two inverter pairs turning on MP7 and turning off MP8. The gate of MP4 is also connected to node n3 through MP7 thus turning off this transistor as well. C1 is charged during this phase through MP2 and MP3.

During the tracking phase, MP9-MN2 and MP10-MN1 act as inverters only until the time Clk1 goes high. After Clk1 goes high, node n4 either goes to zero or slightly negative potential. MP7 transistor turns off as Clk goes to V_{dd} while MP8 turns on. Voltage at node n5 which was previously at V_{dd} starts

going down to zero Volts through MP8 while node n3 is still shorted to V_{dd}. As a result voltage appears across capacitor C2. After a short delay, Clk1 goes to V_{dd} releasing node n3 which also starts to go down as transistor MP4 turns on. When the node voltage at n5 reaches the threshold voltage of transistor MP8, it turns off leaving the node n5 as floating. C2 makes n5 to follow n3 with a difference great enough to keep MP4 properly conducting during this phase. The threshold voltage of MP4 is lowered by connecting its bulk to V_{ss} during the on phase.

4.2.3 TRANSISTOR SIZING

Transistors	W/L (um)	Transistors	W/L (um)
MS	32/0.35	MP7	7/0.35
MP1	15/0.35	MP8	1/0.35
MP2	5/0.35	MP9	4.5/0.35
MP3	4/0.35	MP10	9/0.35
MP4	20/0.35	MN1	1.5/0.35
MP5	15/0.7	MN2	3/0.35
MP6	20/0.35		

Table 4.1. Transistor sizing for Waltari bulk-effect free switch

Some considerations for transistor and capacitor sizing are discussed here. All transistors and capacitors are referred to Fig. 4.1.

Sampling switch MS transistor size like MN-10 in Fig. 3.5 is most critical from channel charge injection and low R_{on} point of view. As discussed in Section 3.3.5 if the size of the sampling transistor is large then it will result in increased charge injection at the output as could be seen from Eq. (3.3). On the other hand in order to have lower value of R_{on} the size of the sampling transistor should be larger. From Simulations an optimum value of 32/0.35 um was selected as the sampling transistor W/L ratio for these trade-offs. It is worth mentioning that the effect of charge injection due to NMOS transistor is negative in hold-mode resulting in decrease in the hold-mode voltage level. Whereas in the case of a PMOS transistor this effect is positive and results in increase in voltage level during hold-mode.

MP-3 transistor is a real bottle-neck transistor for achieving good performance. It shall be discussed in detail in Sec. 4.2.4.

The second most important design component is the capacitor Ca1. It's size is extremely important for allowing transistor MP-4 to conduct properly during track mode by maintaining the difference of voltages large enough at nodes n3 and n5. These two nodes are coupled through capacitor Ca1 during track mode. All transistors in the design have length of 0.35um except MN-5 whose length has been kept to 0.7um. This improves a punch-through voltage of MN-5 as described by Eq. (2.7) in Section 2.2.4.

It is important to mention here that different transistors in the circuit have different threshold values which causes unnecessary delays and distortions in the waveforms. The threshold voltage of transistor MP-4 is kept low by switching node n8 to V_{ss} during the on-phase (track-mode) so that it allows the gate voltage of transistors MS and MP1 to reach the desired value quickly.

R_{on} of MP-4 doesn't need to be be very linear, so its size could be smaller as compared to MS and MP-1. The second bootstrap capacitor Ca1 and transistors MP-7 and MP-8 can also be fairly small. This will reduce parasitic capacitance at node n3. The sizes of Ca and Ca1 has been kept to 5pF and 50fF respectively.

4.2.4 PERFORMANCE DEGRADATION AND PROBLEMS WITH THE ARCHITECTURE

This boot strap switch is used in a differential topology to measure SINAD, SFDR and THD with hold capacitance C_h of 800 fF and input signal voltage of 2 volts. The results are summed up in Table 4.2.

	Waltari Bulk-Free Switch
Input Signal Frequency, f_{in}	49 MHz
Sampling Clock Frequency, f_{clk}	100 MHz
Signal to Noise and Distortion Ratio, SINAD	64.3512 dB
Spurious Free Dynamic Range, SFDR	64.8701 dB
Total Harmonic Distortion, THD	-64.8369 dB

Table 4.2. Performance of Waltari Bulk-Free Switch

The performance of this bulk-effect free boot strap switch is clearly degraded as compared to the bootstrap switch without bulk-effect compensation as discussed in Section 3.3. Theoretically speaking if the bootstrap capacitor Ca is fully charged during hold-mode then it should be able to keep the sampling transistor MS ‘on’ in Fig. 4.1 irrespective of the input voltage. The condition for MS to remain on during tracking mode is

$$V_{gs,t} = V_g - V_s - V_t = V_{c,neg} - V_{in} - V_t \geq 0 \tag{4.3}$$

where $V_{c,neg}$ is the voltage on the negative plate of the bootstrap capacitor Ca. During hold-mode, it should be charged maximum to

$$V_c = V_{dd} - V_{on-MP3} \tag{4.4}$$

where V_{on-MP3} is the voltage drop across the transistor MP-3. From this explanation if the on-resistance of transistor MP-3 is low, then voltage drop across this transistor should also be low resulting in a maximum voltage across capacitor V_c in Eq. (4.4). But when this explanation was tested by replacing transistor MP3 with a resistor, it was found that value of the resistance below $3\text{k}\Omega$ is not good enough to ensure maximum swing of rail to rail. This is because transistor MS doesn’t conduct for the entire track mode because of incomplete charging and hence the low voltage across capacitor Ca. The conclusion from this was drawn that this switch architecture is incapable of conducting for the entire rail to rail swing. This was also supported by [8] where they tested the same switch with 1.5 Volts peak to peak voltage.

The second problem with this architecture is that it has parasitic capacitance plus capacitor Ca1 attached to the negative terminal of the bootstrap capacitor Ca. This is going to reduce gate voltage of MS further at node n3 according to the following equation

$$V_{n3} = (V_{dd} - V_{on-MP3})\frac{C_a}{C_a + C_p + Ca1} - V_{in} \tag{4.5}$$

where C_p is the additional parasitic capacitance attached to node n3.

The switch on-operation of transistor MS is strongly input signal dependent due to incomplete capacitor charging and additional capacitances added to the negative plate of the bootstrap capacitor. That is why it is completely conducting during track phase for input voltages near 3.3 volts and partially con-

ducting during the same phase for low input voltages. This greatly degrades the performance of this switch despite the fact that it is bulk effect compensated.

4.3 MODIFIED STEENSGAARD BOOT STRAP SWITCH ARCHITECTURE WITH BULK EFFECT COMPENSATION

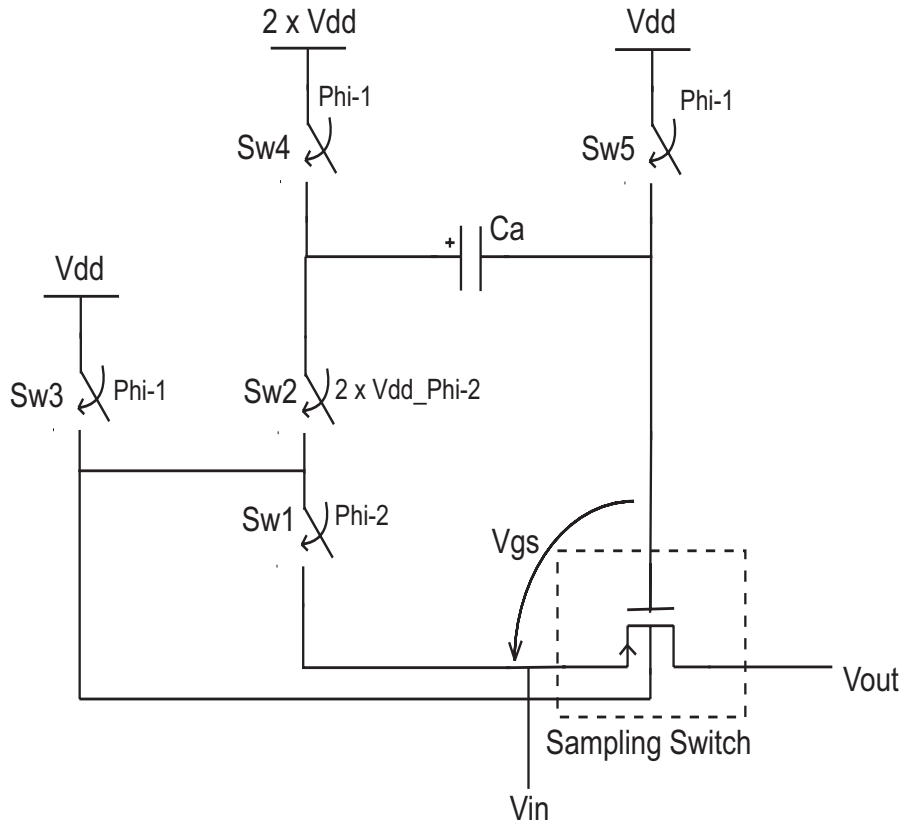

Figure 4.2: Basic bulk-effect ree bootstrap circuit

The fundamental difference between the boot strap switches described previously and the bulk-effect compensated switch discussed in this section is that the bootstrap capacitor Ca is connected directly to the gate terminal of the sampling switch which is a PMOS device. During the hold (off) phase, Sw5

turns off the sampling switch and capacitor Ca is charged between $2V_{dd}$ and V_{dd}. The high potential $2V_{dd}$ is generated by the same clock boosting circuitry as used in the switch architecture shown in Fig. 3.5. In the original Steensgaard switch this high potential is generated by the conventional charge pump circuit shown in Fig. 3.4. During the track (on) phase, Sw1 and Sw2 form a closed loop with the boot strap capacitor Ca. The sampling switch is compensated for the body-effect by connecting its bulk terminal to the input terminal through Sw1. This bulk terminal is connected to V_{dd} during the off-phase of the sampling switch through Sw3. The transistor level implementation of this switch is shown in Fig. 4.3.

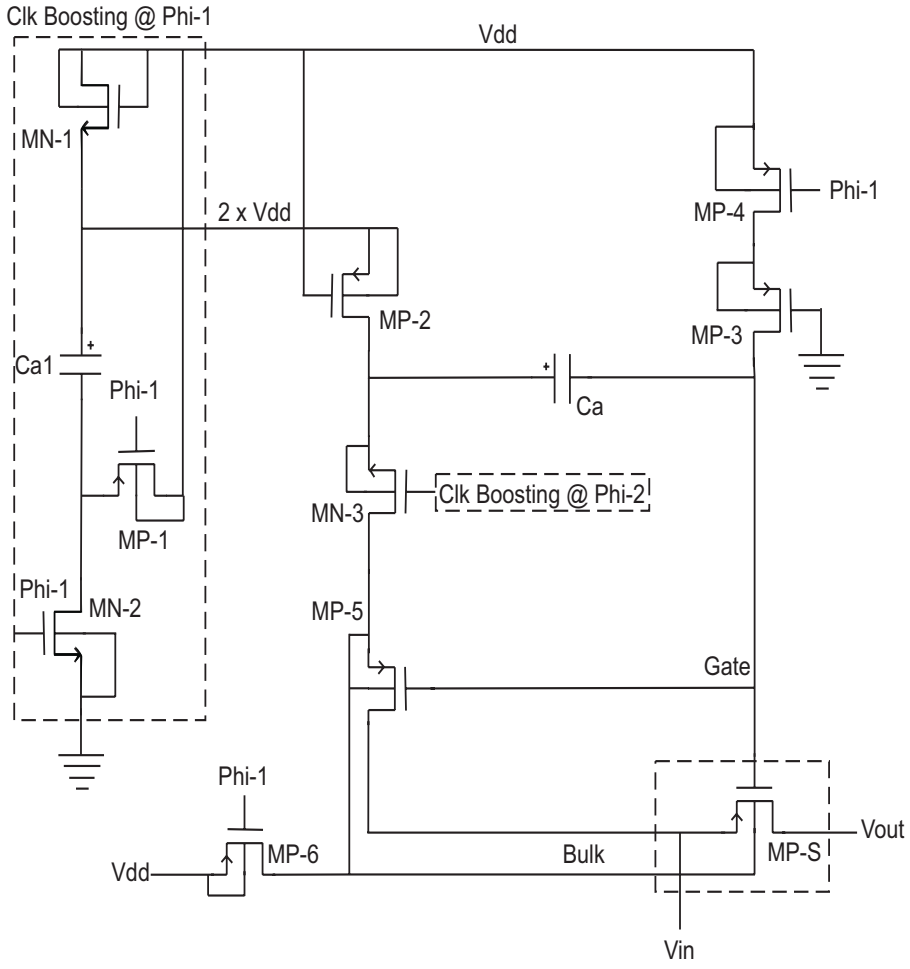

Figure 4.3: Modified Steensgaard Bulk-Effect Compensated Boot Strap Switch in n-well CMOS

4.3.1 RELIABILITY

As discussed above, this bulk effect compensated bootstrap switch is a modified form of Steensgaard switch. The original Steensgaard switch uses conventional charge pump circuit to generate high potential of $2V_{dd}$ as shown in Fig. 3.4. This charge pump circuit is free from reliability limits as the gate source voltage of these transistors is approximately twice as much as the specified supply voltage (3.3 V for 0.35um Process). In the modified switch the charge pump circuit is replaced with a fully reliable clock-boosting circuit shown in dotted box in Fig. 4.3. This clock boosting circuit is the same as the one used in the bootstrap switch architecture discussed in Sec. 3.3.2. The gate oxide of MP-4 in Fig. 4.3 is protected by a cascode PMOS device MP-3. Transistor MN-3 is also operated with the same clock-boosting circuit shown dotted in Fig. 4.3 for reliability considerations.

4.3.2 CIRCUIT OPERATION

Figure 4.3 shows a transistor level implementation of the switch in Fig. 4.2. Phi-1 and Phi-2 are the non-overlapping clocks. Sw4 is implemented as a PMOS device MP-2 whose gate voltage is at constant V_{dd} and source voltage is at $2V_{dd}$ during zero phase of the clock Phi-1. Sw3 and Sw5 are implemented with simple PMOS devices MP-6 and MP-4 in Fig. 4.3. A cascode PMOS device MP-3 is used to protect the gate oxide of MP-4 due to $2V_{dd}$ stress voltage. Sw1 is implemented as a PMOS device with its gate terminal connected to the gate of the main sampling switch MP-S. Both the gate signals are controlled with the negative voltage of the bootstrap capacitor Ca for turning on these transistors and with V_{dd} for turning off these transistors. Sw2 has been implemented as an NMOS device whose gate terminal is connected to another similar clock boosting circuit as shown in dotted box in Fig. 4.3. The only difference is that it gives $2V_{dd}$ during zero phase of the clock Phi-2. There could also be alternative ways of implementing Sw2 as discussed in [7].

During hold (off) phase of the sampling switch MP-S (Phi_1 is zero), the bootstrap capacitor Ca is charged between $2V_{dd}$ and V_{dd} through transistors MP-2, MP-3 and MP-4. V_{dd} comes directly across the gate of the sampling switch MP-S thus turning it off. The bulk of MP_S is connected to V_{dd} during this phase through MP-5. During track (on) phase of the sampling switch MP_S (Phi_2 is zero), MP-5 turns on due to $2V_{dd}$ at its gate terminal gener-

ated by the clock-boosting circuit. This enables the bootstrap loop and the negative plate of Ca plus the input voltage is applied to the gate terminals of transistors MP-5 and MP-S thus turning them on. The bulk terminal of the sampling switch is connected to the input voltage through MP-5 which compensates distortion due to body-effect by making V_{sb} equal to zero.

4.3.3 TRANSISTOR SIZING

Transistors	W/L (um)	Transistors	W/L (um)
MP-1	27/0.35	MP-6	1/0.35
MP-2	9/0.35	MP-S	50/0.35
MP-3	1/0.35	MN-1	15/0.35
MP-4	1/0.35	MN-2	15/0.35
MP-5	3/0.35	MN-3	1/0.35

Table 4.3. Transistor sizing for modified Steensgaard bulk-effect free switch

Some considerations for transistor and capacitor sizing are discussed here. All transistors and capacitor are referred to Fig. 4.3.

Transistor sizing of the sampling switch has been discussed in Sec. 4.2.3. The same considerations apply here for the sizing of sampling Transistor MP-S.
Although the two clock-boosting circuits operating at Phi-1 and Phi2 respectively in Fig. 4.3 are structurally identical but their transistor sizing is different. The reason behind this is that clock-boosting circuit operating at Phi-1 is connected to the source of the transistor MP-2 to allow it to charge the boot strap capacitor Ca between $2V_{dd}$ and V_{dd}. Where as in the case of transistor MP-2 clock-boosting circuit operating at Phi-2 is connected to the gate terminal of the transistor MN-3. In the former case there is a large sourcing of current from the clock boosting circuit as compared to the latter case because the gate of MOS FET offers high electrical isolation. The transistor capacitor sizing for the clock boosting circuit operating at Phi-2 is same as described in Section 3.3.7. The sizes of Ca and Ca1 has been kept to 1 pF and 20 pF respectively.

4.3.4 PERFORMANCE DEGRADATION AND PROBLEMS WITH THE ARCHITECTURE

The performance from linearity point of view obtained from this switch architecture is summarized in the following two Tables 4.4 and 4.5. This bulk-effect free bootstrap switch is used in a differential topology to measure SINAD, SFDR and THD with hold capacitance of 800 fF, rail to rail input signal voltage of 3.3 volts and sampling clock of 100 MHz. The difference between the two tables is that in case of Table. 4.4 the results are taken with ideal clock-boosting sources, where as in Table. 4.5 the results are summarized with the actual clock boosting circuits.

	Modified Steensgaard Bulk-Free Switch
Input Signal Frequency, f_{in}	49 MHz
Sampling Clock Frequency, f_{clk}	100 MHz
Signal to Noise and Distortion Ratio, SINAD	97.6157 dB
Spurious Free Dynamic Range, SFDR	100.6838 dB
Total Harmonic Distortion, THD	-100.4796 dB

Table 4.4. Performance of modified Steensgaard bulk-free switch with ideal clock boosting sources

	Modified Steensgaard Bulk-Free Switch
Input Signal Frequency, f_{in}	49 MHz
Sampling Clock Frequency, f_{clk}	100 MHz
Signal to Noise and Distortion Ratio, SINAD	80.0688 dB
Spurious Free Dynamic Range, SFDR	81.4962 dB
Total Harmonic Distortion, THD	-79.8169 dB

Table 4.5. Performance of modified Steensgaard bulk-effect free switch with actual clock boosting circuit

The problem of the incomplete charging of the bootstrap capacitor in the Waltari switch architecture is nicely addressed in this modified Steensgaard bulk-effect free architecture by charging the capacitor between $2V_{dd}$ and V_{dd} Volts instead of V_{dd} and 0 volts. This bulk-effect free architecture is also

capable of attaining very high linearity, as high as 100 dB corresponding to SFDR and THD values, when operated with ideal clock-boosting sources for rail to rail swing. It is also interesting to observe that SINAD degrades by approximately 17 dB when actual clock boosting circuits are used. The problem also lies within the higher value of sample to hold step or pedestal error for this architecture. This error is typically more than 200mV for this sampling switch for a linearity of around 100 dB. If the sampling switch MP-S size is decreased, pedestal error decreases but at the same time it also results in decreased values of SFDR and THD.

5

CONCLUSION

The non-negotiable specification for the switch requires it to be operated at a sampling clock of 100 MHz with maximum input signal frequency of 50 MHz for a rail to rail swing and differential topology in 0.35υm n-well CMOS technology. The intention is to achieve maximum SINAD, SFDR, THD and minimum on-resistance during track-mode and also minimum sample-to-hold step size during hold-mode. Low-voltage operation for maximum linearity, low power consumption and minimum area are the additional features which are intended. It is very important to develop a precedence order of these performance metrics in order to obtain a criteria for selecting the switches. The precedence order of these performance metrics is described as follows.

- SFDR and THD during track-mode
- SINAD during track-mode
- On-resistance during track-mode
- Sample-to-hold step size during hold-mode
- Low-voltage operation
- Power consumption and area constraints

For all the above mentioned criteria, input signal dependent boot strap architecture without bulk-effect compensation described in Section 3.3 has been found the best. The summary of results has been shown in Table 5.1.

	TG	Waltari Bulk-Effect Compensated Architecture	Modified-Steens-gaard Bulk-Effect Compensa-ted Archi-tecture	Bulk-Effect Free Bootstrap Switch
SINAD [dB]	47.9841	64.3512	80.0688	87.0092
SFDR [dB]	48.3598	64.8701	81.4962	87.1067
THD [dB]	-46.389	-64.8369	-79.8169	-87.102

Table 5.1. Summary of switch architecture from linearity point of view

It was also observed that bulk-effect compensated switch architecture show good improvement in SFDR and THD values for single ended application but for a differential topology they were not able to show a significant improvement. This statement was further confirmed by implementing the boot strap switch described in Section 3.3 as a bulk-effect compensated switch by connecting it's bulk directly to the input terminal and thus zeroing V_{sb}. An improvement of only 1.1 DB was observed in the corresponding SFDR and THD values. The effect of bulk-effect compensation was studied over second and third-order harmonics to extend this study. It was found that bulk-effect compensation significantly reduces the second order harmonic as compared to the third order harmonic for a specified supply voltage of 3.3 volts for 0.35υ m CMOS technology. This also explains that why bulk-effect compensation did not show better improvement from linearity point of view in differential topology.

APPENDIX-A

Extract_sinusoids.m

```
function[mag,fas,offset]=Extract_sinusoids(y,n,WkT)
% [mag,fas,offset]=Extract_sinusoids(y,n,WkT)
% Uses a least squares fit to find the amplitudes, phases,
% and offsets of a sum of sinusoids of known frequencies WkT
% y(n) is the measured data and n is the time index.
% The phases are extracted with reference to the first value
% of n.

aa=[];
for k=1:length(WkT)
 aa=[aa sin(WkT(k)*n)' cos(WkT(k)*n)'];
end
aa=[aa ones(length(n),1)];
AA=aa'*aa;
bb=aa'*y';
E=AA•b;
mag=[];
fas=[];
offset=[];
for k=1:2:length(E)-1
mag=[mag sqrt(E(k)^2+E(k+1)^2)];
if E(k)<0
 fas=[fas atan(E(k+1)/E(k))+pi];
```

```
else
 fas=[fas atan(E(k+1)/E(k))];
end
end
offset=E(length(E));
```

SINAD.m

```
clear;
ytot_diff=dlmread('/home/tde/muhka007/filename,' ') ;
ytot_diff=ytot_diff';
WkT_diff=2*pi*[0.49 0.02 0.47 0.04 0.45];
WkT_diff=2*pi*0.49 ;
n_diff=0:length(ytot_diff)-1;
[mag_diff,fas_diff,offset_diff]=Extract_sinusoids(ytot_diff,n_diff,WkT_diff)
; % Estimated magnitudes and phases of the sinusoids
yhat_diff=0;
for k_diff=1:length(mag_diff)
yhat_diff=yhat_diff+mag_diff(k_diff)*sin(WkT_diff(k_diff)*n_diff+fas_diff
(k_diff));
end
yhat_diff=yhat_diff+offset_diff;
er_diff=ytot_diff-yhat_diff;
SNR_diff=10*log10(sum((yhat_diff-offset_diff).^2)/sum((ytot_diff-
yhat_diff).^2));
disp(['Estimated SNR : ' num2str(SNR_diff) ' DB']);   % ei phases of the
sinusoids
```

SFDR_THD.m

```
load bit-filename;
```

```
n=0:length(bit-filename)-1;
WkT=2*pi*[0.49 0.02 0.47 0.04 0.45];
[mag,fas,offset]=Extract_sinusoids(bit-filename',n,WkT);
thd_2=20*log10*sqrt(sum(mag(2:length(mag)).^2))/abs(mag(1));
display(['THD : ' num2str(thd_2) ' %']);
SFDR=20*log10(mag(1)/max(mag(2:length(mag))));
display(['SFDR : ' num2str(SFDR) ' DB']);
```

SFDRplot.m

```
close all
x=dlmread('/home/tde/muhka007/filename',' ');
X=fft(blackmanharris(length(x)).*x);
wT=linspace(0,2*pi,length(X));
figure(1)
plot(wT/(2*pi),20*log10(abs(X)/max(abs(X))));
title ('SFDR of Boot-Strapped Switch');
xlabel('Normalized frequency');
ylabel ('dB')
```

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