ECE 4435 Learning Activity 2 Report

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I. Intro

The purpose of this lab was to construct a Register File (RF) for our RISC processor.

II. Register File

The RF is responsible for acting as memory for the CPU of our RISC processor. The figures below act as my justification as to why I believe my design meets the requirements.

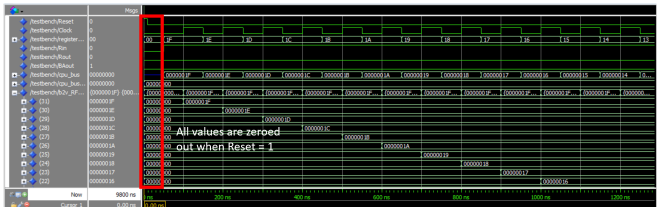

Fig. 1. Verification for Reset

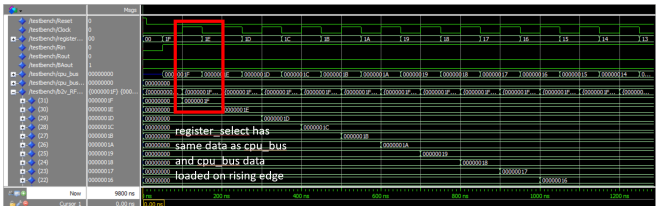

Fig. 2. Verification for Register Select

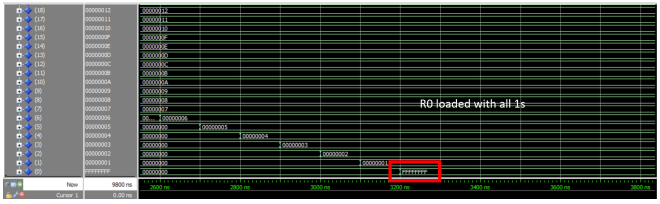

Fig. 3. Verification for R0 (part 1)

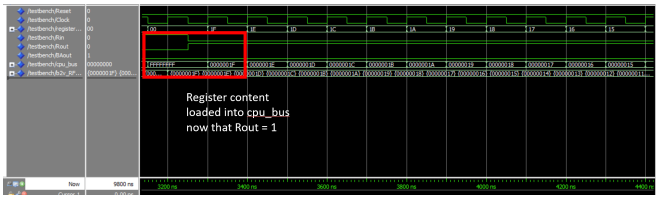

Fig. 4. Verification for Rout

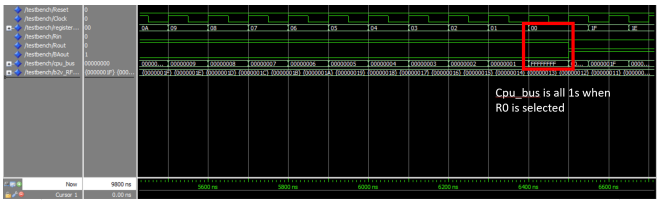

Fig. 5. Verification for R0 (part 2)

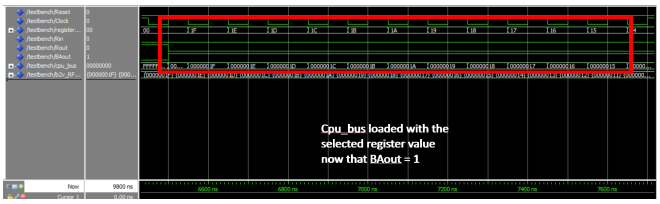

Fig. 6. Verification for BAout

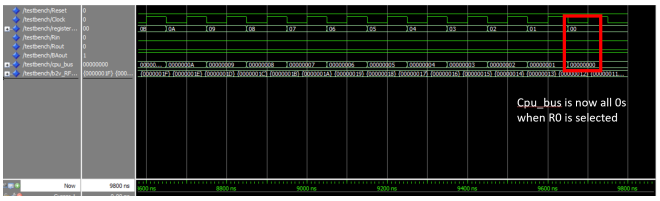

Fig. 7. Verification for R0 (part 3)