ECE 4435 Learning Activity 4 Report

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I. Intro

The purpose of this lab was to construct the Control Signals Logic for our RISC processor.

II. Control Signals Logic

The Control Signals are responsible for acting as a decoder for the opcodes generated by the CPU, which then tells the CPU to perform some instruction. Some of it's functionality includes reading/writing memory, turning components in the datapath on/off, and selecting an input from multiple different input signals. Figure 1 below acts as my justification as to why I believe my design meets the requirements.

```
VSIM 3> run 12000 ns
# ** Note: Number of errors = 0
#    Time: 11600 ns  Iteration: 0  Instance: /testbench
```

Fig. 1. Control Signals Logic (and Opcode Decoder) Verification