ECE 4435 Learning Activity 1 Report

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I. Intro

The purpose of this lab was to become familiar with using Intel Quartus II. This was done by constructing and testing a functioning Program Counter (PC) and Instruction Register (IR).

II. Program Counter

The PC is responsible for holding different memory addresses of certain executions.

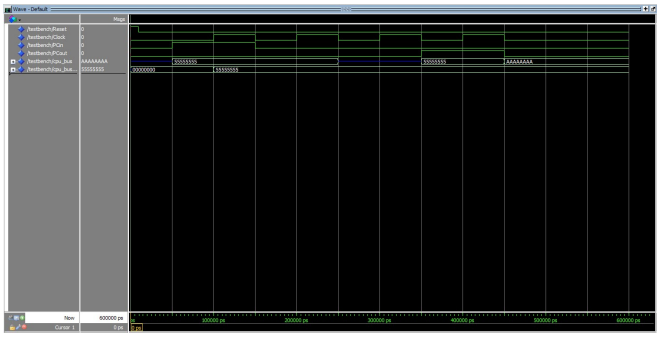

Fig. 1. Verification for Program Counter

Below are the requirements and the justification as to why I believe this design is sufficient:

- When Reset = 1, PC is initialized to all 0's: All values in Figure 1 are zero when Reset = 1.
- If PCin = 1, then PC is loaded with cpu_bus at next clock edge: When PCin goes high at 50 ns, the PC cpu_bus is loaded during the next rising edge.
- If PCout = 1, then cpu_bus is driven with contents of the PC: The bus is loaded when PCout goes high.
- Else, output of PC is tri-stated (value all Z's): On the falling edge after PCout is 0, the cpu_bus goes into high impedance mode.

III. Instruction Register

The IR stores whatever instruction that is currently being executed by the computer.

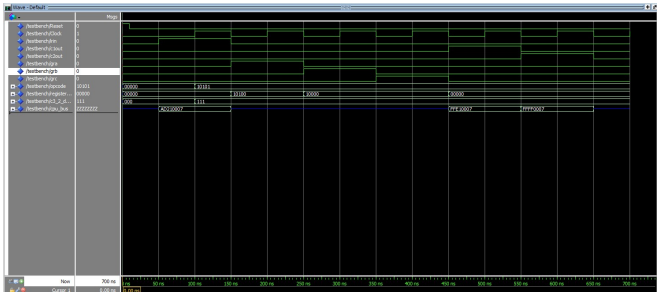

Fig. 2. Verification for Instruction Register

Below are the requirements and the justification as to why I believe this design is sufficient:

- When Reset = 1, IR is initialized to all 0's: All values are 0 when Reset goes high at the beginning of Figure 2.
- If IRin = 1, then IR is loaded with cpu_bus at next clock edge: IRin goes high at 50 ns, and the IR is then loaded with the bus at the next clock edge at 100 ns.
- If c1out = 1, then CPU_bus(21 downto 0) is assigned IR(21 downto 0), and CPU_bus(31 downto 22) is assigned IR(21): At 450 ns, c1 out goes high and the bus is loaded with the correct value.
- If c2out = 1, then CPU_bus(16 downto 0) is assigned IR(16 downto 0), and CPU_bus(31 downto 17) is assigned IR(16): At 550 ns, c2 out goes high and the bus is loaded with the correct value.
- Opcode(4 downto 0) is assigned IR(31 downto 27): At 100 ns, the opcode field is populated with IR(31 downto 27).
- If Gra = 1, then register_select(4 downto 0) is assigned IR(26 downto 22): Gra is 1 at 150 ns, and register_select (4 downto 0) then changes to the correct value, IR(26 downto 22).
- If Grb = 1, then register_select(4 downto 0) is assigned IR(21 downto 17): Grb is 1 at 250 ns, and register_select (4 downto 0) then changes to the correct value, IR(21 downto 27).
- If Grc = 1, then register_select(4 downto 0) is assigned IR(16 downto 12), else, register_select is assigned all 0's: Grc is 1 at 350 ns, and register_select (4 downto 0) then changes to the correct value, IR(16 downto 12).
- c3_2_downto_0(2 downto 0) is assigned IR(2 downto 0): At 100 ns, c3_2_downto_0(2 downto 0) is populated with IR(2 downto 0).