Spyridon Liaskonis

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Research Interests

High-Performance Computing, Hardware Accelerators, Operating Systems, Embedded Systems, Computer Architecture, Deep Learning.

Education

2020 - Present Diploma (5 years) in Electrical and Computer Engineering
University of Thessaly, Volos, Greece

Skills

- **Programming Languages , Libraries:** C, C++, Python, CUDA, OpenMP, OpenMPI, Verilog, HLS C/C++, Pthreads, MATLAB, NumPy, Matplotlib
- **Tools:** git, make, PyTorch, TensorFlow, Xilinx Vitis HLS, Xilinx Vivado, Intel Vtune Profiler, Intel Advisor, LaTeX, Linux, Bash, ONNX

Selected Academic Courses - Projects

— ECE 429 Special Topic: Reinforcement Learning-driven Bitwidth Optimization for Neural Network Quantization on FPGAs (Ongoing)

Collaborating on an existing project that utilizes reinforcement learning to automate and optimize the deployment of neural networks on FPGAs, focusing on achieving high accuracy while adhering to resource and latency constraints.

Project:

- Developing and evaluating new reward functions for the RL agent.
- Adding support for multiple FPGA platforms to the workflow.
- Testing and validating the framework on various network architectures.

Technologies: **FINN, PyTorch, Brevitas, Gymnasium**

— ECE 415: High-Performance Computing

- Parallel implementation of a Sobel Filter with OpenMP.
- GPU acceleration of a separable convolution kernel with CUDA.
- GPU acceleration of a histogram equalization algorithm with CUDA.
- CPU/GPU acceleration of an N-body simulation with OpenMP/CUDA.

Technologies: **C, CUDA, OpenMP**
More information

— ECE 340: Embedded Systems

- Hardware acceleration of the Smith-Waterman Local Sequence Alignment algorithm for Genomics using the Vitis High-Level Synthesis toolset, on a low-power FPGA MPSoC.
- Performance measurement of bare-metal embedded software on an ARM processor.
- IEEE 754 compatible Floating-Point Adder in Verilog on an FPGA.

Technologies: **C, OpenCL, Verilog, Vivado, Vitis HLS**
More Information

— ECE494: Processor Design

- Hardware acceleration of Quantized Deep Neural Networks on FPGAs using the FINN compiler by Xilinx. Evaluation of several levels of quantization and the effects on accuracy, performance, and resource utilization.

Technologies: **FINN, PyTorch, Brevitas, ONNX**

— ECE 445: Parallel & Distributed Computing

- Designed and implemented parallel algorithms for matrix multiplication and the Jacobi method using OpenMP, focusing on thread distribution, scheduling, and performance optimization.

- Designed and implemented parallel algorithms for calculating communication costs in a distributed system, using MPI to measure point-to-point and broadcast communication times, and optimizing performance for matrix-vector multiplication and sorting algorithms.

Technologies: **C, OpenMP, OpenMPI**

— ECE 447: Neuro-Fuzzy Computing

- Fine-tuned the BERT architecture for news classification
- Applied data preprocessing using NLTK.
- Trained and evaluated the model using PyTorch, optimizing performance through hyperparameter tuning.

Technologies: **PyTorch, NLTK**

— ECE 318: Operating Systems

- Benchmarking alternatives of Shortest-Job First (SJF) on a VM that emulates the API of the Linux scheduler.
- Implementation of a user-space file system based on FUSE with support for basic file operations.
- Modifying the SLOB memory allocator to use the First-fit algorithm for both page and block allocation.

— ECE 513: Circuit Simulation Algorithms

Project:

- Development of a complete circuit simulation program like SPICE in C++.
- Implemented parsing, equation formulation, and solution techniques (direct and iterative methods) for linear circuits.
- Utilized sparse matrix techniques and external libraries (Eigen) for efficient computation.
- Performed transient analysis to simulate circuit behavior over time.

Technologies: **C++, FLEX, Bison, Eigen, CMAKE**
More information

— ECE 333: Digital Systems Lab

Verilog Implementation and evaluation on Nexys A7 FPGA of:

- A 7-Segment Display Driver to display a scrolling message.
- A UART serial communication system.
- A VGA driver used to drive a conventional monitor and depict a variety of images.

More information

— ECE 340: Concurrent Programming

- Implemented a coroutine-based system for concurrent code execution with explicit switching, using functions to manage execution contexts. Extended the implementation to support concurrent execution with threads using automatic switching via an alarm/timer and a round-robin scheduling policy.
- Implementation of many concurrent algorithms in C/Java using Semaphores/Monitors.

Technologies: **C, pthreads**
More information

Voluntary Work/Extra Curriculars

- Teaching Assistant for ECE219: Computer Organization and Design (September 2024- Present)
  Examination of laboratory assignments on MIPs assembly programming, Verilog implementation of a MIPs CPU, and performance analysis and optimization of a large program on x86 CPUs. Reference: Prof. Nikolaos Bellas

Languages

English: Professional Working Proficiency (Michigan Lower - ECCE)
Greek: Native Language