ProcessorToLevel Project Status (01/31/2017 - 12:31:28)			
Project File:	lab1.xise	**Parser Errors:**	No Errors
Module Name:	ProcessorToLevel	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3csg324	**• Errors:**	No Errors
Product Version:	ISE 14.6	**• Warnings:**	44 Warnings (2 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	66	18,224	1%	
Number used as Flip Flops	66			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	55	9,112	1%	
Number used as logic	49	9,112	1%	
Number using O6 output only	16			
Number using O5 output only	13			
Number using O5 and O6	20			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	6			
Number with same-slice register load	4			
Number with same-slice carry load	2			
Number with other load	0			
Number of occupied Slices	22	2,278	1%	
Number of MUXCYs used	36	4,556	1%	
Number of LUT Flip Flop pairs used	69			
Number with an unused Flip Flop	9	69	13%	
Number with an unused LUT	14	69	20%	
Number of fully used LUT-FF pairs	46	69	66%	
Number of unique control sets	5			
Number of slice register sites lost to control set restrictions	6	18,224	1%	
Number of bonded IOBs	23	232	9%	
Number of LOCed IOBs	23	23	100%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	1	64	1%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	4	16	25%	
Number used as BUFGs	4			
Number used as BUFGMUX	0			

Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.14			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Tue Jan 31 12:30:34 2017	0	32 Warnings (2 new)	7 Infos (2 new)
Translation Report	Current	Tue Jan 31 12:30:40 2017	0	0	0
Map Report	Current	Tue Jan 31 12:30:54 2017	0	1 Warning (0 new)	8 Infos (0 new)
Place and Route Report	Current	Tue Jan 31 12:31:06 2017	0	10 Warnings (0 new)	3 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Tue Jan 31 12:31:11 2017	0	0	4 Infos (0 new)
Bitgen Report	Current	Tue Jan 31 12:31:24 2017	0	1 Warning (0 new)	1 Info (0 new)

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Tue Jan 31 12:29:35 2017	
WebTalk Report	Current	Tue Jan 31 12:38:55 2017	
WebTalk Log File	Current	Tue Jan 31 12:38:59 2017	

Date Generated: 01/31/2017 - 12:40:10