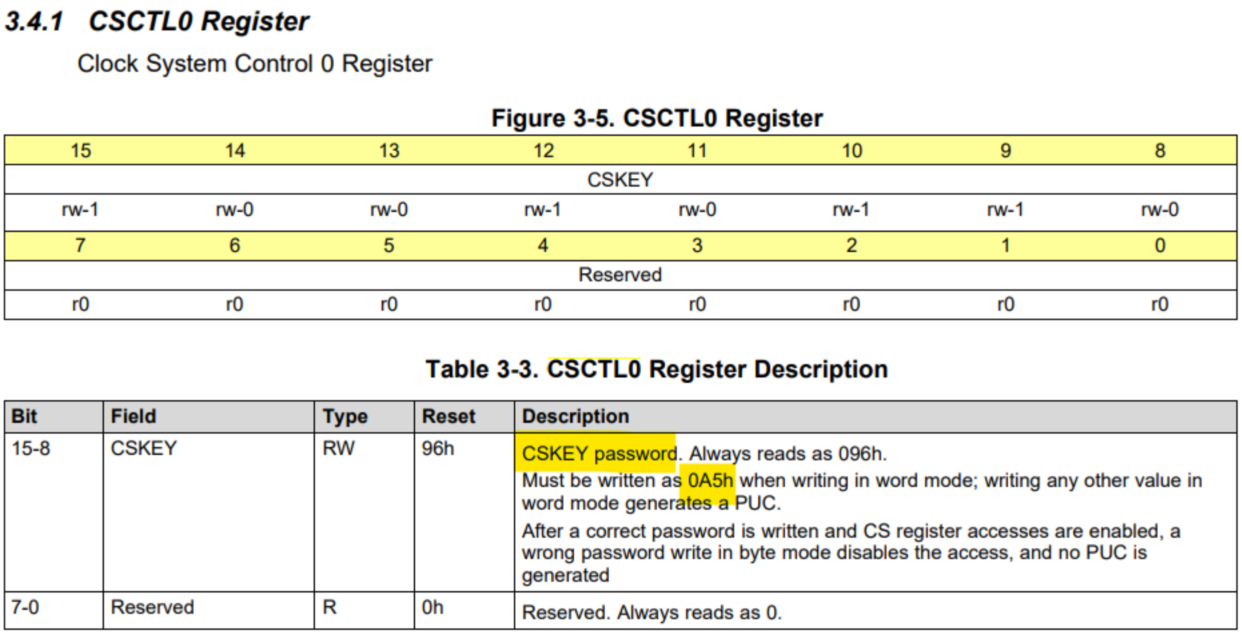
Lab2

Contents

Ex1 – Clock configuration

1. Setup SMCLK to run on DCO



3.4.1 CSCTL0 Register

Clock System Control 0 Register

Figure 3-5. CSCTL0 Register

15	14	13	12	11	10	9	8
CSKEY							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0

Table 3-3. CSCTL0 Register Description

Bit	Field	Type	Reset	Description
15-8	CSKEY	RW	96h	CSKEY password. Always reads as 096h. Must be written as 0A5h when writing in word mode; writing any other value in word mode generates a PUC. After a correct password is written and CS register accesses are enabled, a wrong password write in byte mode disables the access, and no PUC is generated
7-0	Reserved	R	0h	Reserved. Always reads as 0.

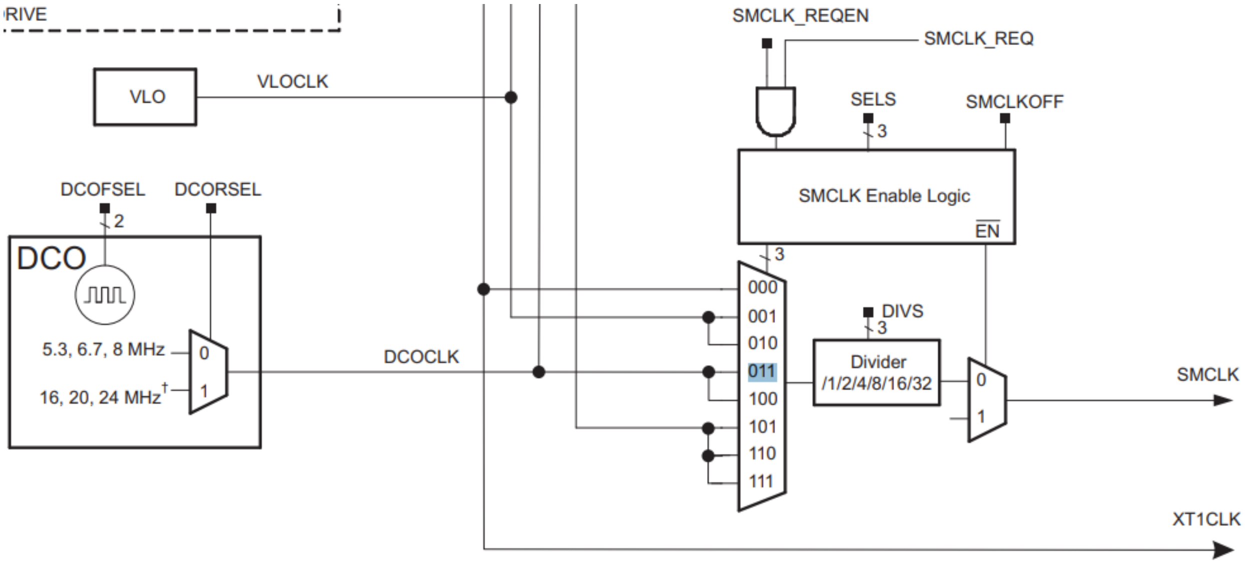


Figure 1 - family guide p. 72

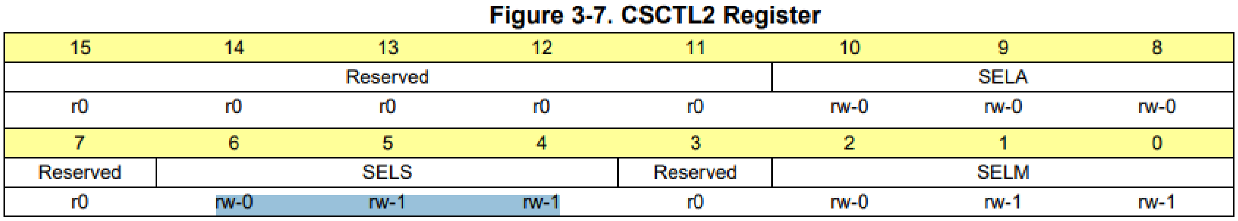


Figure 3-7. CSCTL2 Register

15	14	13	12	11	10	9	8
Reserved					SELA		
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	SELS			Reserved	SELM		
r0	rw-0	rw-1	rw-1	r0	rw-0	rw-1	rw-1

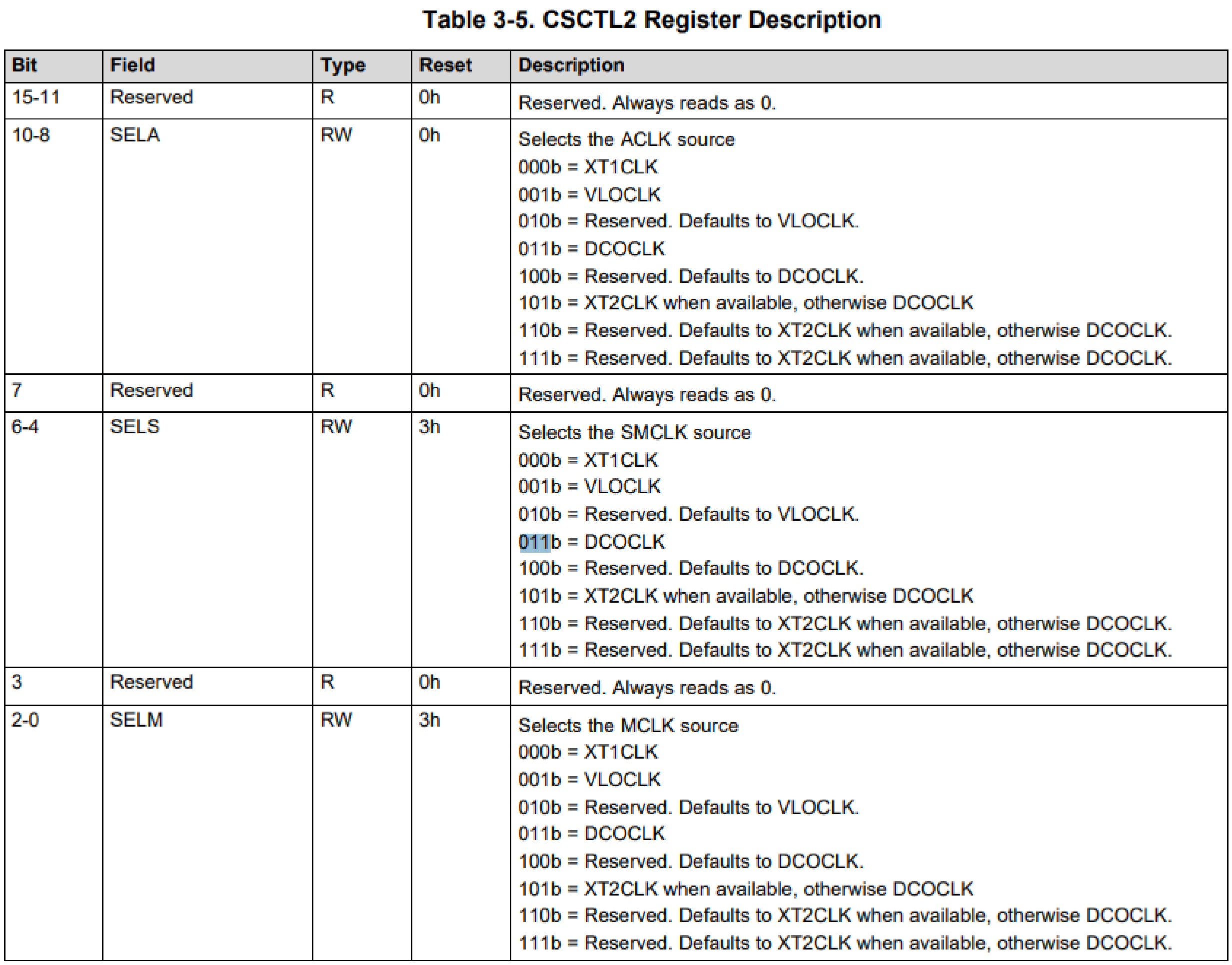
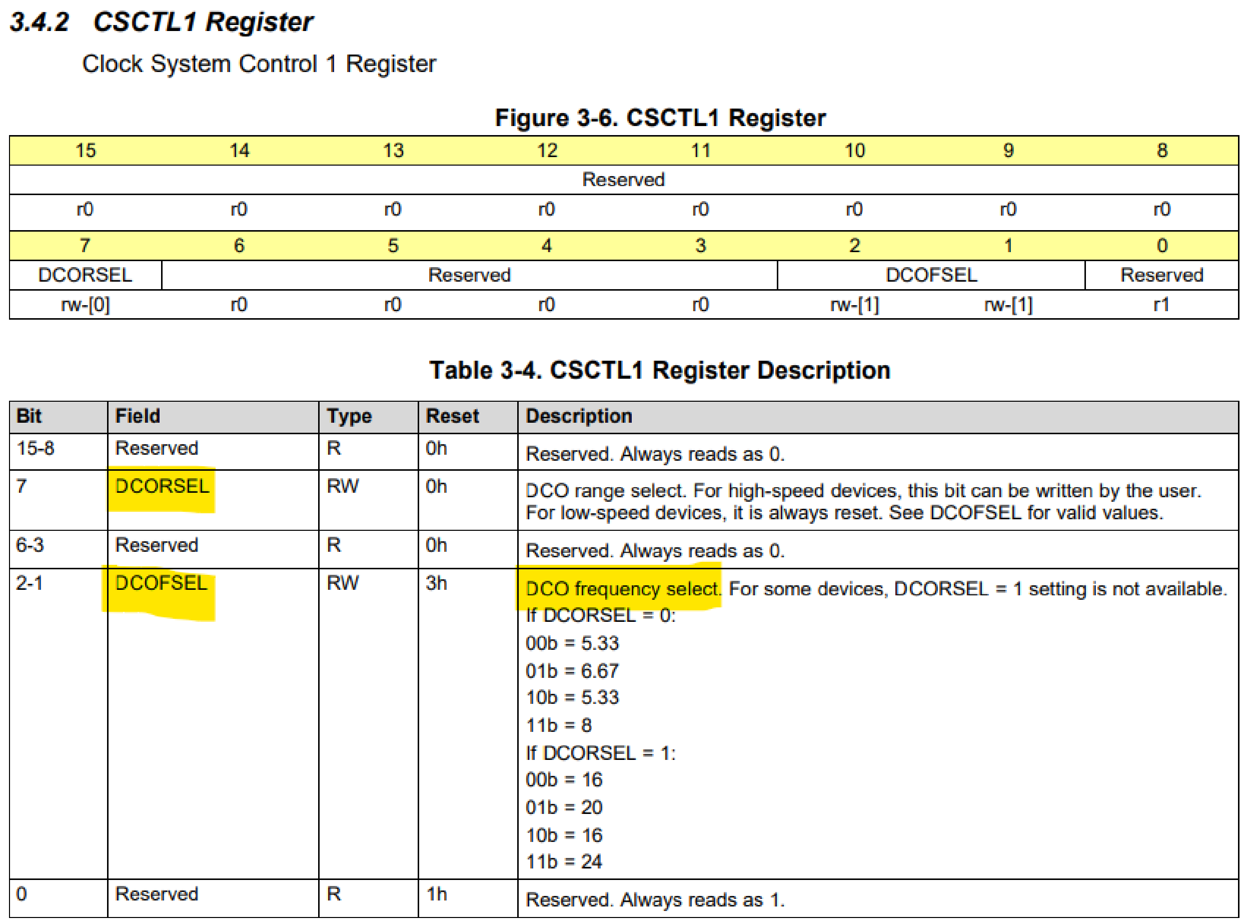


Table 3-5. CSCTL2 Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10-8	SELA	RW	0h	Selects the ACLK source 000b = XT1CLK 001b = VLOCLK 010b = Reserved. Defaults to VLOCLK. 011b = DCOCLK 100b = Reserved. Defaults to DCOCLK. 101b = XT2CLK when available, otherwise DCOCLK 110b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK. 111b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK.
7	Reserved	R	0h	Reserved. Always reads as 0.
6-4	SELS	RW	3h	Selects the SMCLK source 000b = XT1CLK 001b = VLOCLK 010b = Reserved. Defaults to VLOCLK. 011b = DCOCLK 100b = Reserved. Defaults to DCOCLK. 101b = XT2CLK when available, otherwise DCOCLK 110b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK. 111b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK.
3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	SELM	RW	3h	Selects the MCLK source 000b = XT1CLK 001b = VLOCLK 010b = Reserved. Defaults to VLOCLK. 011b = DCOCLK 100b = Reserved. Defaults to DCOCLK. 101b = XT2CLK when available, otherwise DCOCLK 110b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK. 111b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK.

2. Configure the DCO to run at 8 MHz



3.4.2 CSCTL1 Register

Clock System Control 1 Register

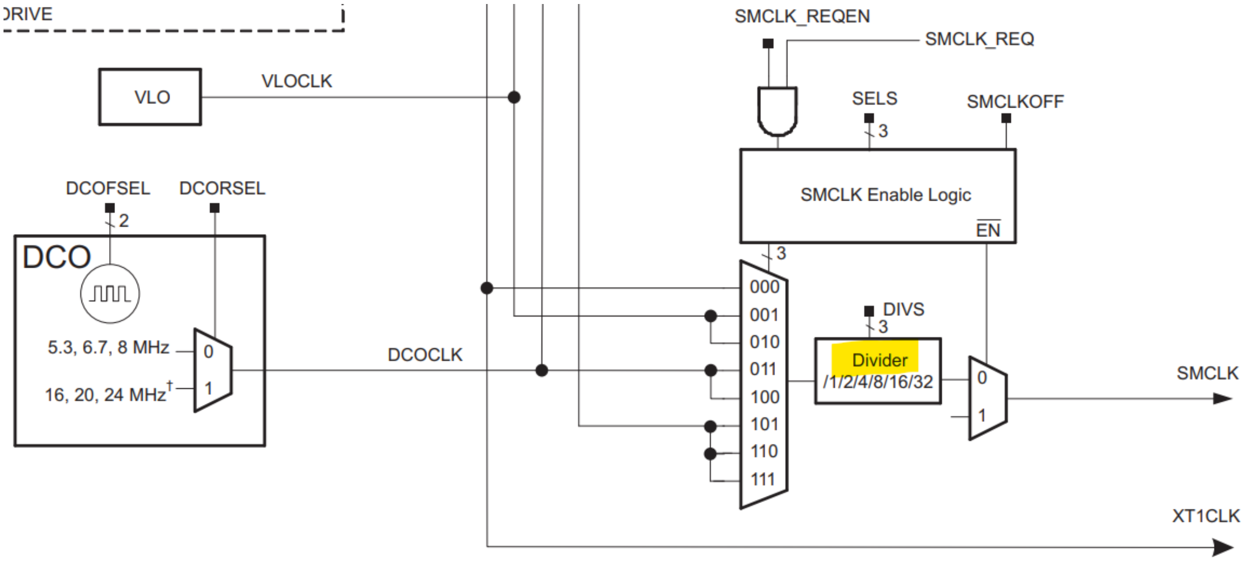
Figure 3-6. CSCTL1 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCORSEL	Reserved				DCOFSEL		Reserved
rw-[0]	r0	r0	r0	r0	rw-[1]	rw-[1]	r1

Table 3-4. CSCTL1 Register Description

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	Reserved. Always reads as 0.
7	DCORSEL	RW	0h	DCO range select. For high-speed devices, this bit can be written by the user. For low-speed devices, it is always reset. See DCOFSEL for valid values.
6-3	Reserved	R	0h	Reserved. Always reads as 0.
2-1	DCOFSEL	RW	3h	DCO frequency select. For some devices, DCORSEL = 1 setting is not available. If DCORSEL = 0: 00b = 5.33 01b = 6.67 10b = 5.33 11b = 8 If DCORSEL = 1: 00b = 16 01b = 20 10b = 16 11b = 24
0	Reserved	R	1h	Reserved. Always reads as 1.

3. Setup SMCLK with a divider of 32



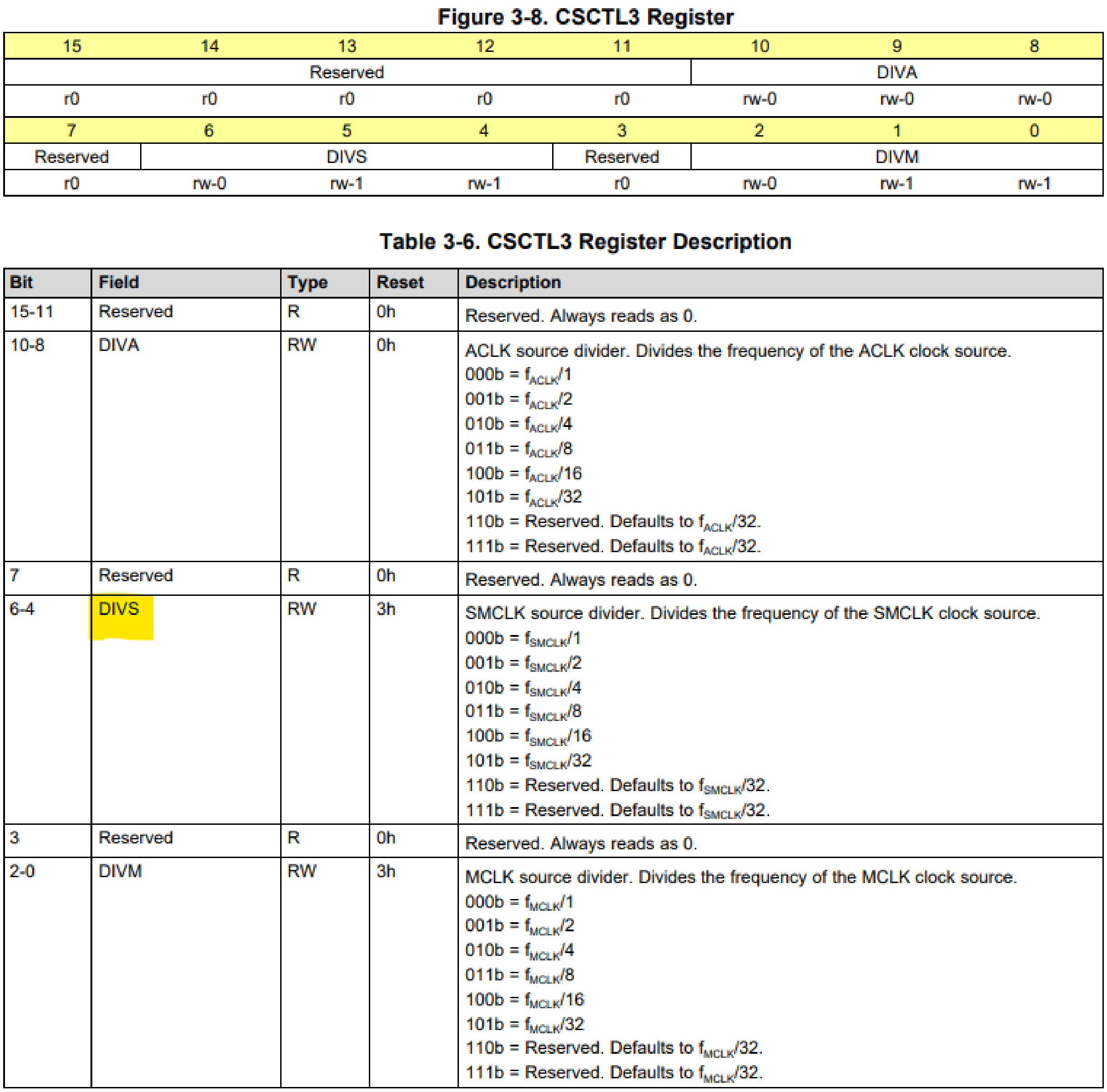


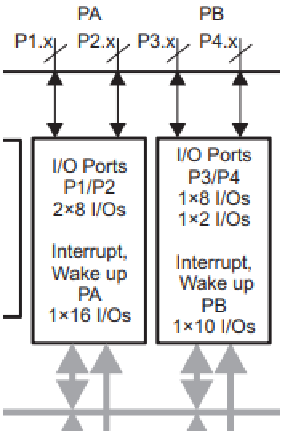
Figure 3-8. CSCTL3 Register

15	14	13	12	11	10	9	8
Reserved					DIVA		
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	DIVS			Reserved	DIVM		
r0	rw-0	rw-1	rw-1	r0	rw-0	rw-1	rw-1

Table 3-6. CSCTL3 Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10-8	DIVA	RW	0h	ACLK source divider. Divides the frequency of the ACLK clock source. 000b = f_{ACLK}/1 001b = f_{ACLK}/2 010b = f_{ACLK}/4 011b = f_{ACLK}/8 100b = f_{ACLK}/16 101b = f_{ACLK}/32 110b = Reserved. Defaults to f_{ACLK}/32. 111b = Reserved. Defaults to f_{ACLK}/32.
7	Reserved	R	0h	Reserved. Always reads as 0.
6-4	DIVS	RW	3h	SMCLK source divider. Divides the frequency of the SMCLK clock source. 000b = f_{SMCLK}/1 001b = f_{SMCLK}/2 010b = f_{SMCLK}/4 011b = f_{SMCLK}/8 100b = f_{SMCLK}/16 101b = f_{SMCLK}/32 110b = Reserved. Defaults to f_{SMCLK}/32. 111b = Reserved. Defaults to f_{SMCLK}/32.
3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	DIVM	RW	3h	MCLK source divider. Divides the frequency of the MCLK clock source. 000b = f_{MCLK}/1 001b = f_{MCLK}/2 010b = f_{MCLK}/4 011b = f_{MCLK}/8 100b = f_{MCLK}/16 101b = f_{MCLK}/32 110b = Reserved. Defaults to f_{MCLK}/32. 111b = Reserved. Defaults to f_{MCLK}/32.

4. Configure P3.4 as output, set it to output SMCLK



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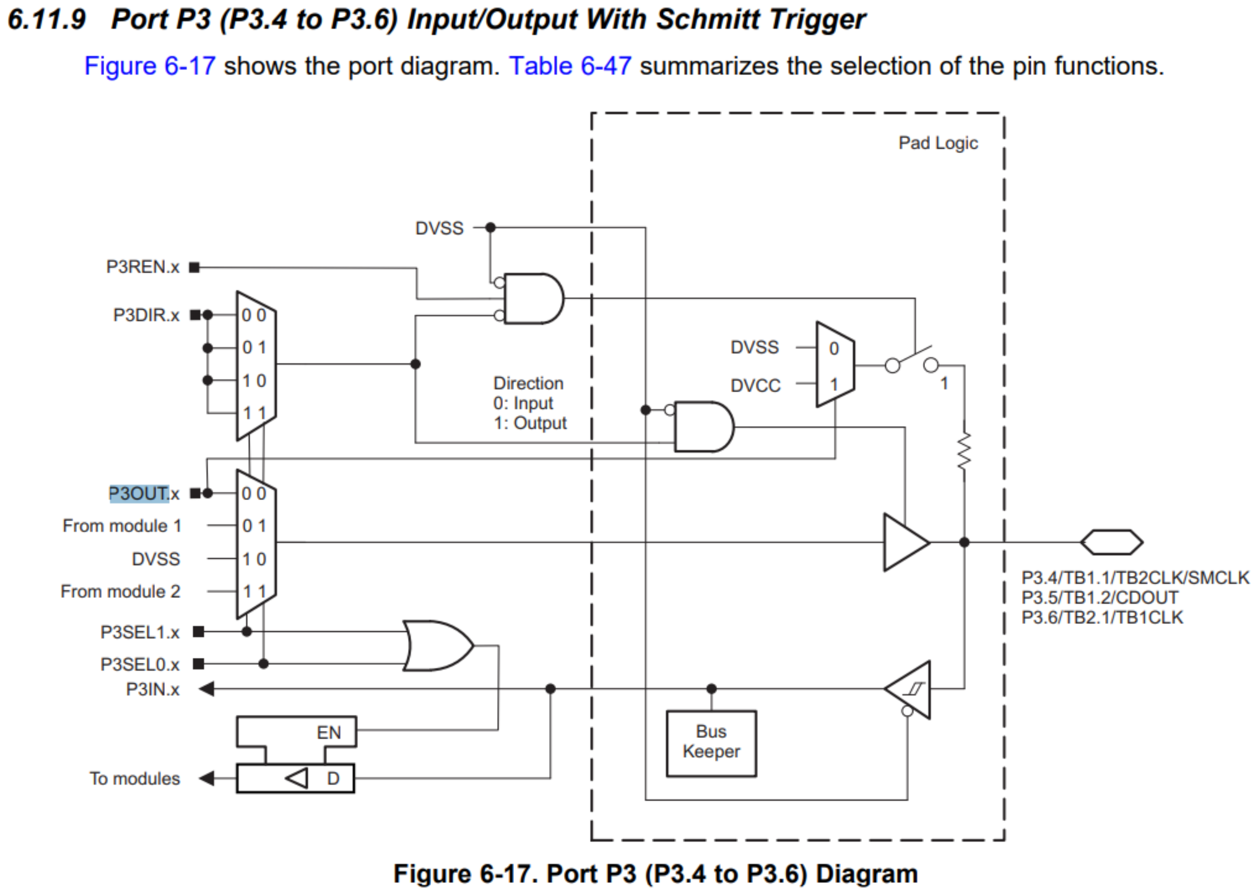

6.11.9 Port P3 (P3.4 to P3.6) Input/Output With Schmitt Trigger

Figure 6-17 shows the port diagram. Table 6-47 summarizes the selection of the pin functions.

Figure 6-17. Port P3 (P3.4 to P3.6) Diagram

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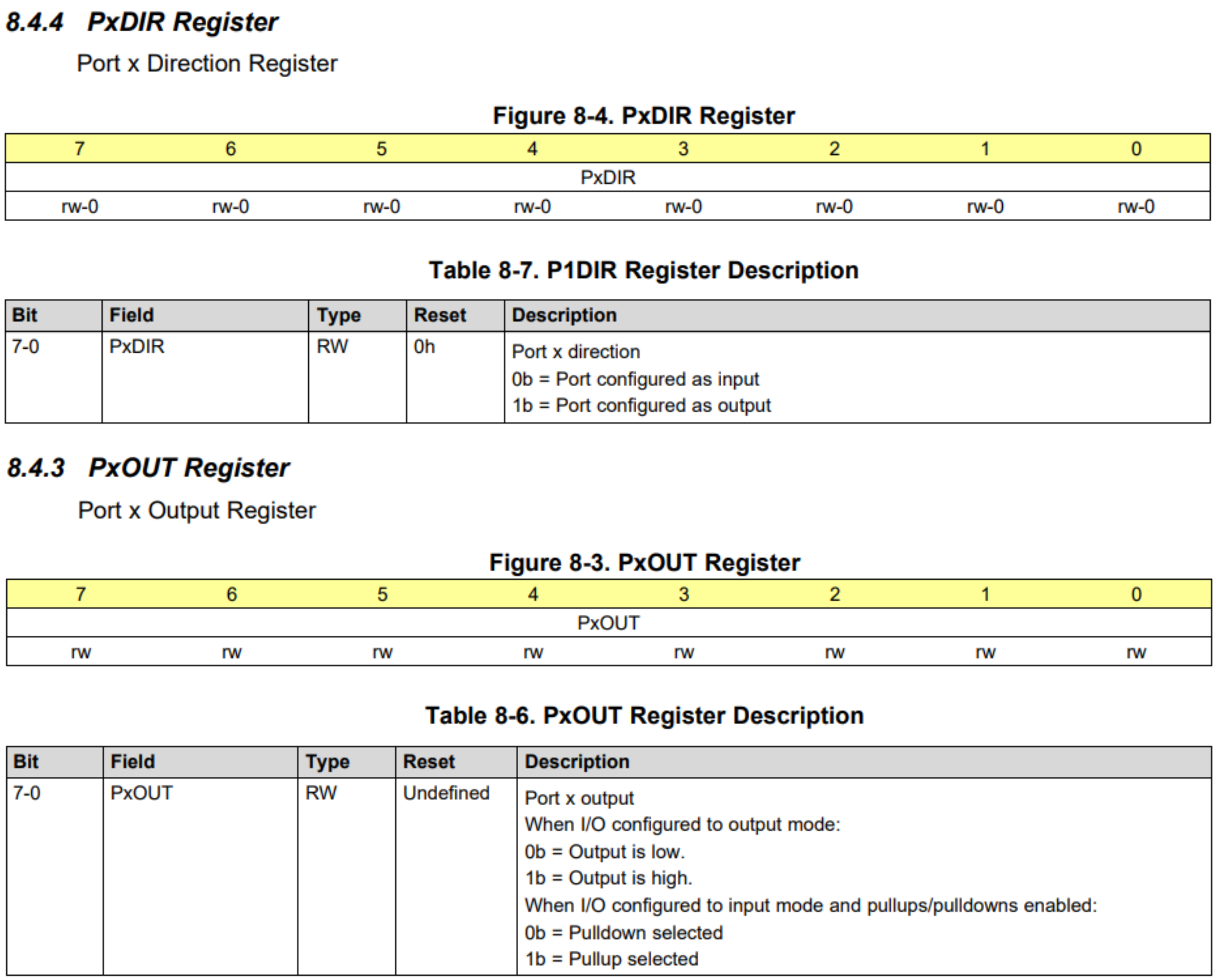


8.4.4 *PxDIR Register*

Port x Direction Register

Figure 8-4. PxDIR Register

7	6	5	4	3	2	1	0
PxDIR							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 8-7. P1DIR Register Description

Bit	Field	Type	Reset	Description
7-0	PxDIR	RW	0h	Port x direction 0b = Port configured as input 1b = Port configured as output

8.4.3 *PxOUT Register*

Port x Output Register

Figure 8-3. PxOUT Register

7	6	5	4	3	2	1	0
PxOUT							
rw	rw	rw	rw	rw	rw	rw	rw

Table 8-6. PxOUT Register Description

Bit	Field	Type	Reset	Description
7-0	PxOUT	RW	Undefined	Port x output When I/O configured to output mode: 0b = Output is low. 1b = Output is high. When I/O configured to input mode and pullups/pulldowns enabled: 0b = Pulldown selected 1b = Pullup selected

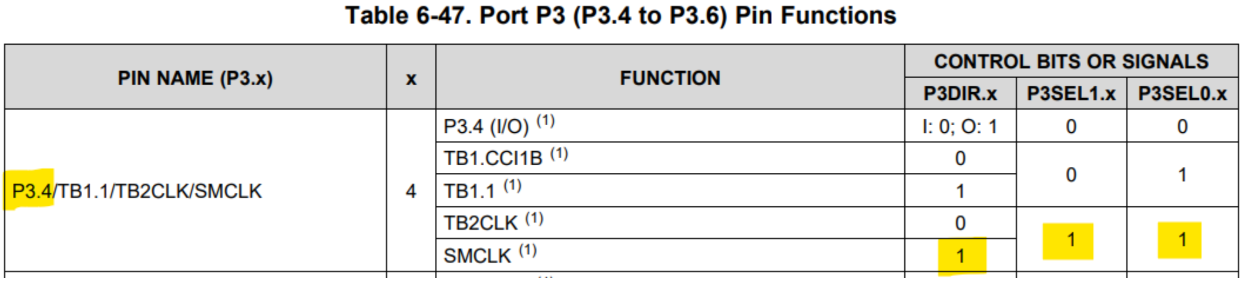
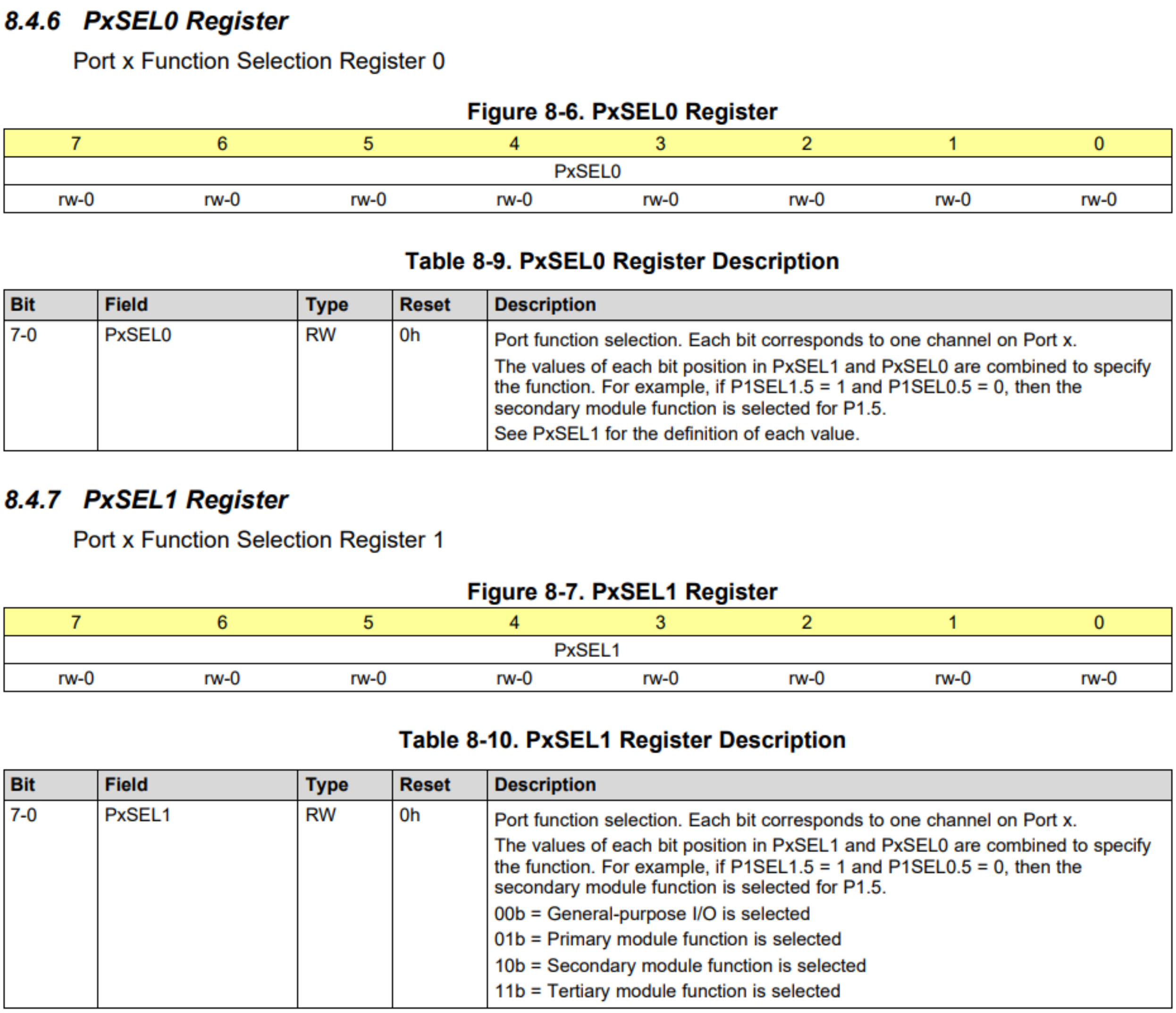


Table 6-47. Port P3 (P3.4 to P3.6) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.4/TB1.1/TB2CLK/SMCLK	4	P3.4 (I/O) [1]	I: 0; O: 1	0	0
		TB1.CCI1B [1]	0	0	1
		TB1.1 [1]	1		
		TB2CLK [1]	0	1	1
		SMCLK [1]	1		



8.4.6 PxSEL0 Register

Port x Function Selection Register 0

Figure 8-6. PxSEL0 Register

7	6	5	4	3	2	1	0
PxSEL0							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 8-9. PxSEL0 Register Description

Bit	Field	Type	Reset	Description
7-0	PxSEL0	RW	0h	Port function selection. Each bit corresponds to one channel on Port x. The values of each bit position in PxSEL1 and PxSEL0 are combined to specify the function. For example, if P1SEL1.5 = 1 and P1SEL0.5 = 0, then the secondary module function is selected for P1.5. See PxSEL1 for the definition of each value.

8.4.7 PxSEL1 Register

Port x Function Selection Register 1

Figure 8-7. PxSEL1 Register

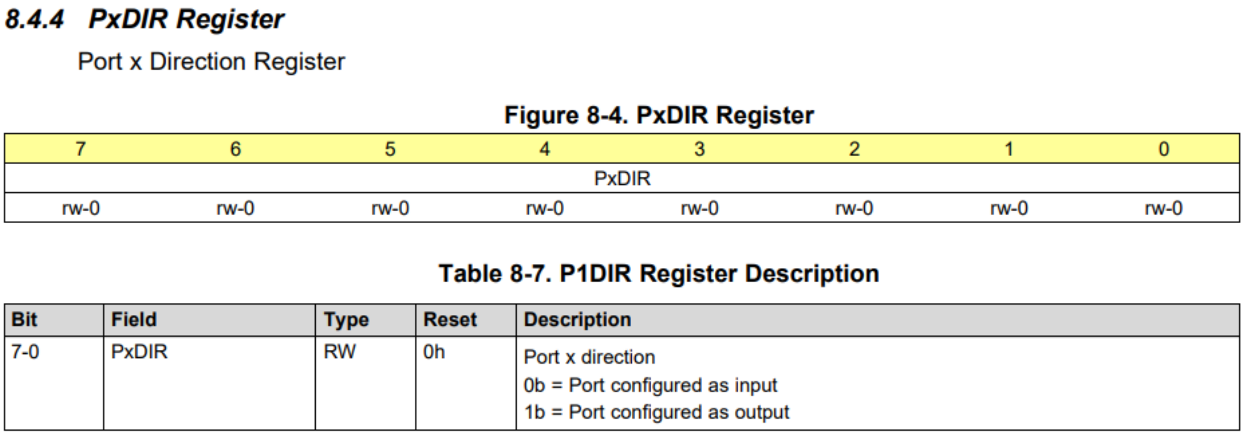
7	6	5	4	3	2	1	0
PxSEL1							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 8-10. PxSEL1 Register Description

Bit	Field	Type	Reset	Description
7-0	PxSEL1	RW	0h	Port function selection. Each bit corresponds to one channel on Port x. The values of each bit position in PxSEL1 and PxSEL0 are combined to specify the function. For example, if P1SEL1.5 = 1 and P1SEL0.5 = 0, then the secondary module function is selected for P1.5. 00b = General-purpose I/O is selected 01b = Primary module function is selected 10b = Secondary module function is selected 11b = Tertiary module function is selected

Ex2 – Digital I/O

1. Configure PJ.0, PJ.1, PJ.2, PJ.3, P3.4, P3.5, P3.6, P3.7 as digital outputs



8.4.4 PxDIR Register

Port x Direction Register

Figure 8-4. PxDIR Register

7	6	5	4	3	2	1	0
PxDIR							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 8-7. P1DIR Register Description

Bit	Field	Type	Reset	Description
7-0	PxDIR	RW	0h	Port x direction 0b = Port configured as input 1b = Port configured as output

2. Set the LEDs 1 to 8 to output 10010011

Value	1	0	0	1	0	0	1	1
LED	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1
Reg	P3.7	P3.6	P3.5	P3.4	PJ.3	PJ.2	PJ.1	PJ.0

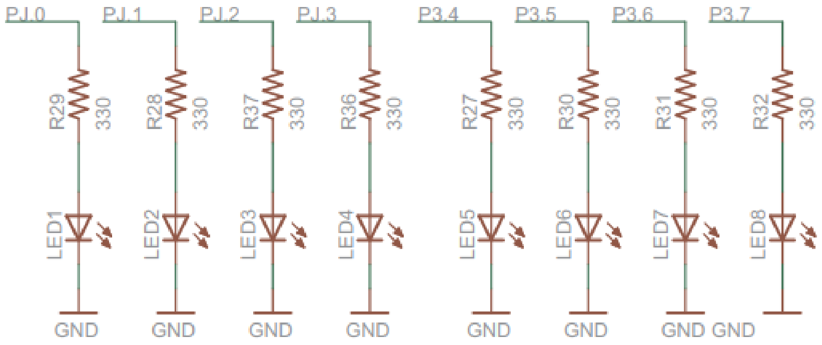
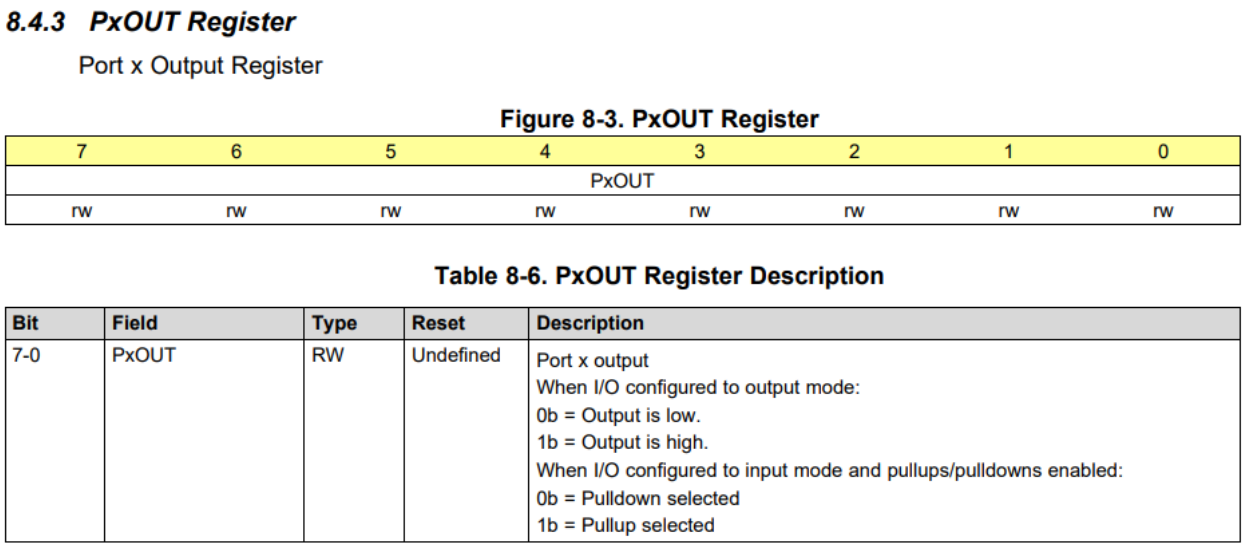


Figure 4 - board datasheet pg. 17



8.4.3 PxOUT Register

Port x Output Register

Figure 8-3. PxOUT Register

7	6	5	4	3	2	1	0
PxOUT							
rw	rw	rw	rw	rw	rw	rw	rw

Table 8-6. PxOUT Register Description

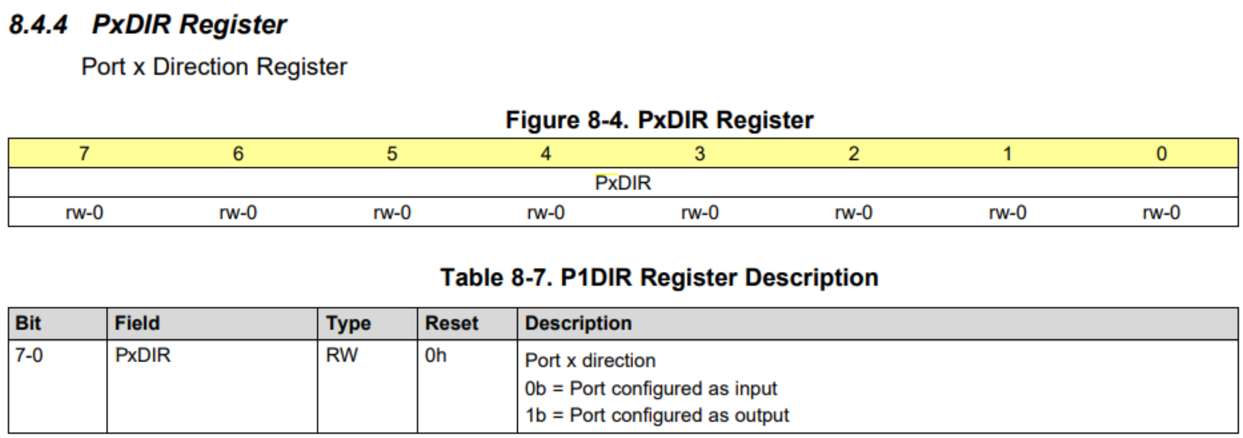
Bit	Field	Type	Reset	Description
7-0	PxOUT	RW	Undefined	Port x output When I/O configured to output mode: 0b = Output is low. 1b = Output is high. When I/O configured to input mode and pullups/pulldowns enabled: 0b = Pulldown selected 1b = Pullup selected

3. Write a program to blink the LEDs that are 0 in step 2. Use a delay loop in the main infinite loop to visibly blink the LED

```
int main(void)
{
        int i;
    WDTCTL = WDTPW | WDTHOLD;    // stop watchdog timer

        // Configure PJ.0, PJ.1, PJ.2, PJ.3, P3.4, P3.5, P3.6, and P3.7 as digital
outputs
        PJDIR |= BIT3 + BIT2 + BIT1 + BIT0;
        P3DIR |= BIT7 + BIT6 + BIT5 + BIT4;

        // Set the LEDs 1 to 8 to output 10010011
        PJOUT |= BIT1 + BIT0;
        PJOUT &= ~(BIT3 + BIT2);
        P3OUT |= BIT7 + BIT4;
        P3OUT &= ~(BIT6 + BIT5);

        while (1) {
            PJOUT ^= (BIT3 + BIT2);
            P3OUT ^= (BIT6 + BIT5);
            for (i = 0; i < 20000; i++) {
                _NOP();
            }
        }


        return 0;
}
```

Ex3 – Interrupts

1. Configure P4.0 as digital input (SW1)



8.4.4 PxDIR Register

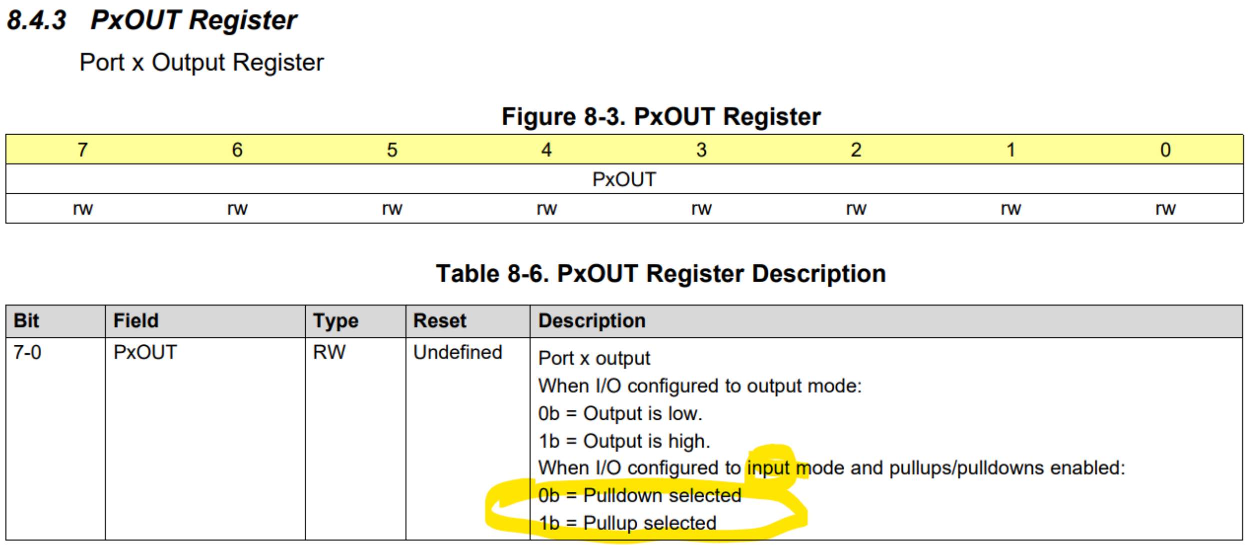
Port x Direction Register

Figure 8-4. PxDIR Register

7	6	5	4	3	2	1	0
PxDIR							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 8-7. P1DIR Register Description

Bit	Field	Type	Reset	Description
7-0	PxDIR	RW	0h	Port x direction 0b = Port configured as input 1b = Port configured as output



8.4.3 PxOUT Register

Port x Output Register

Figure 8-3. PxOUT Register

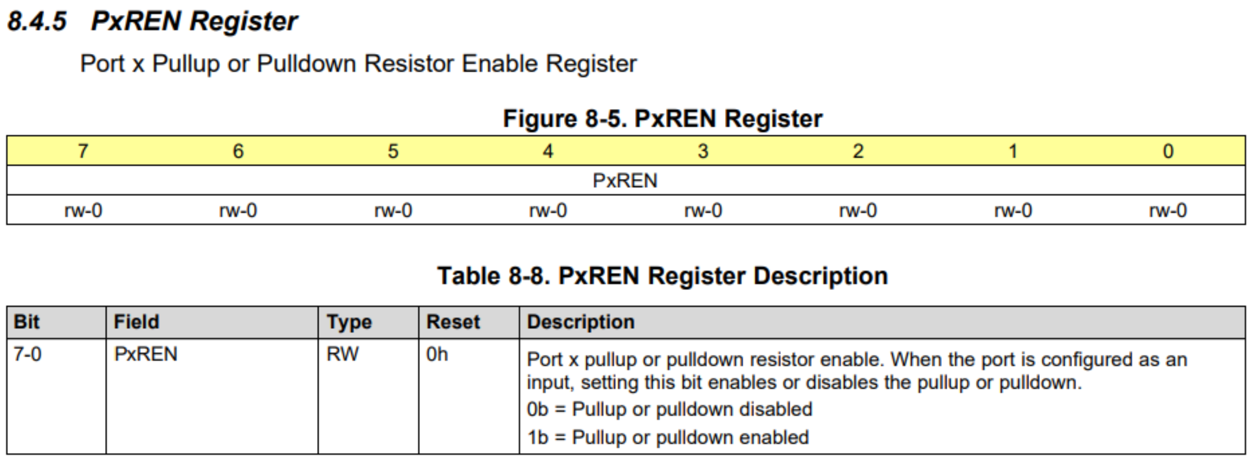
7	6	5	4	3	2	1	0
PxOUT							
rw	rw	rw	rw	rw	rw	rw	rw

Table 8-6. PxOUT Register Description

Bit	Field	Type	Reset	Description
7-0	PxOUT	RW	Undefined	Port x output When I/O configured to output mode: 0b = Output is low. 1b = Output is high. When I/O configured to input mode and pullups/pulldowns enabled: 0b = Pulldown selected 1b = Pullup selected

Set P4OUT.0 to select pullup

2. Enable internal pull up resistors for the switch S1 connected to P4.0 on the EXP board



8.4.5 *PxREN Register*

Port x Pullup or Pulldown Resistor Enable Register

Figure 8-5. PxREN Register

7	6	5	4	3	2	1	0
PxREN							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

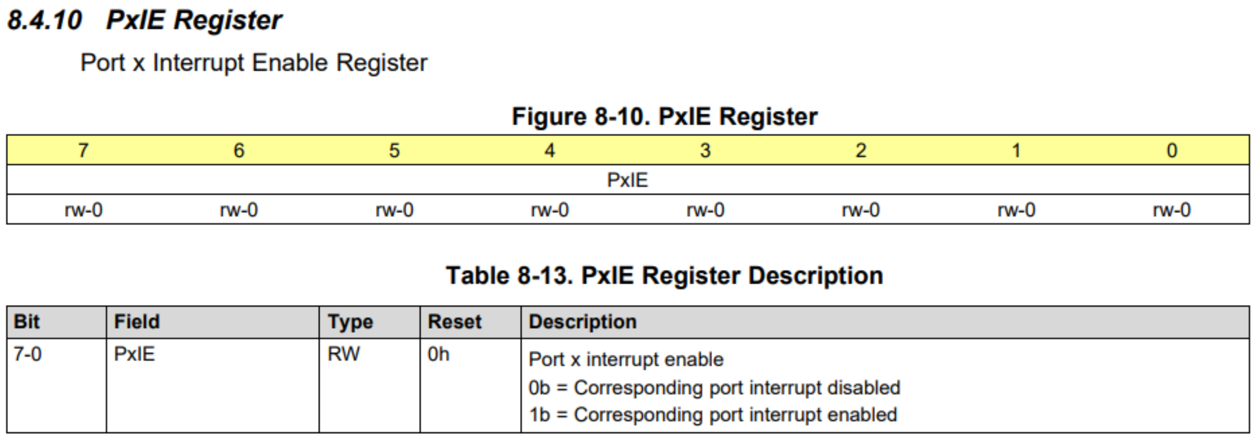
Table 8-8. PxREN Register Description

Bit	Field	Type	Reset	Description
7-0	PxREN	RW	0h	Port x pullup or pulldown resistor enable. When the port is configured as an input, setting this bit enables or disables the pullup or pulldown. 0b = Pullup or pulldown disabled 1b = Pullup or pulldown enabled

PULLUP: open = 1, close = 0

3. Set P4.0 to get interrupted from a rising edge

Interrupted at the release of S1 switch (button)



8.4.10 *PxIE Register*

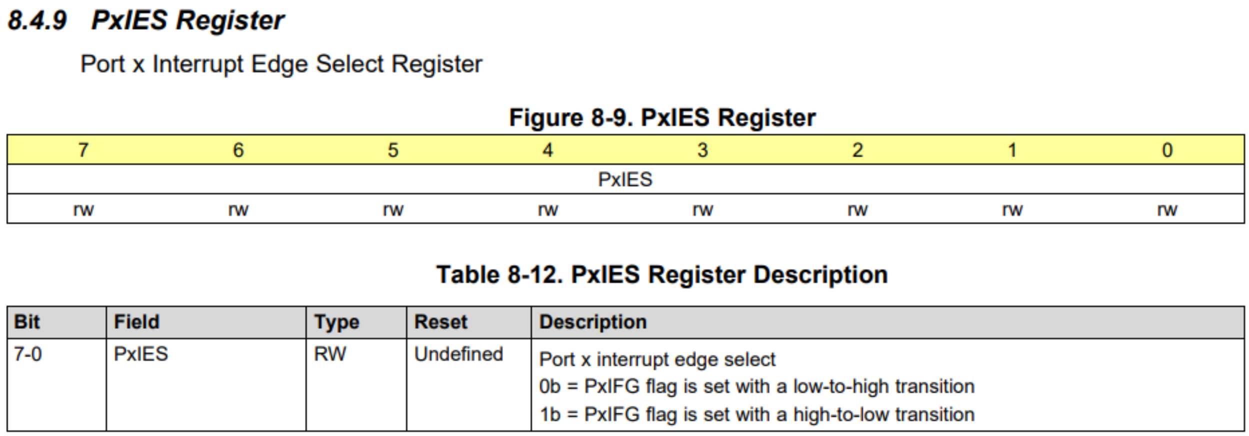
Port x Interrupt Enable Register

Figure 8-10. PxIE Register

7	6	5	4	3	2	1	0
PxIE							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 8-13. PxIE Register Description

Bit	Field	Type	Reset	Description
7-0	PxIE	RW	0h	Port x interrupt enable 0b = Corresponding port interrupt disabled 1b = Corresponding port interrupt enabled



8.4.9 *PxIES Register*

Port x Interrupt Edge Select Register

Figure 8-9. PxIES Register

7	6	5	4	3	2	1	0
PxIES							
rw	rw	rw	rw	rw	rw	rw	rw

Table 8-12. PxIES Register Description

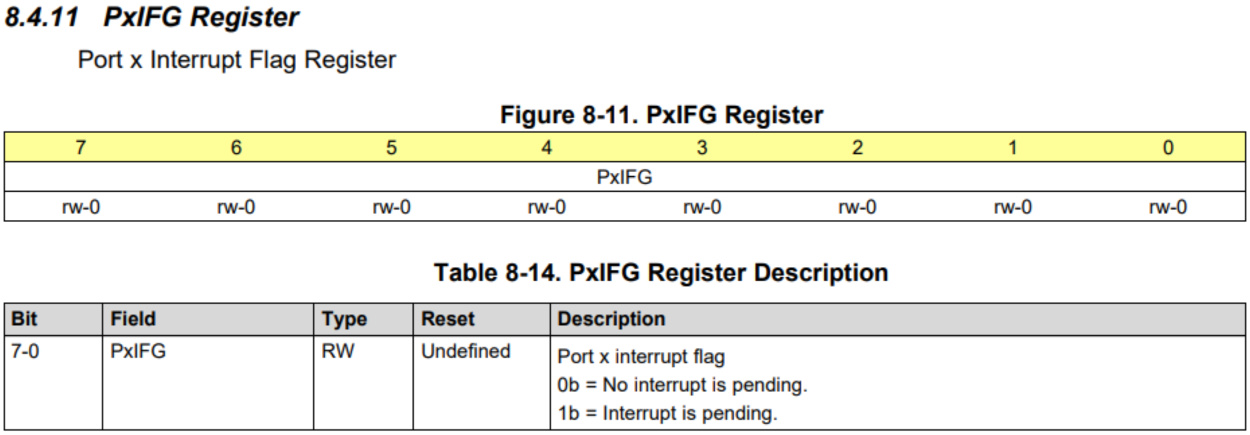
Bit	Field	Type	Reset	Description
7-0	PxIES	RW	Undefined	Port x interrupt edge select 0b = PxIFG flag is set with a low-to-high transition 1b = PxIFG flag is set with a high-to-low transition

```
// enable global interrupt
_EINT();
```

4. Configure P3.7 as output (LED8)

```
// configure P3.7 as output (connected to LED8)
P3DIR |= BIT7;
```

5. Write an ISR to toggle LED8 when S1 provides a rising edge



8.4.11 PxIFG Register

Port x Interrupt Flag Register

Figure 8-11. PxIFG Register

7	6	5	4	3	2	1	0
PxIFG							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 8-14. PxIFG Register Description

Bit	Field	Type	Reset	Description
7-0	PxIFG	RW	Undefined	Port x interrupt flag 0b = No interrupt is pending. 1b = Interrupt is pending.

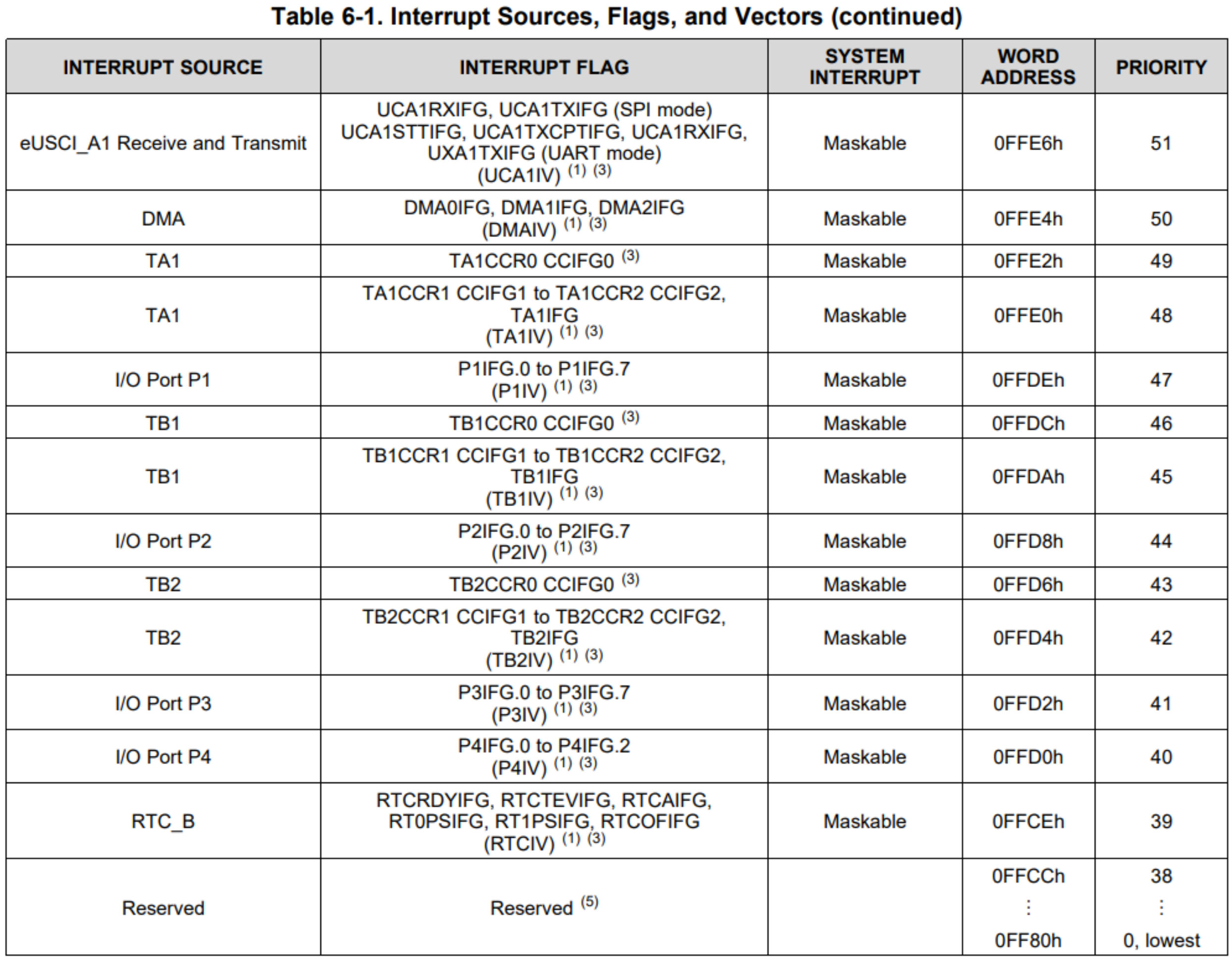


Table 6-1. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
eUSCI_A1 Receive and Transmit	UCA1RXIFG, UCA1TXIFG (SPI mode) UCA1STTIFG, UCA1TXCPTIFG, UCA1RXIFG, UXA1TXIFG (UART mode) (UCA1IV) (1) (3)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) (1) (3)	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0 (3)	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) (1) (3)	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV) (1) (3)	Maskable	0FFDEh	47
TB1	TB1CCR0 CCIFG0 (3)	Maskable	0FFDCh	46
TB1	TB1CCR1 CCIFG1 to TB1CCR2 CCIFG2, TB1IFG (TB1IV) (1) (3)	Maskable	0FFDAh	45
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV) (1) (3)	Maskable	0FFD8h	44
TB2	TB2CCR0 CCIFG0 (3)	Maskable	0FFD6h	43
TB2	TB2CCR1 CCIFG1 to TB2CCR2 CCIFG2, TB2IFG (TB2IV) (1) (3)	Maskable	0FFD4h	42
I/O Port P3	P3IFG.0 to P3IFG.7 (P3IV) (1) (3)	Maskable	0FFD2h	41
I/O Port P4	P4IFG.0 to P4IFG.2 (P4IV) (1) (3)	Maskable	0FFD0h	40
RTC_B	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) (1) (3)	Maskable	0FFCEh	39
Reserved	Reserved (5)		0FFCCh ⋮ 0FF80h	38 ⋮ 0, lowest

Figure 5 - user guide pg. 45

Ex4 – UART

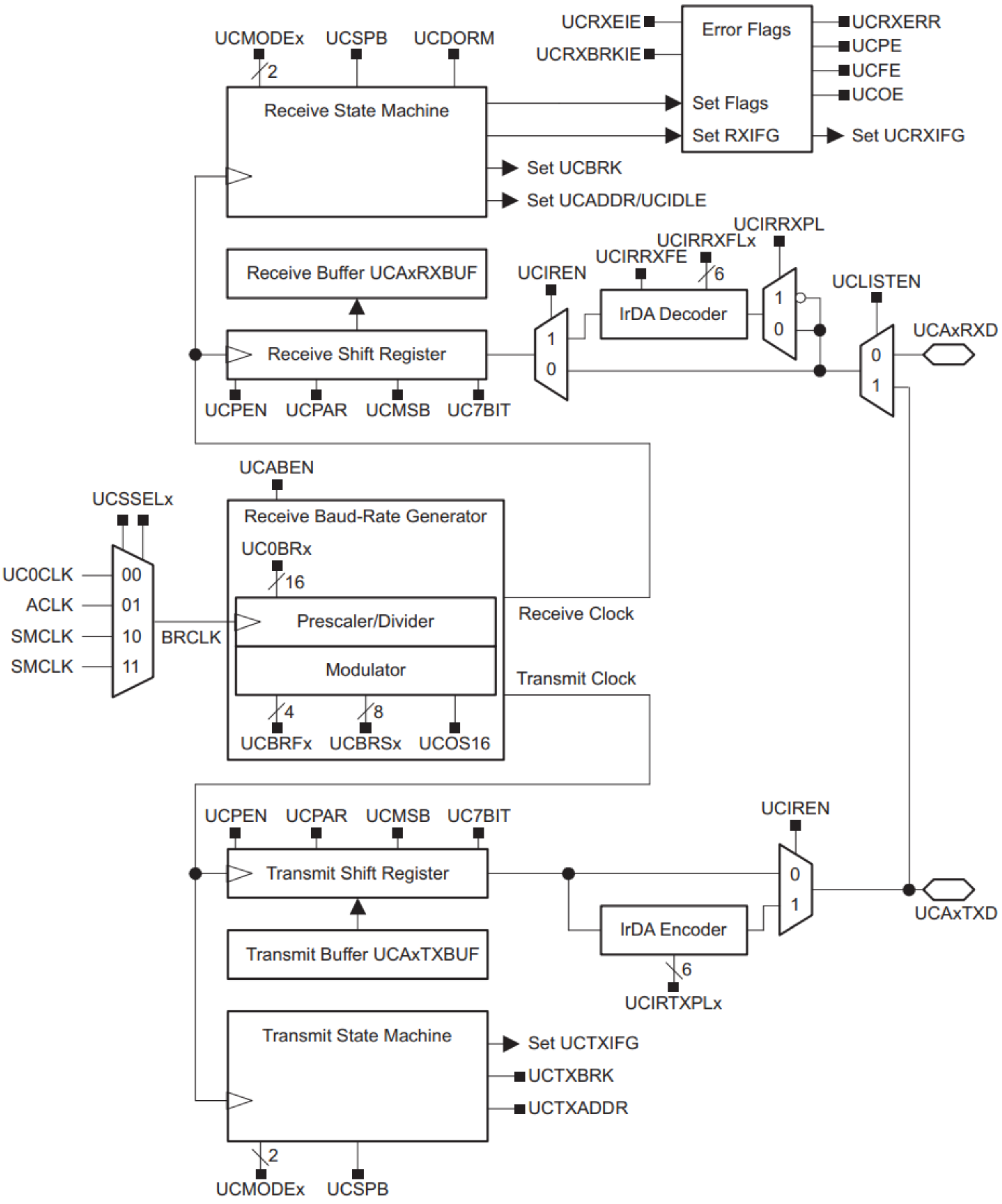


Figure 18-1. eUSCI_Ax Block Diagram – UART Mode (UCSYNC = 0)

1. Configure the UART to operate at 9600, 8, N, 1

Baud rate = 9600 bits/s

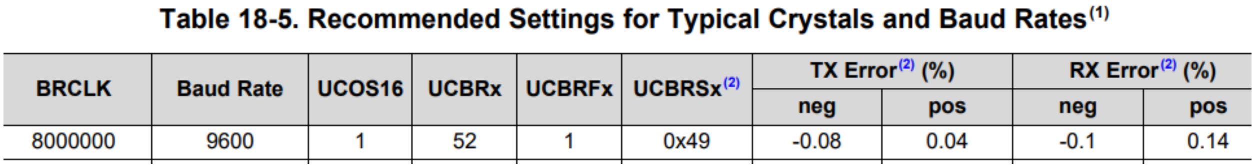


Table 18-5. Recommended Settings for Typical Crystals and Baud Rates[1]

BRCLK	Baud Rate	UCOS16	UCBRx	UCBRFx	UCBRSx[2]	TX Error[2] (%)		RX Error[2] (%)	
						neg	pos	neg	pos
8000000	9600	1	52	1	0x49	-0.08	0.04	-0.1	0.14

Data size = 8 bits

Parity = None

# stop bits = 1

2. Set up P2.0 and P2.1 for UART communications

```
// Configure ports for UART
 P2SEL0 &= ~(BIT0 + BIT1);
 P2SEL1 |= BIT0 + BIT1;
```

3. Write a program to periodically transmit the letter ‘a’ to the serial port

```
while (1)
 {
     // Periodically transmit an "a" character
     while (!(UCA0IFG & UCTXIFG));
     UCA0TXBUF = 'a';
     for (i=0;i<20000;i++)
         _NOP();
 }
```

4. Check the transmission using the CCS terminal in debug (or PuTTY)

CCS terminal -> COM3

Serial terminal, COM3, 9600, 8, None, 1, UTF-8

5. Enable UART receive interrupt. Enable global interrupt

```
 UCA0CTLW0 |= UCSWRST;                // Put the UART in software reset
 UCA0CTLW0 |= UCSSEL0;                // Run the UART using ACLK
 UCA0MCTLW = UCOS16 + UCBRF0 + 0x4900; // Baud rate=9600 from 8 MHz clk
 UCA0BRW = 52;
 UCA0CTLW0 &= ~UCSWRST;               // release UART for operation
```

```
    UCA0IE |= UCRXIE;                       // Enable UART Rx interrupt


    // Global interrupt enable
    _EINT();
```

6. Set up an interrupt service routine so that when a single byte is received, the same byte is transmitted by back (or echoed) to the serial port. Check using CCS terminal/PuTTY.

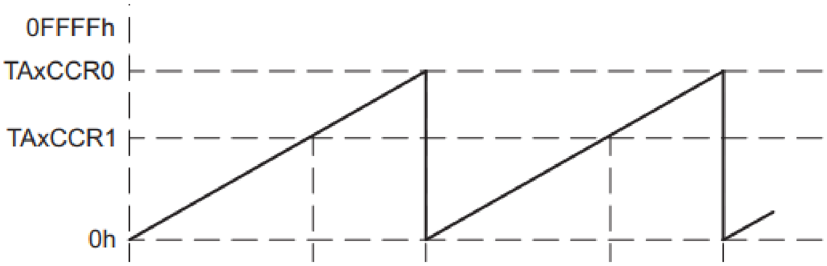
```
#pragma vector = USCI_A0_VECTOR
__interrupt void USCI_A0_ISR(void)
{
    unsigned char RxByte = 0;
    RxByte = UCA0RXBUF;                     // Get the new byte from the Rx 
buffer
    while (!(UCA0IFG & UCTXIFG));           // Wait until the previous Tx is 
finished
    UCA0TXBUF = RxByte;                     // Echo back the received byte
    while (!(UCA0IFG & UCTXIFG));           // Wait until the previous Tx is 
finished
    UCA0TXBUF = RxByte + 1;                 // Echo back the received byte + 
1


    if (RxByte == 'j') PJOUT |= BIT0;       // Turn on LED1 when a 'j' is 
received
    else if (RxByte == 'k') PJOUT &= ~BIT0; // Turn off LED1 when a 'k' is 
received
}
```

7. In addition to echoing, also transmit the next byte in the ASCII table. Check again using PuTTY
8. Add code to turn on LED1 when a ‘j’ is received and turn off LED1 when ‘k’ is received

Ex5 – Timer I

1. Set up Timer B in the “up count” mode.
2. Configure TB1.1 to produce a 500 Hz square wave. You may need to use frequency dividers when setting up the clock and the timer. Output on P3.4. Verify using an oscilloscope. LED5 should also be lit.

Default clock, `TB1CCR0 = 2000` -> 250 MHz (Mode 0)



Want 500 MHz -> TB1CCTL1 |= OUTMOD_7; TB1CCTL2 |= OUTMOD_7;

TB1CCR1 = 1000; // 50% duty cycle

TB1CCR2 = 500; // 25% duty cycle

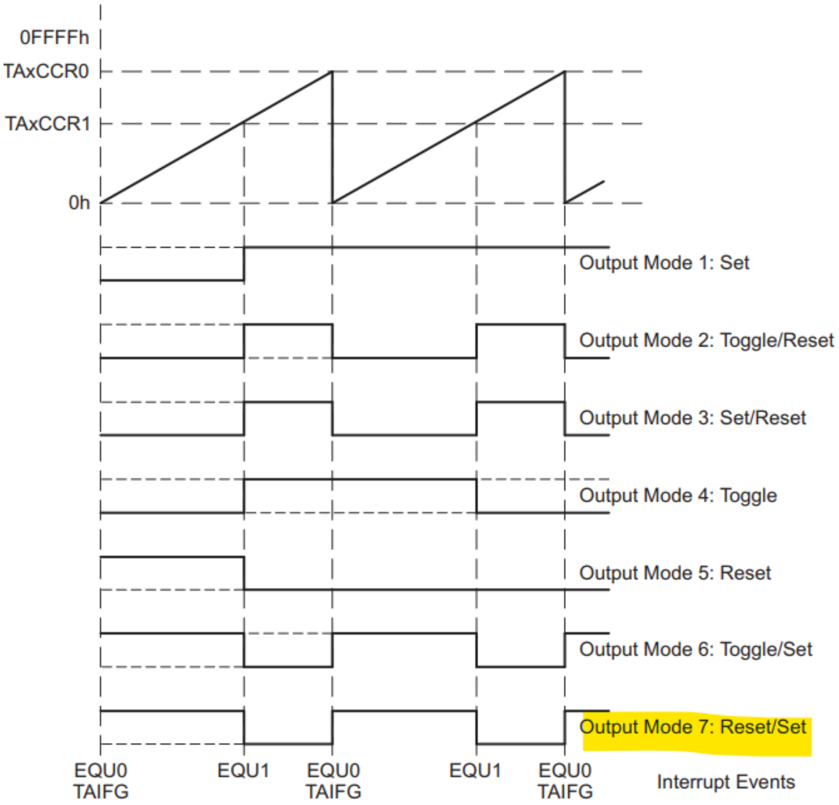


Figure 11-12. Output Example – Timer in Up Mode

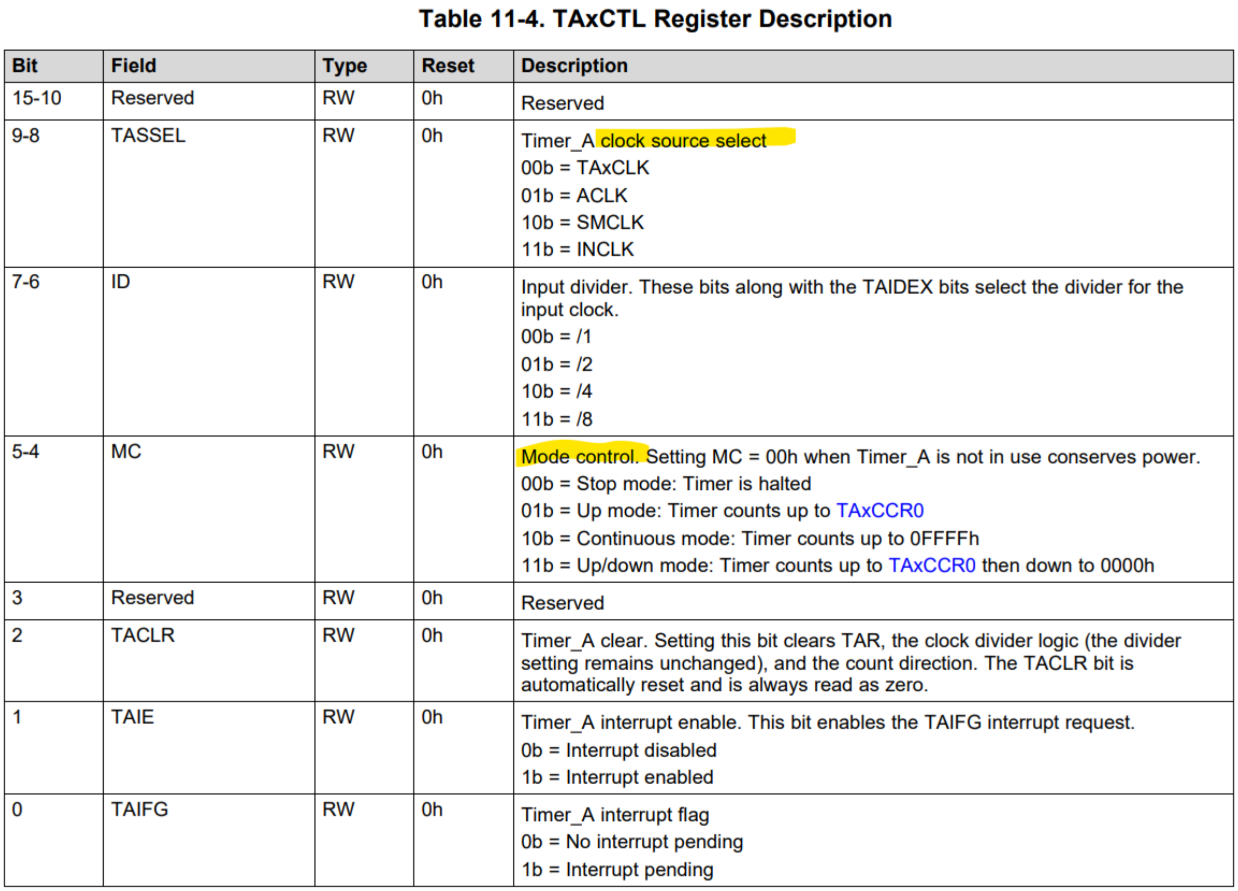


Table 11-4. TAxCTL Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	RW	0h	Reserved
9-8	TASSEL	RW	0h	Timer_A clock source select 00b = TAxCLK 01b = ACLK 10b = SMCLK 11b = INCLK
7-6	ID	RW	0h	Input divider. These bits along with the TAIDEX bits select the divider for the input clock. 00b = /1 01b = /2 10b = /4 11b = /8
5-4	MC	RW	0h	Mode control. Setting MC = 00h when Timer_A is not in use conserves power. 00b = Stop mode: Timer is halted 01b = Up mode: Timer counts up to TAxCCR0 10b = Continuous mode: Timer counts up to 0FFFFh 11b = Up/down mode: Timer counts up to TAxCCR0 then down to 0000h
3	Reserved	RW	0h	Reserved
2	TACLR	RW	0h	Timer_A clear. Setting this bit clears TAR, the clock divider logic (the divider setting remains unchanged), and the count direction. The TACLR bit is automatically reset and is always read as zero.
1	TAIE	RW	0h	Timer_A interrupt enable. This bit enables the TAIFG interrupt request. 0b = Interrupt disabled 1b = Interrupt enabled
0	TAIFG	RW	0h	Timer_A interrupt flag 0b = No interrupt pending 1b = Interrupt pending

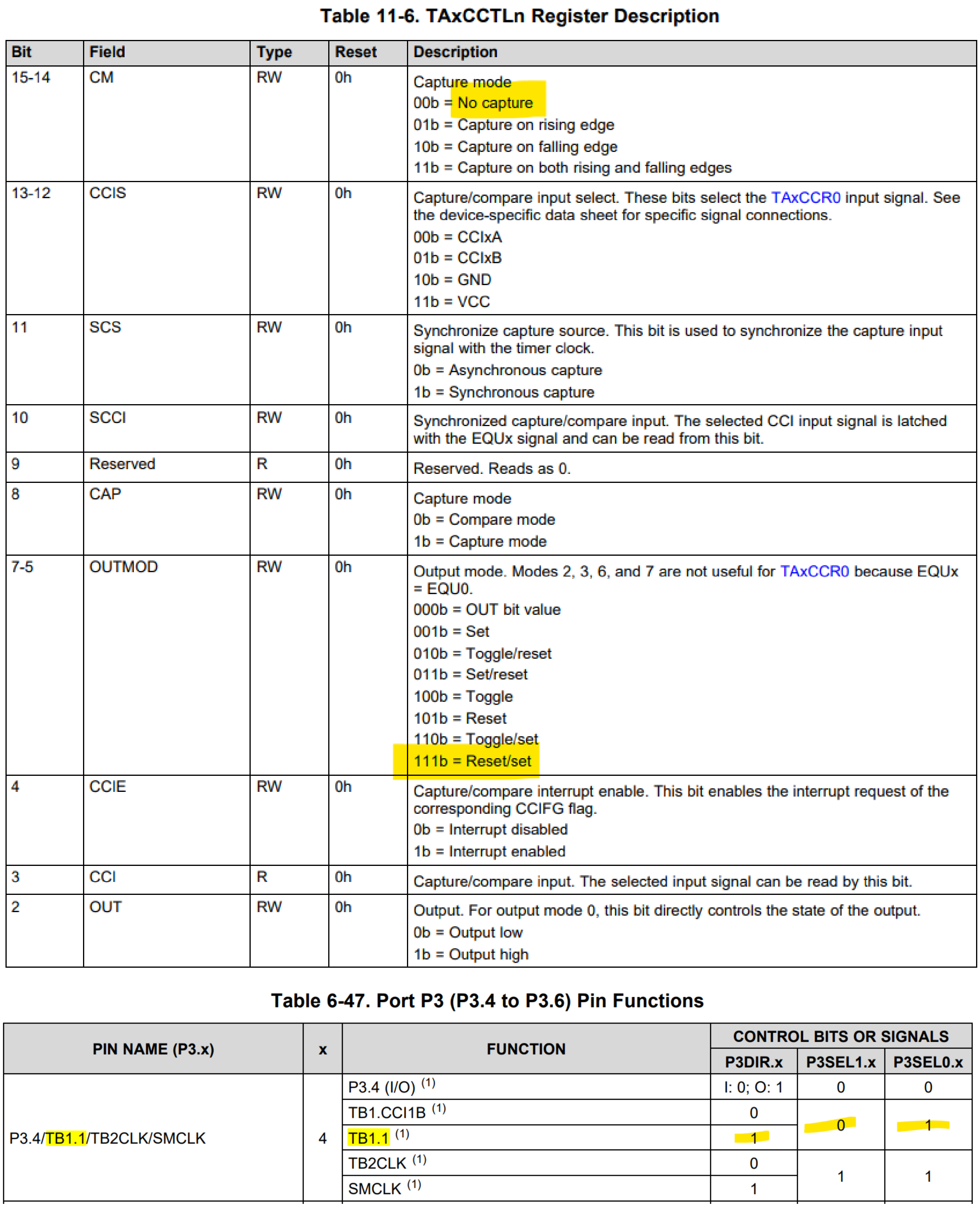


Table 11-6. TAxCCTLn Register Description

Bit	Field	Type	Reset	Description
15-14	CM	RW	0h	Capture mode 00b = No capture 01b = Capture on rising edge 10b = Capture on falling edge 11b = Capture on both rising and falling edges
13-12	CCIS	RW	0h	Capture/compare input select. These bits select the TAxCCR0 input signal. See the device-specific data sheet for specific signal connections. 00b = CCIxA 01b = CCIxB 10b = GND 11b = VCC
11	SCS	RW	0h	Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock. 0b = Asynchronous capture 1b = Synchronous capture
10	SCCI	RW	0h	Synchronized capture/compare input. The selected CCI input signal is latched with the EQUx signal and can be read from this bit.
9	Reserved	R	0h	Reserved. Reads as 0.
8	CAP	RW	0h	Capture mode 0b = Compare mode 1b = Capture mode
7-5	OUTMOD	RW	0h	Output mode. Modes 2, 3, 6, and 7 are not useful for TAxCCR0 because EQUx = EQU0. 000b = OUT bit value 001b = Set 010b = Toggle/reset 011b = Set/reset 100b = Toggle 101b = Reset 110b = Toggle/set 111b = Reset/set
4	CCIE	RW	0h	Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag. 0b = Interrupt disabled 1b = Interrupt enabled
3	CCI	R	0h	Capture/compare input. The selected input signal can be read by this bit.
2	OUT	RW	0h	Output. For output mode 0, this bit directly controls the state of the output. 0b = Output low 1b = Output high

Table 6-47. Port P3 (P3.4 to P3.6) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.4/TB1.1/TB2CLK/SMCLK	4	P3.4 (I/O) (1)	I: 0; O: 1	0	0
		TB1.CCI1B (1)	0	0	1
		TB1.1 (1)	1		
		TB2CLK (1)	0	1	1
		SMCLK (1)	1		

Figure 6 - device datasheet pg 73

3. Configure TB1.2 to produce a 500 Hz square wave at 25% duty cycle. Output on P3.5. Verify using an oscilloscope. LED6 should be lit. Verify that LED6 is dimmer than LED5.

Ex6 – Timer II

1. Set up timer A to measure the length of time of a pulse from a rising edge to a falling edge.
2. Connect the timer output from the previous exercise to the input of this timer.
3. Using the debugger to check the measured 16-bit value