3.4 CS Registers

The CS module registers are listed in Table 3-2. The base address can be found in the device-specific data sheet. The address offset is listed in Table 3-2. The password defined in CSCTL0 controls access to the CS registers. After the correct password is written, write access to the CS registers is enabled. Write access is disabled by writing an incorrect password in byte mode to the CSCTL0 upper byte.

NOTE: All registers have word or byte register access. For a generic register *ANYREG*, the suffix "_L" (*ANYREG_L*) refers to the lower byte of the register (bits 0 through 7). The suffix "_H" (*ANYREG_H*) refers to the upper byte of the register (bits 8 through 15).

Table 3-2. CS Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	CSCTL0	Clock System Control 0	Read/write	Word	9600h	Section 3.4.1
00h	CSCTL0_L		Read/write	Byte	00h	
01h	CSCTL0_H		Read/write	Byte	96h	
02h	CSCTL1	Clock System Control 1	Read/write	Word	0007h	Section 3.4.2
02h	CSCTL1_L		Read/write	Byte	07h	
03h	CSCTL1_H		Read/write	Byte	00h	
04h	CSCTL2	Clock System Control 2	Read/write	Word	0033h	Section 3.4.3
04h	CSCTL2_L		Read/write	Byte	33h	
05h	CSCTL2_H		Read/write	Byte	00h	
06h	CSCTL3	Clock System Control 3	Read/write	Word	0033h	Section 3.4.4
06h	CSCTL3_L		Read/write	Byte	33h	
07h	CSCTL3_H		Read/write	Byte	00h	
08h	CSCTL4	Clock System Control 4	Read/write	Word	C1C1h	Section 3.4.5
08h	CSCTL4_L		Read/write	Byte	C1h	
09h	CSCTL4_H		Read/write	Byte	C1h	
0Ah	CSCTL5	Clock System Control 5	Read/write	Word	0C01h	Section 3.4.6
0Ah	CSCTL5_L		Read/write	Byte	01h	
0Bh	CSCTL5_H		Read/write	Byte	0Ch	
0Ch	CSCTL6	Clock System Control 6	Read/write	Word	0007h	Section 3.4.7
0Ch	CSCTL6_L		Read/write	Byte	07h	
0Dh	CSCTL6_H		Read/write	Byte	00h	

3.4.1 CSCTL0 Register

Clock System Control 0 Register

Figure 3-5. CSCTL0 Register

15	14	13	12	11	10	9	8
CSKEY							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0
7	6	5	4	3	2	1	0
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0

Table 3-3. CSCTL0 Register Description

Bit	Field	Type	Reset	Description
15-8	CSKEY	RW	96h	CSKEY password. Always reads as 096h. Must be written as 0A5h when writing in word mode; writing any other value in word mode generates a PUC. After a correct password is written and CS register accesses are enabled, a wrong password write in byte mode disables the access, and no PUC is generated
7-0	Reserved	R	0h	Reserved. Always reads as 0.

3.4.2 CSCTL1 Register

Clock System Control 1 Register

Figure 3-6. CSCTL1 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
DCORSEL	Reserved				DCOFSEL		Reserved
rw-[0]	r0	r0	r0	r0	rw-[1]	rw-[1]	r1

Table 3-4. CSCTL1 Register Description

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	Reserved. Always reads as 0.
7	DCORSEL	RW	0h	DCO range select. For high-speed devices, this bit can be written by the user. For low-speed devices, it is always reset. See DCOFSEL for valid values.
6-3	Reserved	R	0h	Reserved. Always reads as 0.
2-1	DCOFSEL	RW	3h	DCO frequency select. For some devices, DCORSEL = 1 setting is not available. If DCORSEL = 0: 00b = 5.33 01b = 6.67 10b = 5.33 11b = 8 If DCORSEL = 1: 00b = 16 01b = 20 10b = 16 11b = 24
0	Reserved	R	1h	Reserved. Always reads as 1.

3.4.3 CSCTL2 Register

Clock System Control 2 Register

Figure 3-7. CSCTL2 Register

15	14	13	12	11	10	9	8
Reserved					SELA		
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved	SELS			Reserved	SELM		
r0	rw-0	rw-1	rw-1	r0	rw-0	rw-1	rw-1

Table 3-5. CSCTL2 Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10-8	SELA	RW	0h	Selects the ACLK source 000b = XT1CLK 001b = VLOCLK 010b = Reserved. Defaults to VLOCLK. 011b = DCOCLK 100b = Reserved. Defaults to DCOCLK. 101b = XT2CLK when available, otherwise DCOCLK 110b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK. 111b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK.
7	Reserved	R	0h	Reserved. Always reads as 0.
6-4	SELS	RW	3h	Selects the SMCLK source 000b = XT1CLK 001b = VLOCLK 010b = Reserved. Defaults to VLOCLK. 011b = DCOCLK 100b = Reserved. Defaults to DCOCLK. 101b = XT2CLK when available, otherwise DCOCLK 110b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK. 111b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK.
3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	SELM	RW	3h	Selects the MCLK source 000b = XT1CLK 001b = VLOCLK 010b = Reserved. Defaults to VLOCLK. 011b = DCOCLK 100b = Reserved. Defaults to DCOCLK. 101b = XT2CLK when available, otherwise DCOCLK 110b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK. 111b = Reserved. Defaults to XT2CLK when available, otherwise DCOCLK.

3.4.4 CSCTL3 Register

Clock System Control 3 Register

Figure 3-8. CSCTL3 Register

15	14	13	12	11	10	9	8
Reserved					DIVA		
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved	DIVS			Reserved	DIVM		
r0	rw-0	rw-1	rw-1	r0	rw-0	rw-1	rw-1

Table 3-6. CSCTL3 Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10-8	DIVA	RW	0h	ACLK source divider. Divides the frequency of the ACLK clock source. 000b = f_{ACLK}/1 001b = f_{ACLK}/2 010b = f_{ACLK}/4 011b = f_{ACLK}/8 100b = f_{ACLK}/16 101b = f_{ACLK}/32 110b = Reserved. Defaults to f_{ACLK}/32. 111b = Reserved. Defaults to f_{ACLK}/32.
7	Reserved	R	0h	Reserved. Always reads as 0.
6-4	DIVS	RW	3h	SMCLK source divider. Divides the frequency of the SMCLK clock source. 000b = f_{SMCLK}/1 001b = f_{SMCLK}/2 010b = f_{SMCLK}/4 011b = f_{SMCLK}/8 100b = f_{SMCLK}/16 101b = f_{SMCLK}/32 110b = Reserved. Defaults to f_{SMCLK}/32. 111b = Reserved. Defaults to f_{SMCLK}/32.
3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	DIVM	RW	3h	MCLK source divider. Divides the frequency of the MCLK clock source. 000b = f_{MCLK}/1 001b = f_{MCLK}/2 010b = f_{MCLK}/4 011b = f_{MCLK}/8 100b = f_{MCLK}/16 101b = f_{MCLK}/32 110b = Reserved. Defaults to f_{MCLK}/32. 111b = Reserved. Defaults to f_{MCLK}/32.

3.4.5 CSCTL4 Register

Clock System Control 4 Register

Figure 3-9. CSCTL4 Register

15	14	13	12	11	10	9	8
XT2DRIVE		Reserved	XT2BYPASS	Reserved			XT2OFF
rw-1	rw-1	r0	rw-0	r0	r0	r0	rw-1
7	6	5	4	3	2	1	0
XT1DRIVE		XTS	XT1BYPASS	Reserved		SMCLKOFF	XT1OFF
rw-1	rw-1	rw-0	rw-0	r0	r0	rw-0	rw-1

Table 3-7. CSCTL4 Register Description

Bit	Field	Type	Reset	Description
15-14	XT2DRIVE	RW	3h	The XT2 oscillator current can be adjusted to its drive needs. 00b = Lowest current consumption. XT2 oscillator operating range is 4 MHz to 8 MHz. 01b = Increased drive strength XT2 oscillator. XT2 oscillator operating range is 8 MHz to 16 MHz. 10b = Increased drive capability XT2 oscillator. XT2 oscillator operating range is 16 MHz to 24 MHz. 11b = Maximum drive capability and maximum current consumption for both XT2 oscillator. XT2 oscillator operating range is 24 MHz to 32 MHz.
13	Reserved	R	0h	Reserved. Always reads as 0.
12	XT2BYPASS	RW	0h	XT2 bypass select 0b = XT2 sourced from external crystal 1b = XT2 sourced from external clock signal
11-9	Reserved	R	0h	Reserved. Always reads as 0.
8	XT2OFF	RW	1h	Turns off the XT2 oscillator 0b = XT2 is on if XT2 is selected by the port selection and XT2 is not in bypass mode of operation. 1b = XT2 is off if it is not used as a source for ACLK, MCLK, or SMCLK
7-6	XT1DRIVE	RW	3h	The XT1 oscillator current can be adjusted to its drive needs. 00b = Lowest current consumption for XT1 LF mode. XT1 oscillator operating range in HF mode is 4 MHz to 6 MHz. 01b = Increased drive strength for XT1 LF mode. XT1 oscillator operating range in HF mode is 6 MHz to 10 MHz. 10b = Increased drive capability for XT1 LF mode. XT1 oscillator operating range in HF mode is 10 MHz to 16 MHz. 11b = Maximum drive capability and maximum current consumption for XT1 LF mode. XT1 oscillator operating range in HF mode is 16 MHz to 24 MHz.
5	XTS	RW	0h	XT1 mode select 0b = Low-frequency mode 1b = High-frequency mode
4	XT1BYPASS	RW	0h	XT1 bypass select 0b = XT1 sourced from external crystal 1b = XT1 sourced from external clock signal
3-2	Reserved	R	0h	Reserved. Always reads as 0.
1	SMCLKOFF	RW	0h	SMCLK off. This bit turns off the SMCLK. 0b = SMCLK on 1b = SMCLK off
0	XT1OFF	RW	1h	XT1 off. This bit turns off the XT1. 0b = XT1 is on if XT1 is selected by the port selection and XT1 is not in bypass mode of operation 1b = XT1 is off if it is not used as a source for ACLK, MCLK, or SMCLK

3.4.6 CSCTL5 Register

Clock System Control 5 Register

Figure 3-10. CSCTL5 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
ENSTFCNT2	ENSTFCNT1	Reserved				XT2OFFG[1]	XT1OFFG
rw-(1)	rw-(1)	r0	r0	r0	r0	rw-(0)	rw-(1)

(1) On devices without XT2, this flag is read only zero.

Table 3-8. CSCTL5 Register Description

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	Reserved. Always reads as 0.
7	ENSTFCNT2	RW	1h	Enable start counter for XT2 when available. 0b = Startup fault counter disabled. Counter is cleared. 1b = Startup fault counter enabled
6	ENSTFCNT1	RW	1h	Enable start counter for XT1. 0b = Startup fault counter disabled. Counter is cleared. 1b = Startup fault counter enabled
5-2	Reserved	R	0h	Reserved. Always reads as 0.
1	XT2OFFG	RW	0h	XT2 oscillator fault flag. If this bit is set, the OFIFG flag is also set. XT2OFFG is set if a XT2 fault condition exists. XT2OFFG can be cleared by software. If the XT2 fault condition still remains, XT2OFFG is set. On devices without XT2, this flag is read-only zero. 0b = No fault condition occurred after the last reset. 1b = XT2 fault. An XT2 fault occurred after the last reset.
0	XT1OFFG	RW	1h	XT1 oscillator fault flag (LF mode). If this bit is set, the OFIFG flag is also set. XT1OFFG is set if a XT1 fault condition exists. XT1OFFG can be cleared by software. If the XT1 fault condition still remains, XT1OFFG is set. 0b = No fault condition occurred after the last reset. 1b = XT1 fault (LF mode or HF mode). A XT1 fault occurred after the last reset.

3.4.7 CSCTL6 Register

Clock System Control 6 Register

Figure 3-11. CSCTL6 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved				MODCLKREQEN	SMCLKREQEN	MCLKREQEN	ACLKREQEN
r0	r0	r0	r0	rw-(0)	rw-(1)	rw-(1)	rw-(1)

Table 3-9. CSCTL6 Register Description

Bit	Field	Type	Reset	Description
15-4	Reserved	R	0h	Reserved. Always reads as 0.
3	MODCLKREQEN	RW	0h	MODOSC clock request enable. Setting this enables conditional module requests for MODCLK. 0b = MODCLK conditional requests are disabled 1b = MODCLK conditional requests are enabled
2	SMCLKREQEN	RW	1h	SMCLK clock request enable. Setting this enables conditional module requests for SMCLK. 0b = SMCLK conditional requests are disabled 1b = SMCLK conditional requests are enabled
1	MCLKREQEN	RW	1h	MCLK clock request enable. Setting this enables conditional module requests for MCLK. 0b = MCLK conditional requests are disabled 1b = MCLK conditional requests are enabled
0	ACLKREQEN	RW	1h	ACLK clock request enable. Setting this enables conditional module requests for ACLK. 0b = ACLK conditional requests are disabled 1b = ACLK conditional requests are enabled