BGN: 2191A
P5
Q6

a. 3. The module only has the counter update on the rising edge of the clock signal or the reset signal.

Each LE only has one output which is able to be clocked in this way, and the counter is 3 bits wide, therefore there must be at least 3 LEs

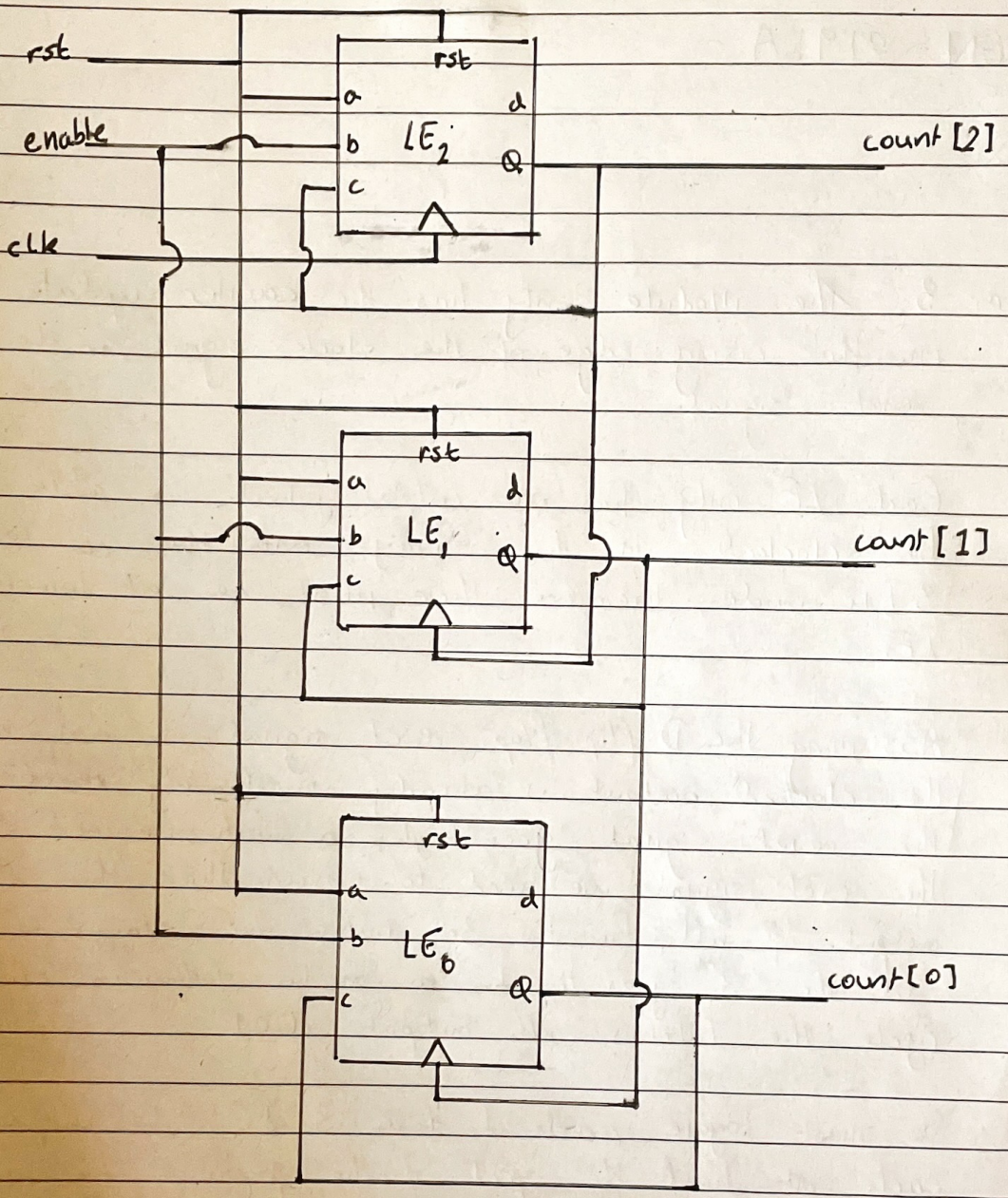
Assuming the D flip-flop reset signal is asynchronous, the clocked output is already immediately reset when the reset signal goes high, so with respect to the reset signal we need to ensure that the d output of all but the 3rd output LE stays as 0, and the 3rd goes to 1, so on the following clock cycle the latches will output 001.

We must toggle each of these 3 LE latch outputs, each at half the speed of the previous, to emulate counting - toggling so long as the enable signal is high and the reset is low

Therefore, each LE must only implement a 3-input logic function on its current latched output, the enable signal, and the reset signal.

Therefore the module can be implemented with 3 LEs

b.


rst
enable
clk
rst
a
b
c
d
Q
LE2
count [2]
rst
a
b
c
d
Q
LE1
count [1]
rst
a
b
c
d
Q
LE0
count [0]

c. LE_0 and LE_1:

a (rst)	b (enable)	c (Q)	d'
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

LE_2:

a(rst)	b(enable)	c(Q)	d'
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1