

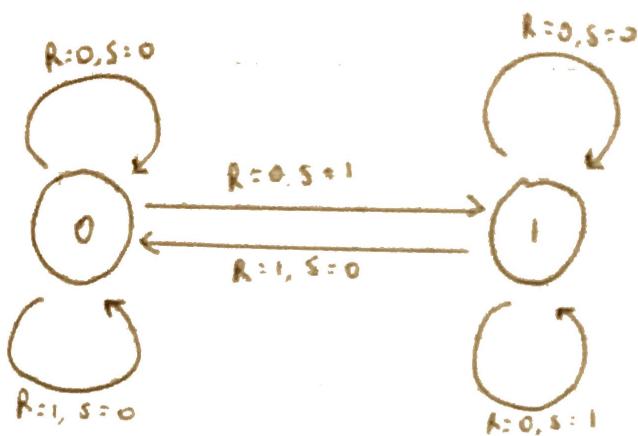
Digital Electronics Syllabus 3

1. A synchronous finite state machine has many possible states and has a logical way of transitioning from one state to the next. Such transitions occur on the rising edge of a clock pulse.
- Moore machines are synchronous FSMs in which the next state is determined purely by the current state
  - Mealy machines are synchronous FSMs in which the next state depends on both the current state and some input signal/s

2. SR Flip Flop

(NOTE: I made a distinction here between the state  $Z$  and the output  $Q$  because they don't quite match up).

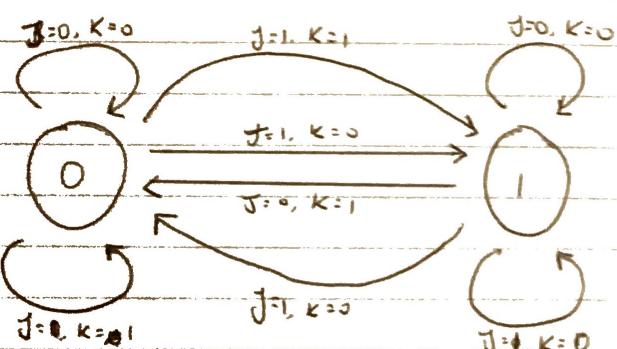
$S$	$R$	$Z_n$	$Z_{n+1}$	$Q$	$\bar{Q}$
0	0	0	0	0	1
0	1	0	0	0	1
1	0	0	1	1	0
1	1	0	invalid	1	1
0	0	1	1	1	0
0	1	1	0	0	1
1	0	1	1	1	0
1	1	1	invalid	1	1



$Z_n$	$Z_{n+1}$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

### JK Flip-Flop

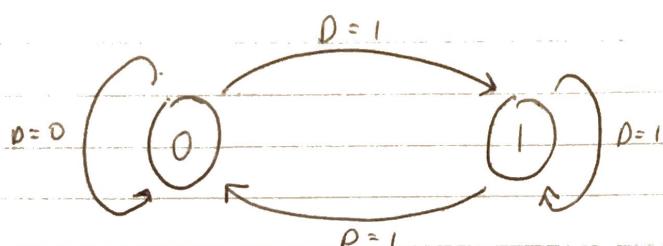
J	K	$Z_n$	$Z_{n+1}$	Q	$\bar{Q}$
0	0	0	0	0	1
0	1	0	0	0	1
1	0	0	1	1	0
1	1	0	1	1	0
0	0	1	1	1	0
0	1	1	0	0	1
1	0	1	1	1	0
1	1	1	0	0	1



$Z_n$	$Z_{n+1}$	$J$	$K$
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

### D Flip Flop

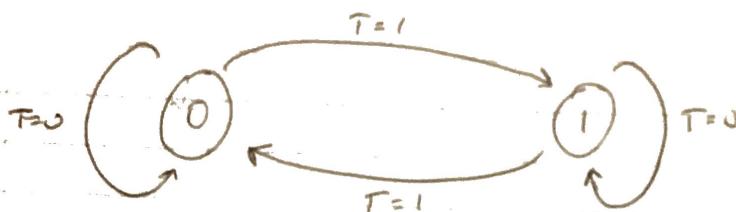
$D$	$Q_n$	$Q_{n+1}$
0	0	0
1	0	1
0	1	0
1	1	1



$Q_n$	$Q_{n+1}$	$D$
0	0	0
0	1	1
1	0	0
1	1	1

## T flip flop

T	$Q_n$	$Q_{n+1}$
0	0	0
1	0	1
0	1	1
1	1	0

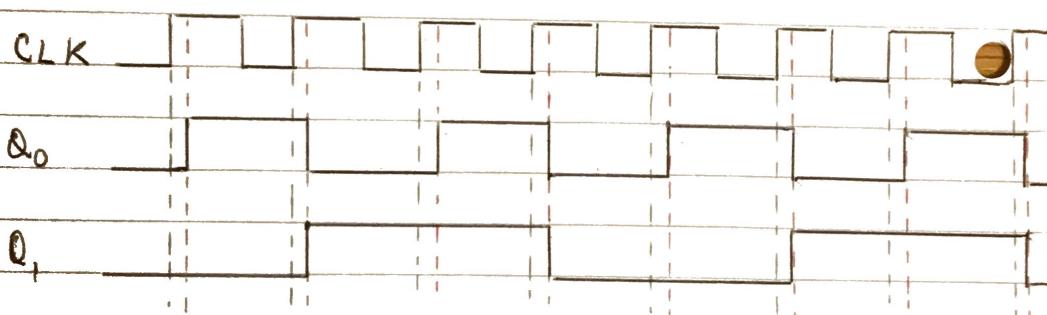


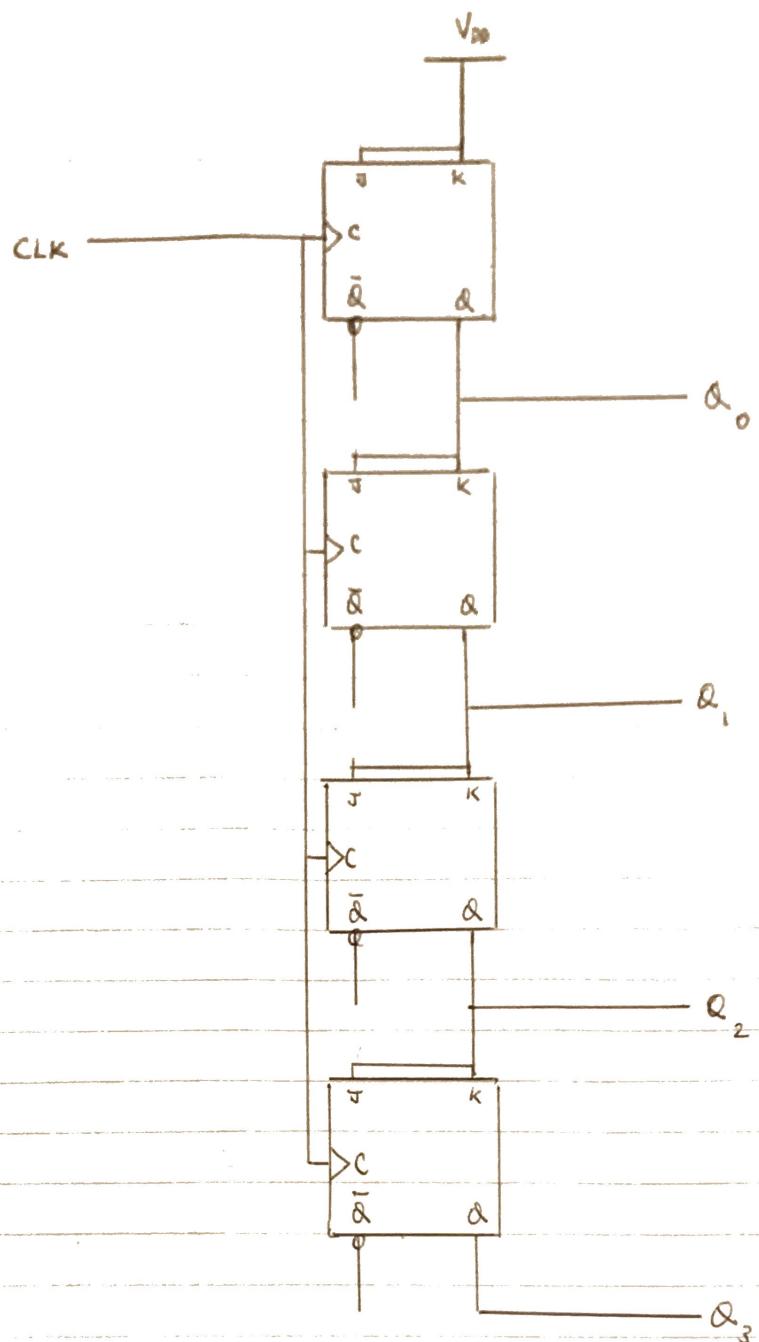
$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

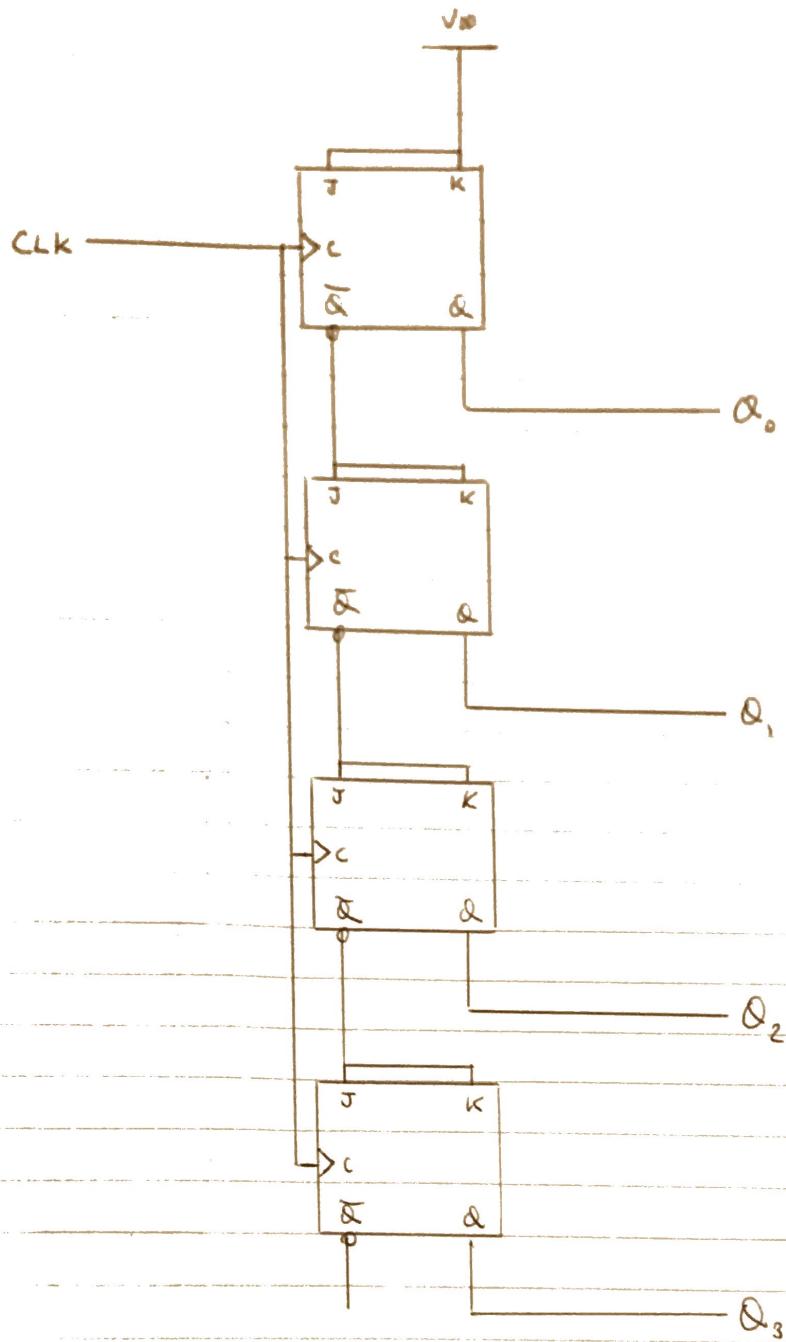
3a) CLK

$Q_0$

$Q_1$







$P$	$Q_0$	$\bar{Q}_0$	$Q_1$	$\bar{Q}_1$	$J_1$	$J_0$	$K_1$	$K_0$
0	0	0	0	0	0	0	x	x
1	0	0	0	1	0	1	x	x
0	0	1	1	0	1	x	x	1
1	0	1	0	1	0	x	x	0
0	1	0	1	0	x	c	0	x
1	1	0	1	1	x	1	0	x
0	1	1	1	1	x	x	0	0
1	1	1	0	0	x	x	1	1

Assuming  $Q_0$  and  $Q_1$  are both outputs of J-K Flip flops, they must have associated values  $J_0$  and  $K_0$ , and  $J_1$  and  $K_1$  respectively. These values can be filled in to the above table from the excitation table of a J-K Flip Flop:

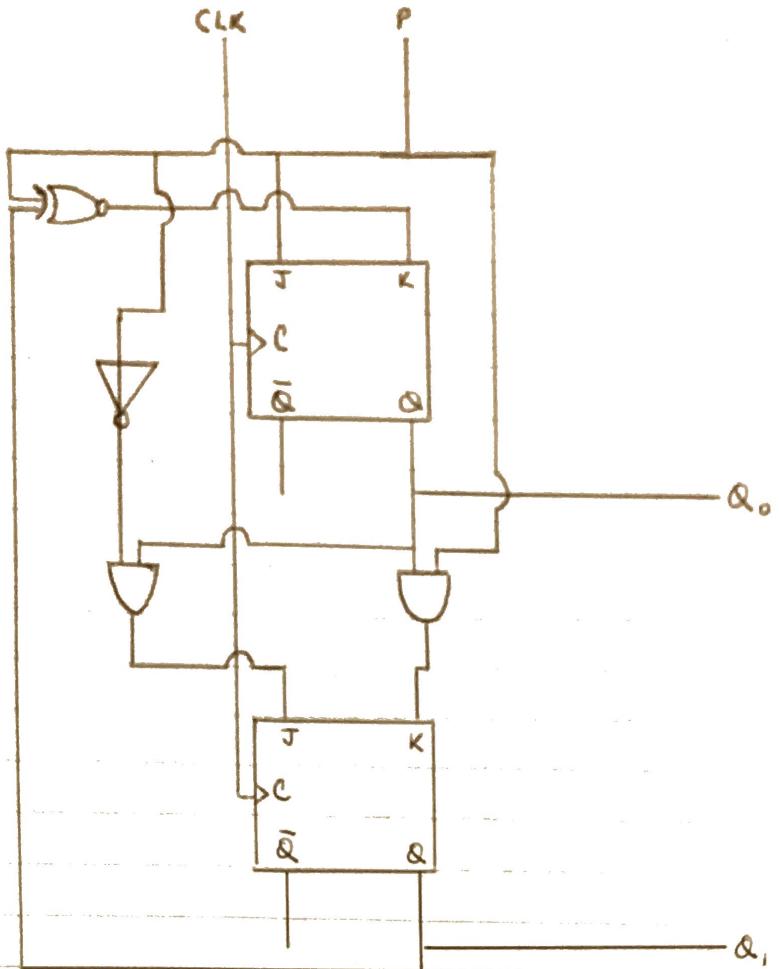
$nQ$	$\bar{n}Q$	$J$	$K$
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

The  $J_1$  column in the top table matches  $P \cdot Q_0$ .

$J_0$  matches  $P$

$K_1$  matches  $P \cdot \bar{Q}_0$

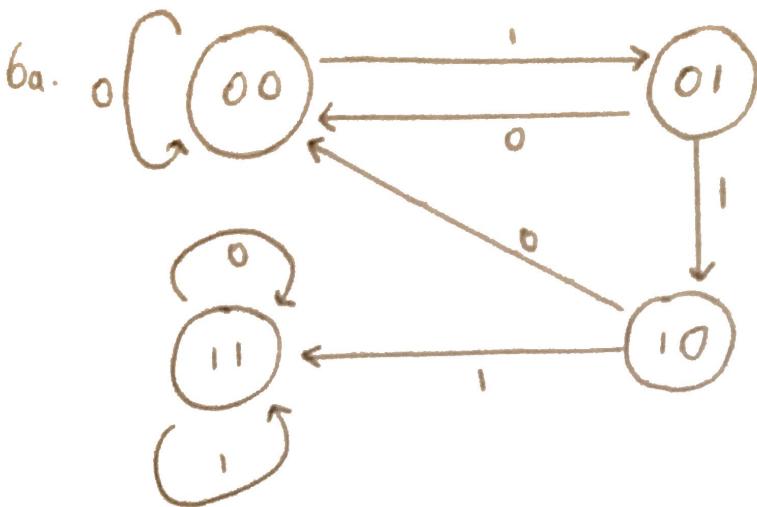
$K_0$  matches  $\overline{P \oplus \bar{Q}_0}$



5. Clock Cycle |  $Q_1$  |  $Q_0$

0	0	0
1	0	1
2	1	0
3	0	0

It counts from 0 to 2 (inclusive) in binary  
and then resets to 0



If the system ends in state 11, then there are at least 3 consecutive 1s. Otherwise, there are not.

### b. Mealy

c. Since I don't know whether  $Q_1$  and  $Q_0$  will be the outputs of J-K Flip Flops or D Flip Flops, I will include the corresponding values of J, K, and D with each transition, under the assumption that we must ~~not~~ either use the J and the K, or the D, whichever ends up being simpler.

P	$nQ_1$	$nQ_0$	$nnQ_1$	$nnQ_0$	J <sub>1</sub>	J <sub>0</sub>	K <sub>1</sub>	K <sub>0</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	0	0	0	0	0	X	X	0
1	0	0	0	1	0	1	X	X	0	1
0	0	1	0	0	0	X	X	1	0	0
1	0	1	1	0	1	X	X	1	1	0
0	1	0	0	0	X	0	1	X	0	0
1	1	0	1	1	X	1	0	X	1	1
0	1	1	1	1	X	X	0	0	1	1
1	1	1	1	1	X	X	0	0	1	1

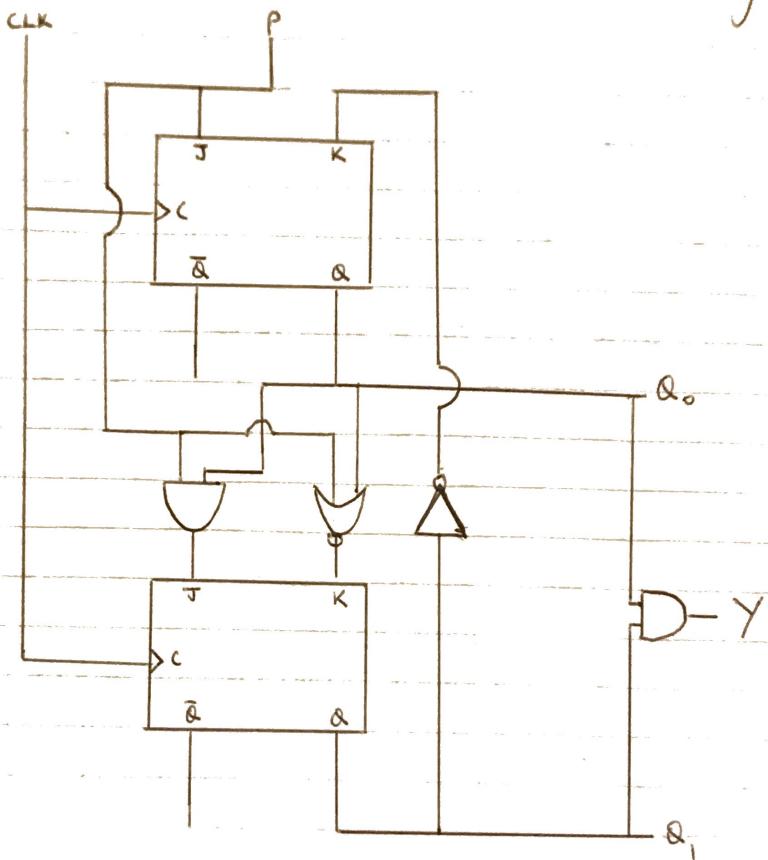
The column  $J_0$  matches  $P \cdot Q_0$ .

$J_0$  matches  $\frac{P}{P+Q_0}$

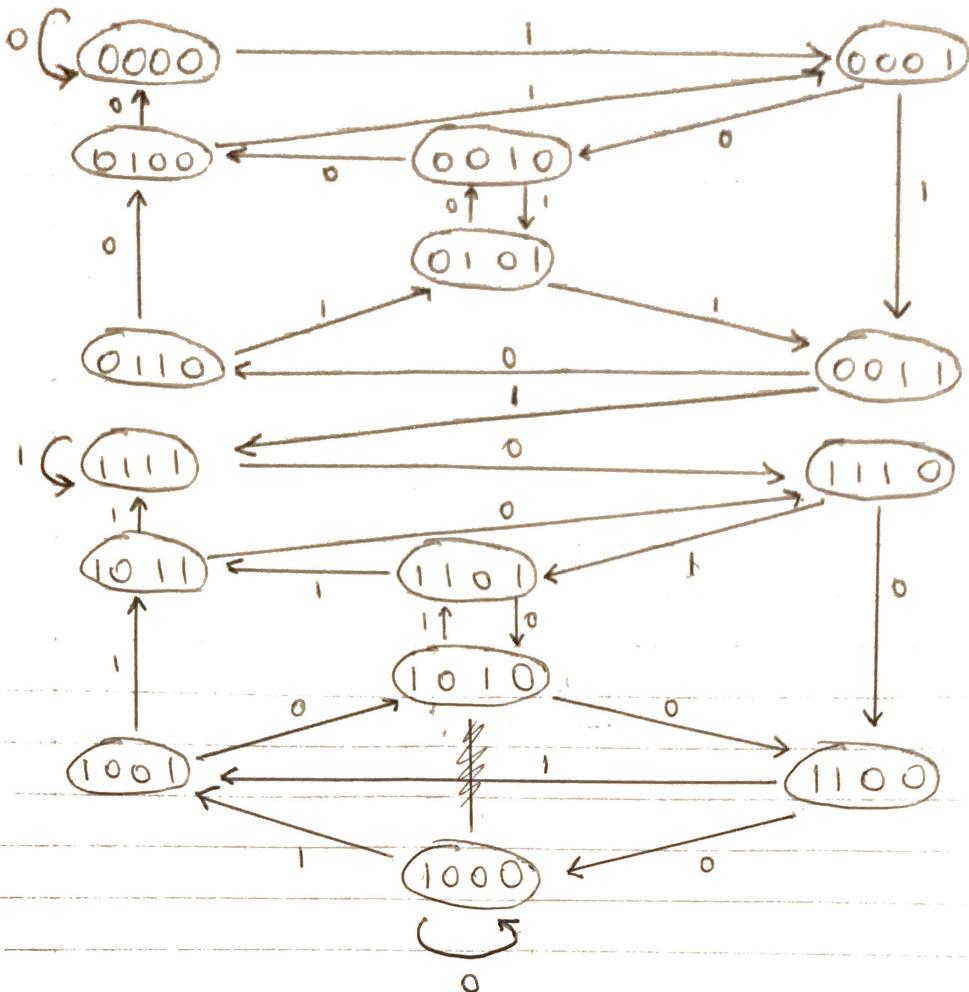
$K_0$  matches  $\frac{Q_0}{P+Q_0}$

$K_0$  matches  $\frac{Q_0}{Q_0}$

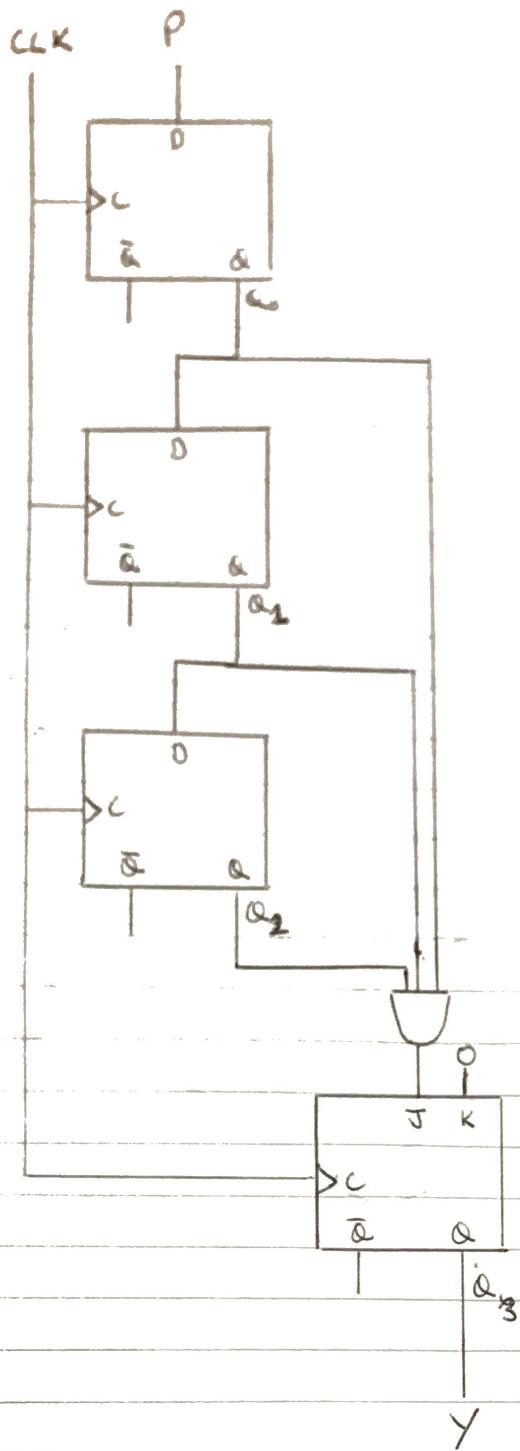
$D_0$  and  $D_1$  do not match any simple combination of  $P$ ,  $Q_0$ , and/or  $Q_1$  which I could see so I think it will be simpler to use 2 J-K flip-flops and no D flip flops. Perhaps this wouldn't be the case if I had used one-hot state encoding.

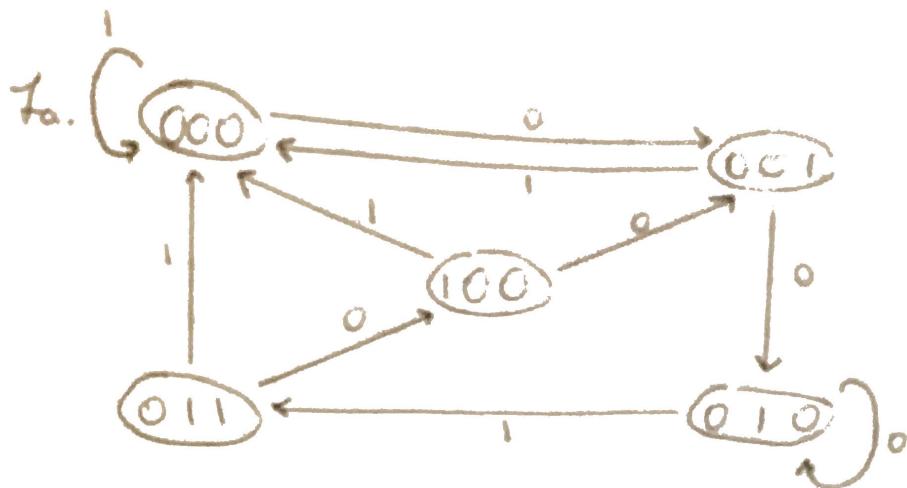


Alternatively, a more complicated state diagram does give an easier-to-understand circuit.



where any state in which the most significant bit is a 1 is a success state.



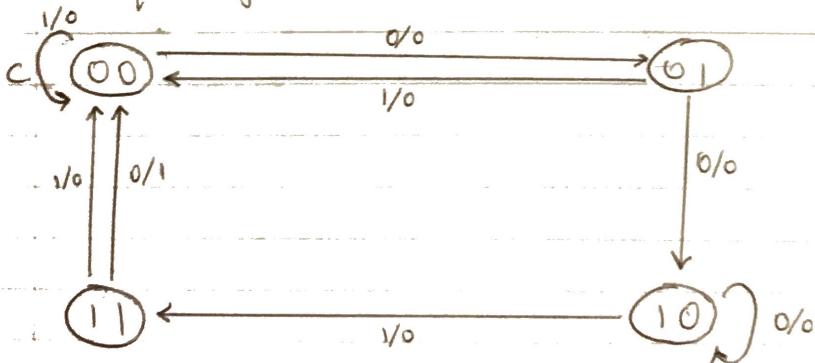


Where  $Q_o$  is the output.

b. Y  $mQ_2$   $mQ_1$   $mQ_0$  |  $mQ_2$   $mQ_1$   $mQ_0$

0	0	0	0	0	0	T
1	0	0	0	0	0	0
0	0	0	1	0	1	0
1	0	0	1	1	0	0
0	0	1	0	0	1	0
1	0	1	0	0	1	1
0	0	1	1	1	0	0
1	0	1	1	0	0	0
0	1	0	0	0	0	1
1	1	0	0	0	0	0

State 100 is equivalent to state 000 and so is redundant. However, if we remove it, we can no longer take a meaningful output from the machine.

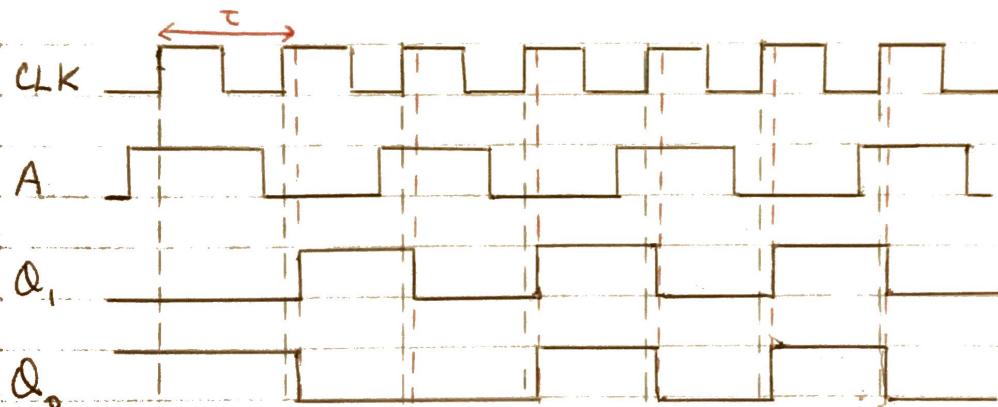


$S_0$	A	$\bar{Q}_1$	$Q_1$	$\bar{Q}_0$	$Q_0$	$D_1$	$D_0$
0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0
1	0	1	1	1	0	1	0
0	1	0	0	0	1	0	1
1	1	0	1	1	1	1	1
0	1	1	0	1	0	1	1
1	1	1	1	1	1	1	1

Where  $D_1$  is the required input to  $Q_1$ , and  $D_0$  is likewise for  $Q_0$ .

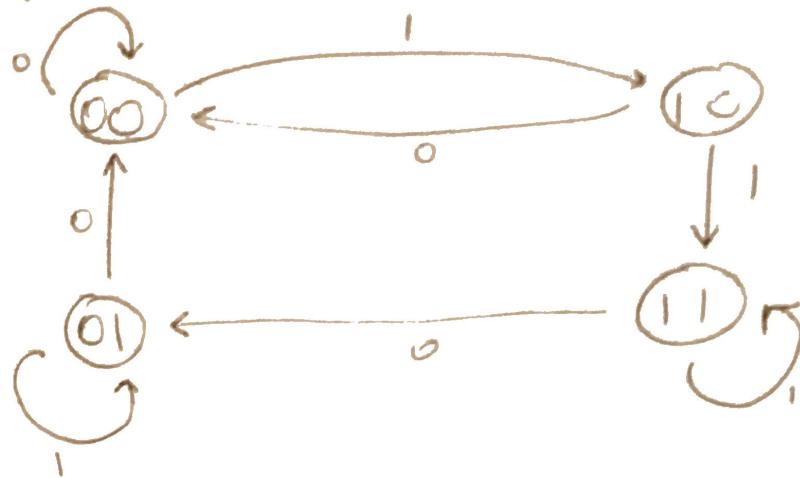
Note that  ~~$D_1 = A$~~   $D_1 = A$  and  $D_0 = \bar{Q}_1$ .  
∴ This is a shift register

- b. If the clock rate is faster than the transmission delay of the flip flops this decreases the likelihood of ~~the~~ the dashed transitions, as shown below:



Instead of alternating  $01 \rightarrow 10 \rightarrow 01 \rightarrow \dots$   
The machine ends up alternating  $11 \rightarrow 00 \rightarrow 11 \dots$

c) Option 1:

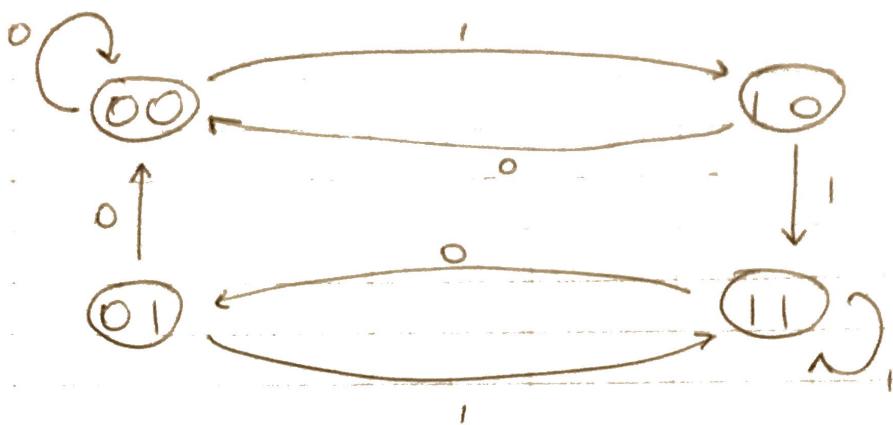


A	${}_{m+1}Q_2$	${}_mQ_1$	${}_{m+1}Q_2$	${}_{m+1}Q_1$
0	0	0	0	0
1	0	0	1	0
0	0	1	0	0
1	0	1	0	1
0	1	0	0	0
1	1	0	1	1
0	1	1	0	1
1	1	1	1	1

$${}_{m+1}Q_2 = A({}_mQ_2 + {}_m\bar{Q}_1)$$

$${}_{m+1}Q_1 = A({}_mQ_2 + {}_mQ_1) + {}_mQ_2 {}_m\bar{Q}_1$$

Option 2.

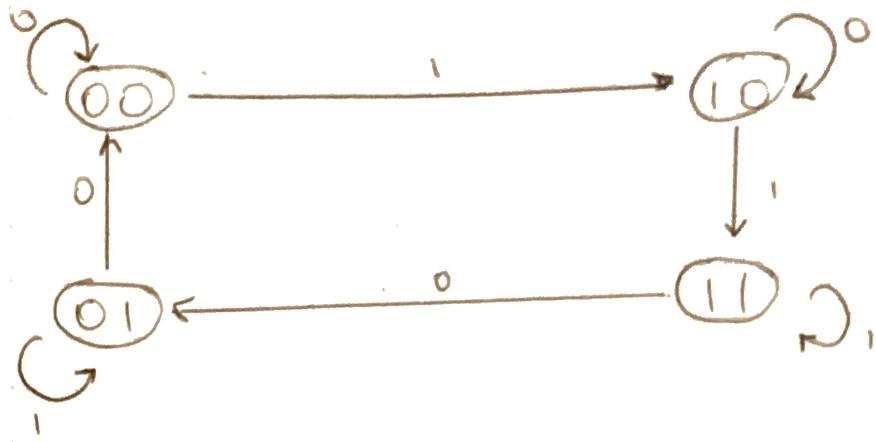


A	$_{mH}\theta_2$	$_{mH}\theta_1$	$_{mn}\theta_2$	$_{mn}\theta_1$
0	0	0	0	0
1	0	0	1	0
0	0	1	0	0
1	0	1	1	1
0	1	0	0	0
1	1	0	1	1
0	1	1	0	1
1	1	1	1	1

$$_{mH}\theta_2 = A$$

$$_{mn}\theta_1 = A( _{mH}\theta_2 + \theta_1) + _{mH}\theta_2 \theta_1$$

### Option 3

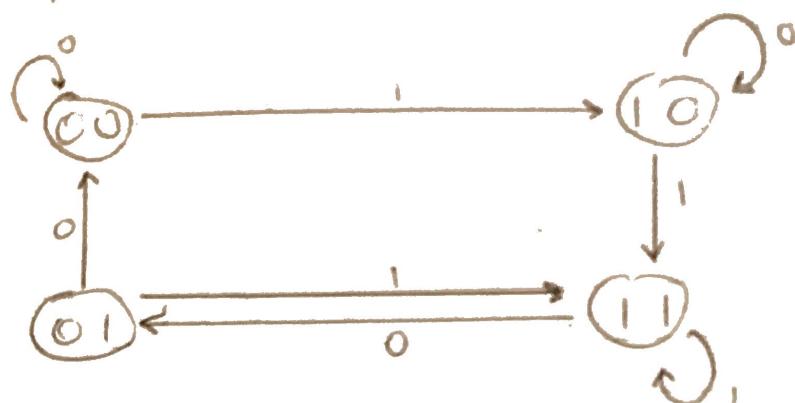


A	$m\bar{Q}_2$	$m\bar{Q}_1$	$m+1\bar{Q}_2$	$m+1\bar{Q}_1$
0	0	0	0	0
1	0	0	1	0
0	0	1	1	0
1	0	1	1	1
0	1	0	0	1
1	1	0	1	1
0	1	1	0	0
1	1	1	1	1

$$m+1\bar{Q}_2 = \cancel{m\bar{Q}_2(A + \bar{Q}_1)} + \bar{A}m\bar{Q}_2\bar{Q}_1$$

$$m+1\bar{Q}_1 = m\bar{Q}_2(A + \bar{Q}_1) + A\bar{m}\bar{Q}_2\bar{Q}_1$$

#### Option 4



A	$mQ_2$	$mQ_1$	$m_{m1}Q_2$	$m_{m1}Q_1$
0	0	0	0	0
1	0	0	1	0
0	0	1	0	0
1	0	1	1	1
0	1	0	1	0
1	1	0	1	1
0	1	1	0	1
1	1	1	1	1

$$m_{m1}Q_2 = \overline{Q_2}A + \overline{Q_2}(A + \overline{Q_1})$$

$$m_{m1}Q_1 = \overline{Q_2}A\overline{Q_1} + \overline{Q_2}(A + \overline{Q_1})$$