Resistors and Resistive Networks

1.1 Objectives

In this lab, you will be examining the behavior of three simple resistive networks: a two-way resistive voltage divider, a two-way resistive current divider, and an R-$2R$ ladder network. Each of these simple networks find applications in more complicated circuits, some of which we will see in later labs. In the process, you should become familiar with the process of building a circuit in LTspice and simulating its behavior and with the use of MATLAB (or whatever other tool you prefer) for analyzing and plotting experimental data.

1.2 Prelab

The following prelab questions have been constructed to help you prepare to do the lab efficiently. Please complete these questions *before* you come to lab. While you may discuss the prelab questions with your lab partner or with other students in the class, each student in a lab group should complete the prelab assignment individually, so that you each understand the circuit(s) that you will be testing and what you will be doing in the lab.

1. **Electrical Measurement Concepts**. Choose the phrases which correctly complete each of the following statements.

   (a) An ideal voltage meter has **(zero|infinite)** internal resistance and should be connected in **(series|parallel)** with the circuit or device being tested.

   (b) An ideal current meter has **(zero|infinite)** internal resistance and should be connected in **(series|parallel)** with the circuit or device being tested.

2. **Resistive Divder Accuracy**. Two-way resistive voltage and current divider ratios are both expressible as the ratio of one resistance to the sum of two resistances. Suppose that each resistance in the divider is subject to some finite tolerance (e.g., typically $\pm 5\%$ for a 0.25-W carbon resistor or $\pm 1\%$ for a metal-film resistor) about its nominal value. Determine how the tolerance on the divider ratio depends on the tolerances of the individual components if the tolerances are conceived of as the coefficient of variations (CVs) of uncorrelated random variables.

3. **R-2R Ladder Network**. Consider the circuit shown in Fig. 1.1. It is called an R-$2R$ *ladder network*, because if you were to turn it sideways it would look like a ladder. This type of circuit is commonly used to build digital-to-analog (D/A) converters to interface computers to the real world, as you will be considering in the postlab section. As a function of the applied voltage, V, and the unit resistance, R, what are the currents, I_1 through I_N, that flow through each of the $2R$ branches?

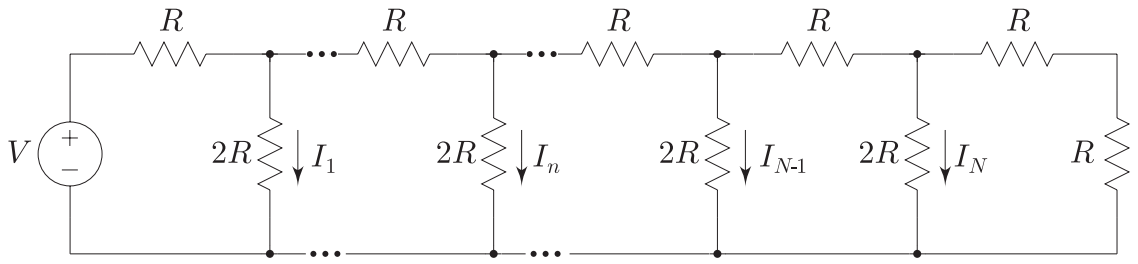

Figure 1.1: An R-$2R$ ladder network.

4. **Accurate 2:1 Resistor Ratios**. In order to obtain accurate current division at each branch in the R-$2R$ ladder network shown in Fig. 1.1, we need to have accurate 2:1 ratios between the various branches in the network. When designing integrated circuits, we obtain the most accurate ratios (for rational numbers) when we use an integral number of well-matched unit-sized devices. In this case, we would like to construct two effective resistances in a 2:1 ratio from three identical resistors, each with a resistance R. Come up with two different methods to accomplish this goal. In building an R-$2R$ ladder network, which method uses fewer unit resistors?

1.3 Experiments

You will be doing three experiments in this lab. In the first experiment, you will be constructing a two-way resistive voltage divider, simulating its voltage transfer characteristic, and extracting the actual divider ratio. In the second experiment, you will be constructing a two-way resistive current divider, simulating its current transfer characteristic, and extracting the actual divider ratio. In the third experiment, you will be constructing an R-$2R$ ladder network and examining the currents in each stage as a function of posititon in the ladder. For all three experiments, you should construct your schematic in LTspice as if you were building it from Bourns thick-film resistor array chips. These sixteen-pin chips have eight independent resistors each of which has a nominal value of $10\,\mathrm{k}\Omega$ integrated into a single package. The pinout for this chip is shown in Fig. 1.2. The tolerance on the absolute resistance values is $\pm 2\%$, but the coefficient of variation for resistances from the same array is typically more like 0.2% or less, so resistors within a single array are quite well matched. Resistances from different arrays from the same tube typically have a coefficient of variation of about 0.35%, so the resistors even match reasonably well across arrays taken from the same tube.

In your lab report, you should include graphs of all theoretical and experimental curves. In general, you should plot the measurements in a point style so the individual points are distinguishable. Any theoretical fits to the data should be plotted on the same graph as the experimental data in a line style.

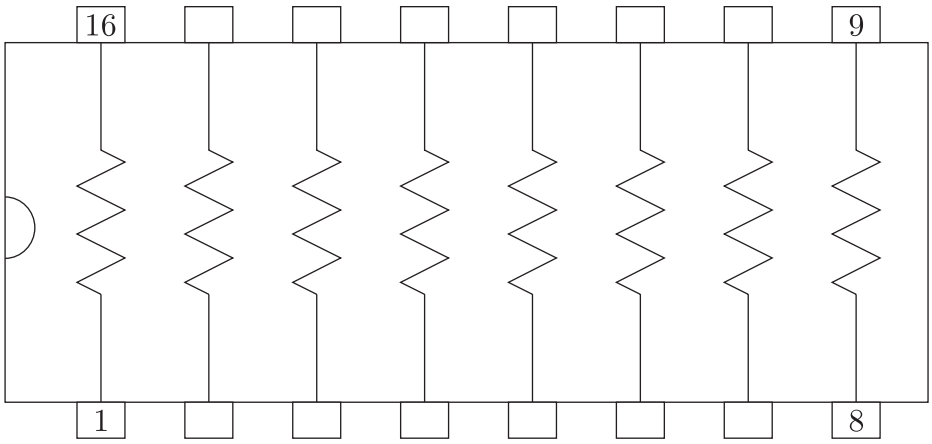

Figure 1.2: Pinout of the Bourns isolated thick-film resistor array.

1.3.1 Experiment 1: Resistive Voltage Division

Construct a two-way resistive voltage divider in which the divider ratio is a ratio of two small integers from nominal 10-kΩ unit resistors by connecting these unit resistors in series or in parallel. You should set up your resistors so that they are subject to a pseudorandom gaussian variation with a coefficient of variation (CV) of 0.2% to simulate the mismatch typical of the Bourns resistor arrays. With a voltage source, apply an input voltage and measure the output voltage as a function of input voltage. Perform a batch of 500 Monte Carlo simulations of your voltage divider's VTC using LTspice. In your report, include a schematic showing your LTspice set up. Using MATLAB (or some other appropriate tool of your choice), fit a straight line to the divider's voltage transfer characteristic for each simulation step and extract the value of the divider ratio. Make a plot showing both the simulated data and the theoretical fit along with the extracted value of the divider ratio for a single simulation step. How does the actual divider ratio compare to the nominal theoretical one?

Make a plot showing a histogram of the extracted voltage divider ratios along with the coefficient of variation of the extracted divider ratios. Is the coefficient of variation that you obtain from the population of your curve fits consistent with what you would expect based on the per-unit sensitivities of your voltage divider to each resistor and the 0.2% coefficient of variation of your simulated resistors?

1.3.2 Experiment 2: Resistive Current Division

Next, construct a two-way resistive current divider in which the divider ratio is a ratio of two small integers from nominal 10-kΩ unit resistors by connecting these resistors in series or parallel. As you did in the first experiment, set up your resistors to be subject to a pseudorandom gaussian variation with a CV of 0.2%. Apply an input current to the divider with a current source as you measure the output current with an ammeter. Perform a single DC sweep simulation of your current divider's current transfer characterstic using

LTspice. In your report, include a schematic showing your LTspice experimental set up. Using MATLAB (or some other appropriate software), fit a straight line to the divider's current transfer characteristic and extract the value of the divider ratio. Make a plot showing both the measured data and the theoretical fit along with the extracted value of the divider ratio. How does the extracted divider ratio compare to the theoretical one?

1.3.3 Experiment 3: R-2R Ladder Network

From nominal 10-kΩ unit resistors, construct an R-$2R$ ladder network with four $2R$ branches. Set up your with pseudorandom variation as you did in the first two experiments. Apply a voltage to the network with a voltage source and measure the current flowing in each of the $2R$ branches in turn with ammeters. Perform a DC sweep simulation of these currents for three values of the input voltage source. In your report, include a schematic of your LTspice set up. Export your results into MATLAB (or other tool) and make a semilog plot of current as a function of position for all three values of input voltage on a single graph along with appropriate theoretical expected values. Do these currents vary with position as you expect?

1.4 Postlab

We live in a physical world of analog signals, such as light intensity, sound pressure, force, position, acceleration, and temperature, whose values can vary continuously. As digital computers have become smaller, cheaper, and more powerful, we have tried to put these remarkable devices almost everywhere in order to monitor and control physical systems in ways that, a few years ago, would have been inconceivable. Information is usually represented inside of digital computers as binary numbers, a representation that is usually not directly compatible with the analog world. Consequently, if our computer systems are to monitor and control bits and pieces of the physical world, we need to build some kind of system that can convert both from the analog representation to the digital format and from the digital format back to the analog format. The former devices are called *analog-to-digital* (A/D) converters while the latter devices are called *digital-to-analog* (D/A) converters.

Binary numbers are just like decimal numbers, except that the value of each *b*inary dig*it* (bit) can only take on the values of 0 or 1 instead of any integral value between 0 and 9. Also, in the binary number system, the weight assigned to each position is a successive power of two instead of a power of ten, as it is in the decimal system; that is, for a binary number, we have a ones position (i.e., 2^0), a twos position (i.e., 2^1), and a fours position (i.e., 2^2), instead of a ones position (i.e., 10^0), a tens position (i.e., 10^1), and a hundreds position (i.e., 10^2) that we would have for a decimal number. Accordingly, the value of a binary number that has been expressed as a string of N bits $b_{N-1} \ldots b_1 b_0$ is given by

$$\sum_{n=0}^{N-1} b_n 2^n,$$

where b_n is the value of the nth bit, which can be equal either to 0 or to 1.

An N-bit D/A converter is an analog circuit that takes N bits and produces an analog signal (usually either a current or a voltage) whose value is proportional to the sum just

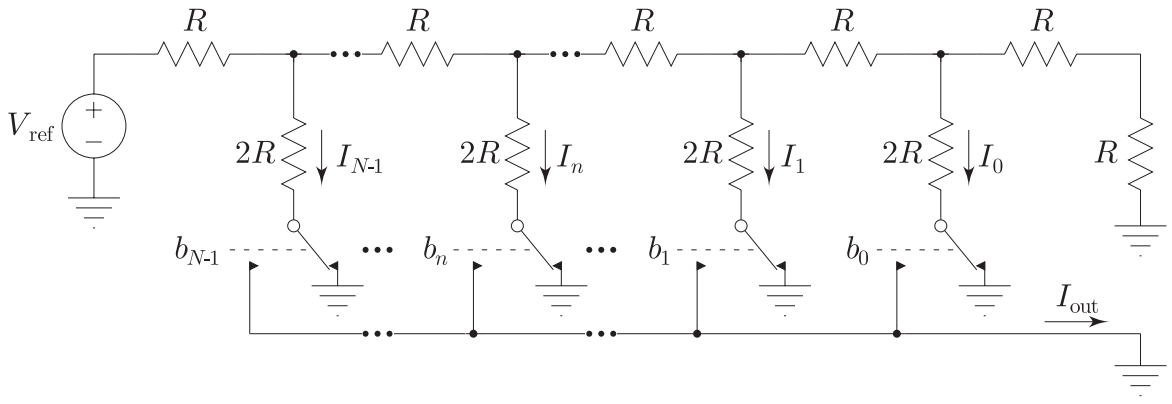

Figure 1.3: A conceptual N-bit R-$2R$ ladder D/A converter. The position of each switch is controlled by a different bit of the N bit binary number to be converted into an analog current value. In this case, all switches shown are in the 0 position.

given. In order to perform this operation, we need to produce voltages or currents that are in ratios of successive powers of two, and then to add them up selectively, depending on whether the value of a particular bit is zero or one. If a given bit is a zero, then the current or voltage at its position is not added into the sum. If a given bit is a one, then the current or voltage at its position is added to the sum.

Consider the circuit shown in Fig. 1.3, called an *R-2R ladder network*, which is a commonly used structure in building D/A and A/D converters. Derive an expression relating the current flowing through each of the $2R$ resistors to the reference voltage, V_{ref} and to the *unit resistance*, R. In the circuit shown in Fig. 1.3, each switch selectively steers one of these currents to the left or to the right based on the value of one of the binary digits in an N-bit binary number. Those currents that are steered to the left are combined to form an output current, I_{out}, flowing into ground. Derive an expression relating I_{out} to the values of the binary digits (i.e., $b_{N-1},\ldots, b_0$), the reference voltage (i.e., V_{ref}), and the unit resistance (i.e., R).