

Cache Simulator Project Report

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CS 5513
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- A brief description of the implementation of the simulator

This cache simulator is to simulate set associative caches with different replacement policy. The simulator would take command-line parameter of memory trace file name, with optional choice of cache size, associativity, and replacement policy including LRU, Second Chance, FIFO and LIFO, then read these memory addresses line by line and simulate their accesses to cache. By default, this simulator is configured with an LRU write-back cache of 1 MB with 16-ways. The parser.py handles reading in cache sequence from the file. The sim.py is the main program reads optional configuration and take the tag bits from sequence, determine if cache hit or cache miss in cache.py, with different kind of replacement policy.

- A description of your experiments and the experiment results with figures and/or tables

The experiments simulate the memory accesses from memory traces obtained from real applications to with different sizes, ways and replacement policies to determine the configuration gives the lowest cache miss rate.

1KB 64B:

	2-ways				4-ways				8-ways				16-ways			
	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO
1 KB	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%
32 KB	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%
256 KB	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%
1 MB	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%
4 MB	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%

4MB 4B:

	2-ways				4-ways				8-ways				16-ways			
	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO
1 KB	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%
32 KB	6.25%	6.25%	6.25%	6.23%	6.25%	6.25%	6.25%	6.23%	6.25%	6.25%	6.25%	6.22%	6.25%	6.25%	6.25%	6.22%
256 KB	6.25%	6.25%	6.25%	6.12%	6.25%	6.25%	6.25%	6.05%	6.25%	6.25%	6.25%	6.02%	6.25%	6.25%	6.25%	6.01%
1 MB	6.25%	6.25%	6.25%	5.73%	6.25%	6.25%	6.25%	5.47%	6.25%	6.25%	6.25%	5.34%	6.25%	6.25%	6.25%	5.27%
4 MB	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%	2.08%

32MB 4B:

	2-ways				4-ways				8-ways				16-ways			
	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO
1 KB	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%
32 KB	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%	6.25%
256 KB	6.25%	6.25%	6.25%	6.23%	6.25%	6.25%	6.25%	6.23%	6.25%	6.25%	6.25%	6.22%	6.25%	6.25%	6.25%	6.22%
1 MB	6.25%	6.25%	6.25%	6.18%	6.25%	6.25%	6.25%	6.15%	6.25%	6.25%	6.25%	6.14%	6.25%	6.25%	6.25%	6.13%
4 MB	6.25%	6.25%	6.25%	5.99%	6.25%	6.25%	6.25%	5.86%	6.25%	6.25%	6.25%	5.79%	6.25%	6.25%	6.25%	5.76%

bw mem:

[illegible]

ls:

[illegible]

gcc:

[illegible]

native_dgemm:

[illegible]

native_dgemm_full:

	2-ways				4-ways				8-ways				16-ways			
	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO
1 KB	55.48%	57.74%	57.74%	60.82%	55.47%	55.48%	57.0%	66.15%	55.47%	55.47%	55.47%	76.81%	55.47%	55.47%	55.47%	98.12%
32 KB	49.4%	49.4%	49.4%	49.56%	49.4%	49.4%	49.4%	49.73%	49.4%	49.4%	49.4%	50.06%	49.39%	49.4%	49.4%	51.1%
256 KB	49.38%	49.38%	49.38%	49.4%	49.38%	49.38%	49.38%	49.4%	49.37%	49.38%	49.38%	49.43%	49.37%	49.37%	49.37%	49.49%
1 MB	0.13%	0.15%	0.15%	0.64%	0.13%	0.15%	0.17%	24.95%	0.13%	0.15%	0.17%	25.6%	0.13%	0.15%	0.17%	21.0%
4 MB	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%	0.08%

openblas_dgemm:

	2-ways				4-ways				8-ways				16-ways			
	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO
1 KB	62.75%	62.84%	62.84%	67.19%	61.72%	61.8%	61.85%	79.71%	61.76%	61.85%	61.95%	81.49%	61.78%	61.8%	61.93%	83.08%
32 KB	18.43%	19.45%	19.45%	17.94%	13.44%	21.47%	22.2%	19.81%	16.33%	23.11%	23.16%	16.2%	22.13%	25.05%	25.01%	14.38%
256 KB	8.34%	9.12%	9.12%	7.75%	8.3%	8.39%	9.08%	7.43%	8.3%	8.37%	9.06%	7.71%	8.3%	8.35%	9.1%	7.98%
1 MB	4.03%	4.08%	4.08%	3.38%	5.17%	4.95%	5.04%	3.41%	6.57%	6.19%	6.34%	3.32%	8.06%	7.97%	8.01%	3.13%
4 MB	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%	2.27%

openblas_dgemm_full:

	2-ways				4-ways				8-ways				16-ways			
	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO	LRU	SC	FIFO	LIFO
1 KB	51.49%	51.66%	51.66%	56.7%	50.65%	50.75%	50.88%	68.36%	50.39%	50.48%	50.64%	72.74%	50.41%	50.43%	50.63%	75.65%
32 KB	15.52%	16.39%	16.39%	26.03%	11.58%	18.05%	18.58%	30.88%	13.83%	19.21%	19.33%	33.95%	18.42%	20.76%	20.83%	38.64%
256 KB	7.54%	8.17%	8.17%	9.36%	7.5%	7.53%	8.13%	11.09%	7.5%	7.51%	8.13%	14.38%	7.5%	7.51%	8.15%	25.99%
1 MB	3.02%	3.15%	3.15%	7.92%	4.26%	4.16%	4.32%	8.35%	5.66%	5.41%	5.71%	9.3%	7.2%	6.83%	7.11%	11.02%
4 MB	0.88%	0.93%	0.93%	1.4%	0.94%	0.94%	0.93%	2.17%	0.96%	0.95%	0.97%	7.7%	0.98%	0.96%	0.98%	8.12%

• Individual contribution summary

Many thanks to Bilal contributed the key part of the simulator program, including implements different types of replacement policies and the structure of cache. Zhongxiu handled the parsing sequence from file, tested the correctness of program and did the experiments for all memory trace files.