Kaitlin **Lucio**

Electrical and Computer Engineer

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Education

Harvey Mudd College — *Claremont, CA*

B.S. in Engineering — *Aug 2019 - Dec. 2024*

GPA: 3.057

Work Experience

Design Automation Intern — *Remote*

Blue Cheetah Analog — *May 2024 - Present*

- Refactored existing RTL files using a YAML representation influenced by IP-XACT, enabling rapid reuse of IP across projects.
- Added simulator-agnostic wave database creation and probing to internal tool used for design verification and debugging.
- Wrote Python to link codebases to generate addressing logic in SystemVerilog, ensuring rapid design and addressing of APB bus signals.
- Assisted other interns with tasks as necessary.

Clay-Wolkins Fellowship Research Assistant — *Claremont, CA*

Harvey Mudd College — *May 2022 - Present*

- Automated testing of processor functionality for OpenHWGroup's processor CVW-Wally via a test script
- Modified existing scripts and testbenches to allow for automated testing of the Linux boot process.
- Rebuilt AHBLite bus' finite-state machine to implement burst mode, resulting in a 2% performance increase.
- Designed tests for a GPIO, PLIC, and UART in RISC-V Assembly and implemented them in testbenches to verify processor functionality.

Digital Design Intern — *Claremont, CA*

Qualcomm — *Aug. 2023 - Present*

- Worked with a team of four students to analyze RTL projects to determine when a project will cause problems in logic synthesis.
- Wrote wrapper script to perform synthesis with Synopsys Design Compiler for RTL Projects to analyze synthesis results.
- Synthesized projects to create AND-Inverter graphs in the AIGER format for analysis using logical effort
- Used Python to analyze AND-Inverter Graphs for parameters identified to cause synthesis issues such as congestion and timing

R&D Intern — *Westwood, CA*

Silvus Technologies — *Jun. 2023 - Aug. 2023*

- Characterized the frequency response of an embedded radio using an RF Testbench controlled via MATLAB using VISA commands.
- Built a parser for Synopsys netlists using Python, speeding up detection of transistor issues and saving hundreds of hours of manual searching.
- Automated phase calibration of multi-antenna high-speed embedded radios, allowing for testing and production of phase-calibrated radios.

Skills

Programming & Computer Languages, SystemVerilog, C, Assembly, Python, MatLAB, Linux, TCL, Bash, git

CAD Programs, KiCad, LTSpice, Synopsys Design Compiler, ModelSim, Verilator

Projects

Harvey Mudd College — *Claremont, CA*

Graphics Card Digital Designer — *Nov 2023 - Dec 2023*

- Took charge of creating system schematic for an eight color 32x20 graphics driver over VGA from the ground up.
- Wrote SystemVerilog HDL to implement and test system architecture.
- Used Python to generate testvectors for pre-silicon design verification.
- Used oscilloscope to verify correctness of HSync and VSync traces when monitor failed to recognize VGA signal

Other Experience

Humans vs Zombies — *Claremont, CA*

Head Moderator for Humans vs Zombies — *Feb. 2022 - Present*

- Ran semesterly week-long games of infection tag to bring joy to hundreds of students' lives.
- Led moderation team to write stories and missions and move objects required for the game to event locations.
- Negotiated with college administration to ensure the game would not disrupt other events to promote a fun environment on campus.