Kaitlin **Lucio**

ELECTRICAL ENGINEER

📱 (+1) 909-736-7148 | ✉ kaitlin.verilog@gmail.com | 🐙 slmnemo | 💼 kaitlinverilog

Education

Harvey Mudd College *Claremont, CA*

B.S. IN ENGINEERING *Aug 2019 - Dec. 2024*

Work Experience

Clay-Wolkins Fellowship Research Assistant *Claremont, CA*

HARVEY MUDD COLLEGE *May 2022 - Present*

- Automated testing of processor functionality for OpenHWGroup's processor CVW-Wally using SystemVerilog testbenches and python.
- Modified existing scripts and testbenches to allow for easier testing of the Linux boot process.
- Worked on the AHBLite bus as well as peripheral tests for open source microprocessor CVW-Wally.
- Rebuilt AHBLite bus' finite-state machine to implement burst mode, resulting in a 2% performance increase.
- Designed tests for a GPIO, PLIC, and UART in RISC-V Assembly and implemented them in SV testbenches to verify processor functionality.

Digital Design Intern *Claremont, CA*

QUALCOMM *Aug. 2023 - Present*

- Worked with a team to analyze RTL projects to determine when a project will cause problems in logic synthesis.
- Wrote wrapper script to perform synthesis with Synopsys Design Compiler for RTL Projects to analyze synthesis performance.
- Synthesized projects using yosys to create AND-Inverter graphs in the AIGER format for analysis in Python.
- Used Python to analyze AND-Inverter Graphs for parameters identified to cause synthesis issues such as high logical effort.

R&D Intern *Westwood, CA*

SILVUS TECHNOLOGIES *Jun. 2023 - Aug. 2023*

- Characterized the frequency response of an embedded radio using an RF Testbench controlled via MATLAB using VISA commands
- Built a parser for Synopsys netlists using Python, speeding up detection of transistor issues and saving hundreds of hours of manual searching.
- Used existing codebase to automate phase calibration of multi-antenna high-speed embedded radios.

Machine Learning Intern *Claremont, CA*

TESLA *Jan. 2023 - May 2023*

- Used Python to analyze a large dataset of manufacturing test failures to predict failure causes with 78% accuracy
- Wrote Python scripts using RegEx to feature engineer an existing database into a csv for ML methods.
- Delivered framework for testing and training models based on Tesla's database

Skills

SystemVerilog, Python, C, Assembly, MATLAB, Regex, Analog Circuit Design, SPICE, KiCAD, Synopsys Design Compiler, Design Verification, VLSI Design, Linux, Bash, TCL, git, Excel, Word

Personal Projects

2024	**Home Media Server**, Docker, Docker Compose, Linux
2023	**FPGA Graphics Card**, SystemVerilog, Breadboarding
2023	**BJT Op-Amp**, SPICE, Breadboarding, Analog Design
2022	**Autonomous Underwater Robot**, Arduino, Systems Engineering
2022	**64-bit Floating-Point Multiply-Accumulate**, SystemVerilog, IEEE-754

Other Experience

Humans vs Zombies *Claremont, CA*

HEAD MODERATOR FOR HUMANS VS ZOMBIES *Feb. 2022 - Present*

- Ran semesterly week-long games of infection tag for hundreds of students.
- Led moderation team to write stories and missions for each game
- Negotiated with administration to ensure the game will not disrupt other events