Kaitlin Lucio

Electrical and Computer Engineer

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Education

Harvey Mudd College *Claremont, CA*

B.S. in Engineering *Aug 2019 - Dec. 2024*

GPA: 3.057

Work Experience

Firmware Engineer *Redmond, WA*

Second Order Effects *Feb. 2025 - Present*

- Worked with other engineers to design and execute a FPGA to convert unorthrodox LVDS image data to MIPI CPI for use on a star tracker.
- Led embedded team effort to adopt UVM testbenches for robust pre-hardware testing of SystemVerilog designs on various projects.
- Created a test system to log USB dropouts and replicate test conditions to debug a statistical EMI failure caused by a high voltage electromagnetic coilhead.
- Repurposed phased speaker array originally meant to play directional car horns to create an interactive demo for office visitors.

Design Automation Intern *Remote*

Blue Cheetah Analog *May 2024 - Dec. 2024*

- Refactored existing SystemVerilog files into an internal YAML format influenced by IP-XACT, enabling rapid reuse of IP across projects.
- Developed generator to generate addressing logic in SystemVerilog from a file definition to route APB bus signals based on addresses.
- Added functionality that added internal signals and logic operations to a Python tool that generates SystemVerilog from a YAML file.
- Increased productivity by adding simulation options for coverage, analog designs, and waveform viewing to existing automation tools.
- Refactored Pytest-BDD testing directory to enhance readability, modularity, and flexibility when adding or debugging tests.

Clay-Wolkins Research Assistant *Claremont, CA*

Harvey Mudd College *May 2022 - Present*

- Rebuilt AHBLite bus' finite-state machine to implement burst mode, resulting in a 2% performance increase.
- Designed tests for a GPIO, PLIC, and UART in RISC-V Assembly for implementation in testbenches to verify processor functionality.
- Automated nightly regressions of processor functionality using git and Python for OpenHWGroup's processor CVW-Wally using Linux commands
- Maintained buildroot creation, regression, and traced down bugs in the buildroot process caused by bad interrupts and address failures.

Digital Design Clinic Team *Claremont, CA*

Qualcomm Capstone *Aug. 2023 - May 2024*

- Worked with a team of five students to analyze RTL projects to determine when a design would fail to close PPA constraints in logic synthesis.
- Generated AND-Inverter graphs using the open source CAD tool Yosys/ABC to extract features correlated with reactivity to synthesis constraints.
- Analyzed and extracted features from generated graphs in Python to predict when a design might react a lot to different PPA constraints.
- Developed an optimized custom implementation of DAG topological sort to determine top-level source nodes for any given node in the graph, speeding up analysis by a factor of 100x.
- Predicted module reactivity to PPA constraints during synthesis of HDL modules with an accuracy of 89%.

Skills

Programming & Computer Languages: SystemVerilog, C, Assembly, Python, MatLAB, Linux, TCL, Bash, git

CAD Programs: LTSpice, Synopsys Design Compiler, ModelSim, Verilator

Projects

OpenSUSE Webserver *OpenSUSE Leap 15.6*

Home Improvement *Jan 2024 - Present*

- Wrote and implemented docker compose files to host various gaming servers, websites, and files from a local machine.
- Designed and built a simple mini-ITX computer to satisfy low power consumption requirements while remaining fast enough to game on.
- Implemented Apache reverse proxies through HTTPS through DuckDNS to serve servers and webpages over the internet.
- Enabled Hardware accelerated transcoding in docker containers by exposing AMD's Linux drivers as files in the docker container.

Graphics Card Digital Designer *Claremont, CA*

Harvey Mudd College *November 2024 - December 2024*

- Created block-level system schematic with another student for an 1-bit color 32x24 graphics driver over VGA to play snake with a displayed score.
- Wrote SystemVerilog RTL to implement block-level design and test functionality through the use of testbenches.
- Wrote Python scripts to generate a sweep of testvectors in binary format for pre-silicon design verification.
- Used an oscilloscope to verify correctness of HSync and VSync traces when monitor failed to recognize VGA signal.
- Integrated an MCU to write pixel colors, locations, and score via five different 8-bit packets transmitted via an SPI connection.
- Displayed snake on a VGA monitor during a demo day, allowing other students to play a 30x22 grid of snake using a simple 5 button controller.