Kaitlin **Lucio**

Electrical Engineer

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Education

Harvey Mudd College — *Claremont, CA*

B.S. in Engineering — *Aug 2019 - Dec. 2024*

Work Experience

Harvey Mudd College — *Claremont, CA*

Clay-Wolkins Fellowship VLSI Research — *Mar. 2024 - Present*

- Automated recurring design verification and performance verification for OpenHWGroup's processor CVW-Wally using Systemverilog testbenches and python.

Qualcomm through Harvey Mudd College — *Claremont, CA*

Qualcomm VLSI Engineer — *Aug. 2024 - Present*

- Worked with a team to analyze RTL projects to determine when a project will cause problems in logic synthesis.
- Wrote wrapper script to perform synthesis with Synopsys Design Compiler for RTL Projects to analyze synthesis performance.
- Synthesized projects using yosys to create AND-Inverter graphs in the AIGER format for analysis in Python.
- Used Python to analyze AND-Inverter Graphs for parameters identified to cause synthesis issues such as high logical effort.

Silvus Technologies — *Westwood, CA*

R&D Intern — *Jun. 2024 - Aug. 2024*

- Characterized the frequency response of a complex embedded radio using an RF Testbench controlled via MATLAB using VISA commands to validate design
- Built a parser for DC Synopsys files using Python, speeding up detection of transistor issues, reducing the chance of signal skew in manufacturing.
- Used existing codebase to automate phase calibration of multi-antenna high-speed embedded radios.

Tesla through Harvey Mudd College — *Claremont, CA*

Tesla ML Engineer — *Jan. 2023 - May 2023*

- Developed a Machine Learning algorithm using Python to analyze a large dataset of car test successes and failures to determine which connector is causing issues.
- Wrote Python scripts using REGEX to feature engineer an existing database into a csv for ML methods.
- Automated sweeps of different parameters for ML models to determine the best model for Tesla's dataset.

Harvey Mudd College — *Claremont, CA*

Clay-Wolkins Fellowship VLSI Research — *May 2022 - Jul. 2022*

- Worked on the AHBLite bus as well as peripheral tests for open source microprocessor CVW-Wally.
- Rebuilt AHBLite bus' finite-state machine to implement burst mode, resulting in a 2% performance increase.
- Designed verification tests for GPIO, PLIC, and UART in RISC-V Assembly and implemented them to verify processor functionality using SystemVerilog testbenches.
- Handled daily design verification using existing infrastructure to ensure the processor would remain functional for testing.

skills

Python, SystemVerilog, Assembly, MATLAB, German, SPICE, Design Verification, Linux, git, Synopsys Design Compiler

Personal Projects

2024 **Home Media Server**, Docker, Docker Compose, Linux

2023 **FPGA Graphics Card**, SystemVerilog, Breadboarding

2023 **BJT Op-Amp**, SPICE, Breadboarding

2023 **Autonomous Robot**, Arduino, Systems Engineering

2022 **64-bit Floating-Point Multiply-Accumulate**, SystemVerilog, IEEE-754

Certificates

2019 **A2 German Certification**, Goethe-Institut