[redacted]

Electrical and Computer Engineer

[redacted]

Education

[redacted]

B.S. in Engineering — *Aug 2019 - Dec. 2024*

GPA: 3.057

Work Experience

Design Automation Intern — [redacted]

[redacted] — *May 2024 - Present*

- Refactored existing SystemVerilog files into an internal YAML format influenced by IP-XACT, enabling rapid reuse of IP across projects.
- Added wire and always block statement capability to an internal YAML to SystemVerilog generator tool.
- Increased developer productivity by adding features for coverage, analog designs, and waveform viewing to existing CAD automation tools.
- Developed generator to generate addressing logic in SystemVerilog from a file definition to route APB bus signals based on addresses.
- Refactored Pytest-BDD testing directory to enhance readability, modularity, and flexibility in testing, pre-commit, and CI/CD.

Clay-Wolkins Research Assistant — [redacted]

[redacted] — *May 2022 - Present*

- Automated nightly regressions of processor functionality using git and Python for OpenHWGroup's processor CVW-Wally using Linux commands
- Modified existing scripts and testbenches to allow for automated testing of the Linux boot process.
- Maintained buildroot creation, regression, and traced down bugs in the buildroot process caused by bad interrupts and address failures.
- Rebuilt AHBLite bus' finite-state machine to implement burst mode, resulting in a 2% performance increase.
- Designed tests for a GPIO, PLIC, and UART in RISC-V Assembly for implementation in testbenches to verify processor functionality.

Digital Design Co-op — [redacted]

[redacted] — *Aug. 2023 - May 2024*

- Worked with a team of four students to analyze RTL projects to determine when an RTL design caused extra processing effort in logic synthesis.
- Wrote a wrapper script using Bash and TCL to perform synthesis through Synopsys Design Compiler.
- Automated Yosys synthesis using Bash and TCL to generate AND-Inverter graphs to extract parameters that determine synthesis performance.
- Utilized Python to analyze AIGs for use in a Machine Learning pipeline to detect whether a design would cause extra processing effort.
- Developed a speed-optimized custom implementation of DAG topological sort in Python to determine where nodes were sourced from.

R&D Intern — [redacted]

[redacted] — *Jun. 2023 - Aug. 2023*

- Developed a custom RF testbench using Python and MATLAB to characterize radio frequency response bands.
- Designed from the ground up a netlist parser to create graphs out of transistor designs, speeding up detection of transistors causing clock skew.
- Automated phase calibration of multi-antenna radios using an RF testbench, allowing for production of phase-calibrated radios.

Skills

Programming & Computer Languages: SystemVerilog, C, Assembly, Python, MatLAB, Linux, TCL, Bash, git

CAD Programs: KiCad, LTSpice, Synopsys Design Compiler, ModelSim, Verilator

Projects

Graphics Card Digital Designer — [redacted]

[redacted] — *November 2024 - December 2024*

- Created block-level system schematic with another student for an 1-bit color 32x20 graphics driver over VGA to play snake on a computer monitor.
- Wrote SystemVerilog RTL to implement block-level design and test functionality through the use of testbenches.
- Wrote Python scripts to generate a sweep of testvectors in binary format for pre-silicon design verification.
- Used an oscilloscope to verify correctness of HSync and VSync traces when monitor failed to recognize VGA signal.
- Integrated an MCU to write pixel colors, locations, and score via five different 8-bit packets transmitted via an SPI connection.
- Found bug caused by lack of documentation related to Block RAM hold time constraints on iCE40UP5K.
- Developed and implemented RTL for a bitmap representation of hex numerals displayed by reading the current score and drawn pixel.
- Displayed snake on a VGA monitor during a demo day, allowing other students to play a 30x18 grid of snake using a simple 5 button controller.

Other Experience

Head Moderator — [redacted]

Humans vs Zombies — *Feb. 2022 - Present*

- Ran semesterly week-long games of infection tag to bring joy to hundreds of students' lives.
- Led moderation team to write stories and missions and move objects required for the game to event locations.
- Negotiated with college administration to ensure the game would not disrupt other events to promote a fun environment on campus.