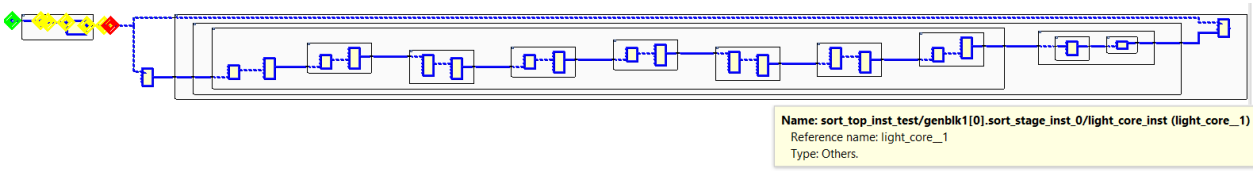
sort_max			
Strategy implementation: **Performance_Explore**			
frequency: ***f* = 500 MHz**			
N = 7, M = 32 (*photo 1, 2*)			
Utilization			
LUT	25070	W = 32	
FF	7628		
LUT_inst	788 (1 stage)		
Timing Summary			
Setup		Hold	
WNS	-13,668	WHS	0,041
TNS	-73347,132	THS	0
N = 8, M = 16 (*photo 3, 4*)			
Utilization			
LUT	7004		
FF	2314		
LUT_inst	459 (1 stage)		
Timing Summary			
Setup		Hold	
WNS	-8,186	WHS	0,621
TNS	-14498,413	THS	0
	N = 9, M = 8 (*photo 5, 6*)		
Utilization			
LUT	1974		
FF	736		
LUT_inst	260 (1 stage)		
Timing Summary			
Setup		Hold	
WNS	-6,025	WHS	0,621
TNS	-3138,786	THS	0
N = 16, M = 64 (*photo 7, 8*)			
Utilization			
LUT			
FF			
LUT_inst			
Timing Summary			
Setup		Hold	
WNS		WHS	
TNS		THS	

sort_min			
Strategy implementation: **Performance_Explore**			
frequency: ***f* = 500 MHz**			
N = 7, M = 32, W = 32 (*photo 1, 2*)			
Utilization			
LUT	25127		
FF	7627		
LUT_inst	671 (1 stage)		
Timing Summary			
Setup		Hold	
WNS	-12,579	WHS	0,035
TNS	-69636,533	THS	0
N = 8, M = 16, W = 16 (*photo 3, 4*)			
Utilization			
LUT	7034		
FF	2316		
LUT_inst	375 (1 stage)		
Timing Summary			
Setup		Hold	
WNS	-8,245	WHS	0,043
TNS	-14671,142	THS	0
	N = 9, M = 8, W = 8 (*photo 5, 6*)		
Utilization			
LUT	2214		
FF	807		
LUT_inst	256 (1 stage)		
Timing Summary			
Setup		Hold	
WNS	-5,629	WHS	0,042
TNS	-3231,633	THS	0
N = 16, M = 64 (*photo 7, 8*)			
Utilization			
LUT			
FF			
LUT_inst			
Timing Summary			
Setup		Hold	
WNS		WHS	
TNS		THS	



Tcl Console | Messages | Log | Reports | Design Runs | DRC | Methodology | Power | Timing

Intra-Clock Paths - clk - Setup

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Methodology Summary (800)
- Check Timing (145)
- Intra-Clock Paths
  - clk
    - Setup -3,375 ns (10)

	Slack	Levels	High Fa...	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clo
4	-3.371	21	20	sort_top_inst_test...ff_reg[5][0][7]/C	sort_top_inst_tes..._y_q_reg[6][7]/D	5.238	1.995	3.243	2.0	clk
5	-3.362	22	13	i_chi_ff_reg[2][7]/C	sort_top_inst_tes..._y_q_reg[0][2]/D	5.234	2.252	2.982	2.0	clk
6	-3.360	21	16	sort_top_inst_tes...][7]_replica_1/C	sort_top_inst_tes..._y_q_reg[3][4]/D	5.297	2.266	3.031	2.0	clk
7	-3.358	18	16	i_chi_ff_reg[2][7]/C	sort_top_inst_tes...f_reg[0][4][7]/D	5.139	1.899	3.240	2.0	clk
8	-3.356	19	10	i_chi_ff_reg[2][7]/C	sort_top_inst_tes...f_reg[0][8][7]/D	5.183	1.917	3.266	2.0	clk
9	-3.356	21	16	sort_top_inst_test...ff_reg[1][2][7]/C	sort_top_inst_tes..._y_q_reg[2][2]/D	5.257	2.297	2.960	2.0	clk
10	-3.356	21	16	sort_top_inst_test...ff_reg[1][2][7]/C	sort_top_inst_tes..._y_q_reg[2][5]/D	5.251	2.419	2.832	2.0	clk

Timing Summary - impl_1 (saved)