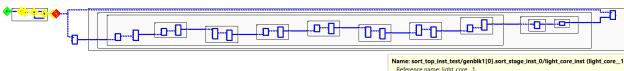
	sort_	max					
Strategy implem Performance_I							
	frequency: f	= 500 MHz					
	N = 7, M = 32	2 (photo 1, 2)					
	Utiliz	ation					
LUT	25070						
FF	7628						
LUT_inst	788 (1 stage)						
	Timing S						
	Setup	Но					
WNS	-13,668	WHS	0,041				
TNS	-73347,132	THS	0				
	N = 8, M = 16	¥ ' /					
LITT	Utiliz	atıon					
LUT		7004					
FF	2314						
LUT_inst	459 (1 stage)						
	Timing S		1.1				
WINIC	Setup	Hold					
WNS TNS	-8,186 -14498,413	WHS THS	0,621				
1110	N = 9, M = 8 (U				
	Utiliz	* '					
IIIT	1974	auon					
LUT FF	736						
LUT_inst	260 (1 stage)						
LO 1_mst	Timing S	ummary					
	Setup Timing S	Но	old				
WNS	-6,025	WHS	0,621				
TNS	-3138,786	THS	0				
	N = 16, M = 6						
	Utiliz						
LUT							
FF							
LUT_inst							
	Timing S	ummary					
	Setup	Но	old				
WNS		WHS					
TNS		THS					

	sort_	_min							
Strategy impler	nentation:								
Performance_	Explore								
	frequency: f	= 500 MHz							
	N = 7, M = 32, W	= 32 (photo 9, 10)							
	Utiliz	<u> </u>							
LUT	25127								
FF	7627								
LUT_inst	671 (1 stage)								
	Timing S	ummary							
	Setup	Hold							
WNS	-12,579	WHS	0,035						
TNS	-69636,533	THS	0						
	N = 8, M = 16, W =	= 16 (<i>photo 11, 12</i>)							
	Utiliz	ation							
LUT	7034								
FF	2316								
LUT_inst	375 (1 stage)								
	Timing S	ummary							
	Setup	Hold							
WNS	-8,245	WHS	0,043						
TNS	-14671,142	THS	0						
	N = 9, M = 8, W =	8 (photo 13, 14)							
	Utiliz	ation							
LUT	2214								
FF	807								
LUT_inst	256 (1 stage)								
	Timing S	ummary							
	Setup	Hold							
WNS	-5,629	WHS	0,042						
TNS	-3231,633	THS	0						
	N = 16, M = 64	(photo 15, 16)							
	Utiliz	ation							
LUT									
FF									
LUT_inst									
	Timing S								
	Setup	Hole	d						
WNS		WHS							
TNS		THS							



Name: sort_top_inst_test/genblk1[0].sort_stage_inst_0/light_core_inst (light_core_1)
Reference name: light_core_1
Type: Others.

cl Console Messages Log F	Reports	Design Runs	DRC	Methodo	logy Power Timing ×						? _ 🗆
Q 🛨 💠 🕕		a - 🗷	\$ _	M O	Intra-Clock Paths - clk - Setup						
General Information	^	Slack ^1	Levels	High Fa	From	То	Total Delay	Logic Delay	Net Delay	Requirement	Source CI
Timer Settings	4	-3.371	21	20	sort_top_inst_testff_reg[5][0][7]/C	sort_top_inst_tesy_q_reg[6][7]/D	5.238	1.995	3.243	2.0	clk
Design Timing Summary	5	-3.362	22	13	i_chi_ff_reg[2][7]/C	sort_top_inst_tesy_q_reg[0][2]/D	5.234	2.252	2.982	2.0	clk
Clock Summary (1)	6	-3.360	21	16	sort_top_inst_tes][7]_replica_1/C	sort_top_inst_tesy_q_reg[3][4]/D	5.297	2.266	3.031	2.0	clk
Methodology Summary (800)	7	-3.358	18	16	i_chi_ff_reg[2][7]/C	sort_top_inst_tesf_reg[0][4][7]/D	5.139	1.899	3.240	2.0	clk
General Check Timing (145)	8	-3.356	19	10	i_chi_ff_reg[2][7]/C	sort_top_inst_tesf_reg[0][8][7]/D	5.183	1.917	3.266	2.0	clk
■ Intra-Clock Paths	9	-3.356	21	16	sort_top_inst_testff_reg[1][2][7]/C	sort_top_inst_tesy_q_reg[2][2]/D	5.257	2.297	2.960	2.0	clk
∨ 庙 clk	10	-3.356	21	16	sort_top_inst_testff_reg[1][2][7]/C	sort_top_inst_tesy_q_reg[2][5]/D	5.251	2,419	2.832	2.0	clk
Setup -3,375 ns (10)	v <										1