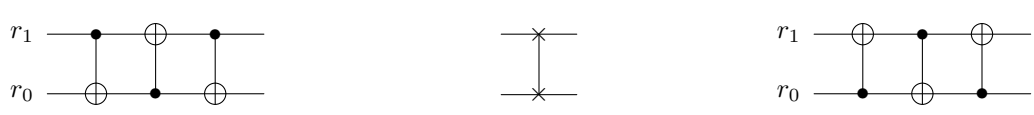
Due to the limitations of the connectivity of many processors we often require a process of moving qubits across a processor. To complete this information movement we select a *path* of nearest-neighbour connected registers $|\alpha_n\alpha_{n-1}\cdots\alpha_0\rangle$ and evolve to system where the state of α_0 moves to the most significant bit location $|\alpha_0\cdots\rangle$. In the general case we denote this process as a *transfer* of α_0. Due to the constraints of quantum processors we discuss patterns which accomplish reversible nearest-neighbour state transfer (transfer patterns). In a given path we define the least significant register as the source register and the most significant register as the destination register. We wish that the state in the source register be moved into the destination register to achieve transfer.

We also discuss patterns which accomplish reversible nearest-neighbour circular shift (shift patterns). A shift pattern evolves the state $|\alpha_n\alpha_{n-1}\cdots\alpha_0\rangle$ to $|\alpha_0\alpha_n\cdots\alpha_1\rangle$. We denote the states along the path by α and emphasize state α_0 being transferred as ψ.

The conventional method of moving qubits around a processor is through swapping physical qubits until a logical qubit (the state being transferred) has moved to the desired physical position. The $SWAP$ gate can be constructed from $CNOT$ gates as shown in Figure 1. There are two logically identical patterns for this decomposition which we label Up and Down. Swap-Up and Swap-Down are distinct patterns when relative to a path such as r_0, r_1. We can perform a series of swap operations to move a logical qubit within a processor.

Figure 1: $SWAP$ decomposition.

(a) $SWAP$ decomposed into Swap-Up. (b) $SWAP$ gate. (c) $SWAP$ decomposed into Swap-Down.

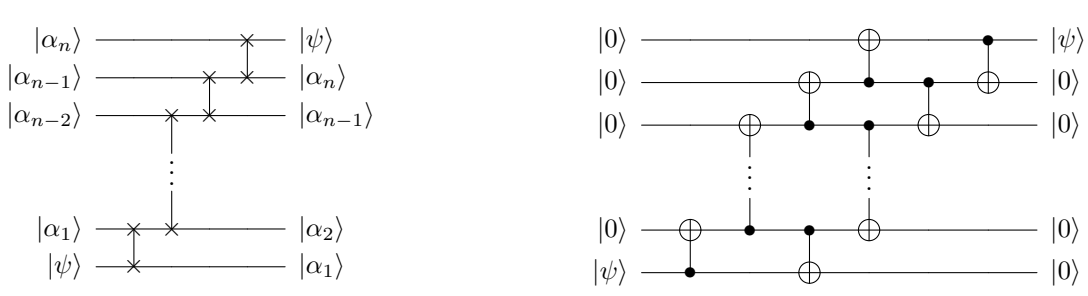


For any given path with n connections, we can simplify our shift operation when all of the states on the path are known to be $|0\rangle$. As shown in Figure 2(a) the standard shift path has a depth of $3n$ but we can construct a Z-Transfer pattern as shown in Figure 2(b), which only has a depth of $n+2$, for $n>1$. As error builds up in the system, the assumption that the states along the path are in position $|0\rangle$ will be less likely to be true. Error is propagated in each step of the Z-Transfer pattern, resulting in the destination qubit being set to the state of $\psi\oplus e$, where e is the error in the path. As such, the Z-Transfer pattern should be avoided when the path is known to be noisy.

Each of the patterns in Figure 2 and 3 have acceptable Up and Down versions with the exception of the Z-Transfer pattern as Z-Transfer-Up would propagate the source qubit along the length of the path. With the exception of Z-Transfer, we denote either of the Up or Down patterns variants when the variant is not specified. The Up variations of all the patterns can be obtained from the Down variations by inverting the direction of all $CNOT$ gates in the patterns. S-Shift-Down is defined by Figure 2(a) where each of the $SWAP$ gates are implemented by the Swap-Down pattern.

Figure 2: Shift and transfer patterns.

(a) Standard shift pattern (S-Shift). (b) Transfer pattern (Z-Transfer) with zeroed values of α.



(c) Garbage transfer pattern (G-Transfer-Down).

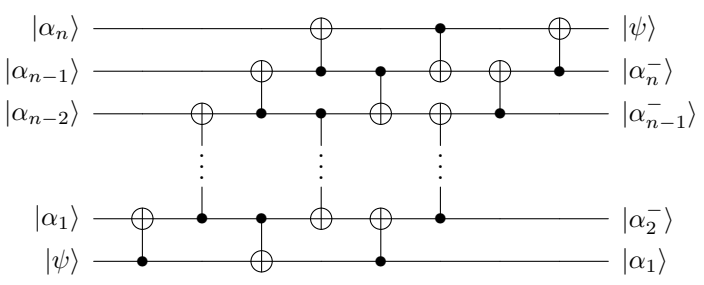


Figure 2(c) shows how to construct the garbage transfer (G-Transfer) pattern. In some cases we may generate *garbage qubits* which cannot be measured without interfering with the state of other qubits and have no further use in our circuit. Because we do not care if we change the state of garbage qubits, we can perform this additional optimization. When the qubits along the path are in a zeroed state then the G-Transfer pattern behaves like the Z-Transfer pattern.

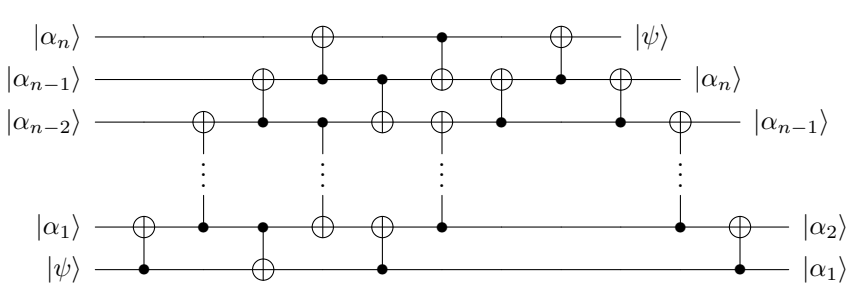
It may be useful to distinguish G-Transfer-Down and G-Transfer-Up by which logical qubits they maintain. The Down variant maintains α_1 whereas the Up variant maintains α_n. Depending on the conditions of the circuit and considering how error is propagated along the path one variant may be more desirable than the other.

In Figure 3(a) we can perform a cleanup operation on our G-Transfer pattern in order to perform a shift operation in reduced time. This cleanup reduced depth shift (C-Reduced) pattern completes in $2n+3$ time with our destination qubit being ready after only $n+4$ steps, for $n>1$. This comes at a cost of an additional $n-1$ total $CNOT$ gates.

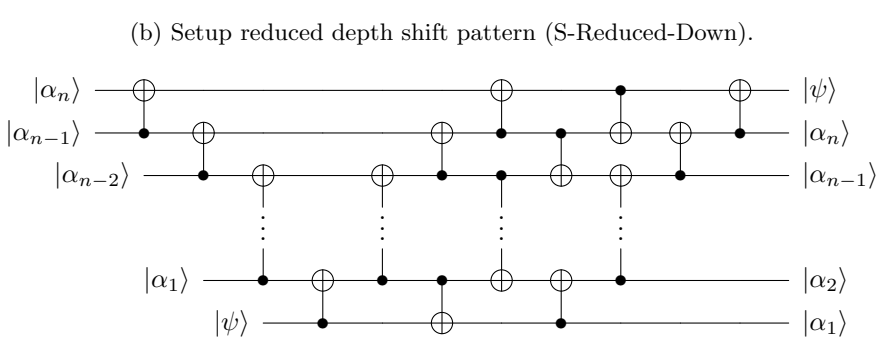
In some cases when we want to transfer a state between two ends of a processor, the registers at the destination of the path may be ready to perform computational work before the state ψ is ready. In this case we can perform a setup operation to prepare the path instead of the cleanup operation. This setup reduced shift (S-Reduced) pattern is shown in Figure 3(b).

Figure 3: Reduced depth shift patterns.

(a) Cleanup reduced depth shift pattern (C-Reduced-Down).



(b) Setup reduced depth shift pattern (S-Reduced-Down).



If we care most about the depth of the shifting circuit as n becomes large then we can combine S-Reduced and C-Reduced to achieve circular shift with a depth of $n+8$. If we use C-Reduced-Down and S-Reduced-Up (DUT-Reduced) or C-Reduced-Up and S-Reduced-Down (UDT-Reduced) we can perform the $CNOT$ following the setup of S-Reduced before the $CNOT$ preceding the cleanup of C-Reduced achieving circular shift with a depth of $n+6$ as shown in Figure 4. UDT-Reduced can be obtained from DUT-Reduced by reversing the direction of all the $CNOT$ gates. k indicates the transition qubit in the pattern. In practice we search for a value of k which minimizes the total depth of the circuit. We choose a smaller k when we want the cleanup step to be finished earlier or we choose a larger k when we want the setup step to start later. We denote either of the patterns DUT-Reduced or UDT-Reduced by T-Reduced.

Figure 4: Down-Up transition reduced depth shift pattern (DUT-Reduced).

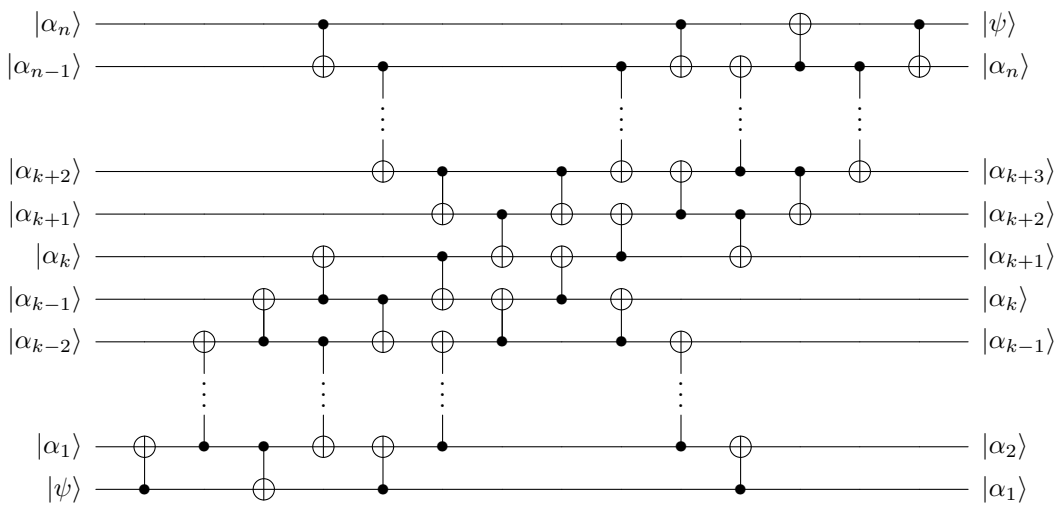


Table 1: Properties of shift and transfer patterns.

	S-Shift	C-Reduced	S-Reduced	T-Reduced	Z-Transfer	G-Transfer
Circuit depth	$3n$	$2n+3$	$2n+3$	$n+6$	$n+2$	$n+4$
$CNOT$ total	$3n$	$4n-1$	$4n-1$	$4n-2$	$2n$	$3n$
Dest. ready time	$3n$	$n+4$	$2n+3$	$n+6$	$n+2$	$n+4$
Source start time	0	0	n	0	0	0
Logical states of path	Maintained	Maintained	Maintained	Maintained	Zeroed	Garbage xor Zeroed

n is the number of connections in the path and $n>2$.
Where $k=\lfloor\frac{n}{2}\rfloor$.