ECSE 444
Timers

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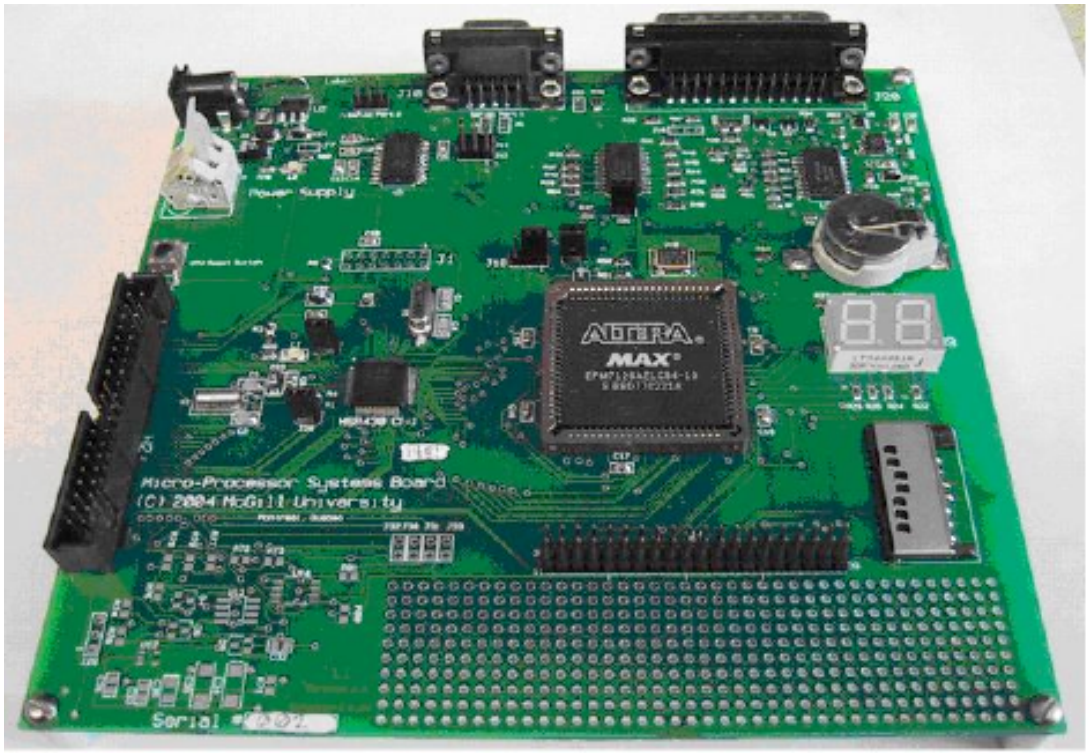

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Acknowledgments: to STMicroelectronics for material on processors and the board

Outline

- Timers
  - Basics, principles of operation
  - Modes of use
- Lab: Part 2 of Lab 2
  - Finalizing Experiments, Code
- Lab 3 Incoming
- Quiz 2 on March 7th

Timers

GENERAL PURPOSE TIMERS (TIM)

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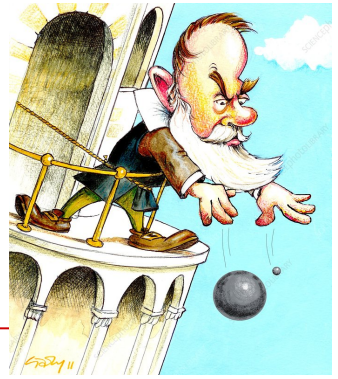
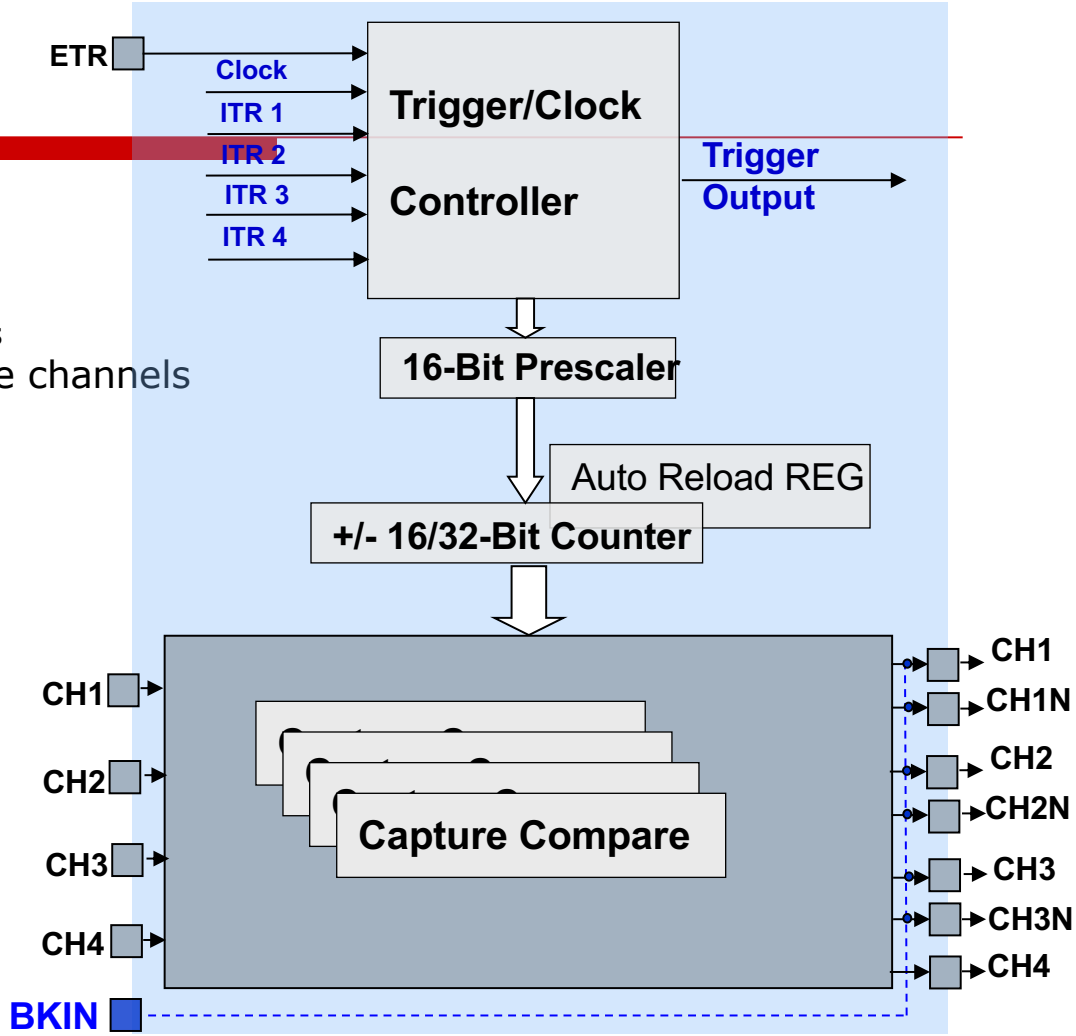
Why Timers?



- Timepieces, counters, original "processors"
  - Sequencing ops (e.g., laundry machines), control (electrical engines), waveforms (TVs)
  - Celebrated physics experiments (e.g., tower of Pisa)
  - Sophisticated sensors (e.g., LIDAR, TOF); other advanced applications
- Offload processor and other blocks
- Ties well with the rest of embedded cores
  - Interrupts, DMA, ADC, DAC, sensors, actuators, …

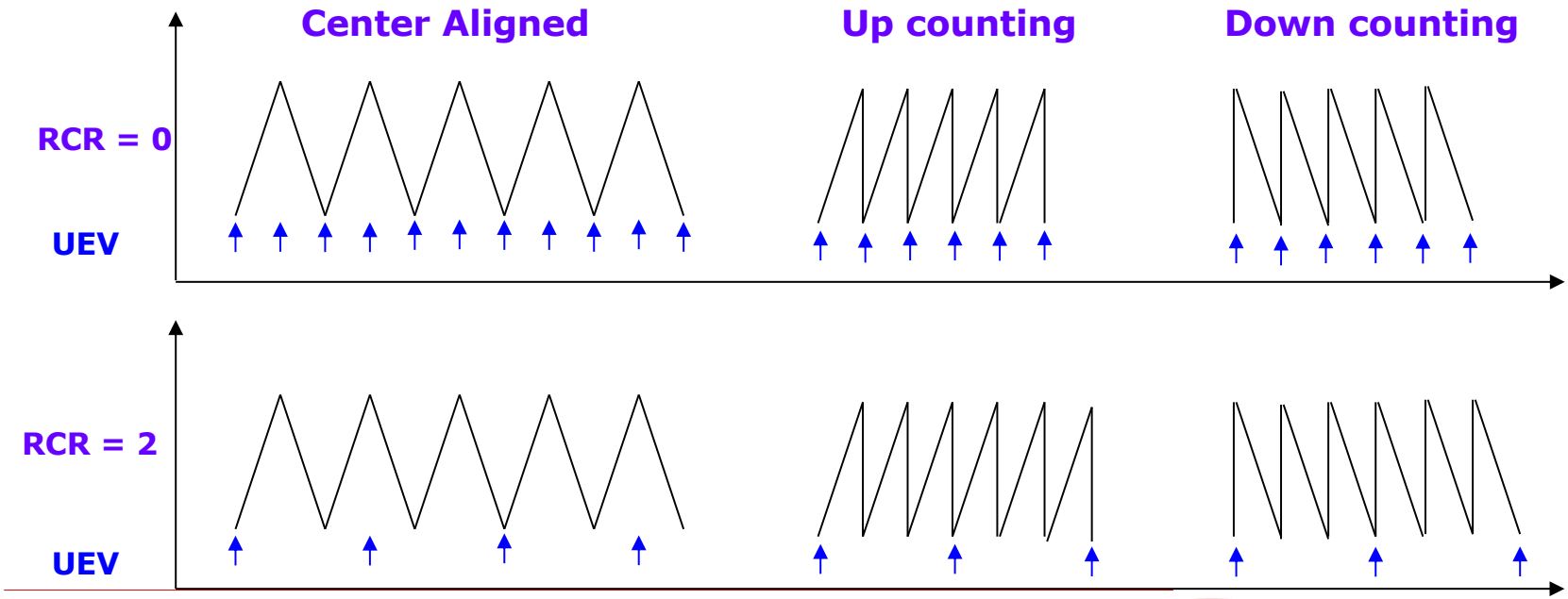
Timer Features

- General Purpose Timer
- 16/32-bit Counters
  - Auto Reload
  - Up, down and centered counting modes
- 4x 16 High resolution Capture Compare channels
  - Programmable direction of the channel: input/output
  - Output Compare: Toggle, PWM
  - Input Capture
  - PWM Input Capture
- Synchronization
- Up to 8 IT/DMA Requests
- Motor Control Specific Feature
- OC Signal Management
  - 6 Complementary outputs
  - Dead-time management
  - Repetition Unit
- Encoder Interface
- Hall sensor Interface
- Embedded Safety features
  - Break sources: BKIN pin/ CSS
  - Lockable unit configuration



Counter Modes

- Three counter modes:
  - **Up counting mode**
  - **Down counting mode**
  - **Center-aligned mode**
- When using the Repetition Counter (case of TIM1 and TIM8 only)



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Timer Features Overview (1/2)

	Counter resolution	Counter type	Prescaler factor	DMA	Capture Compare Channels	Complementary output	Synchronization	
							Master Config	Slave Config
Advanced TIM1 and TIM8	16 bit	up, down and up/down	1..65536	YES	4	3	YES	YES
General purpose (1) TIM2 and TIM5	32 bit	up, down and up/down	1..65536	YES	4	0	YES	YES
General purpose TIM3 and TIM4	16 bit	up, down and up/down	1..65536	YES	4	0	YES	YES
Basics TIM6 and TIM7	16 bit	up	1..65536	YES	0	0	YES	NO
General Purpose TIM15, TIM16 and TIM17	16 bit	up	1..65536	YES	2/1/1	1	YES(OC signal)	NO
Low-Power LPTIM	16 bit	up	1..65536	NO	2	0	NO	YES

Timer Features Overview 2/2

	Counter clock source	Output Compare	PWM	Input Capture	PWMI	OPM	Encoder interface	Hall sensor interface	XOR Input
Advanced TIM1 and TIM8	-Internal clock APB2 -External clock: ETR/TI1/TI2/TI3/TI4 pins -Internal Trigger: ITR1/ITR2/ITR3/ITR4 -Slave mode	7 channels	7 channels	4 channels	2 channels	2 channels	Yes	Yes	Yes
General Purpose TIM2 and TIM5	-Internal clock APB1 -External clock: ETR/TI1/TI2/TI3/TI4 pins -Internal Trigger: ITR1/ITR2/ITR3/ITR4 -Slave mode	4 channels	4 channels	4 channels	2 channels	2 channels	Yes	No	Yes
General Purpose TIM3 and TIM4	-Internal clock APB1 -External clock: ETR/TI1/TI2/TI3/TI4 pins -Internal Trigger: ITR1/ITR2/ITR3/ITR4 -Slave mode	4 channels	4 channels	4 channels	2 channels	2 channels	Yes	No	Yes
Basics TIM6 and TIM7	-Internal clock APB1	No	No	No	No	No	No	No	No
General Purpose TIM15/16/1	-Internal clock APB1/APB2	1 Channel	1 Channel	1 Channel	No	No	No	No	No
Low-Power LPTIM	-Internal clock APB1/APB2 -External clock: TI1/TI2/TI3/TI4 pins -Internal Trigger: ITR1/ITR2/ITR3/ITR4 -Slave mode	2 channels	2 channels	2 channels	2 channels	2 channels	No	No	No

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Update Event

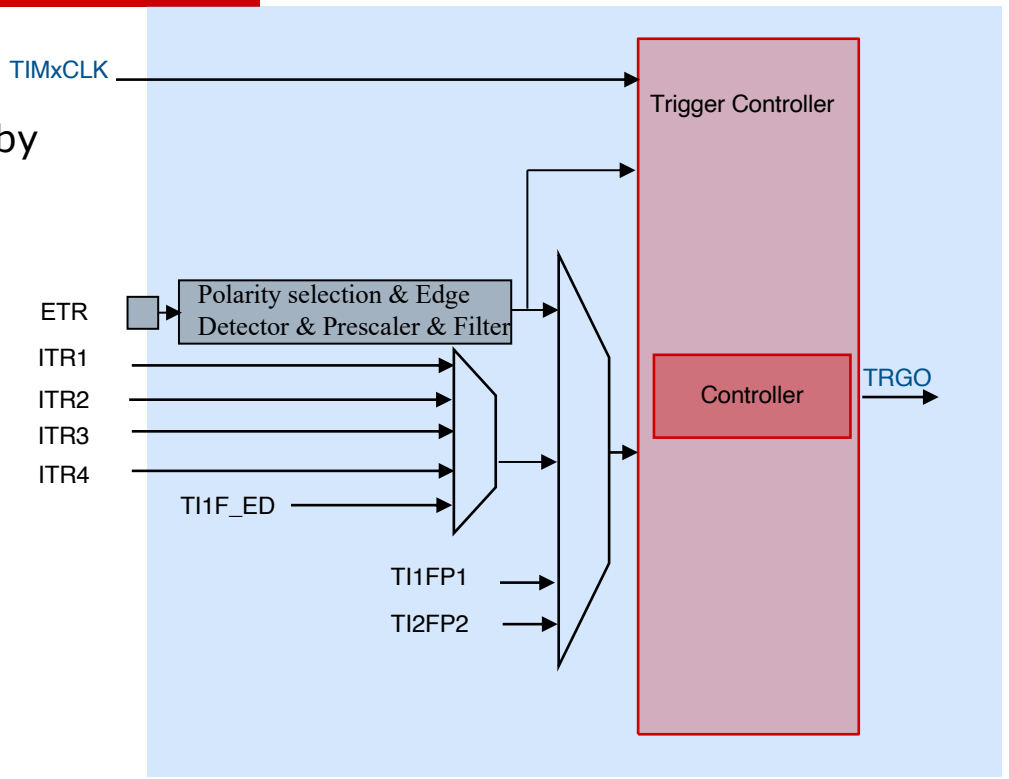
- The content of the preload register is transferred in the shadow register (depending on the auto-reload preload is enable or not):
  - Immediately
  - At each update event UEV

- The Update Event is generated:
  - when the counter reaches overflow/undeflow
  - when the Repetition counter equals to 0 (only for TIM1)
  - By software by setting the UG (Update Generation) bit

- The Update event UEV requests can be selected as follow:
  - The requests are sent only when the counter reachs the overflow/underflow.
  - The request are sent when (counter overflow/underflow or set of UG bit or update generation through the slave mode controller

Counter Clock Selection

- Clock can be selected out of 8 sources
  - Internal clock TIMxCLK provided by the RCC
  - Internal trigger input 1 to 4:
    - ITR1 / ITR2 / ITR3 / ITR4
    - Using one timer as prescaler for another timer
  - External Capture Compare pins
    - Pin 1: TI1FP1 or TI1F_ED
    - Pin 2: TI2FP2
  - External pin ETR
    - Enable/Disable bit
    - Programable polarity
    - 4 Bits External Trigger Filter
    - External Trigger Prescaler:
      - Prescaler off
      - Division by 2
      - Division by 4
      - Division by 8



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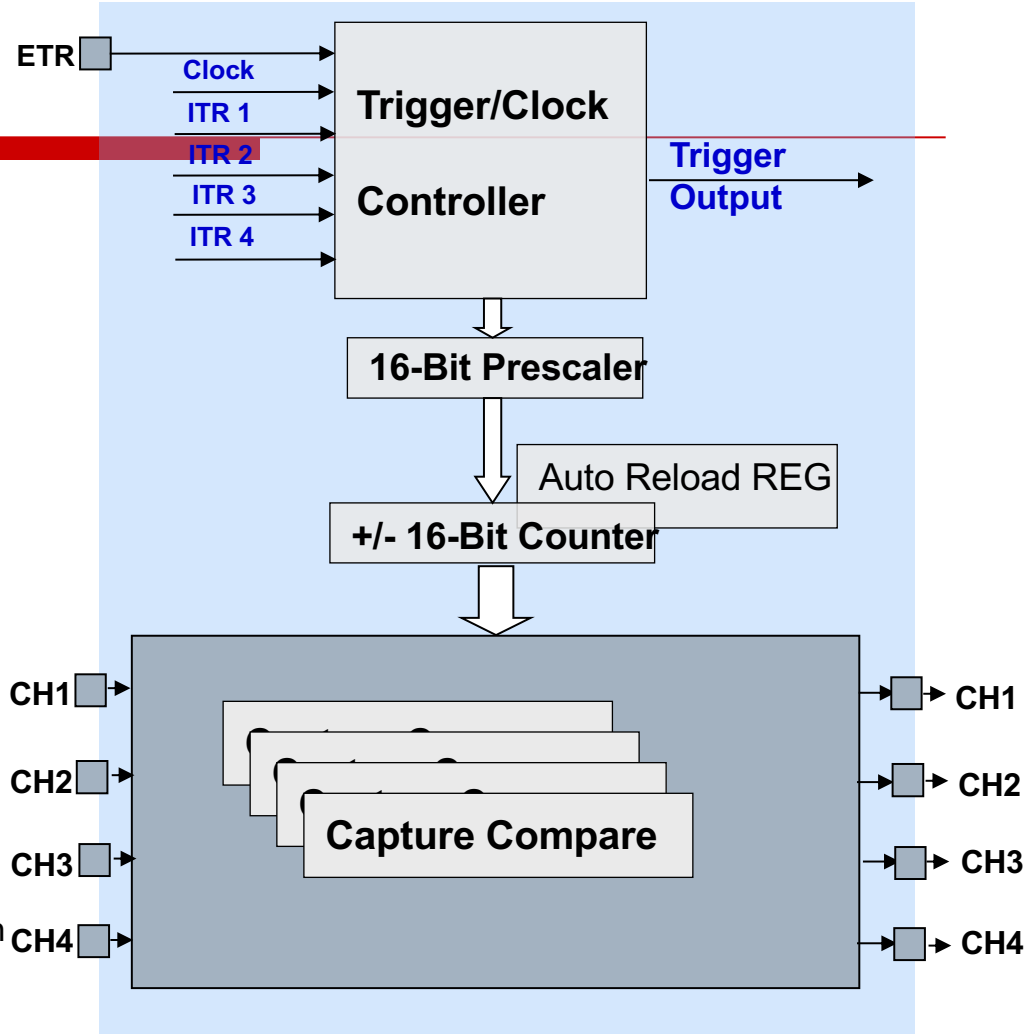
General Timer Features

- TIM2, 3, 4 and 5 on Low Speed APB (APB1)
- 16-bit Counter for TIM3 and 4
- 32-bit Counter for TIM2 and 5
  - Up, down and centered counting modes
  - Auto Reload
- 4 x 16 High resolution Capture Compare Channels
  - Programmable direction of the channel: input/output
  - Output Compare
  - PWM
  - Input Capture, PWM Input Capture
  - One Pulse Mode
- Synchronization
  - Timer Master/Slave
  - Synchronisation with external trigger
  - Triggered or gated mode
- Encoder interface
- 6 Independent IRQ/DMA Requests generation
  - At each Update Event
  - At each Capture Compare Events
  - At each Input Trigger



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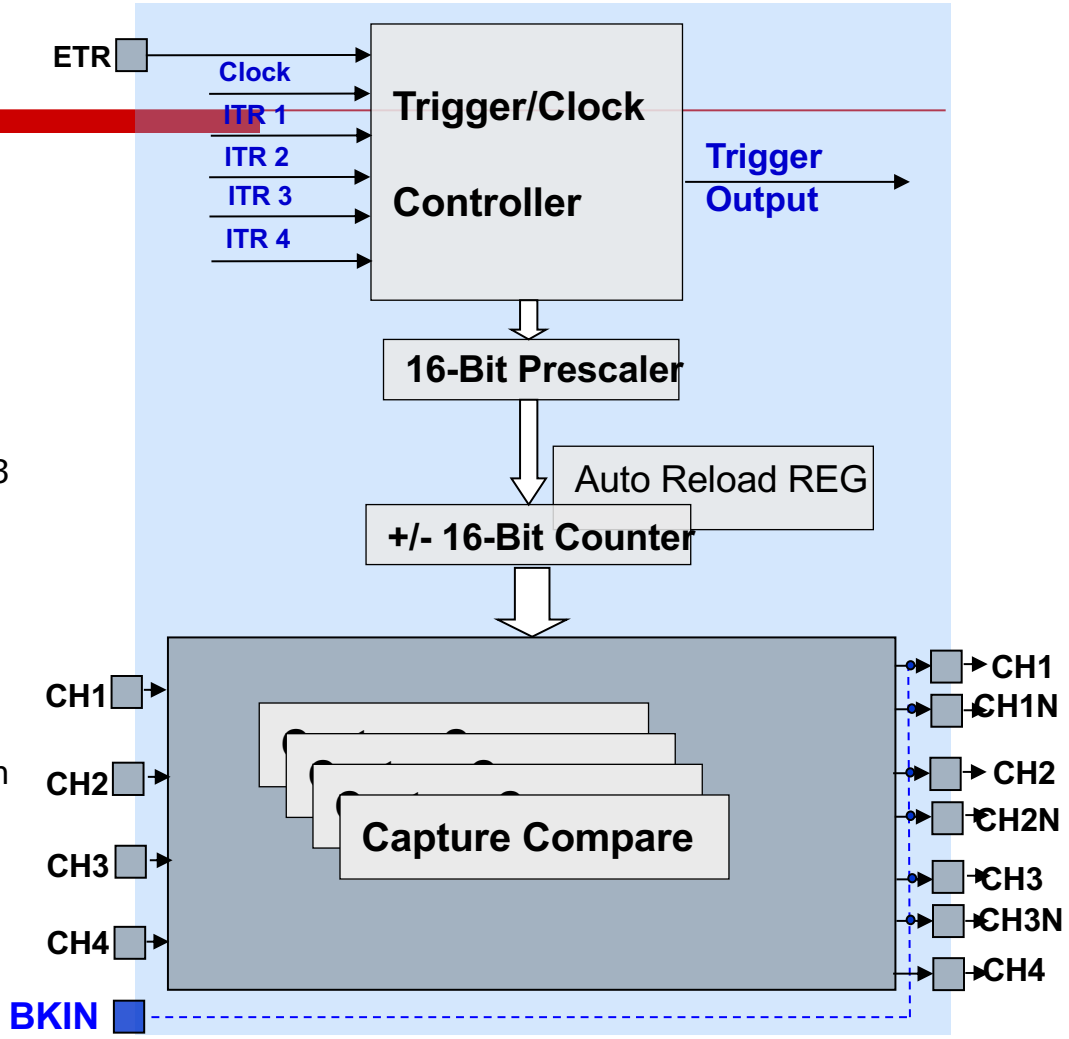
Advanced Features

- TIM1 and TIM8 on High Speed APB (APB2)
- 16-bit Counter
  - Up, down and centered counting modes
  - Auto Reload
- 4 x 16 High resolution Capture Channels
  - Output Compare
  - PWM
  - Input Capture, PWM input Capture
  - One Pulse Mode
- 6 Complementary outputs: Channel1, 2 and 3
- Output Idle state selection independently for each output
- Polarity selection independently for each output
- Programmable PWM repetition counter
- Hall sensor interface
- Encoder interface
- 8 Independent IRQ/DMA Requests Generation
  - At each Update Event
  - At each Capture Compare Events
  - At each Trigger Input Event
  - At each Break Event
  - At each Capture Compare Update
- Embedded Safety features
  - Break input
  - Lockable unit configuration: 3 levels



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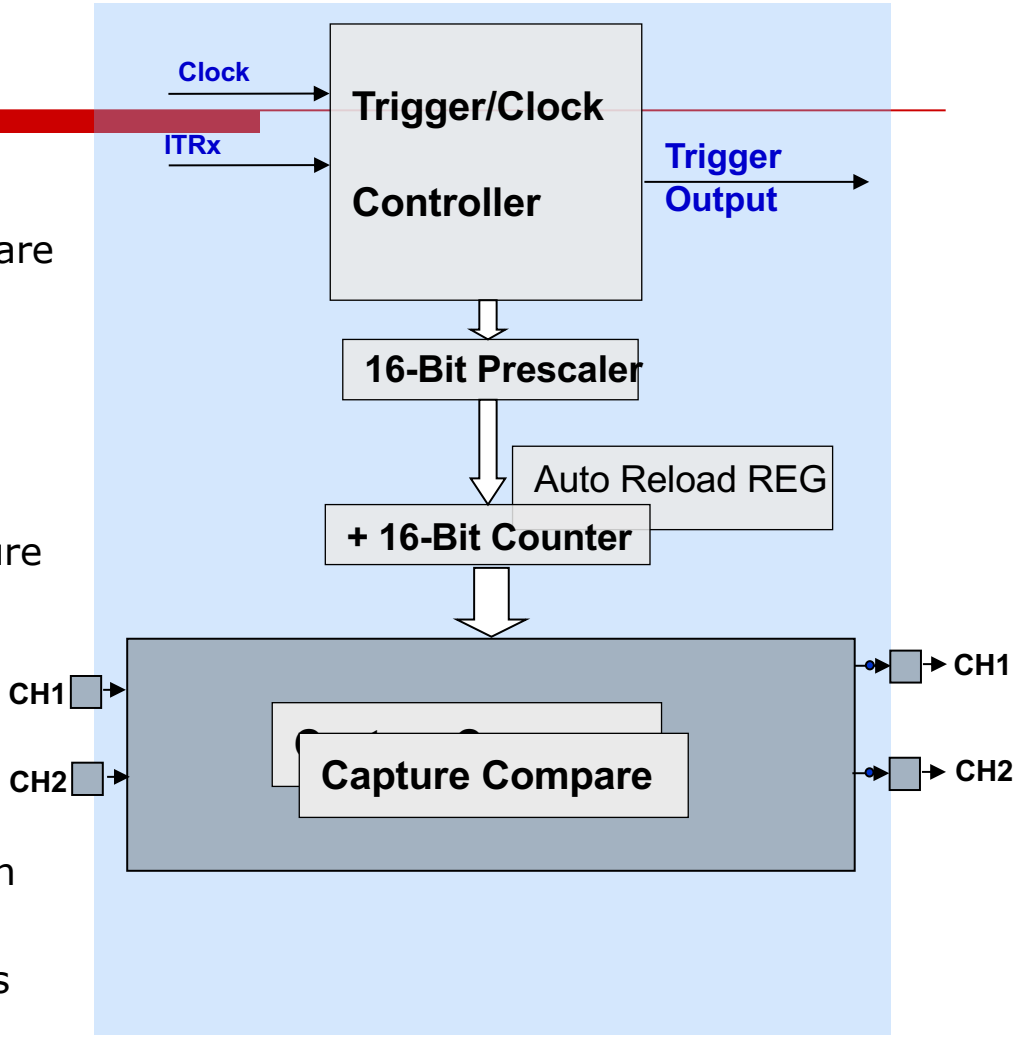
General Purpose 2 Channels (TIM9 & TIM12 on F4)

- TIM9 on High speed APB (APB2) and TIM12 on Low Speed APB (APB1)
- 16-bit Counter
  - Up counting mode
  - Auto Reload
- 2 x 16 High resolution Capture Compare Channels
  - Programmable direction of the channel: input/output
  - Output Compare
  - PWM
  - Input Capture, PWM Input Capture
  - One Pulse Mode
- Synchronization Timer Master/Slave
  - Synchronization with external trigger
  - Triggered or gated mode
- Independent IRQ Requests generation
  - At each Update Event
  - At each Capture Compare Events
  - At each Input Trigger



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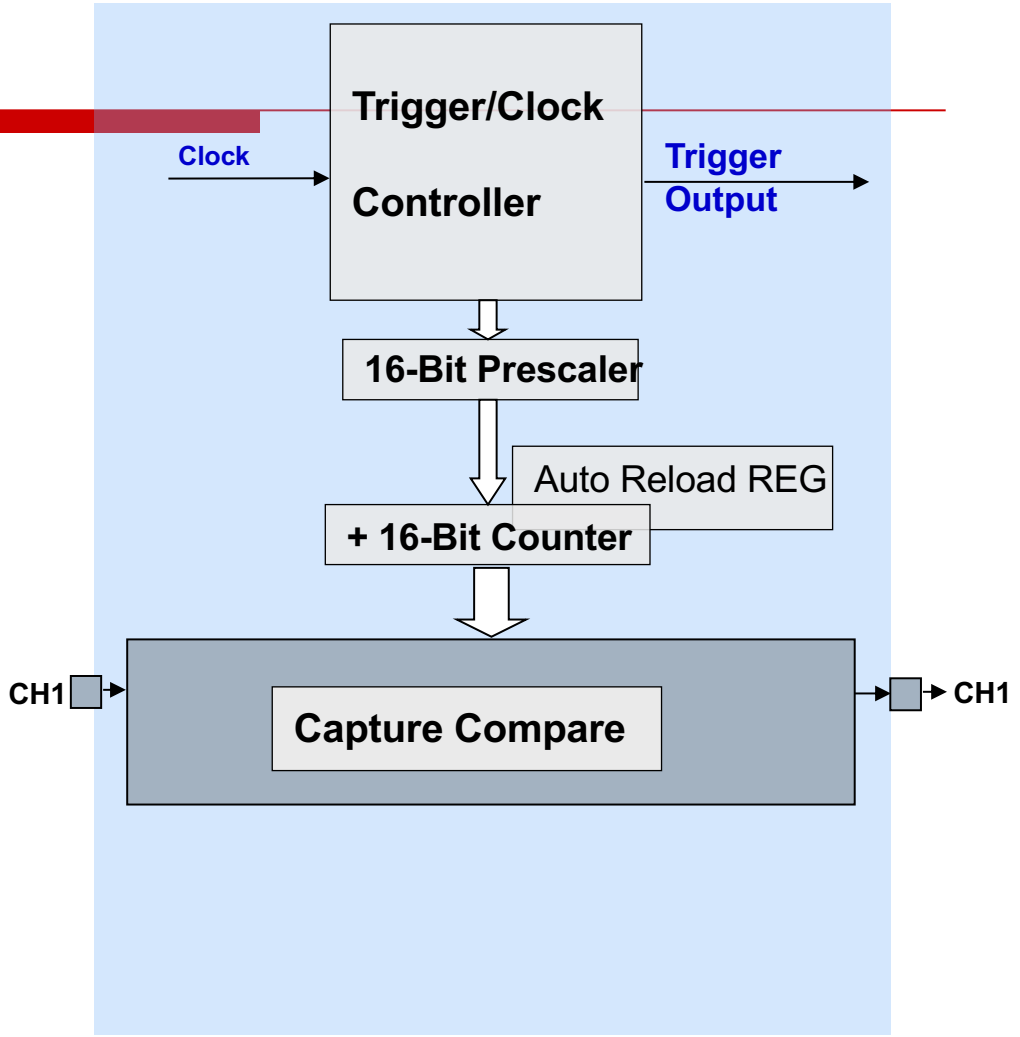
GP 1 Channels (TIM10..11 & TIM13..14 on F4)

- TIM10..11 on High speed APB (APB2) and TIM13..14 on Low Speed APB (APB1)
- Internal clock up to **168 MHz for TIM10/11**
- Internal clock up to **84 MHz for TIM13/14**
- 16-bit Counter
  - Up counting mode
  - Auto Reload
- 2 x 16 High resolution Capture Compare Channels
  - Programmable direction of the channel: input/output
  - Output Compare
  - PWM
  - Input Capture
- Independent IRQ Requests generation
  - At each Update Event
  - At each Capture Compare Events



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Capture Compare Array

- The Capture Compare Array is composed of:
  - Capture Compare channels
    - 4 Identical for TIM2, 3, 4 and 5
    - 3 Channels with possible complementary signals generation + 1 no complementary Channel only for TIM1 and TIM8
    - 2 Identical for TIM9 and 12
    - Only One for TIM10, 11, 13 and 14
  - Break functionality only for TIM1 and TIM8
- Programmable direction of each channel: input/output use
- Each Channel is composed of:
  - Capture/Compare register
  - Input stage for capture:
    - 4 bits digital filter
    - Input Capture Prescaler:
      - Capture done at each an edge is detected
      - Capture done once every 2 events
      - Capture done once every 4 events
      - Capture done once every 8 events
  - Output stage for Compare:
    - Comparator
    - Output control
    - Dead Time generator for TIM1 and TIM8 only

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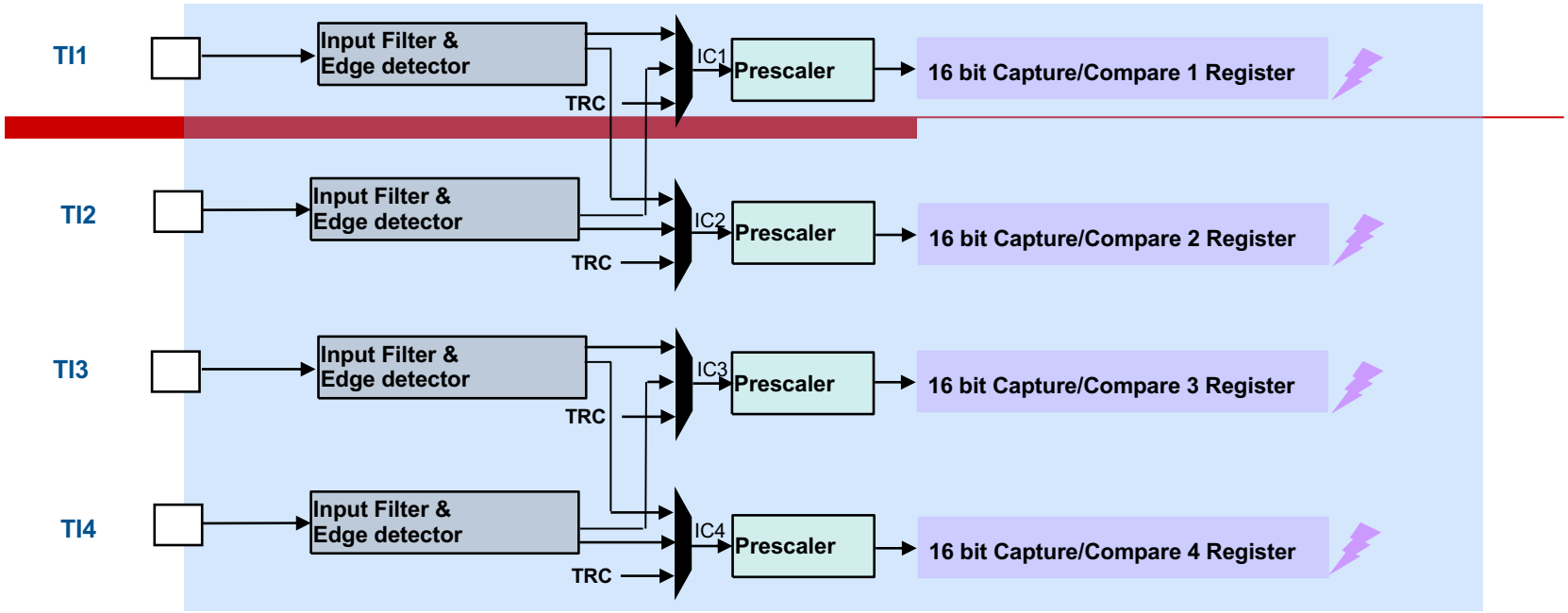
Input Capture Mode



- IC1, IC2, IC3 and IC4 are specific as they can be independently mapped by software on TI1, TI2, TI3 or TI4.
- 4x16-bit capture compare registers are programmable to be used to latch the value of the counter after a transition detected by the corresponding Input Capture.
- When a capture occurs, the corresponding CCXIF flag is set and an interrupt or a DMA request can be sent if they are enabled.
- Possible set of an over-capture flag If a capture occurs while the CCxIF flag was already high

Note: The input capture circuit is sensitive to Rising edge, to Falling edge and to both rising and falling edges.

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Input Capture Mode

Exercise:

How to configure the Input Capture Mode to measure the period of an external signal?

Use the following procedure:

- ✓ Select the counter clock source (internal/external, prescaler)
- ✓ Select the active input.
- ✓ Select the edge, Filter and Prescaler of the active transition on the ICx channel
- ✓ Enable capture from the counter into the capture register.

Input Capture Configuration tips:

To measure the signal period from the first active edge IC event (only for signals connected on TI1 and TI2):

1. Select the Reset Slave Mode: rising edges of the selected trigger signal resets the counter.

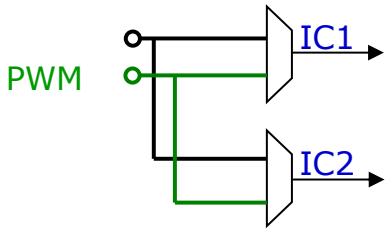
2. Select the corresponding Input as Input trigger

PWM Input Mode

PWMI Configuration tips:

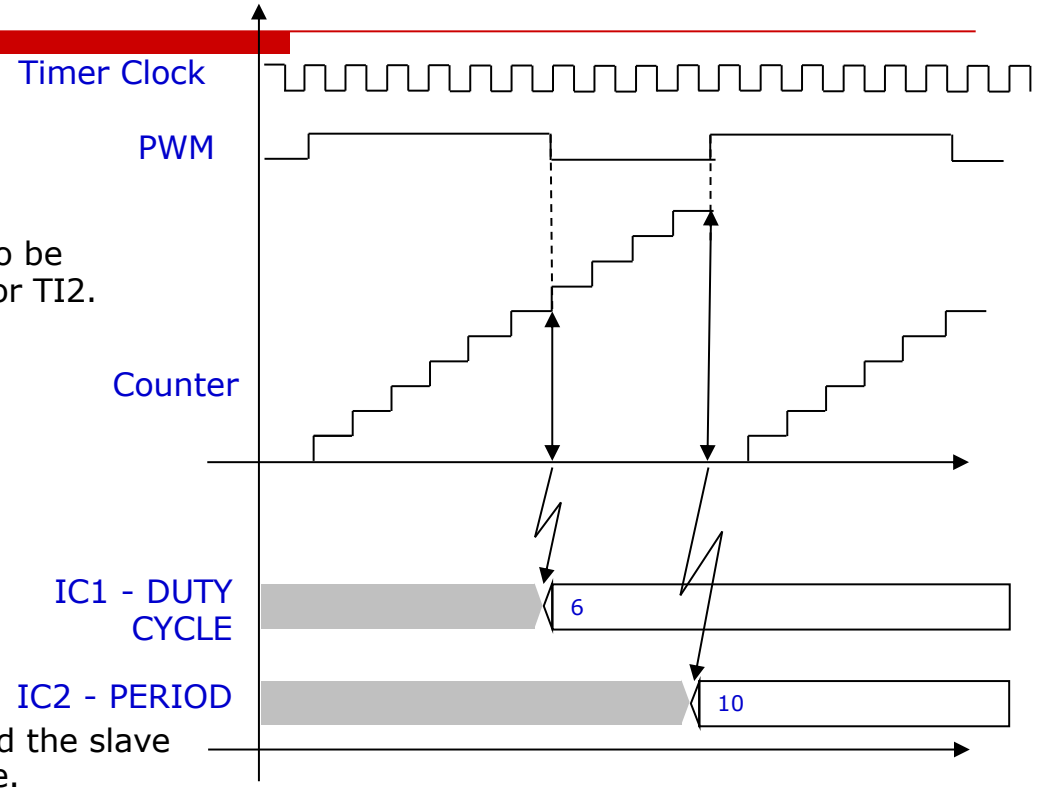
- IC1 and IC2 must be configured to be connected together to the PWM signal:

⇨ IC1 and IC2 are redirected internally to be mapped to the same external pin TI1 or TI2.



- IC1 and IC2 active edges must have opposite polarity.

- IC1 or IC2 is selected as trigger input and the slave mode controller is configured in reset mode.



The PWM Input functionality enables the measurement of the period and the pulse width of an external waveform.

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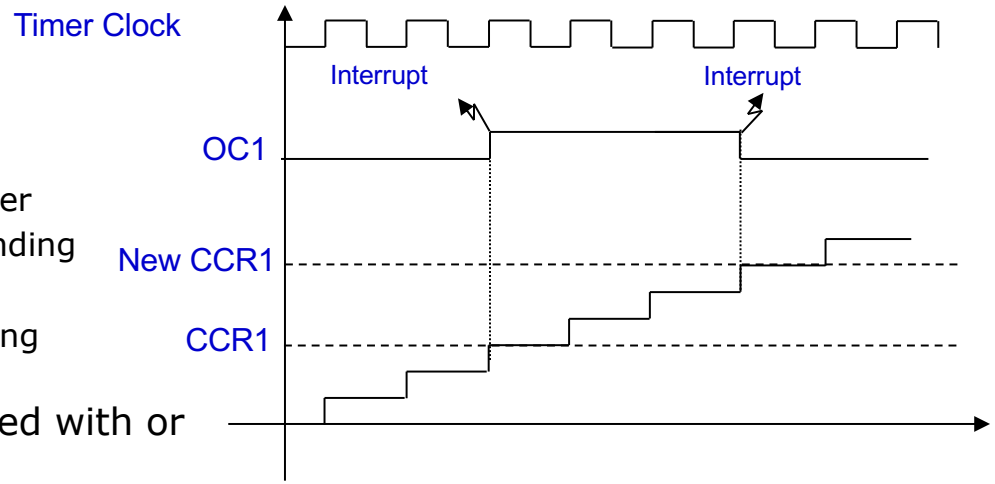
Output Compare Mode

The Output Compare is used to control an output waveform or indicate when a period of time has elapsed.

- When a match is found between the capture/compare register and the counter:
  - The corresponding output pin is assigned to the programmable Mode, it can be:
    - Set
    - Reset
    - Toggle
    - Remain unchanged
  - Set a flag in the interrupt status register
  - Generates an interrupt if the corresponding
  - interrupt mask is set
  - Send a DMA request if the corresponding
  - enable bit is set
- The CCRx registers can be programmed with or without preload registers



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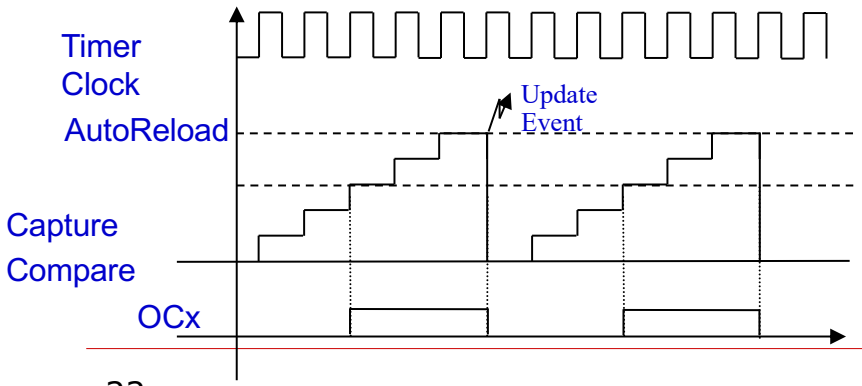
PWM Mode

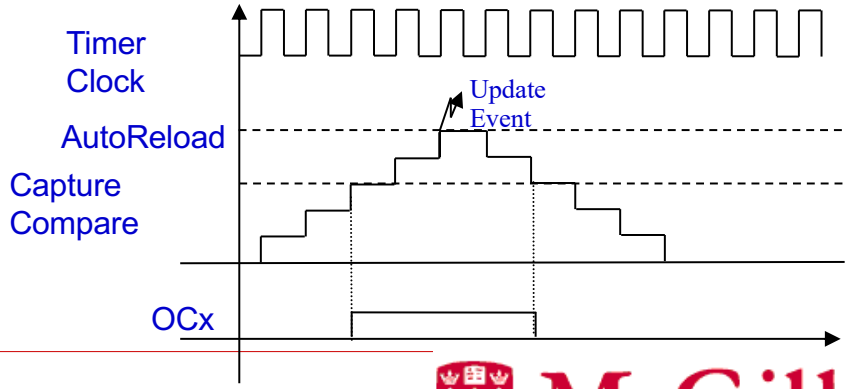
- The PWM mode allows to generate:
  - 7 independent signals for TIM1 and TIM8
  - 4 independent signals for TIM2, 3, 4 and 5
  - 2 independent signals for TIM9 and 12
  - 1 signals for TIM10, 11, 13 and 14
  - The frequency and a duty cycle determined as follow:
    - One auto-reload register to defined the PWM period.
    - Each PWM channel has a Capture Compare register to define the duty cycle.

  ➔ Example: to generate a 40 KHz PWM signal w/ duty cycle of 50% on TIM1 clock at 72MHz:
    - Load Prescaler register with 0 (counter clocked by TIM1CLK/(0+1)), Auto Reload register with 1799 and CCRx register with 899
- There are two configurable PWM modes:
  - Edge-aligned Mode
  - Center-aligned Mode

Edge-aligned Mode



Center-aligned Mode



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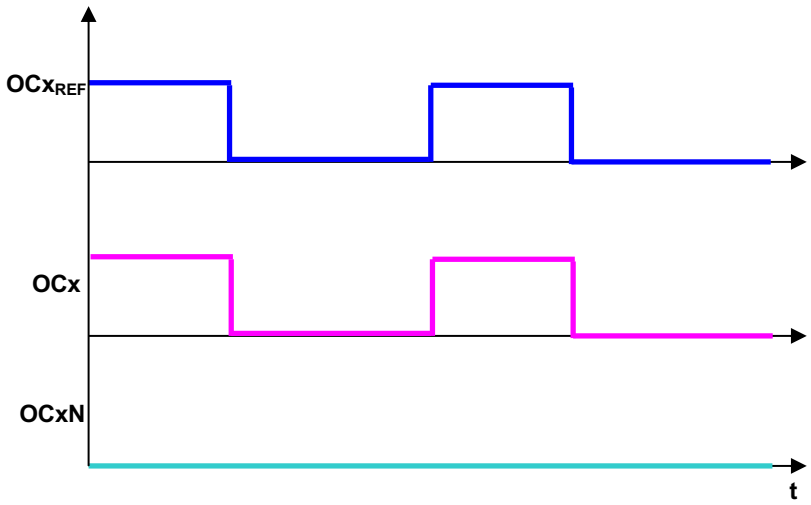
Advanced Control timer TIM1 and TIM8
Complementary PWM outputs for motor control

- This mode allows the TIM1 and TIM8 to:
  - Output two complementary signals for each three channels.
  - Output two independent signals for each three channels.
  - Manage the dead-time between the switching-off and the switching-on instants of the outputs.
- One reference waveform OCx_{REF} to generate 2 outputs OCx and OCxN for the three channels.
- Full modulation capability (0 and 100% duty cycle), edge or center-aligned patterns
- Dedicated interrupt and DMA requests for TIM1 period and duty cycles updating.
- Three programmable write protection levels
  - Level1: Dead Time and Emergency enable are locked.
  - Level2: Level1 + Polarities and Off-state selection for run and Idle state are locked.
  - Level3: Level2 + Output Compare Control and Preload are locked.

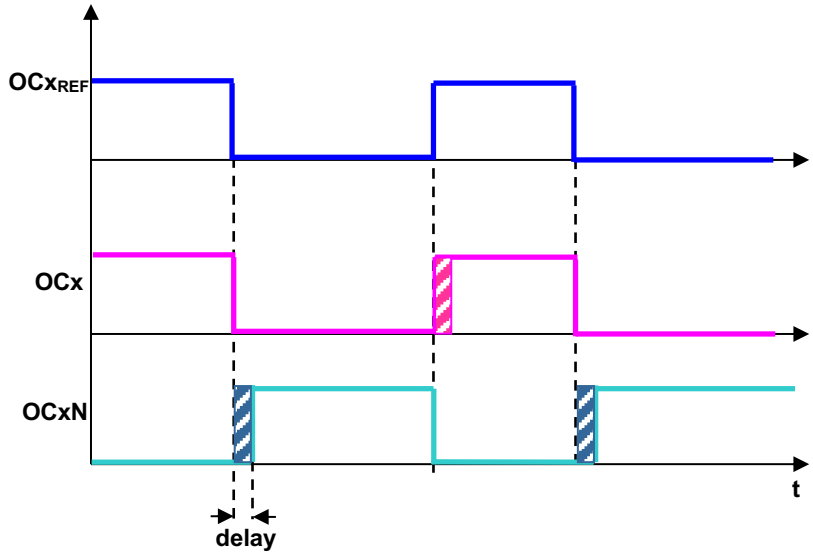
Advanced Control timer TIM1 and TIM8
Complementary PWM outputs for motor control

Examples of OCx waveform in Complementary PWM mode

Dead-time disabled



Dead-time enabled



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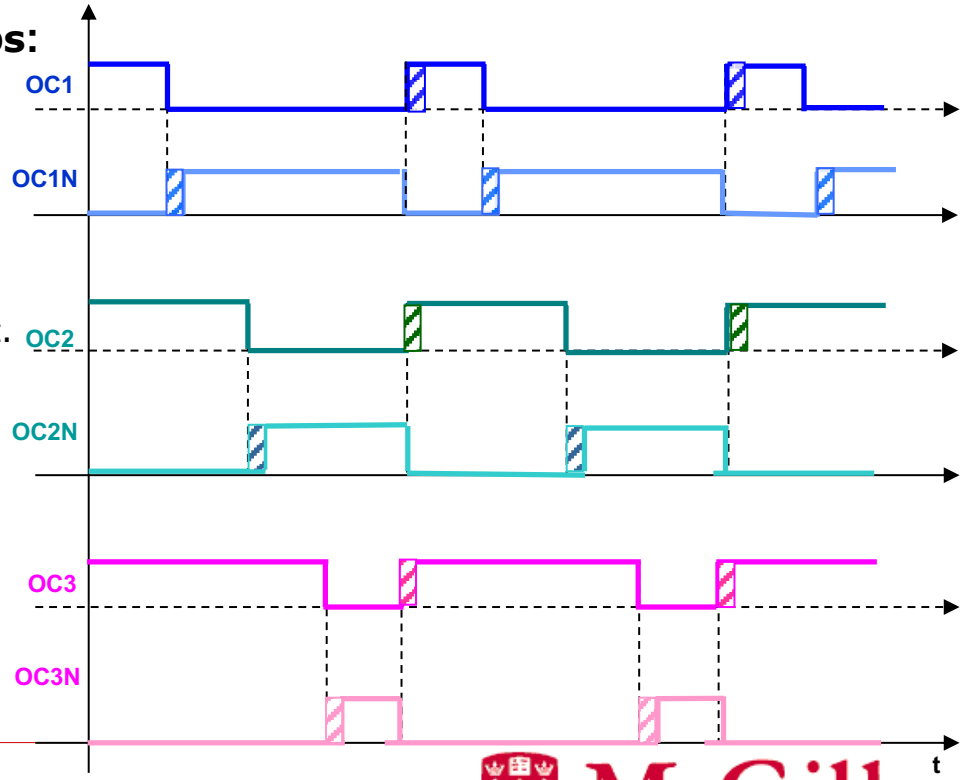
Advanced Control timer TIM1 and TIM8
Complementary PWM outputs for motor control

Exercise:

How to configure the PWM to generate three complementary Pulse Width Modulation waveforms with dead time insertion?

Complementary PWM configuration steps:

1. Select the PWM mode.
2. Activate the three complementary signals:
   i. Enable: Main Output, OCx and OCxN
   ii. Select the different off-state for Run and Idle state.
3. Set the corresponding polarity for each output.
4. Define the dead-time, the frequency and duty cycles.
5. Set the locking level and enable the input Break if necessary.
6. Enable the counter.
7. Set The Main Output Enable bit and/or the Automatic Output Enable bit.



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Advanced Control timer TIM1 and TIM8
The break function

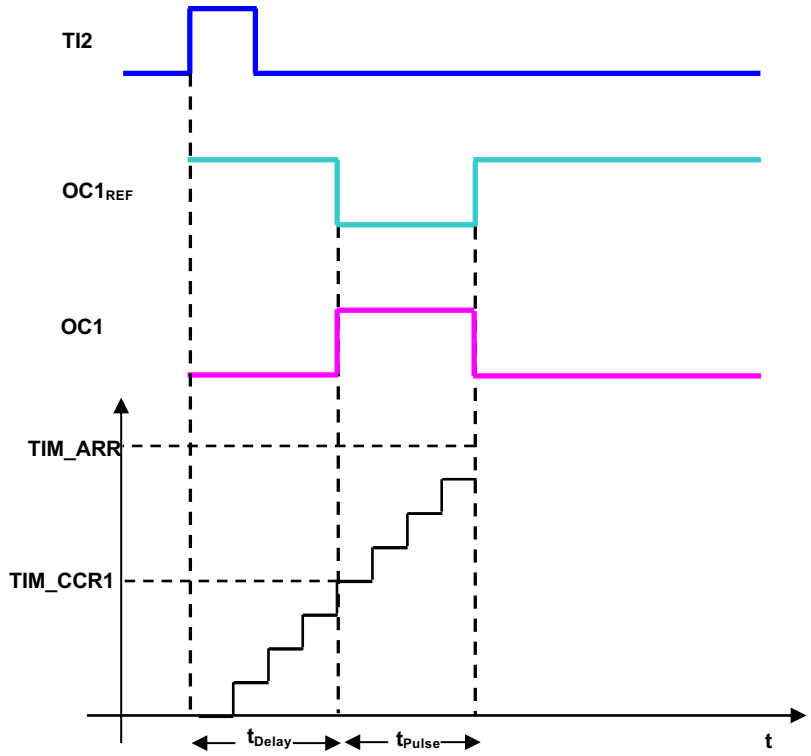
- The break can be generated by:
  - The BRK input which has a programmable polarity and an enable bit BKE
  - The Clock Security System
- When a break occurs:
  - The MOE bit: Main Output Enable is cleared
  - Each output channel is driven with the level programmed in the OISx bit
  - The break status flag is set.
  - An interrupt or a DMA request can be generated if the BIE bit is set or if the BDE bit is set.
- Break applications:
  - If the AOE: Automatic Output Enable bit is set, the MOE bit is automatically set again at the next update event UEV

    ⇨ This mode can be used to perform a regulation.
  - If the AOE is Reset, the MOE remains low until you write it to '1' again

    ⇨ In this case, used for security; one can connect the break input to an alarm from power drivers, thermal sensors or any security components.

One Pulse Mode

- One Pulse Mode (OPM) is a particular case of the previous modes: Ouput Compare and Input Capture.
- It allows the counter to be started in response to a stimulus and to generate a pulse with a programmable length after a programmable delay.
- There are two One Pulse Mode waveforms selectable by software:
  - Single Pulse
  - Repetitive Pulse



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One Pulse Mode

Exercise:

How to configure One Pulse Mode to generate a repetitive Pulse in response to a stimulus ?

One Pulse Mode configuration steps

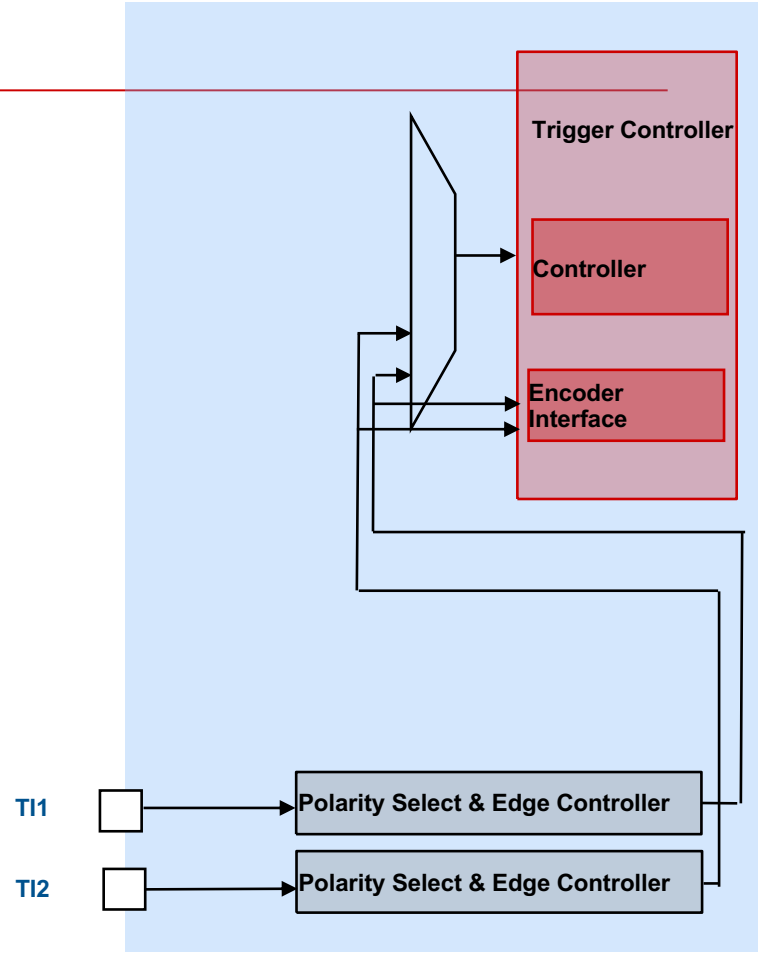
1. Input Capture Module Configuration:
   i. Map TIxFPx on the corresponding TIx.
   ii. TIxFPx Polarity configuration.
   iii. TIxFPx Configuration as trigger input.
   iv. TIxFPx configuration to start the counter (Trigger mode)

2. Output Compare Module Configuration:
   i. OCx configuration to generate the corresponding waveform.
   ii. OCx Polarity configuration.
   iii. t_{Delay} and t_{Pulse} definition.

3. **One Pulse Module Selection: Set or Reset the corresponding bit (OPM) in the Configuration register (CR1).**

Encoder Interface

- Encoders are used to measure position and speed of motion systems (either linear or angular)
- The encoder interface mode acts as an external clock with direction selection
- The counter provides information on the current position (for instance angular position of an electric motor's rotor)
- To obtain dynamic information (speed, acceleration) on must measure the number of counts between two periodic events, generated by another timer
- Encoders and Microcontroller connection example:
  - An external incremental encoder can be connected directly to the MCU without external interface logic.
  - The third encoder output which indicates the mechanical zero position, may be connected to an external interrupt and trigger a counter reset.



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Encoder Interface

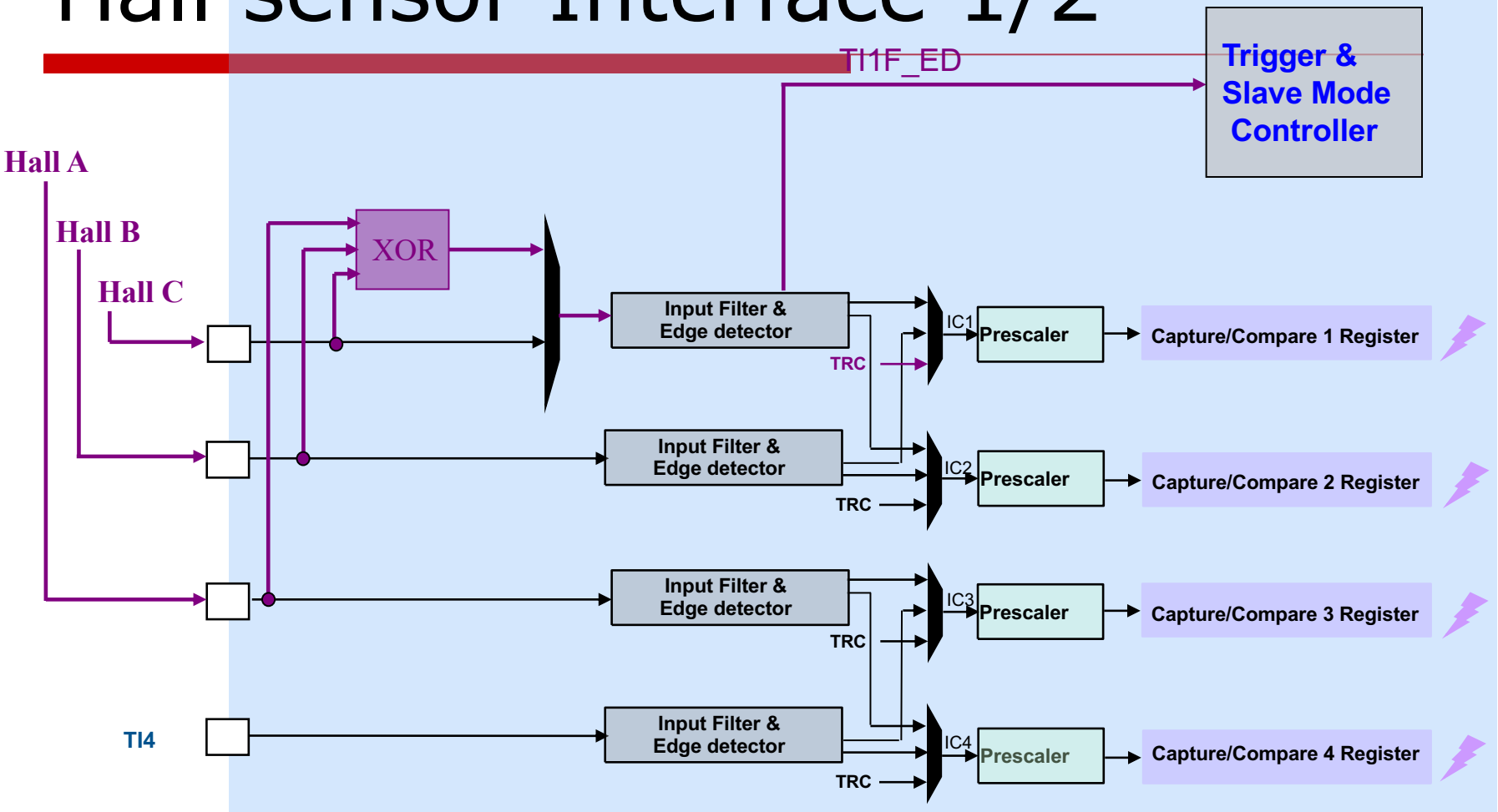
Exercise:

How to configure the Encoder interface to detect the rotation direction of a motion system?

Encoder interface configuration steps:

1. Select the active edges: example counting on TI1 and TI2.
2. Select the polarity of each input: example TI1 and TI2 polarity not inverted.
3. Select the corresponding Encoder Mode.
4. Enable the counter.

Hall sensor Interface 1/2



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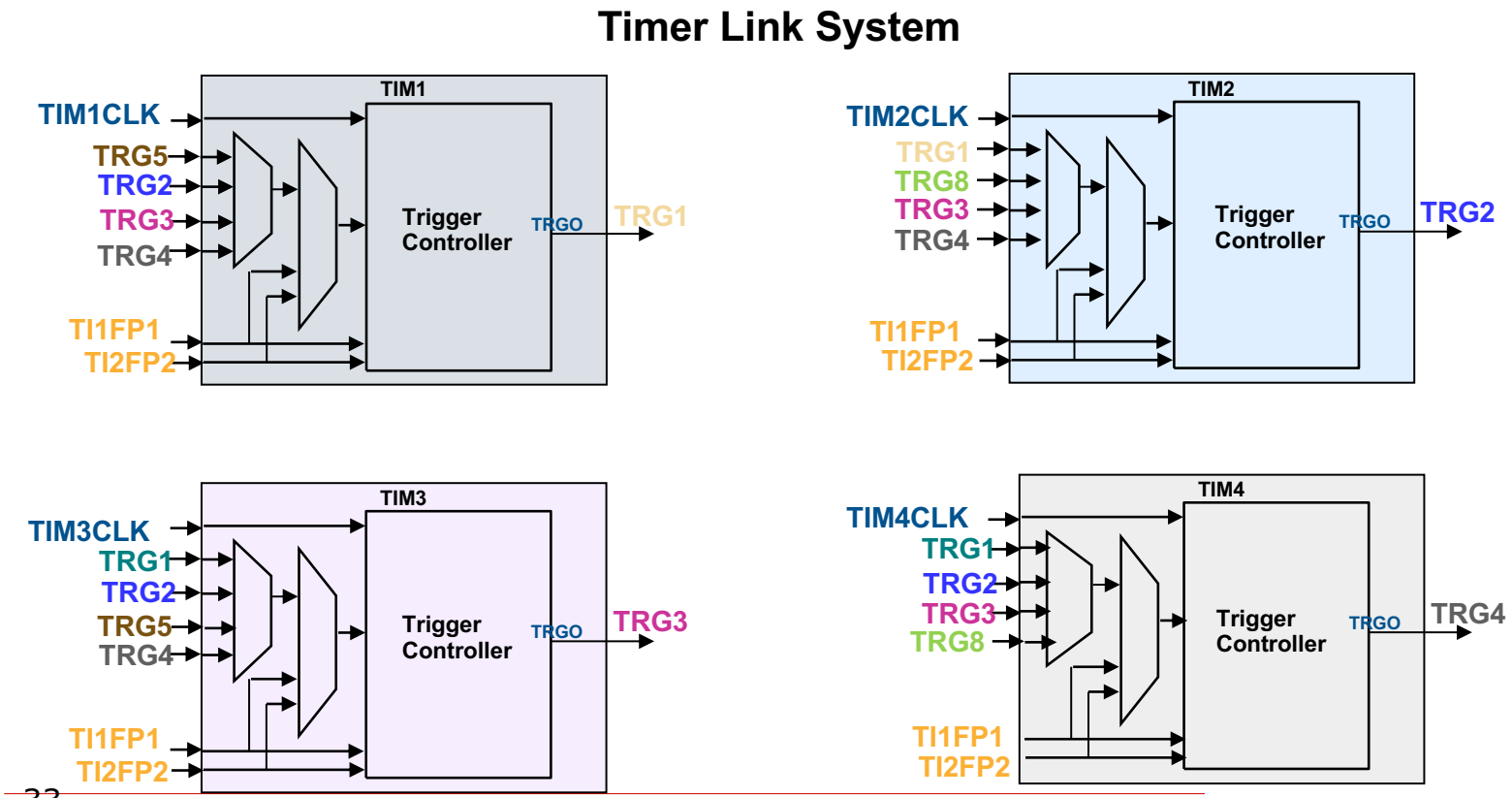
Hall sensor Interface 2/2

- Hall sensors are used for:
  - Speed detection
  - Position sensor
  - Brushless DC Motor Sensor
- How to configure the TIM to interface with a Hall sensor?
  - Select the hall inputs for TI1: TI1S bit in the CR2 register
  - The slave mode controller is configured in reset mode
  - TI1F_ED is used as input trigger
- To measure a motor speed:
  - Use the Capture/Compare Channel 1 in Input Capture Mode
  - The Capture Signal is the TRC signal
  - The captured value which correspond to the time elapsed between 2 changes on the inputs, gives an information about the motor speed

TIMs Synchronization(1/2)

Eight Timers are linked together for timer synchronization or chaining.



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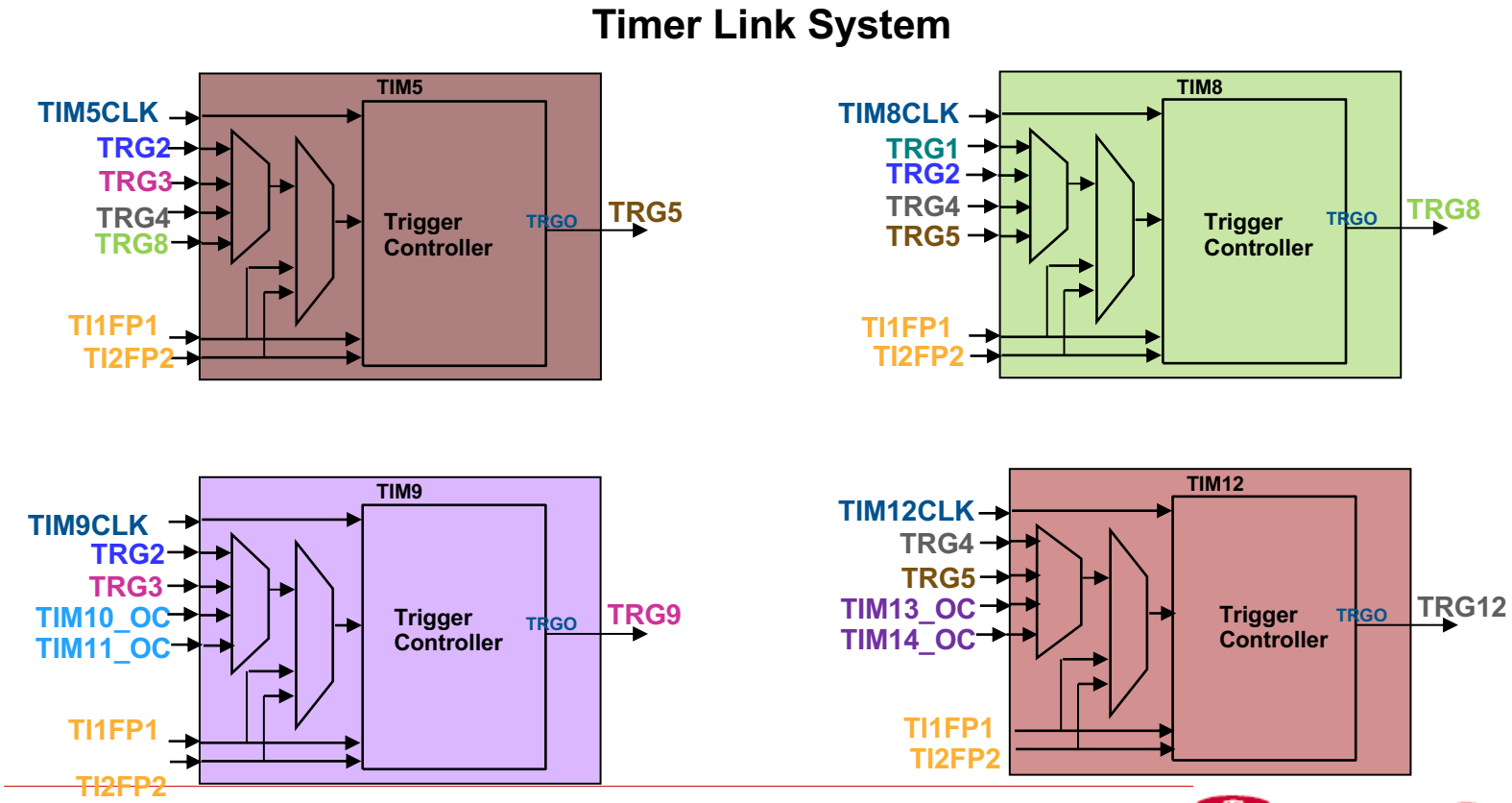
TIMs Synchronization(2/2)

Eight Timers are linked together for timer synchronization or chaining.



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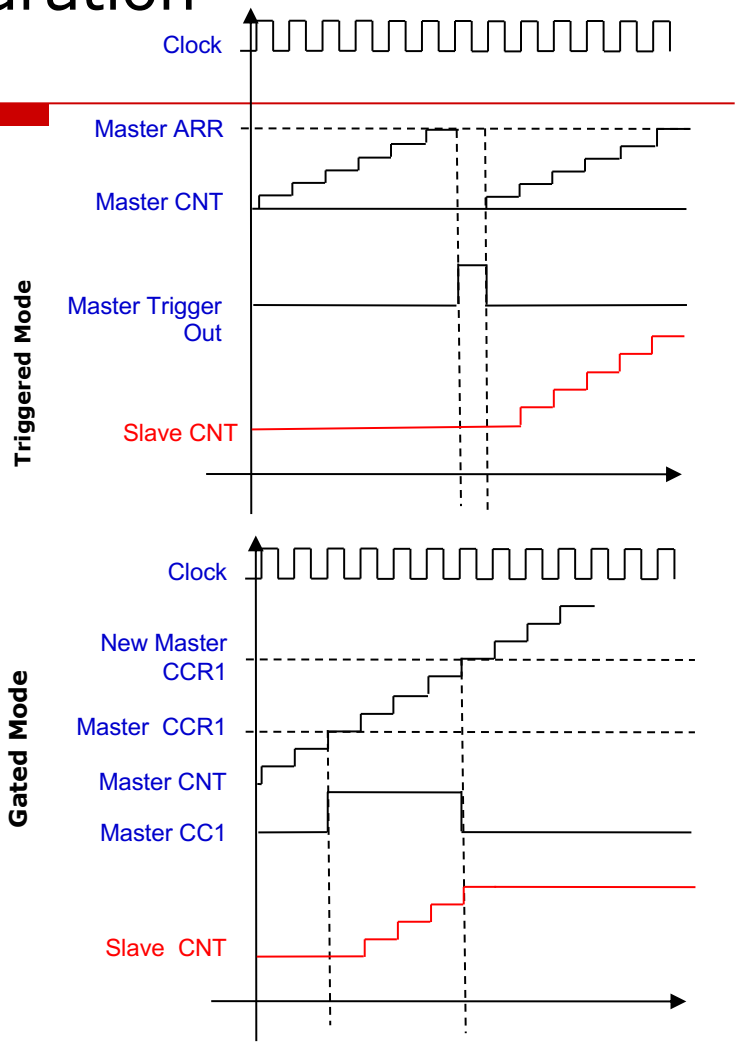
Synchronization Mode Configuration

- The Trigger Output can be controlled on:
  - Counter reset
  - Counter enable
  - Update event
  - OC1 / OC1Ref / OC2Ref / OC3Ref / OC4Ref signals
- The slave timer can be controlled in two modes:
  - Triggered mode : only the start of the counter is controlled.
  - Gated Mode: Both start and stop of the counter are controlled.



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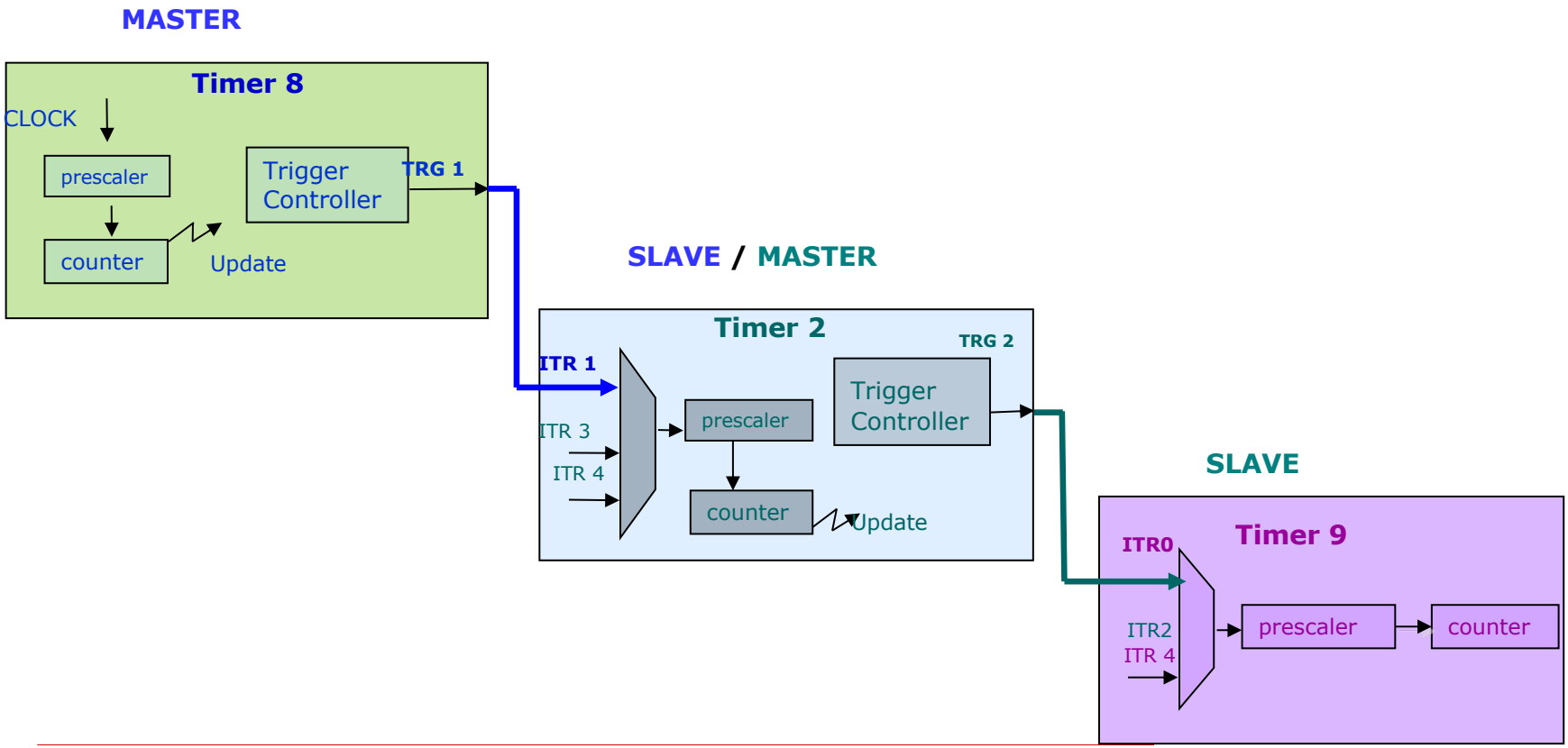
Synchronization – Configuration examples (1/3)

- Cascade mode:
  - TIM8 used as master timer for TIM2
  - TIM2 configured as TIM8 slave, and master for TIM9.



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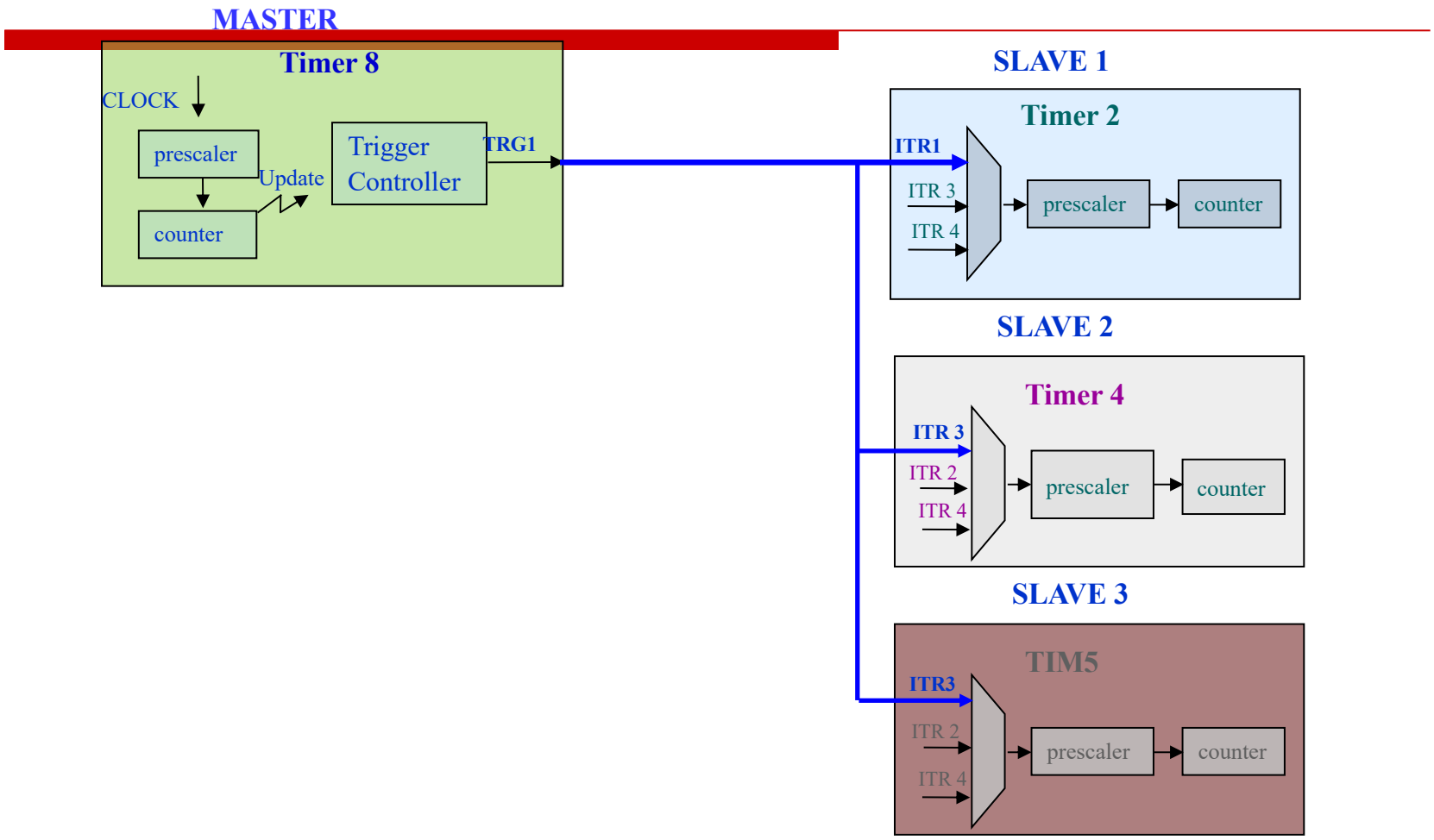
Synchronization – Configuration examples (2/3)

- One Master several slaves: TIM8 used as master for TIM2, TIM4 and TIM5.



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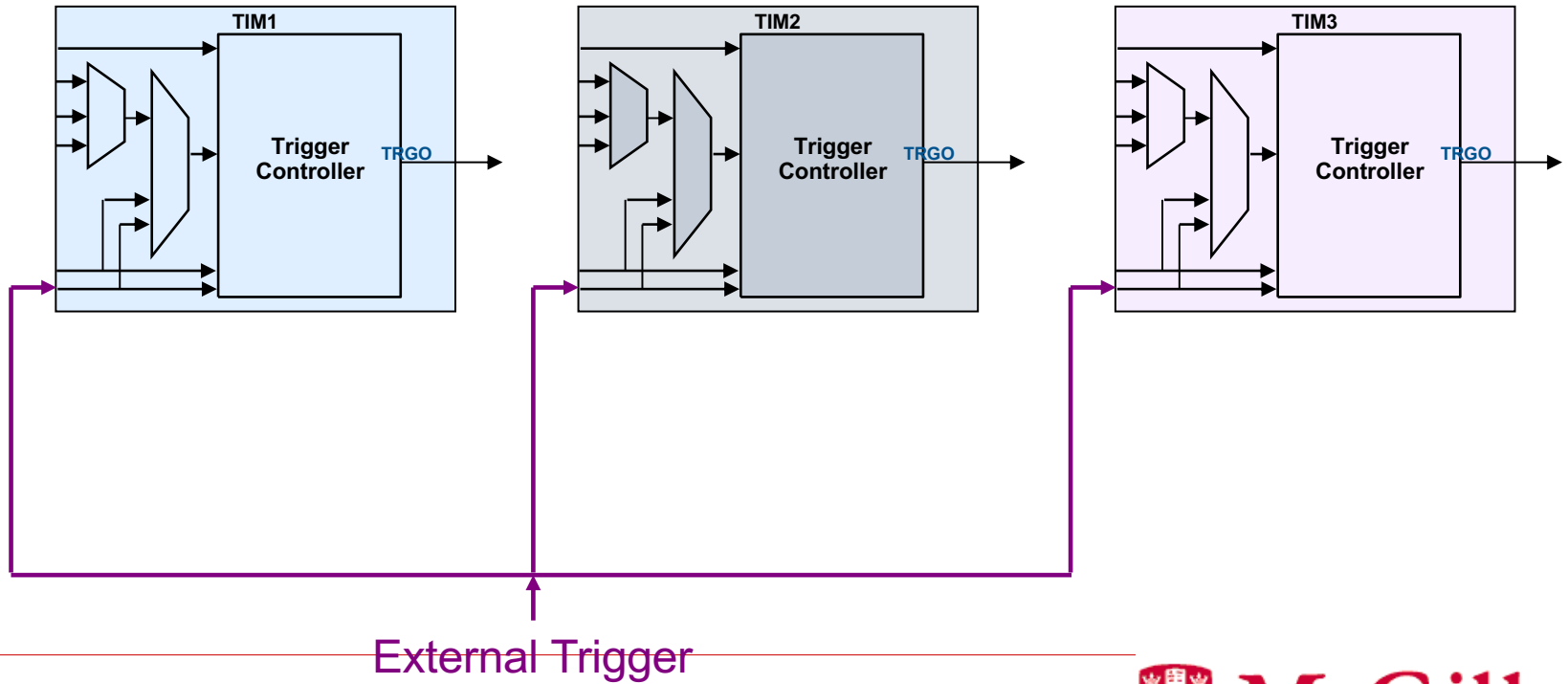
Synchronization – Configuration examples (3/3)

- Timers and external trigger synchronization
  - TIM1, TIM2 and TIM3 are slaves for an external signal connected to respective Timers inputs



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Closure on Timers

- Rich set of functions
  - Timing
  - Counting
  - Waveforms
- Use of HAL functions and Cube IDE
  - CubeMX
  - To do: Interrupts, DMA, Timers, …