ECSE 444
Analog Interfaces: ADC & DAC

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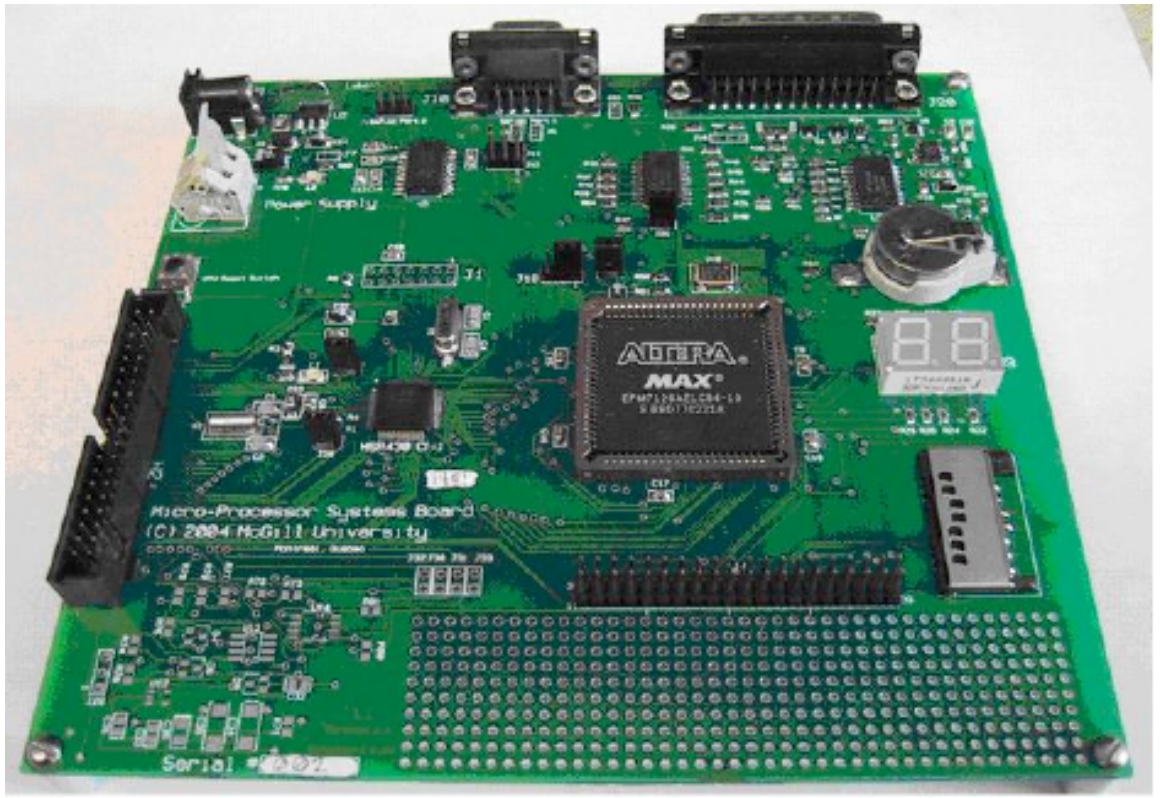

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Acknowledgments: to STMicroelectronics for material on processors and the board

Outline

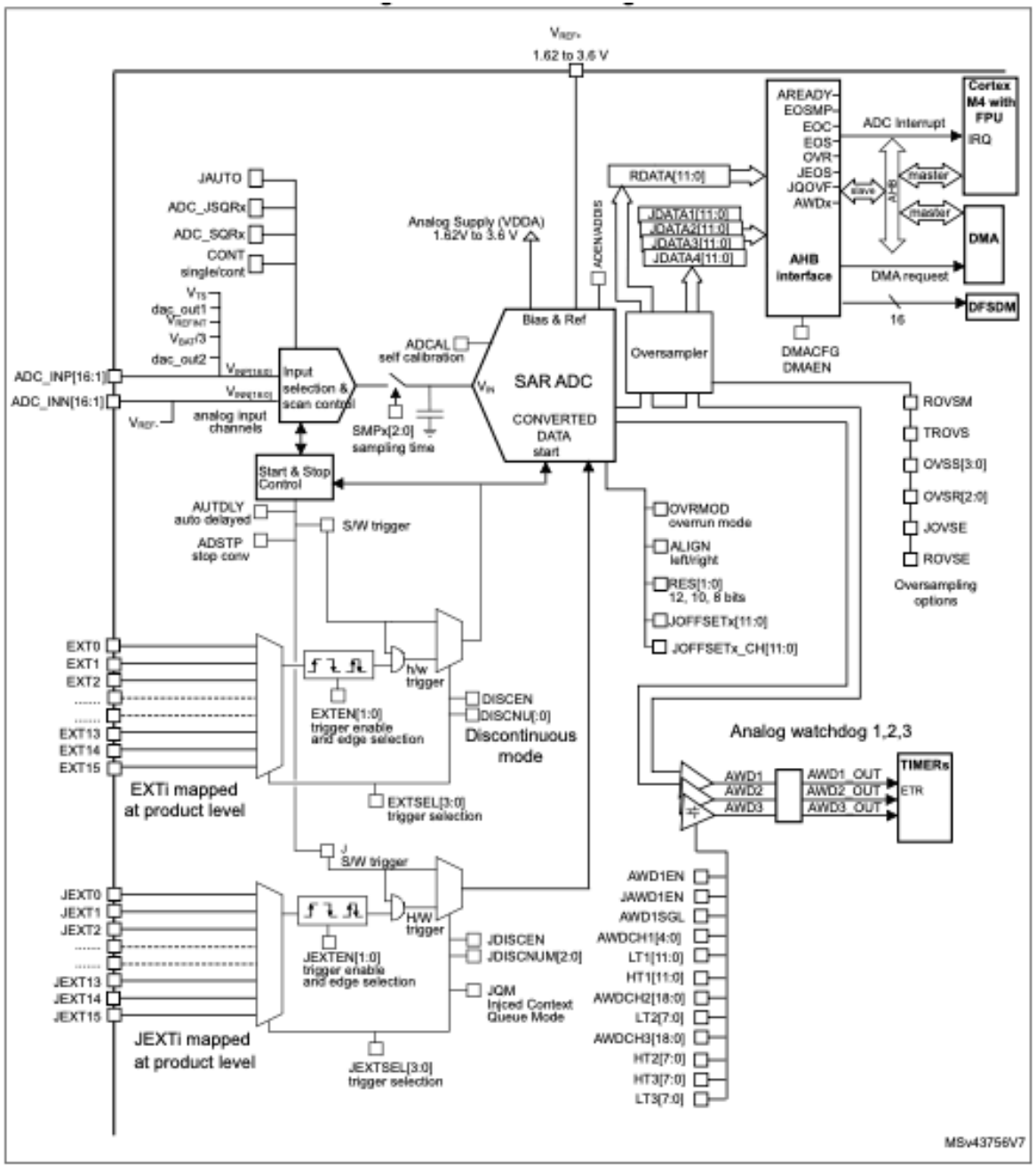
- Analog to Digital Converter (ADC)
  - Basics, principles of operation
  - ADC modes of use
- Digital to Analog Converter (DAC)
- Lab: Part 1 of Lab 2
  - Progress and Structuring of Experiments

Analog-to-Digital Converters

- 2 ADCs : ADC1 (master), ADC2 (slave)
- Maximum frequency of the ADC analog clock: 120MHz
- 12-bits, 10-bits, 8-bits or 6-bits configurable resolution
- ADC conversion rate with 12 bit resolution (16 bits with oversampling)
- Conversion range: 0 to 3.6 V
- ADC supply: VDDA = 2.4V to 3.6V at full speed, down to 1.65V at lower speed
- Up to 16 external channels
- 3 ADC1 internal channels connected to:
  - Temperature sensor,
  - Internal voltage reference : V_{REFINT} (1.2V typ),
  - VBAT for internal battery monitoring.

ADC Features

- External trigger option
- Single and continuous modes
- Left or right data alignment with data coherency
- Channel by channel programmable sampling time
- Discontinuous mode
- Dual ways
- …



ADC Features – DMA, Interrupt

- DMA capability
  - DMA request generation during regular channel conversion in single mode,
  - “ADC-DMA mode 1” used in regular simultaneous Dual ADC mode,
  - “ADC-DMA mode 2” used in interleaved Dual ADC mode as well as in regular simultaneous Dual ADC mode,
  - “ADC-DMA mode 3” used in interleaved Dual ADC mode with 6-bits and 8-bits resolution.
- Analog Watchdog on high and low thresholds.
- Interrupt generation on:
  - End of Conversion
  - End of Injected conversion
  - Analog watchdog
  - Overrun

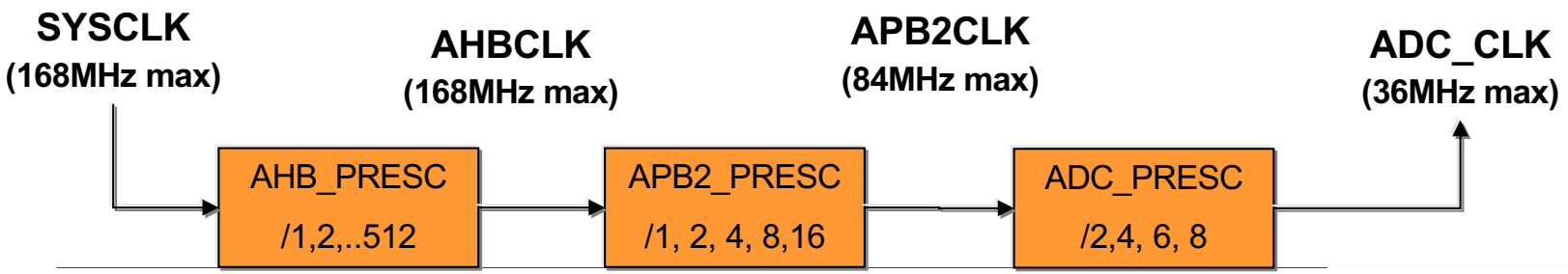
ADC Speed Performances – F4

AHBCLK	APB2CLK	ADC_CLK	ADC speed (15 cycles)
168MHz	(a) 84MHz	(2) 21MHz	0.714µs **1.4 Msample/s**
144MHz	(a) 72MHz	(1) 36MHz	0.416µs **2.4 Msample/s**
120MHz	(a) 60MHz	(1) 30MHz	0.5µs **2 Msample/s**
96MHz	(a) 48MHz	(1) 24MHz	0.625µs **1.6 Msample/s**
72MHz	(b) 72MHz	(1) 36MHz	0.416µs **2.4 Msample/s**

(1). ADC_PRESC = /2
(2). ADC_PRESC = /4

(a) APB_PRESC = /2

(b) APB_PRESC = /1



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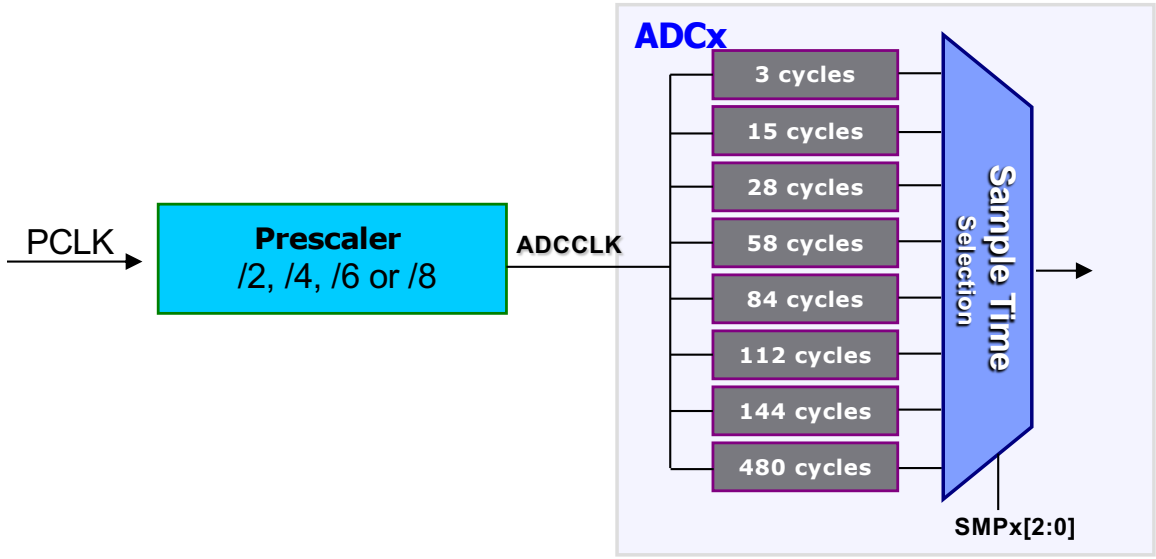
ADC Sampling Time ($T_{Sampling}$)

- ADCCLK, up to 36MHz, taken from PCLK through a prescaler (Div2, Div4, Div6 and Div8).
- Three bits programmable sample time for each channel:
  - 3 cycles
  - 15 cycles
  - 28 cycles
  - 58 cycles
  - 84 cycles
  - 112 cycles
  - 144 cycles
  - 480 cycles



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Total Conversion Time

- Total conversion Time = $T_{Sampling}$ + $T_{Conversion}$

Resolution	$T_{Conversion}$
12 bits	12 Cycles
10 bits	10 Cycles
8 bits	8 Cycles
6 bits	6 Cycles

- With Sample time= 3 cycles @ ADC_CLK = 36MHz ➔ total conversion time:

resolution	Total conversion Time	
12 bits	**12 + 3 = 15cycles**	**0.416 us → 2.4 Msps**
10 bits	10 + 3 = 13 cycles	0.361 us → 2.71 Msps
8 bits	8 + 3 = 11 cycles	0.305 us → 3.27 Msps
6 bits	6 + 3 = 9 cycles	0.25 us → 4 Msps

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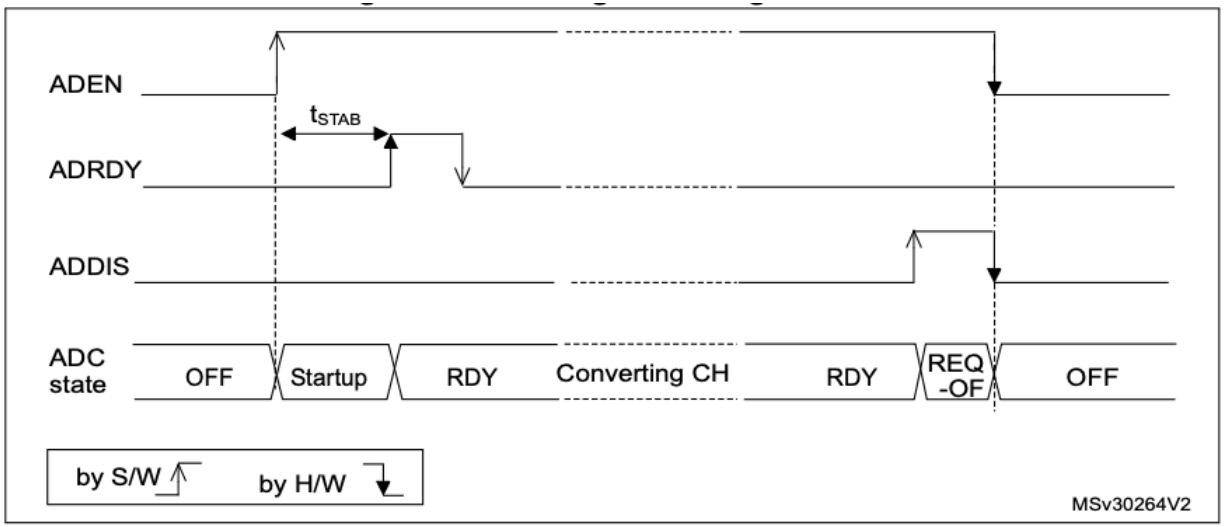
Enabling ADC in Software

- Initiate the enable signal (ADEN signal)
- ADC can be used when ready (ADRDY signal)
- Disabling when conversion done (ADDIS signal)



- Reference Manual: Sec. 21.4.9 (page 629)

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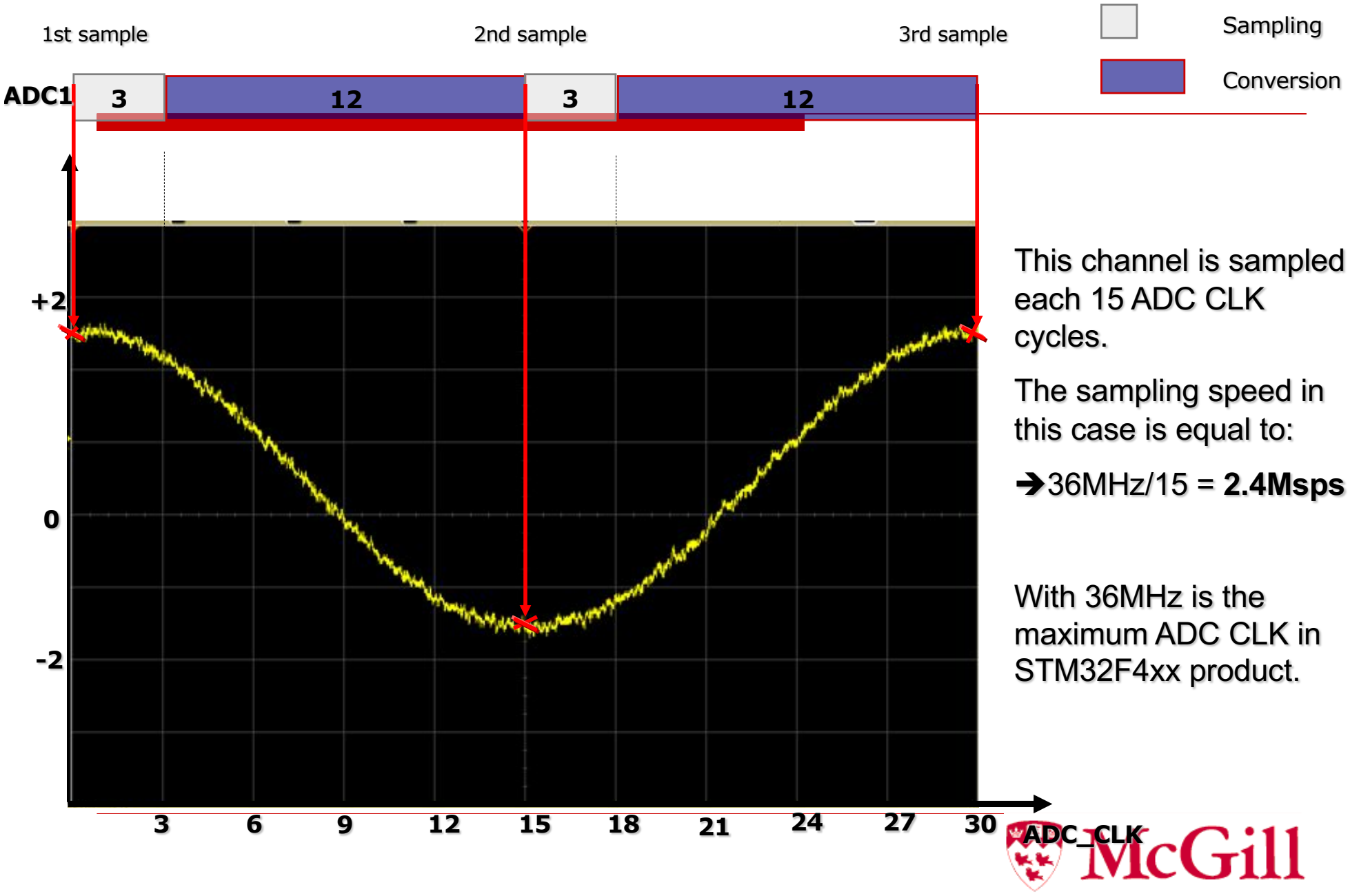
ADC conversion in single mode (12 bit resolution)



This channel is sampled each 15 ADC CLK cycles.

The sampling speed in this case is equal to:

➔36MHz/15 = **2.4Msps**

With 36MHz is the maximum ADC CLK in STM32F4xx product.

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ADC Regular / Injected Channels

- Programmable number of **regular** channels: Up to 16 conversions.
- Programmable sample time and conversion sequence.
- Conversion started by:
  - Software: through start bit,
  - External trigger generated by:
    - EXTI IT11,
    - 15 triggers from 6 TIMERS,
- Programmable number of **injected** channels: Up to 4 conversions.
- Programmable sample time and conversion sequence.
- Conversion started by:
  - JAUTO: automatic injected conversion after regular channels conversion,
  - Software: through start bit,
  - External trigger generated by:
    - EXTI IT15,
    - 15 triggers from 6 TIMERS.

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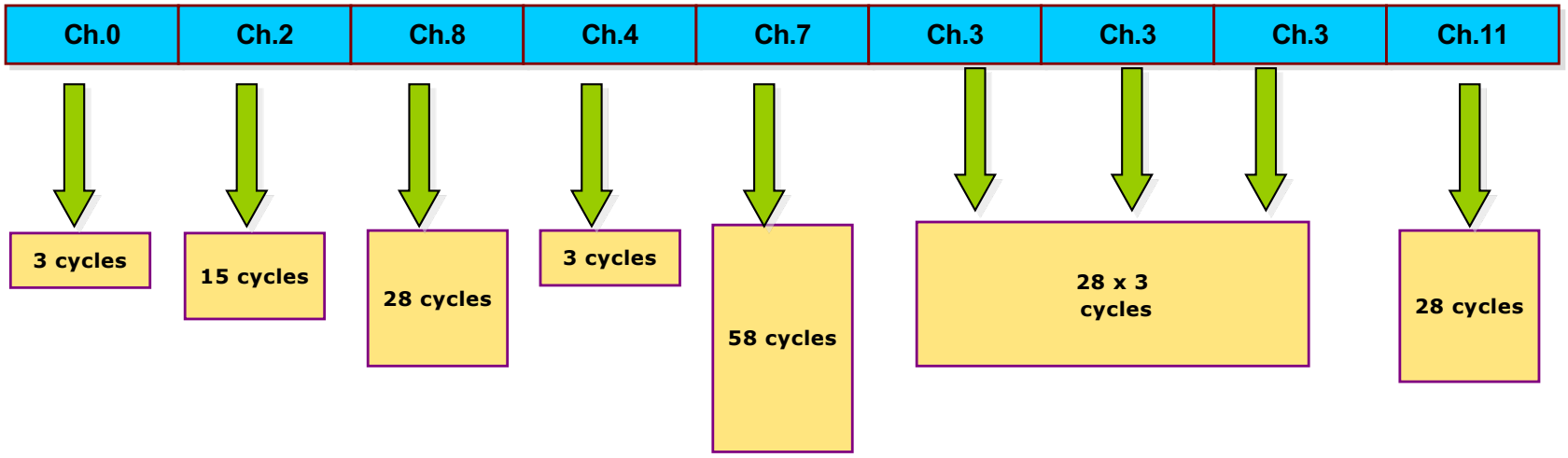
ADC Sequencer

- Up to 16 regular and 4 injected conversions with programmable order, sampling time and over-sampling

Example: - Conversion of channels: 0, 2, 8, 4, 7, 3, 3 ,3 and 11

- Different sampling time

- Over-sampling of channel 3



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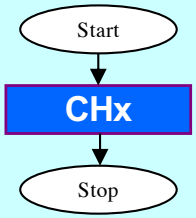
ADC conversion modes

- Five conversion modes available:

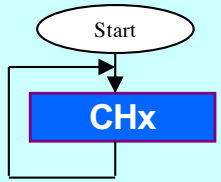
Single channel

single conversion mode



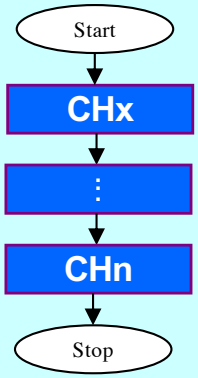
Single channel

Continuous conversion mode



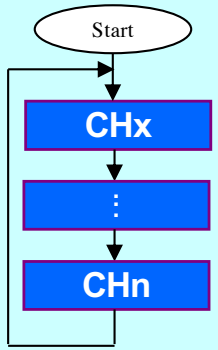
Multi-channels (Scan)

single conversion mode



Multi-channels (Scan)

continuous conversion mode



Discontinuons conversion mode

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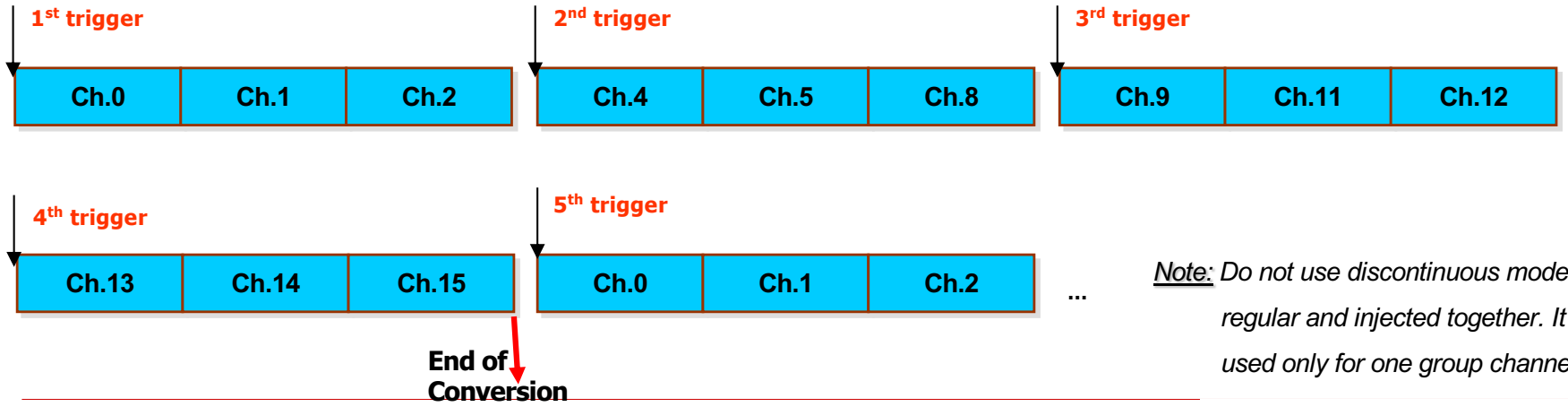
ADC Discontinuous Conversion

- Split channels conversion sequence into sub-sequences
- Available for both regular and injected groups:
  - Up to 8 conversions for regular group
  - Up to 3 conversions for injected group

Example:

- Conversion of regular channels: 0, 1, 2, 4, 5, 8, 9, 11, 12, 13, 14 and 15

- Discontinuous mode Number of conversions: 3



Note: Do not use discontinuous mode for both regular and injected together. It can be used only for one group channel

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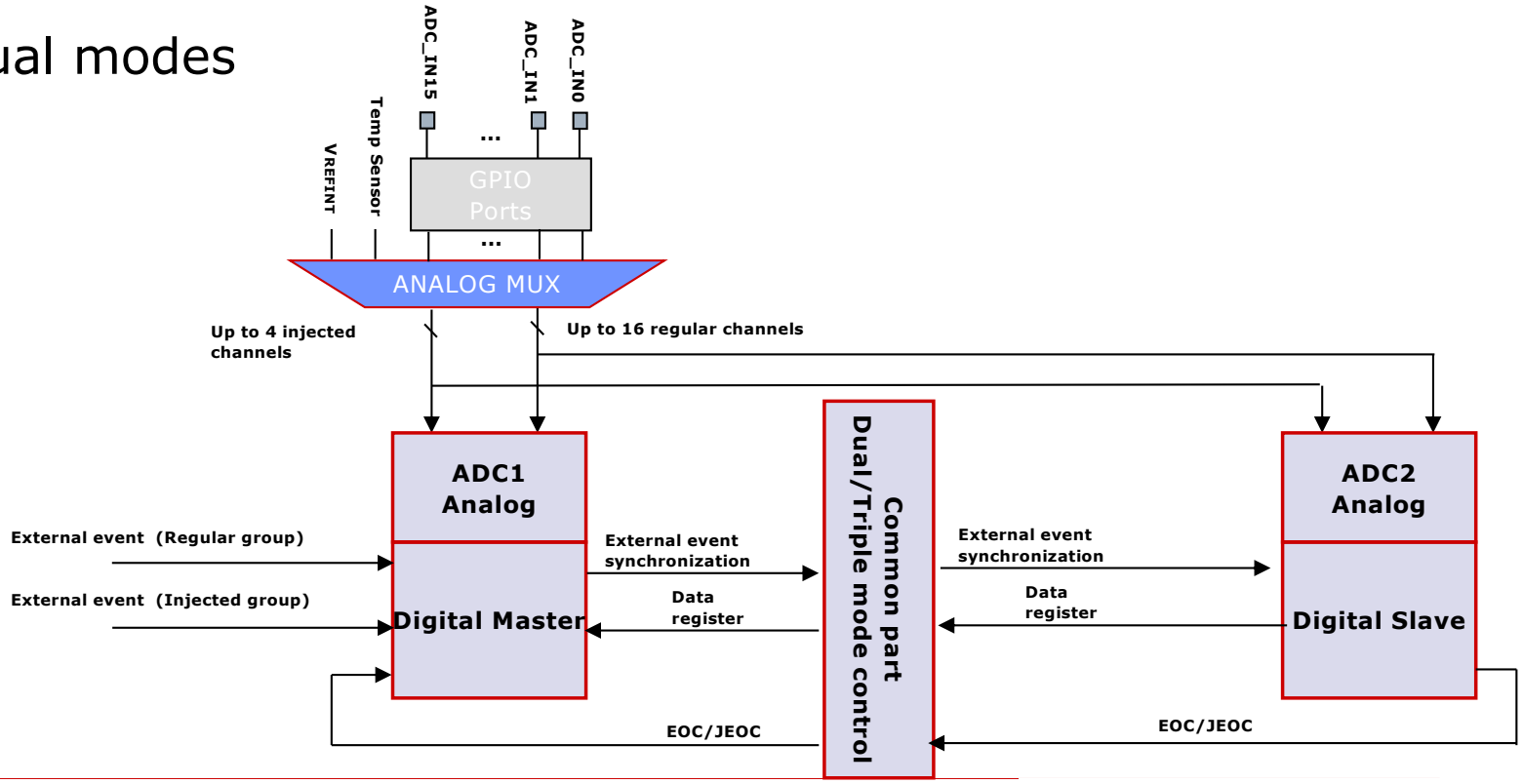
ADC dual modes

- ADCs: ADC1 master and ADC2 slave, ADC3 is independently
- Start of conversion triggered alternately or simultaneously by the ADC1 master to the ADC2
- 6 ADC dual modes



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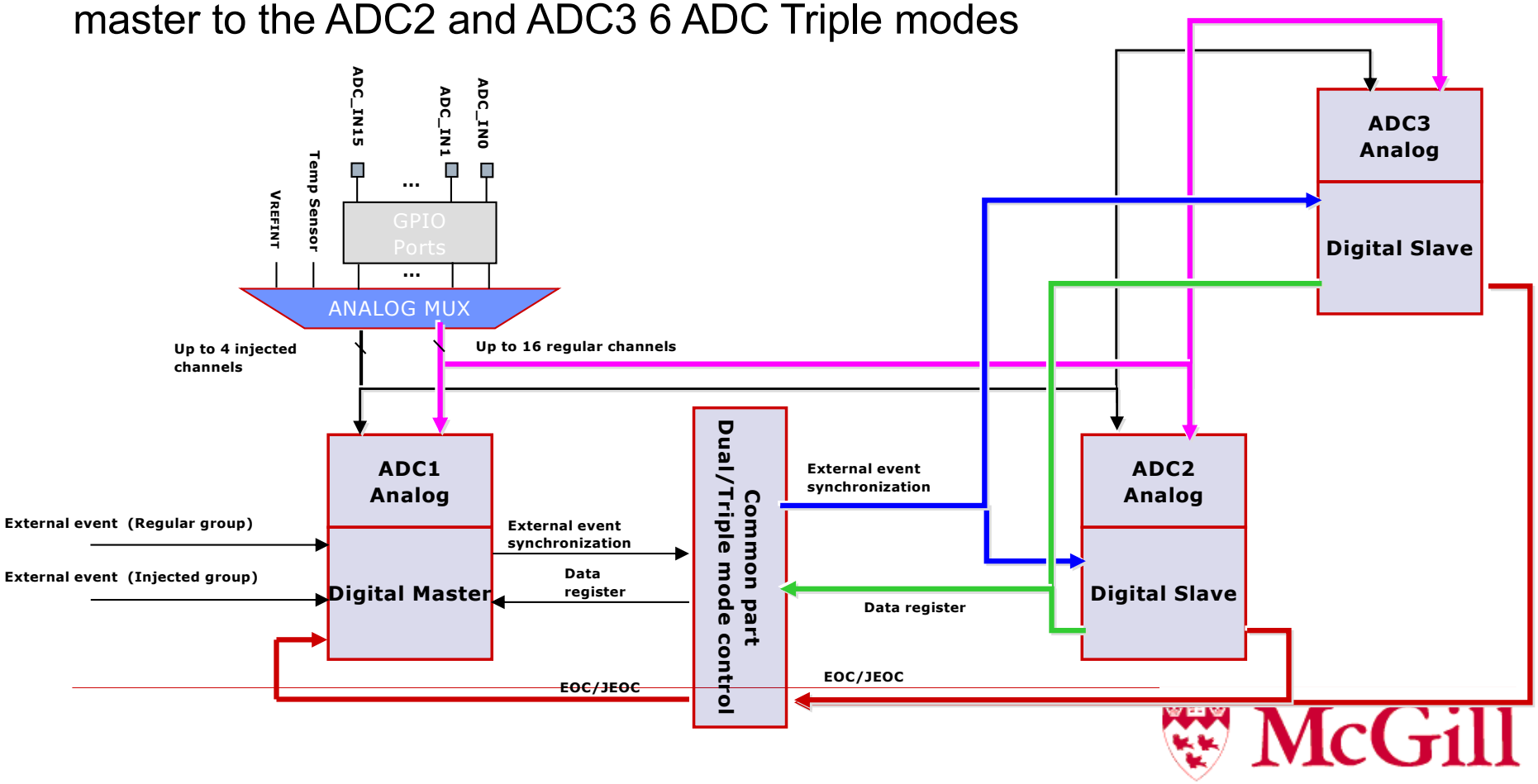
ADC Triple modes (F4, G4)

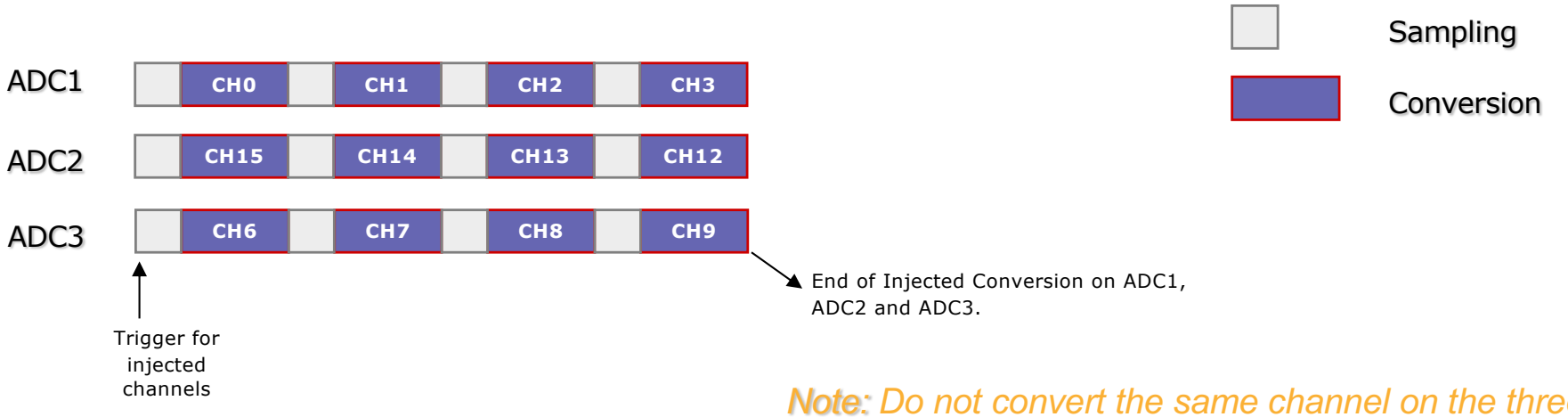
- ADCs: ADC1 master, ADC2 and ADC3 slaves
- Start of conversion is triggered alternately or simultaneously by the ADC1 master to the ADC2 and ADC3 6 ADC Triple modes



ADC Triple modes Injected simultaneous mode

- Converts an injected channel group
- External trigger source, which start the conversion, comes from ADC1 (simultaneous trigger provided to ADC2 and ADC3 slaves)
- An end of injected conversion is generated at the end of all channels conversion
- Results stored on injected data registers of each ADC.

Injected simultaneous mode on 4 injected channels:



Note: Do not convert the same channel on the three ADCs.

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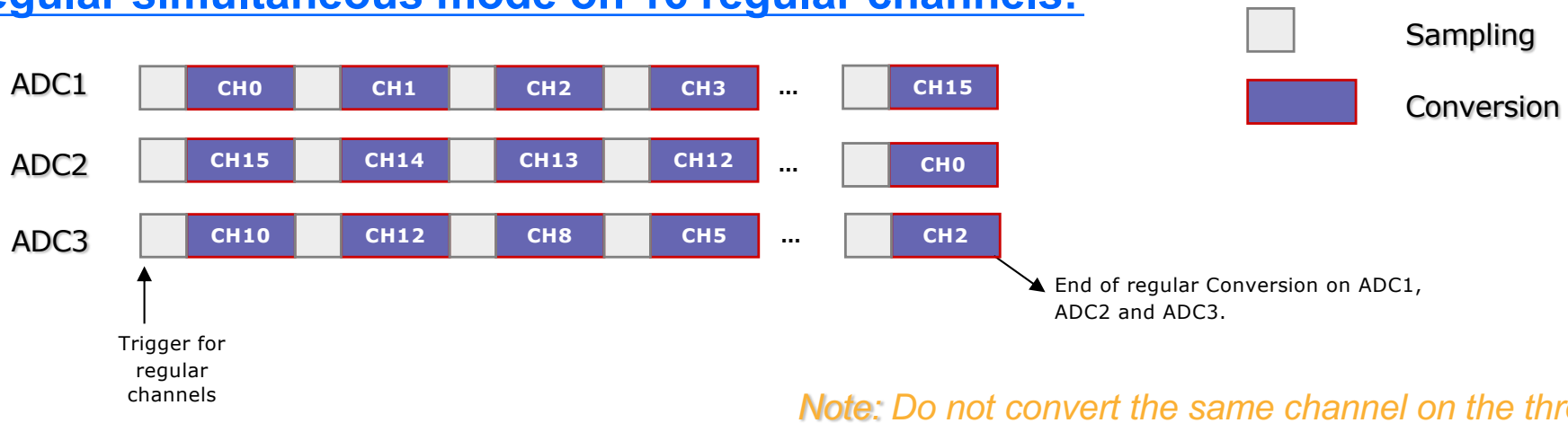
ADC Triple modes Regular simultaneous mode

- Converts a regular channel group
- The external trigger source, which start the conversion, comes from ADC1 (simultaneous trigger provided to ADC2 and ADC3 slaves)
- An end of regular conversion is generated at the end of all channels
- Results stored on the common data register ADC_CDR

Regular simultaneous mode on 16 regular channels:



Note: Do not convert the same channel on the three ADCs.

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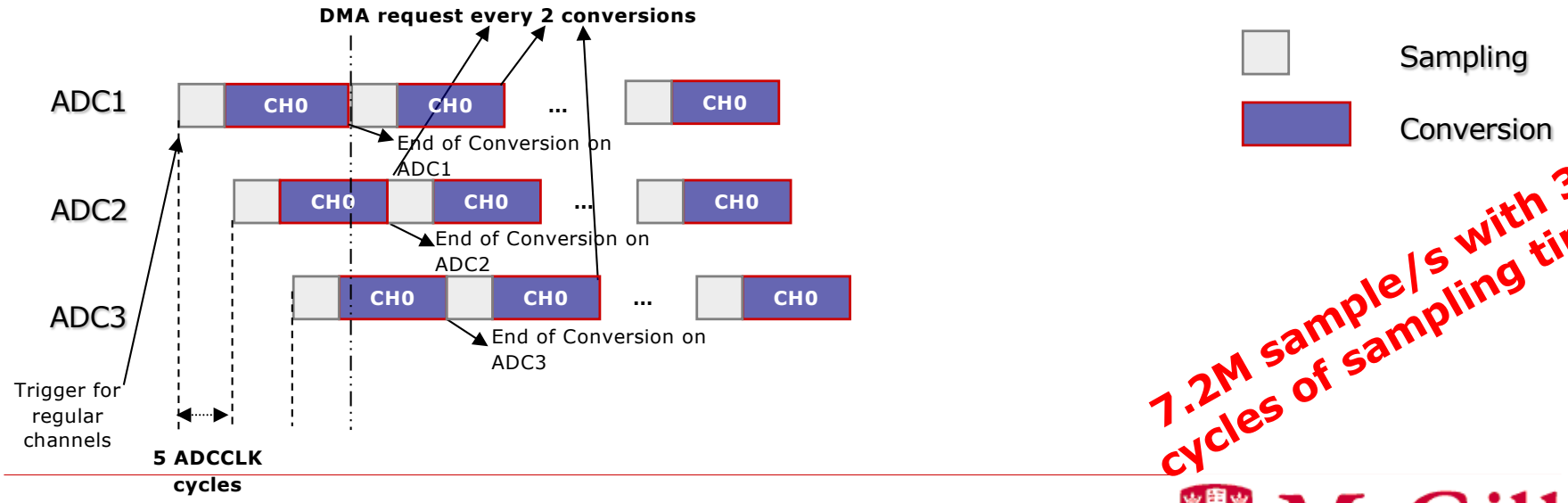
ADC Triple modes Interleaved mode

- Converts a regular channel group (usually one channel)
- The external trigger source, which start the conversion, comes from ADC1:
  - ADC1 starts immediately
  - ADC2 starts after a delay of 5 ADC clock cycles
  - ADC3 starts after a delay of 5 ADC clock cycles referred to the ADC2 conversion
- In this mode the sampling criteria to respect is always "Tsampling + 2 ADC Cycles " as minimum delay
- Results stored on the common data register ADC_CDR

Interleaved mode on 1 regular channel in continuous conversion mode:



7.2M sample/s with 3 cycles of sampling time

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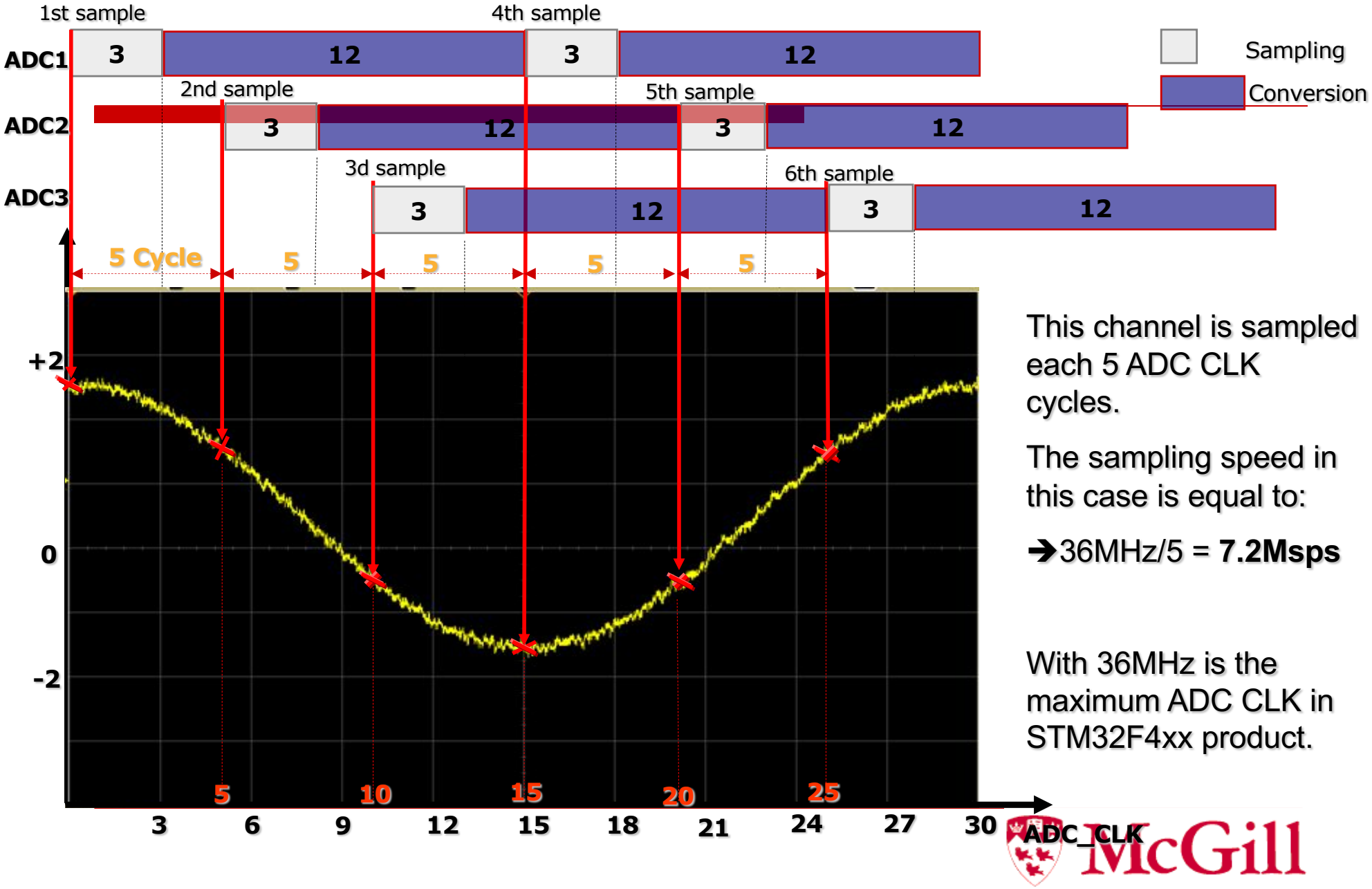
ADC conversion in Triple Interleaved mode (12 bit resolution)



This channel is sampled each 5 ADC CLK cycles.

The sampling speed in this case is equal to:

➔36MHz/5 = **7.2Msps**

With 36MHz is the maximum ADC CLK in STM32F4xx product.

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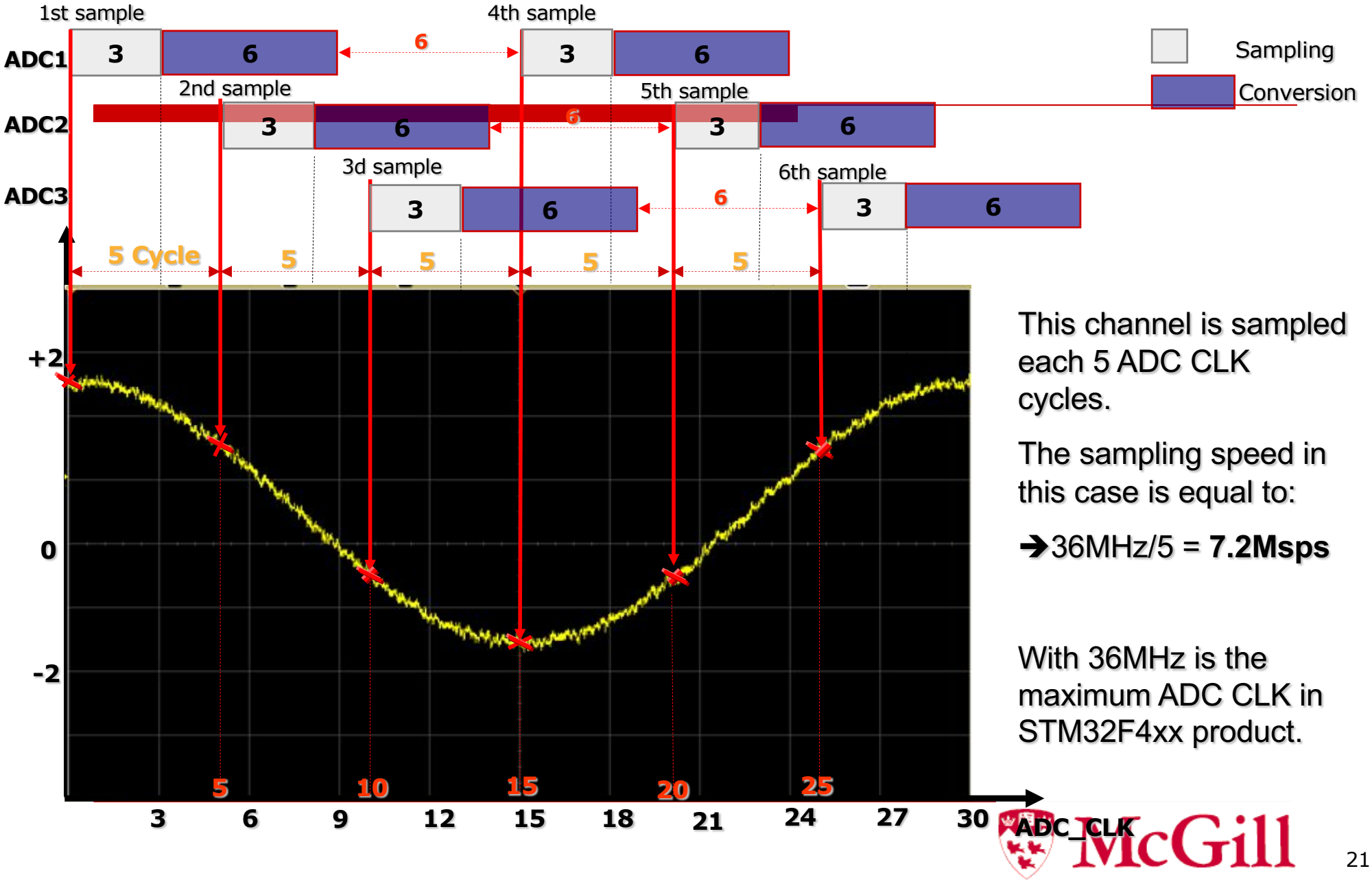
ADC conversion in Triple Interleaved mode (6 bit resolution)



This channel is sampled each 5 ADC CLK cycles.

The sampling speed in this case is equal to:

➔36MHz/5 = **7.2Msps**

With 36MHz is the maximum ADC CLK in STM32F4xx product.

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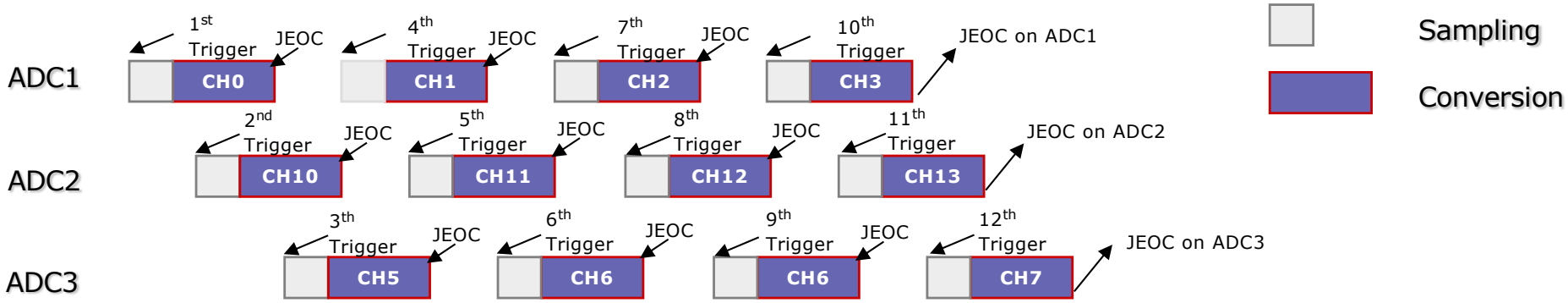
ADC Triple modes Alternate Trigger mode

- Converts an injected channel group.
- External trigger source, which start the conversion, comes from ADC1:
  - On 1st trigger, the first injected group channel in ADC1 is converted
  - On 2nd trigger, the first injected group channel in ADC2 is converted
  - On 3rd trigger, the first injected group channel in ADC3 is converted…
- An end of injected conversion is generated at the end of each conversion
- Results stored on injected data registers of each ADC.

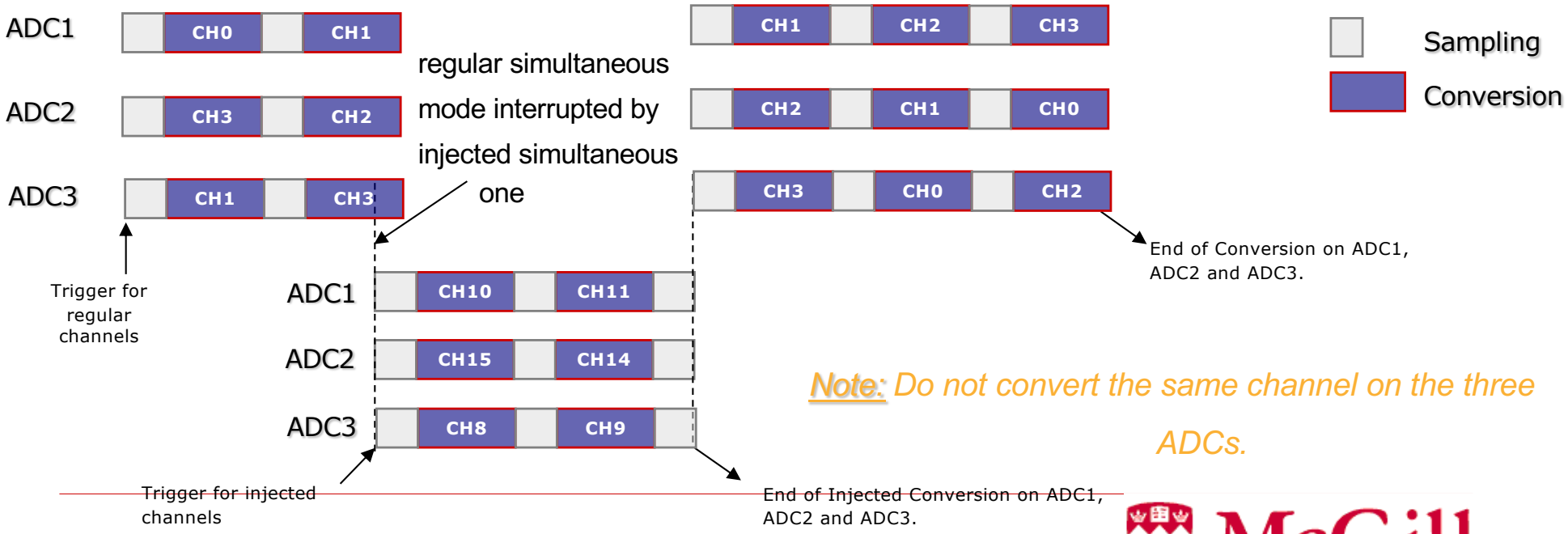
Alternate Trigger mode on 4 injected channels:



ADC Triple modes Combined Regular + Injected simultaneous mode

- Converts an injected and regular channel groups.
- The external triggers sources, which start the conversions, comes from ADC1 (simultaneous trigger provided to ADC2 and ADC3): injected simultaneous mode can interrupt all channels conversions.
- Results of injected channels stored on injected data registers of each ADC, and regular channels on the common data register ADC_CDR.

Combined Regular/Injected simultaneous mode on 4 regular channels and 2 injected channels:



Note: Do not convert the same channel on the three ADCs.

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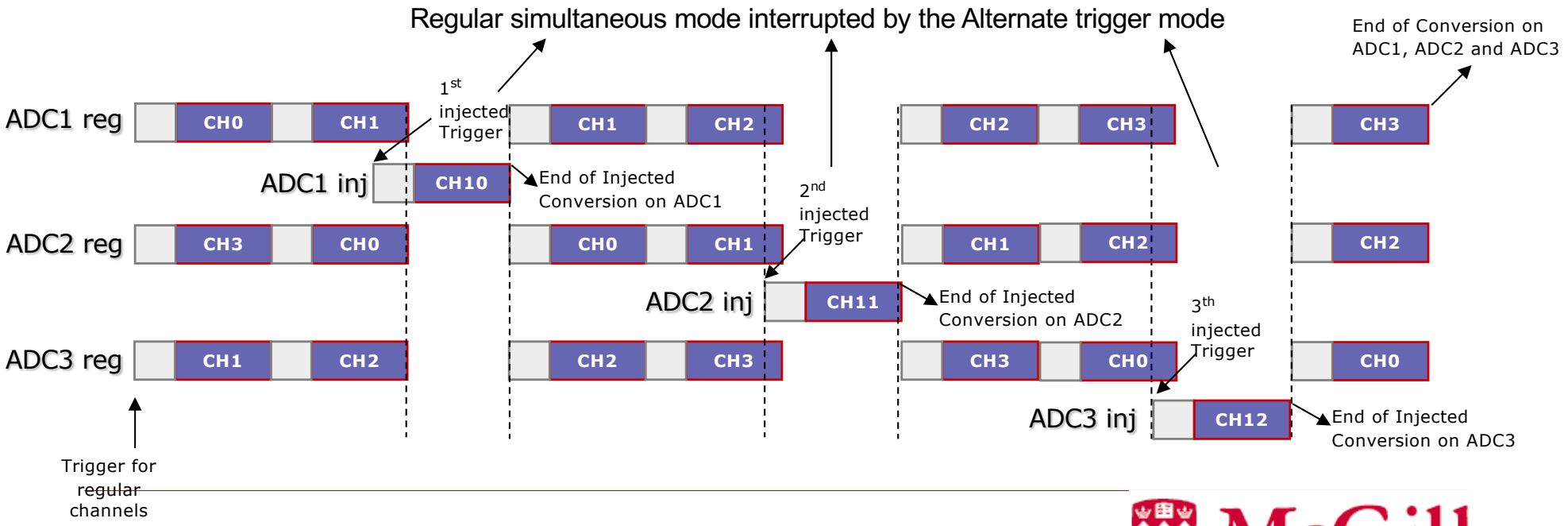
ADC Triple modes (7/7)

Combined Regular simultaneous + Alternate Trigger mode

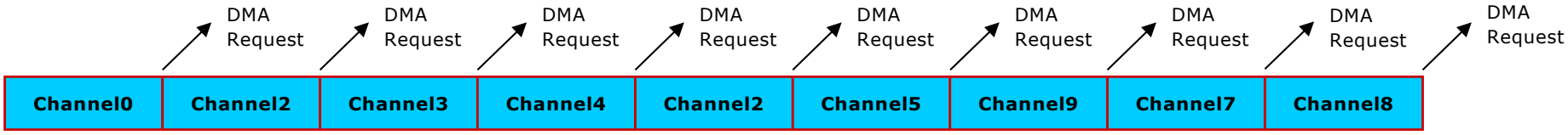
- Converts an injected and regular channel groups.
- The external triggers sources, which start the conversions, comes from ADC1 (simultaneous trigger provided to ADC2 and ADC3): alternate trigger mode can interrupt all channels conversions.
- Results of injected channels stored on injected data registers of each ADC, and regular channels on the common data register ADC_CDR.

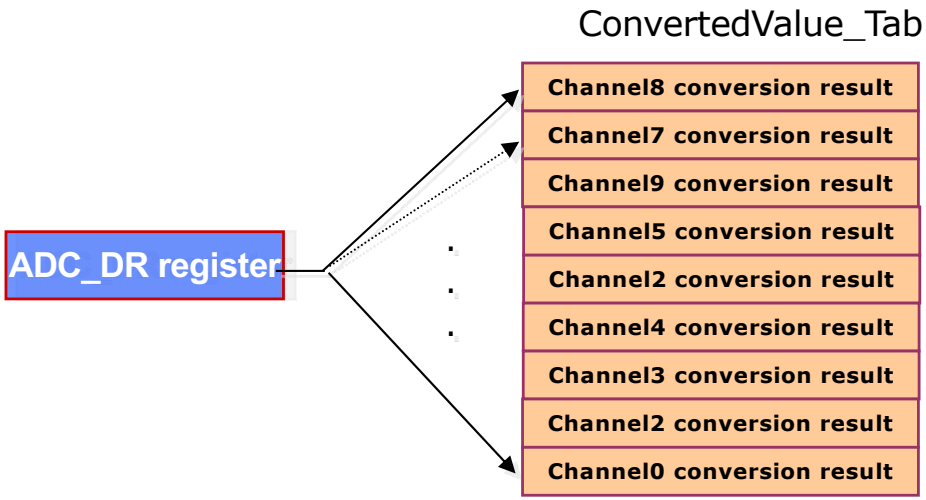
Combined Regular simultaneous + Alternate trigger mode:



ADC and DMA: Single mode

- DMA request generated on each ADC end of regular channel conversion (Not in injected channels)





Example:

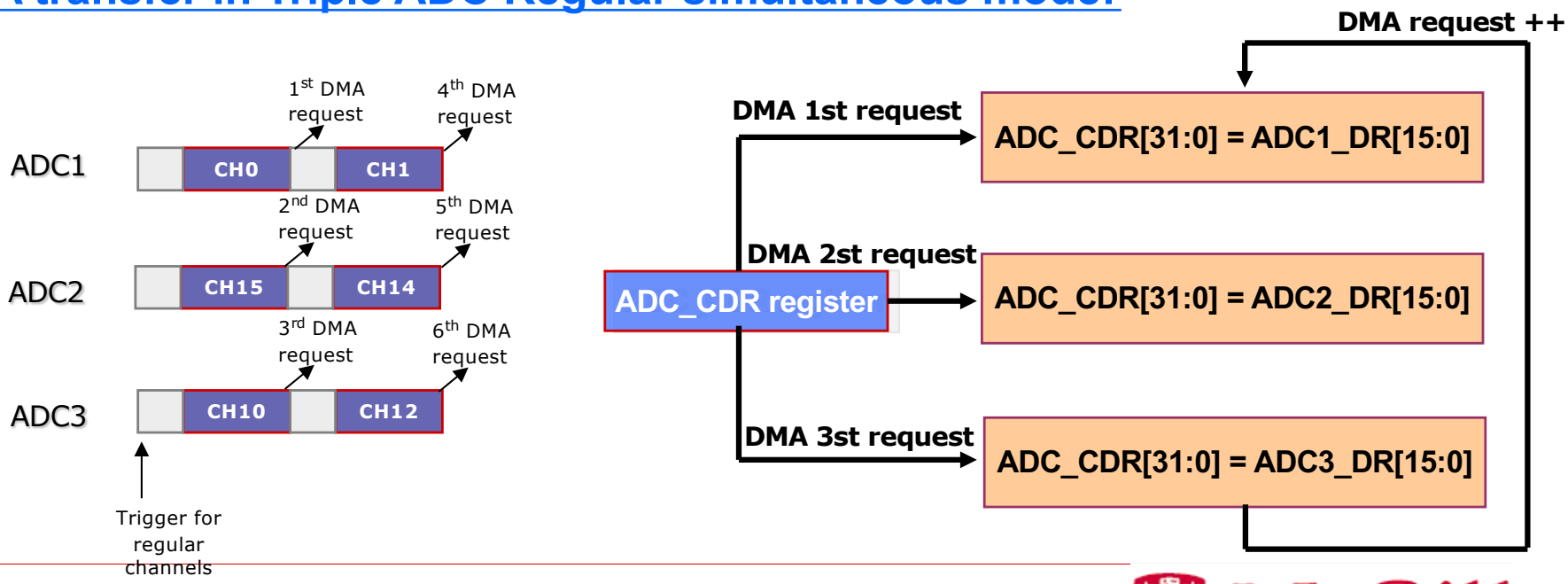
- Conversion of regular channels: 0, 2, 3, 4, 2, 5, 9, 7 and 8
- Converted data stored in ConvertedValue_Tab[9]
- DMA transfer enabled (destination address auto incremented)

Note: Each time DMA accessed to ADC_DR register, EOC flag is automatically cleared

ADC and DMA: ADC_DMA mode "1"

- Used in regular simultaneous Dual/Triple ADC mode
- DMA ensure the access to the converted regular channel values which are stored into the common data register ADC_CDR
- On each DMA request, a half-word representing an ADC-converted data item is transferred
- DMA bits in common control register ADC_CCR must be set at 0b01

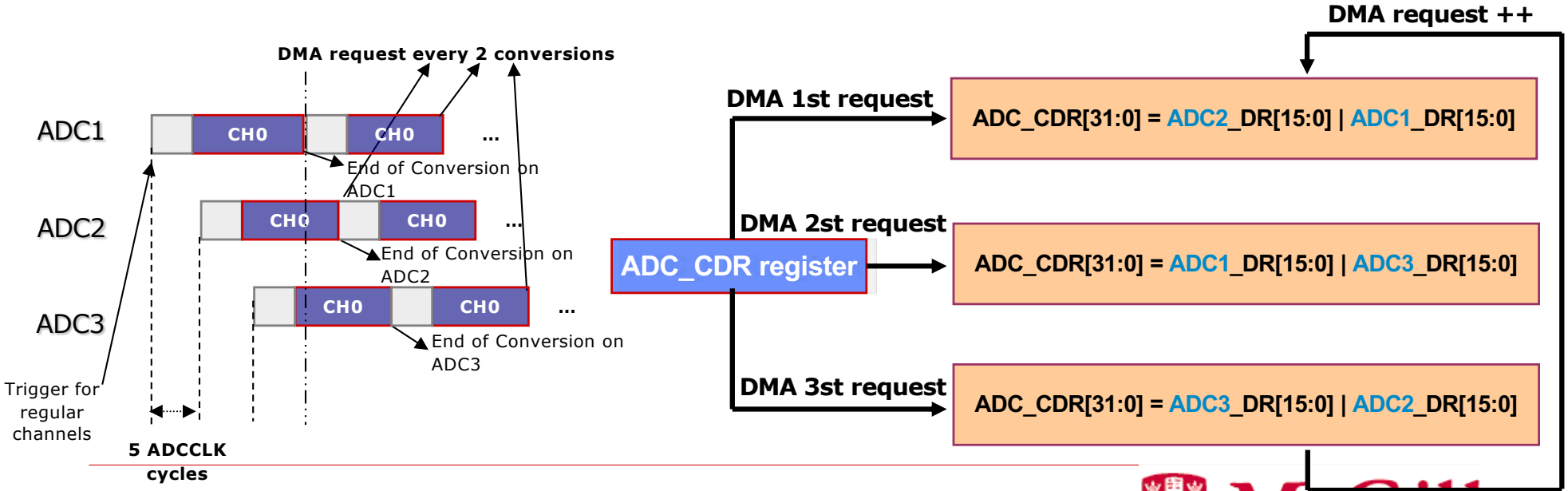
DMA transfer in Triple ADC Regular simultaneous mode:



ADC and DMA: ADC_DMA mode "2"

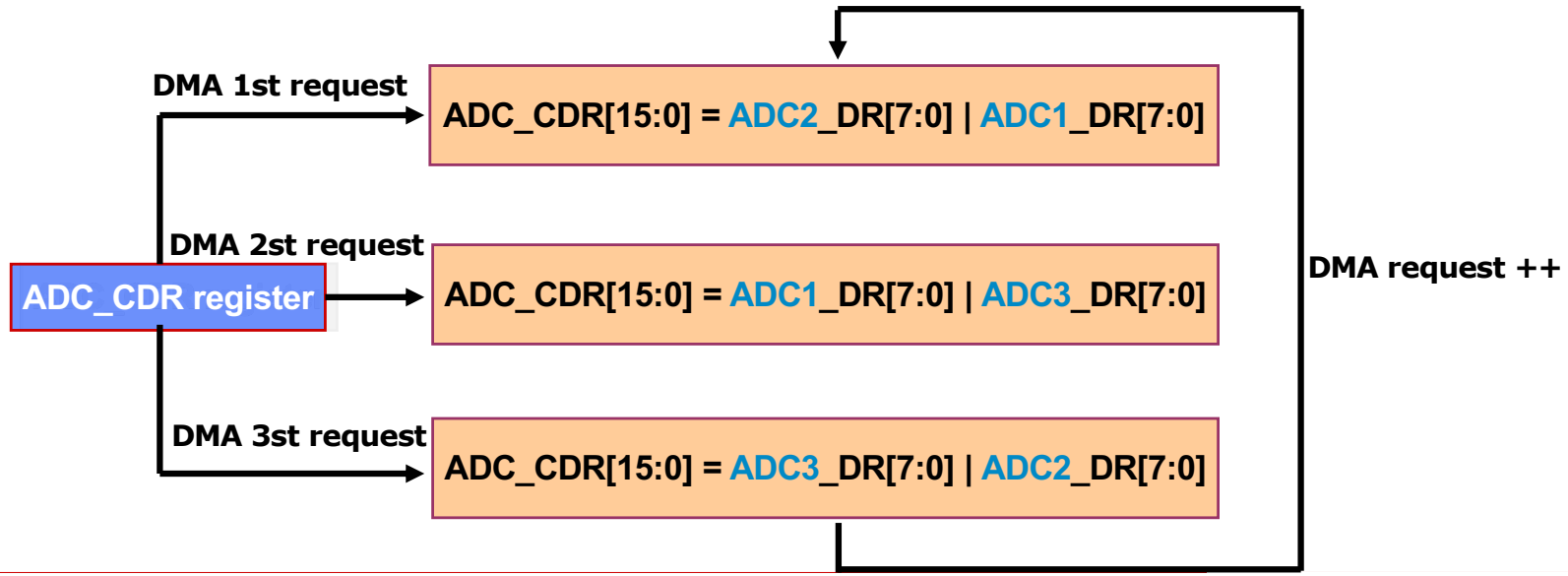
- Used in interleaved Dual/Triple ADC mode and in regular simultaneous Dual ADC mode
- DMA ensure the access to the converted regular channel values which are stored into the common data register ADC_CDR
- On each DMA request, two half-words representing two ADC-converted data items are transferred as a word
- DMA bits in common control register ADC_CCR must be set at 0b10

DMA transfer in Triple ADC interleaved mode:



ADC and DMA(4/4): ADC_DMA mode "3"

- Used in interleaved Dual/Triple ADC mode and in regular simultaneous Dual ADC mode with 6-bits and 8-bits resolutions
- DMA ensure the access to the converted regular channel values which are stored into the common data register ADC_CDR
- On each DMA request, two bytes representing two ADC-converted data items are transferred as a half-word
- DMA bits in common control register ADC_CCR must be set at 0b11



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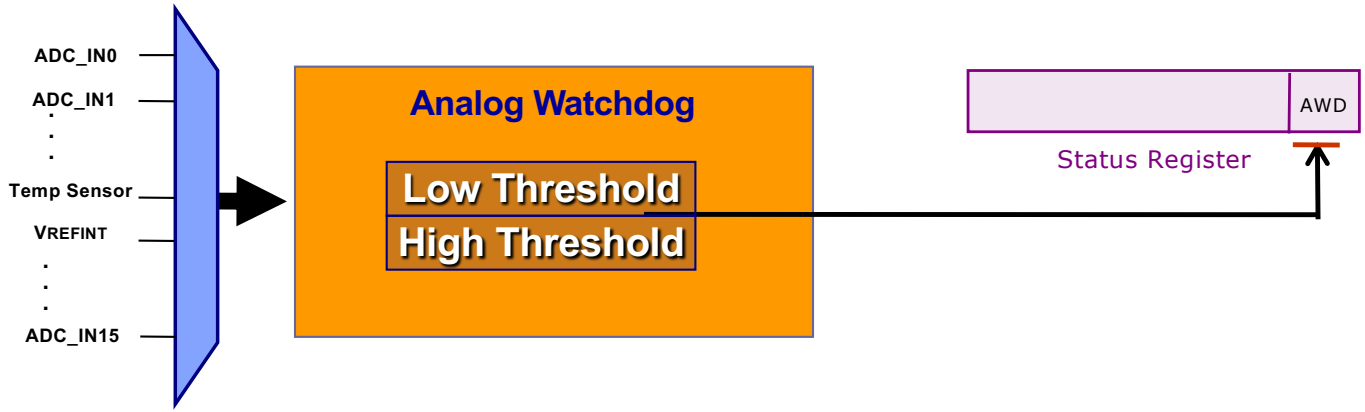
ADC Analog Watchdog

- 12-bit programmable analog watchdog low and high thresholds
- Enabled on one or all converted channels: one regular or/and injected channel, all injected or/and regular channels
- Interrupt generation on low or high thresholds detection



ADC Flags and interrupts

OVR : Overrun detection when regular converted data are lost

EOC : « Regular channel end of conversion » to indicate (depending on EOCS bit) the end of :

➔ a regular **CHANNEL** conversion

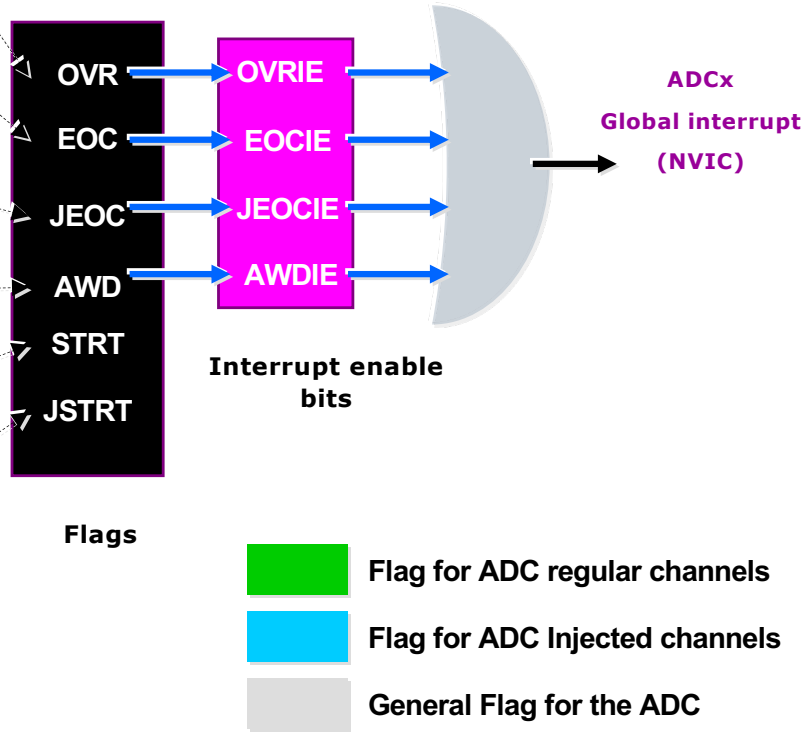
➔ sequence of regular **GROUP** conversions .

JEOC : « Injected channel end of conversion» to indicate at the end of injected **GROUP** conversion

AWD : « Analog watchdog » to indicate if the converted voltage crosses the programmed thresholds values.

STRT: « Regular channel start » to indicate when regular **CHANNEL** conversion starts.

JSTRT: « Injected channel start **»** to indicate hardware when injected **GROUP** conversion starts.



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Temp. Sensor, V_{REF} & V_{BAT} Monitors

- Temperature Sensor internally connected to ADC1_IN17 input
- Measured value: V_{TS}; Two factory-calibrated points V_{Cal1} & V_{Cal2}

  $$\text{Temp } [^oC] = f(V_{TS}\text{-}V_{Cal1})/\text{Avg\_Slope} + 30$$

  - Reading and conversion procedure: L4+ Reference Manual, page 689
  - Locations for calibrated values: STM32L4S5 Datasheet, page 44, Table 8
- V_{REF} voltage connected to ADC1_IN0
  - Calibrated voltage stored as per STM32L4S5 Datasheet, page 44, Table 9
- Also, V_{BAT} input voltage can be converted on ADC1_IN18 input for Battery monitoring
  - As V_{BAT} voltage could be higher than VDDA, for correct operating condition of the ADC, the Input voltage is V_{BAT} followed by a bridge divider by 2

Quiz

- What is the maximum ADC clock frequency?

  _____

- What are the different ADC resolution possibilities?

  _____

- What is the minimum sampling time of the ADC?

  _____

- How many modes the ADC offers in Multi mode? What are they?

  _____

- What is the maximum “Msample/s” that ADCs could achieve ? In which mode?

  _____

- What are the different ADC_DMA modes and uses?

  _____

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