

Using the VGA connector



Using the VGA

Master's Degree in Automation Engineering

Digital Programmable Systems

Department of Electrical and Information Engineering

Politecnico di Bari

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Using the VGA connector



Useful references

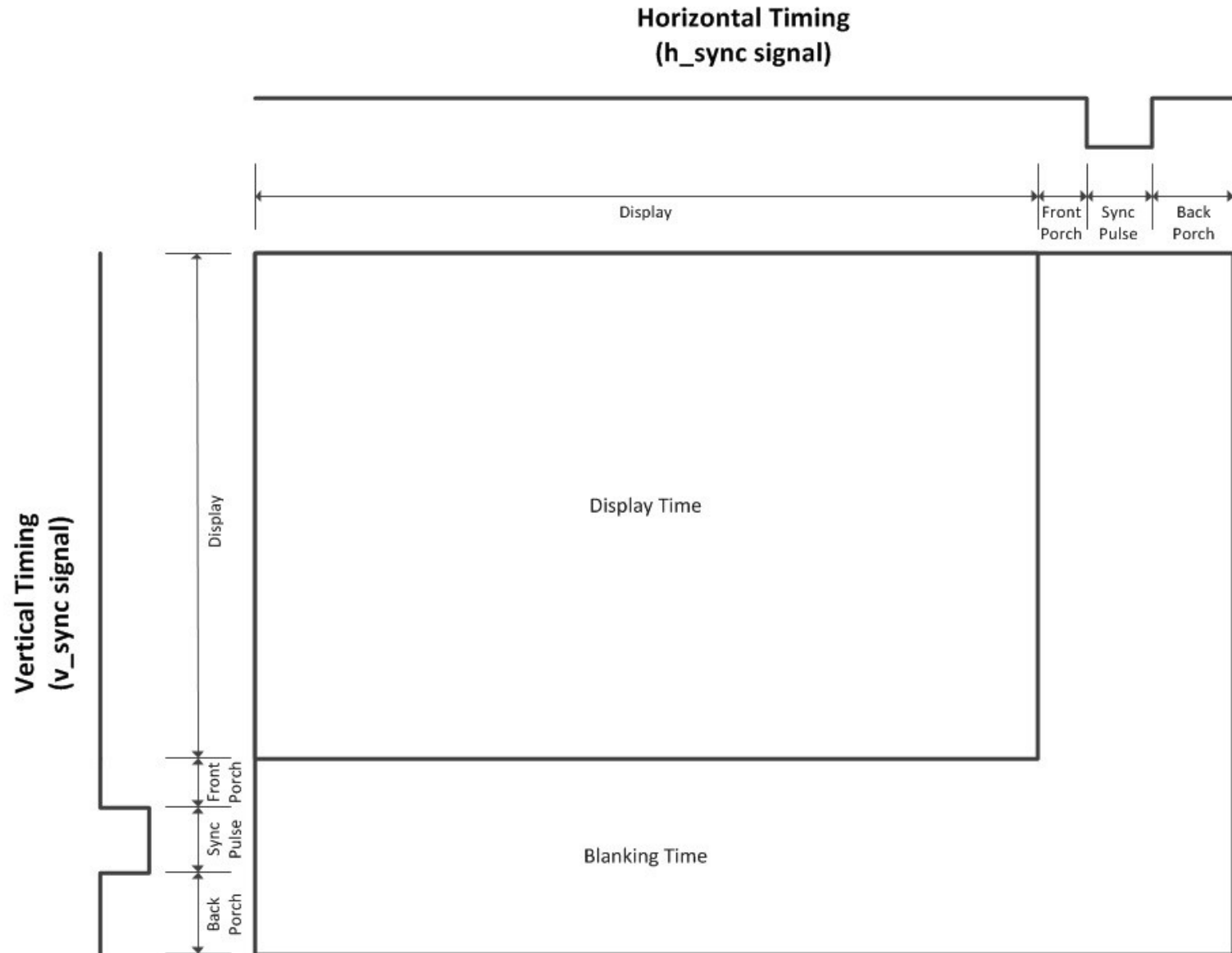
For the explanation of the VGA

<https://forum.digikey.com/t/vga-controller-vhdl/12794>

For the timing of the VGA

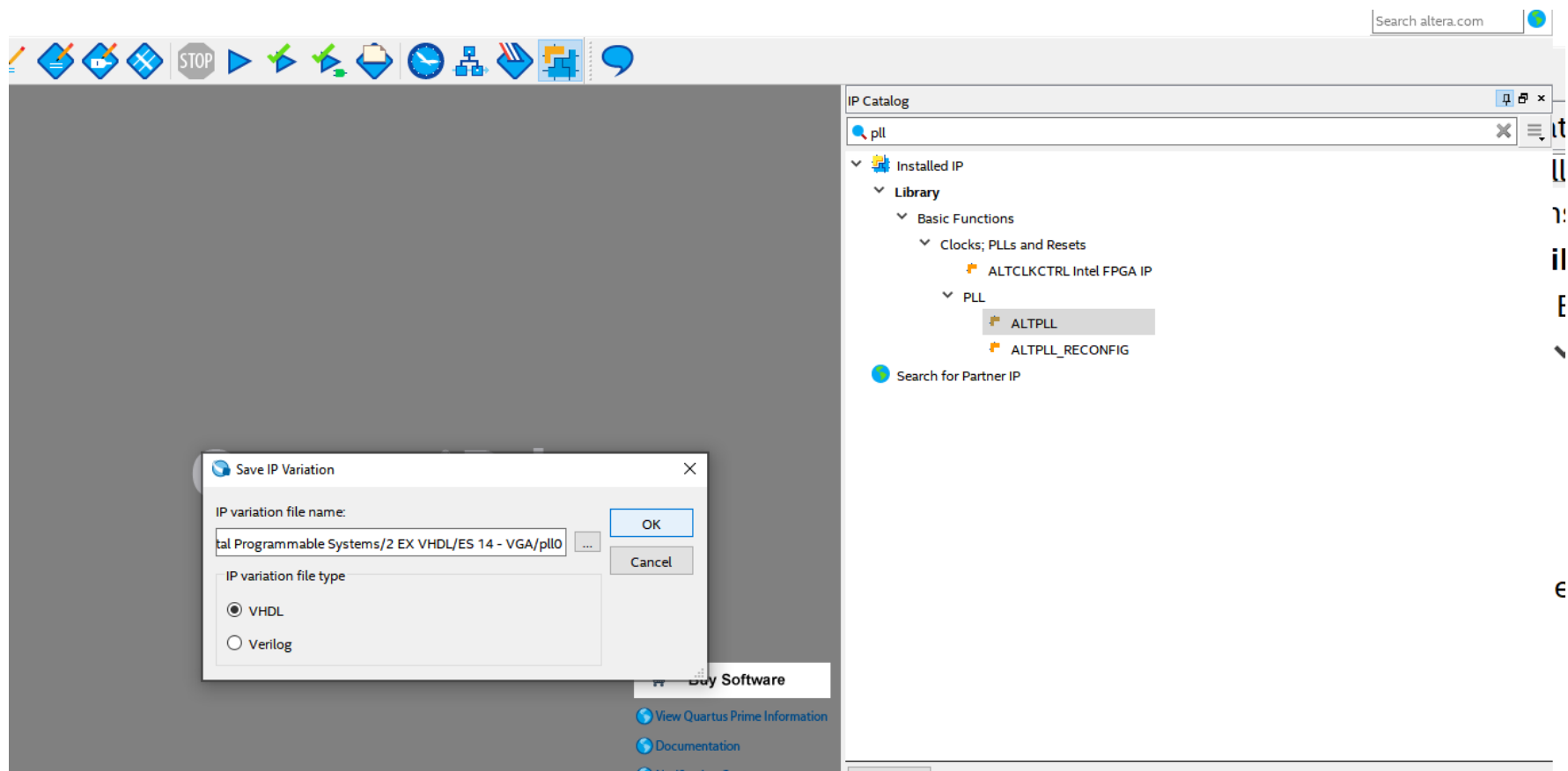
<http://tinyvga.com/vga-timing>

Using the VGA connector



Using the VGA

Create a new project



Using the VGA

MegaWizard Plug-In Manager [page 1 of 12]

ALTPLL [About](#) [Documentation](#)

1 Parameter Settings 2 PLL Reconfiguration 3 Output Clocks 4 EDA 5 Summary

General/Modes Inputs/Lock Bandwidth/SS Clock switchover

Currently selected device family: MAX 10 ☒ Match project/default

pll0

inclk0 areset c0 locked

inclk0 frequency: 50.000 MHz
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	1/1	0.00	50.00

MAX 10

Able to implement the requested PLL

General

Which device speed grade will you be using? Any

☐ Use military temperature range devices only

What is the frequency of the inclk0 input? 50.000 MHz

☐ Set up PLL in LVDS mode Data rate: Not Available Mbps

PLL Type

Which PLL type will you be using?

☐ Fast PLL ☐ Enhanced PLL ☒ Select the PLL type automatically

Operation Mode

How will the PLL outputs be generated?

☒ Use the feedback path inside the PLL

☒ In normal mode

☐ In source-synchronous compensation Mode

☐ In zero delay buffer mode

☐ Connect the fbimic port (bidirectional)

☐ With no compensation

☐ Create an 'fbim' input for an external feedback (External Feedback Mode)

Which output clock will be compensated for? c0

Cancel < Back Next > Finish

Using the VGA

MegaWizard Plug-In Manager [page 2 of 12]

ALTPLL [About](#) [Documentation](#)

1 Parameter Settings 2 PLL Reconfiguration 3 Output Clocks 4 EDA 5 Summary

General/Modes > Inputs/Lock > Bandwidth/SS > Clock switchover >

pll0

inclk0
areset

inclk0 frequency: 50.000 MHz
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	1/1	0.00	50.00

c0

MAX 10

Able to implement the requested PLL

Optional Inputs

- ☐ Create an 'pllena' input to selectively enable the PLL
- ☒ Create an 'areset' input to asynchronously reset the PLL
- ☐ Create an 'pfdena' input to selectively enable the phase/frequency detector

Lock Output

- ☐ Create 'locked' output
- ☐ Enable self-reset on loss lock

Advanced Parameters
Using these parameters is recommended for advanced users only

- ☐ Create output file(s) using the 'Advanced' PLL parameters
 - Configurations with output clock(s) that use cascade counters are not supported

Cancel < Back Next > Finish

Using the VGA

MegaWizard Plug-In Manager [page 6 of 12]

ALTPLL [About](#) [Documentation](#)

1 Parameter Settings 2 PLL Reconfiguration 3 **Output Clocks** 4 EDA 5 Summary

clk c0 > clk c1 > clk c2 > clk c3 > clk c4 >

pll0

inclk0
areset

inclk0 frequency: 50.000 MHz
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	58/15	0.00	50.00

c0

MAX 10

c0 - Core/External Output Clock

Able to implement the requested PLL

☒ Use this clock

Clock Tap Settings

☐ Enter output clock frequency:

☒ Enter output clock parameters:

	Requested Settings	Actual Settings
Enter output clock frequency:	193.33000000 MHz	193.333333
Clock multiplication factor	58	58
Clock division factor	15	15
Clock phase shift	0.00 deg	0.00
Clock duty cycle (%)	50.00	50.00

<< Copy

Description	Val
Primary clock VCO frequency (MHz)	58...
Modulus for M counter	58

Per Clock Feasibility Indicators

c0 c1 c2 c3 c4

Note: The displayed internal settings of the PLL is recommended for use by advanced users only

Cancel < Back Next > Finish

Using the VGA

MegaWizard Plug-In Manager [page 12 of 12]

ALTPLL [About](#) [Documentation](#)

1 Parameter Settings 2 PLL Reconfiguration 3 Output Clocks 4 EDA 5 Summary

pll0

inclk0
areset
c0

inclk0 frequency: 50.000 MHz
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	58/15	0.00	50.00

MAX 10

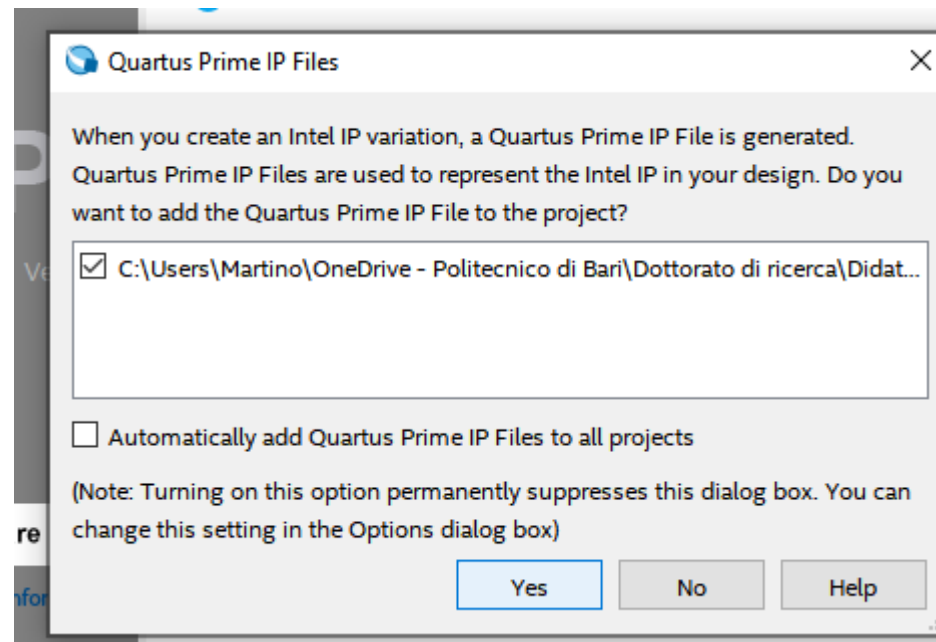
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.

The MegaWizard Plug-In Manager creates the selected files in the following directory:
C:\Users\Martino\OneDrive - Politecnico di Bari\Dottorato di ricerca\Didattica\Digital Programmable Systems\2 EX VHDL\ES 14 - VGA\

File	Description
<input checked="" type="checkbox"/> pll0.vhd	Variation file
<input checked="" type="checkbox"/> pll0.ppf	PinPlanner ports PPF file
<input type="checkbox"/> pll0.inc	AHDL Include file
<input checked="" type="checkbox"/> pll0.cmp	VHDL component declaration file
<input type="checkbox"/> pll0.bsf	Quartus Prime symbol file
<input type="checkbox"/> pll0_inst.vhd	Instantiation template file

Cancel < Back Next > Finish

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