Using IP in Quartus II

ADC with DE- series boards

Master Degree in Automation Engineering
Digital Programmable Systems
Department of Electrical and Information Engineering
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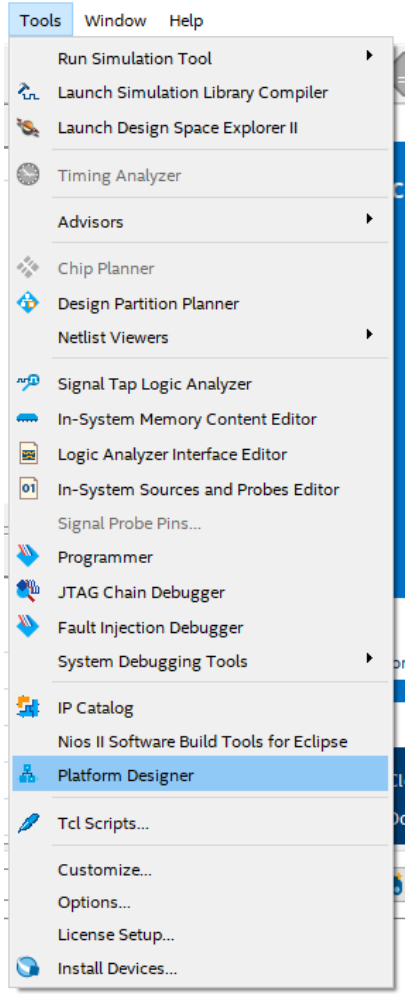
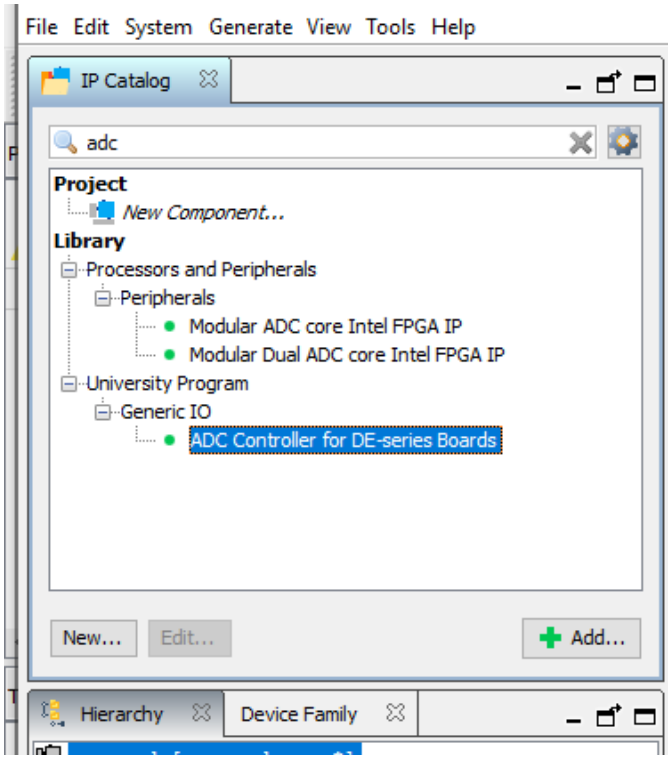
ADC with DE- series boards

1) Open a new blank project

2) Go on Tools -> Platform Designer



3) Search on the left for "ADC Controller for DE-series boards" and double click



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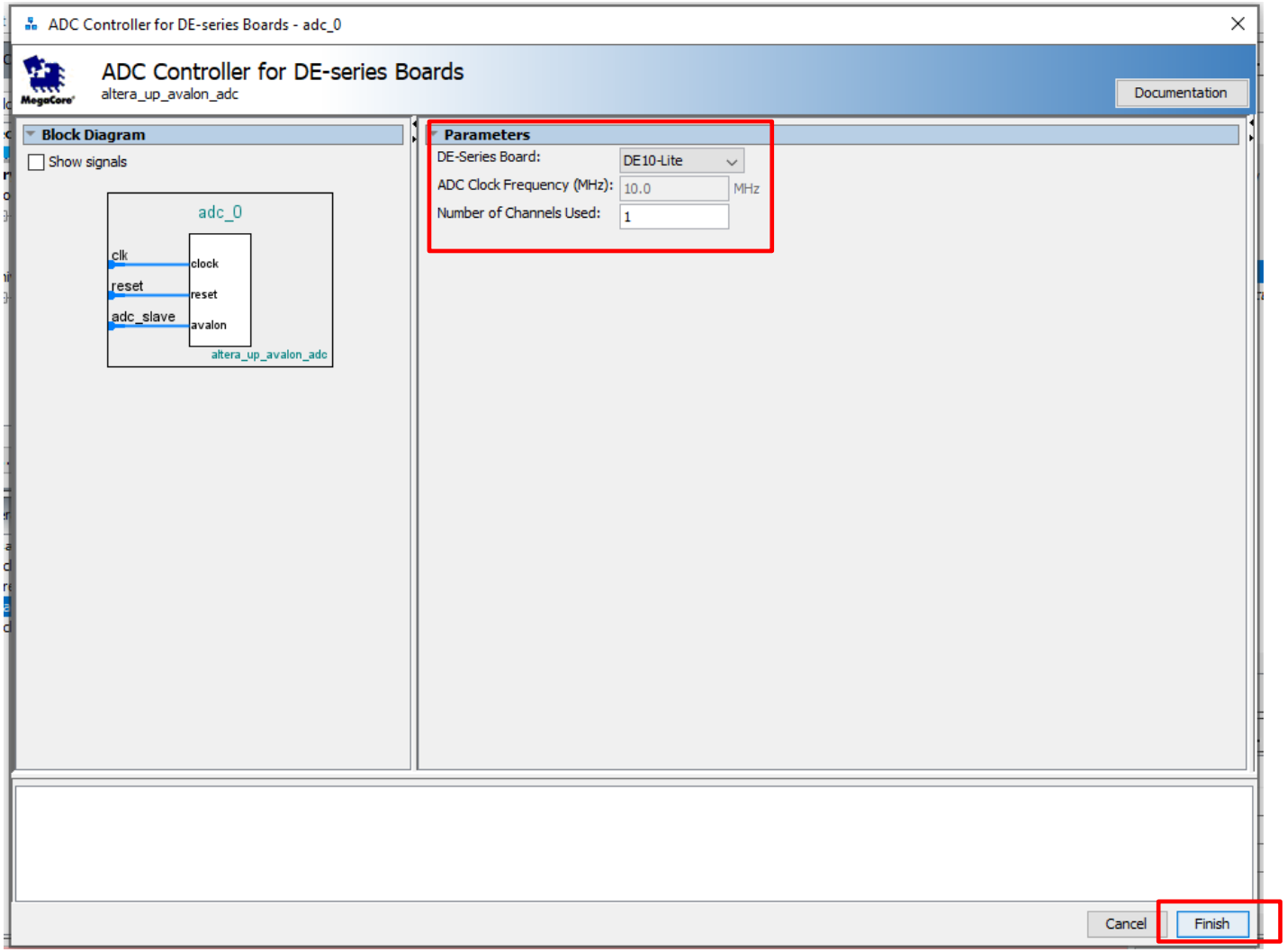
4) Set parameters as in Fig and click on "Finish"



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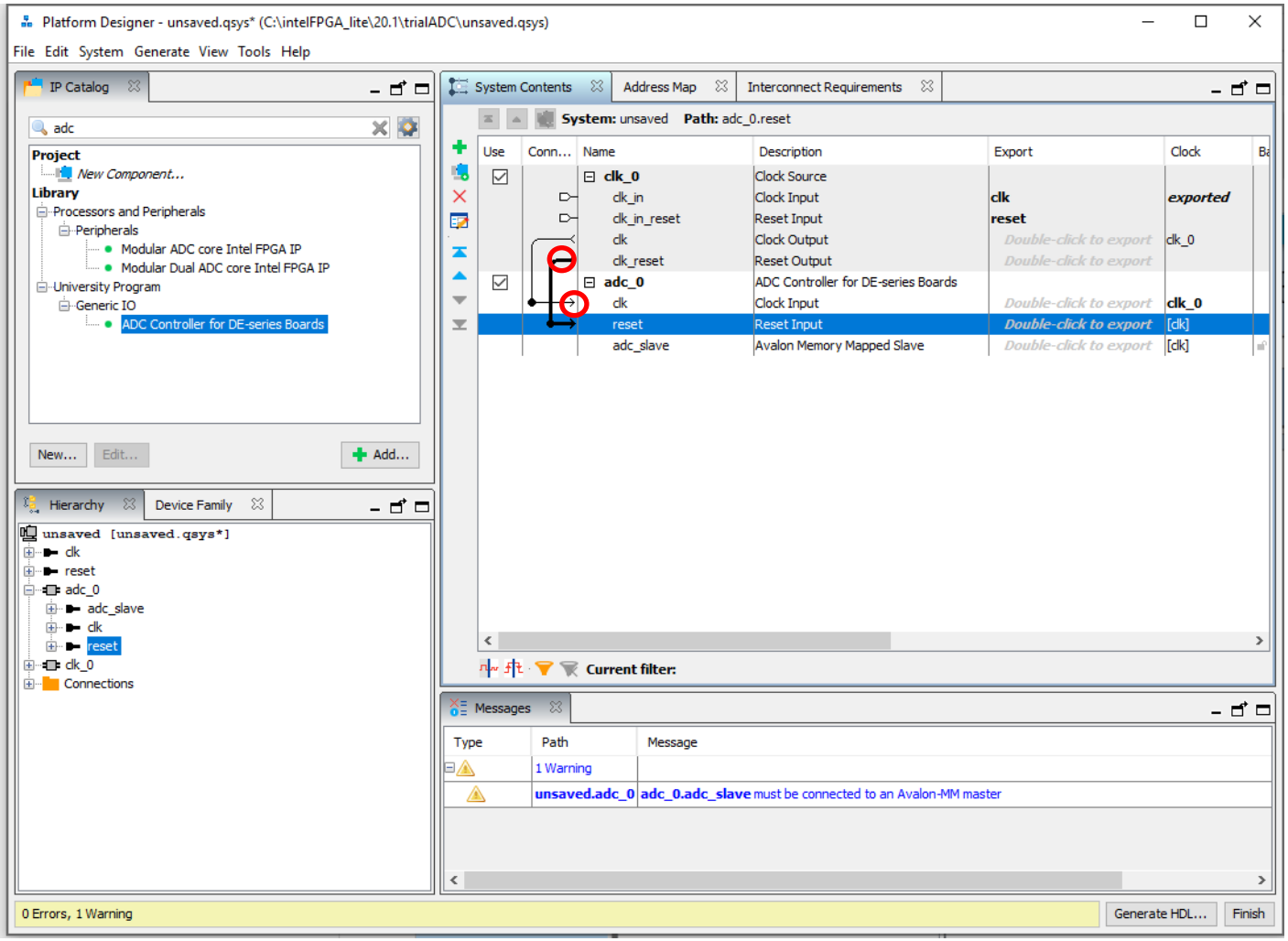
5) Click on the grey dots to activate the connections (the links should become black)



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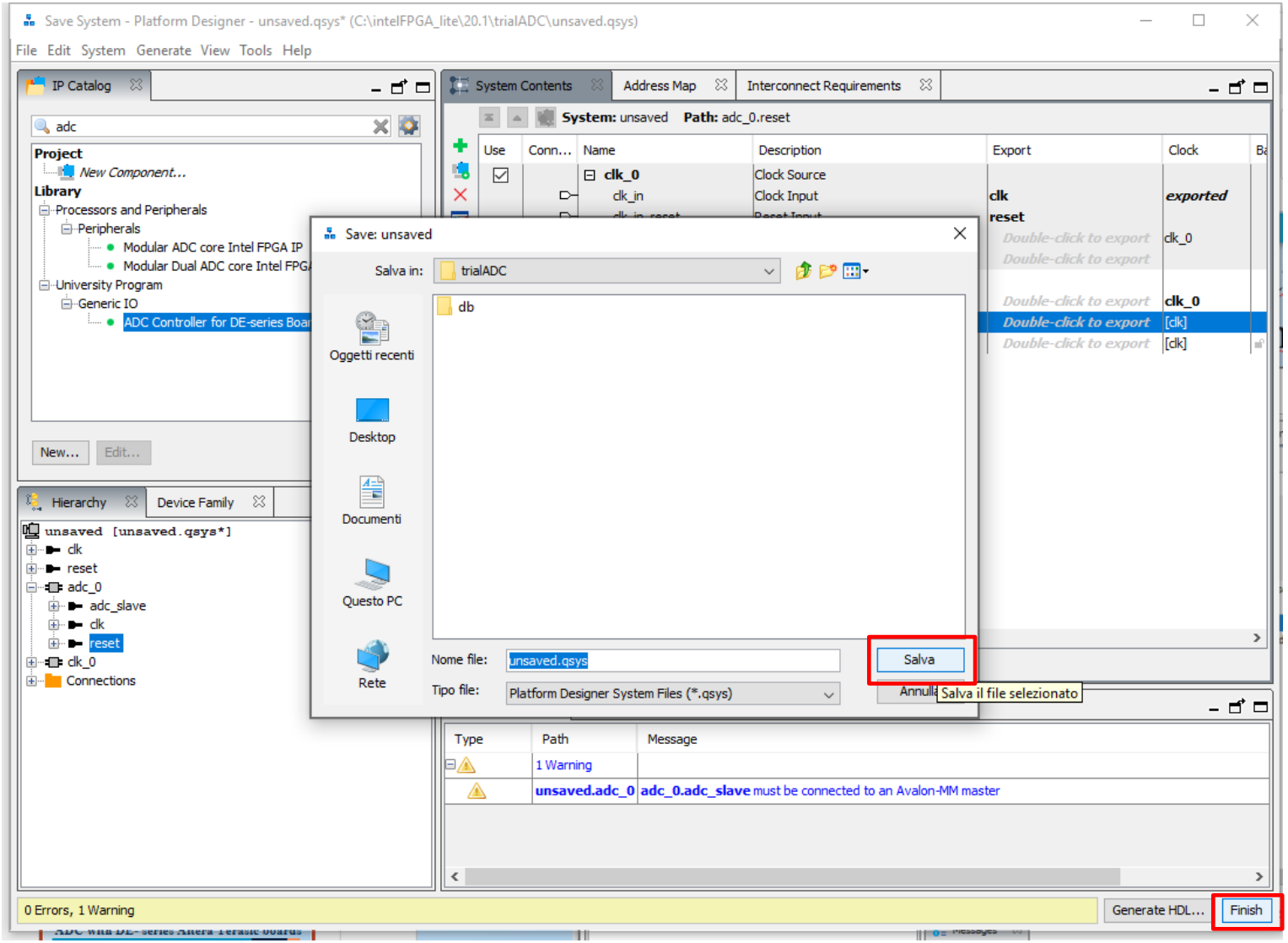
6) Click on "Finish" and save when asked



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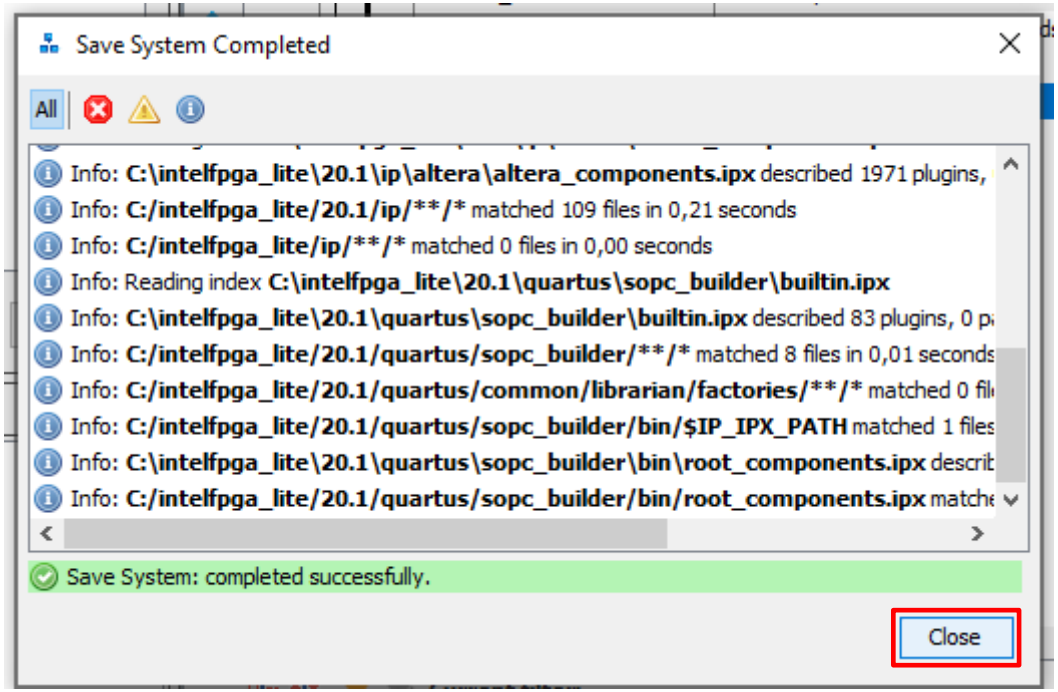
7) Click on "Close"



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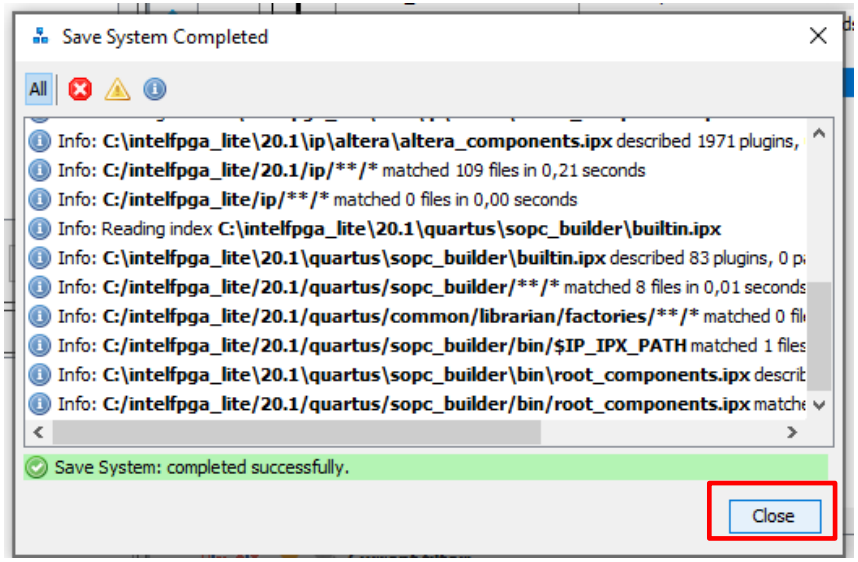
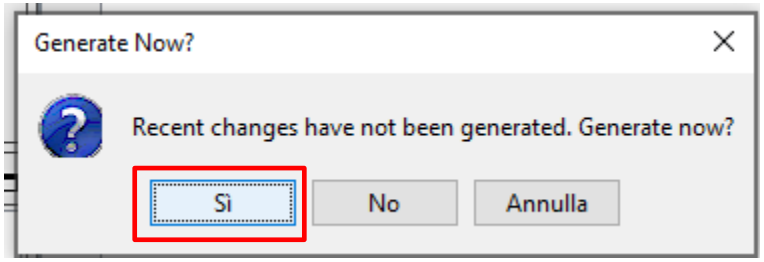
8) Click on "Close"



9) Click on "Yes" when asked to generate the code



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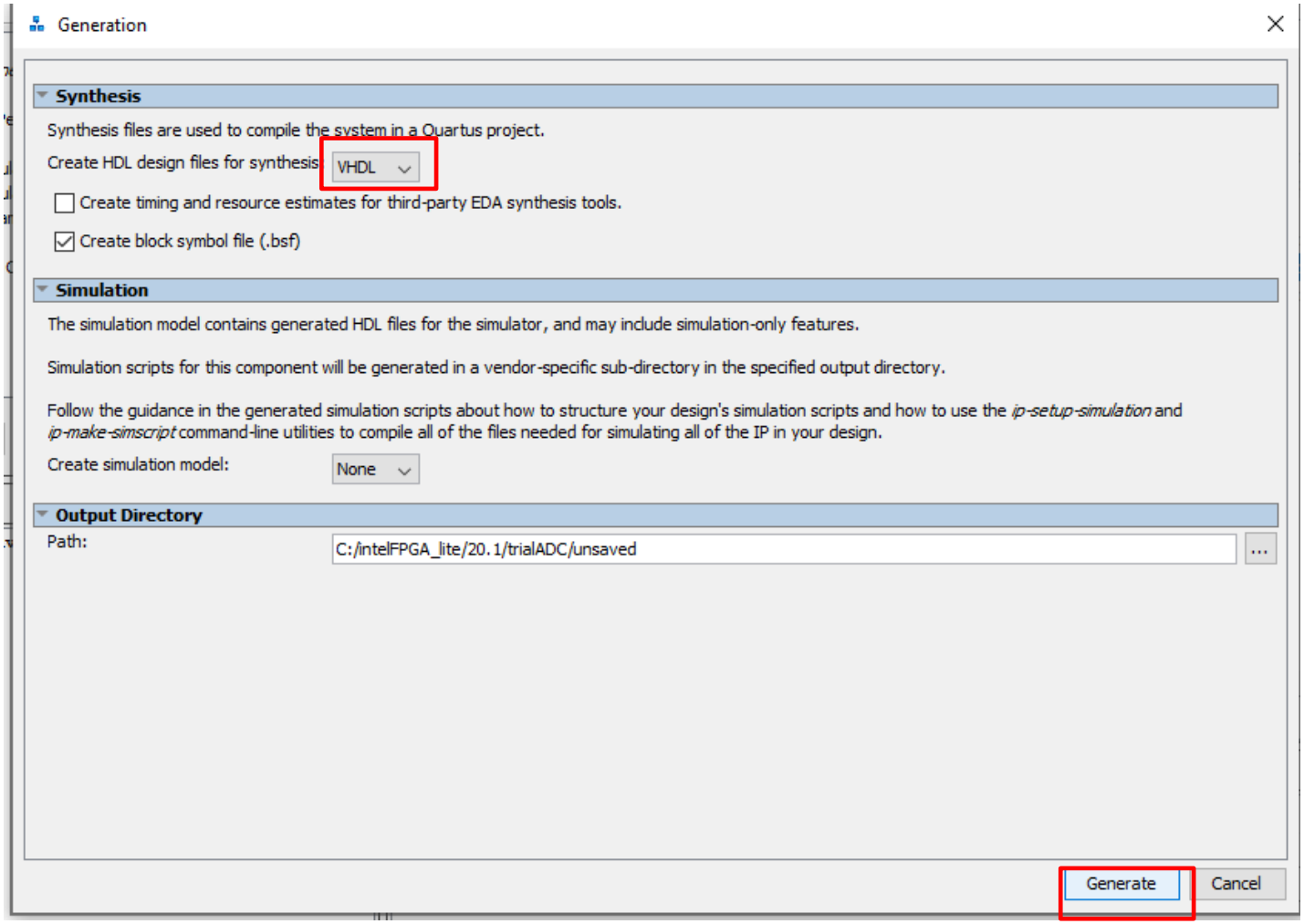
10) Select "VHDL" and click "Generate"



11) Click on "Finish"

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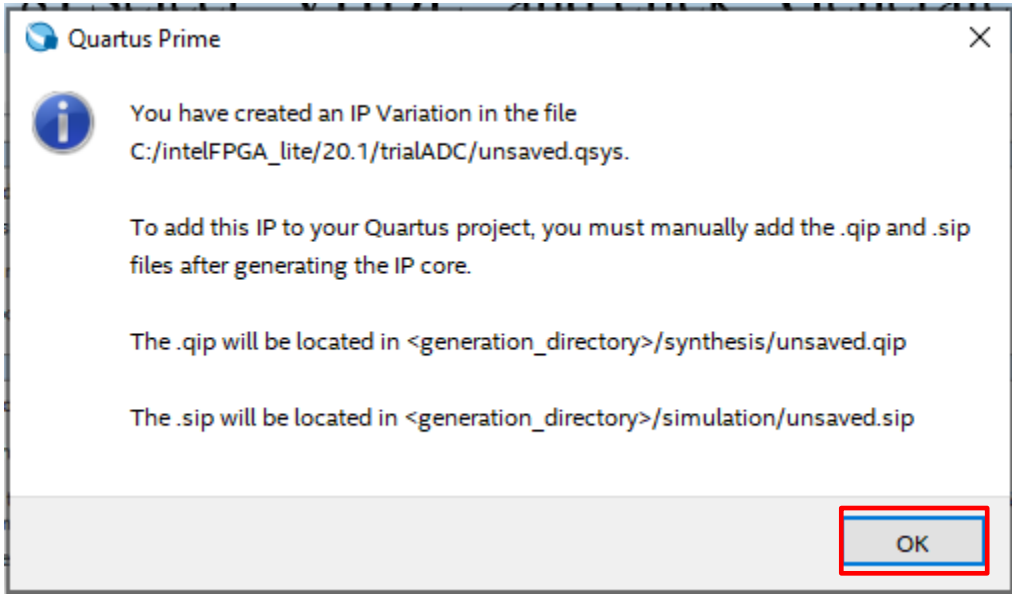
12) Click on "Finish" and then "OK"



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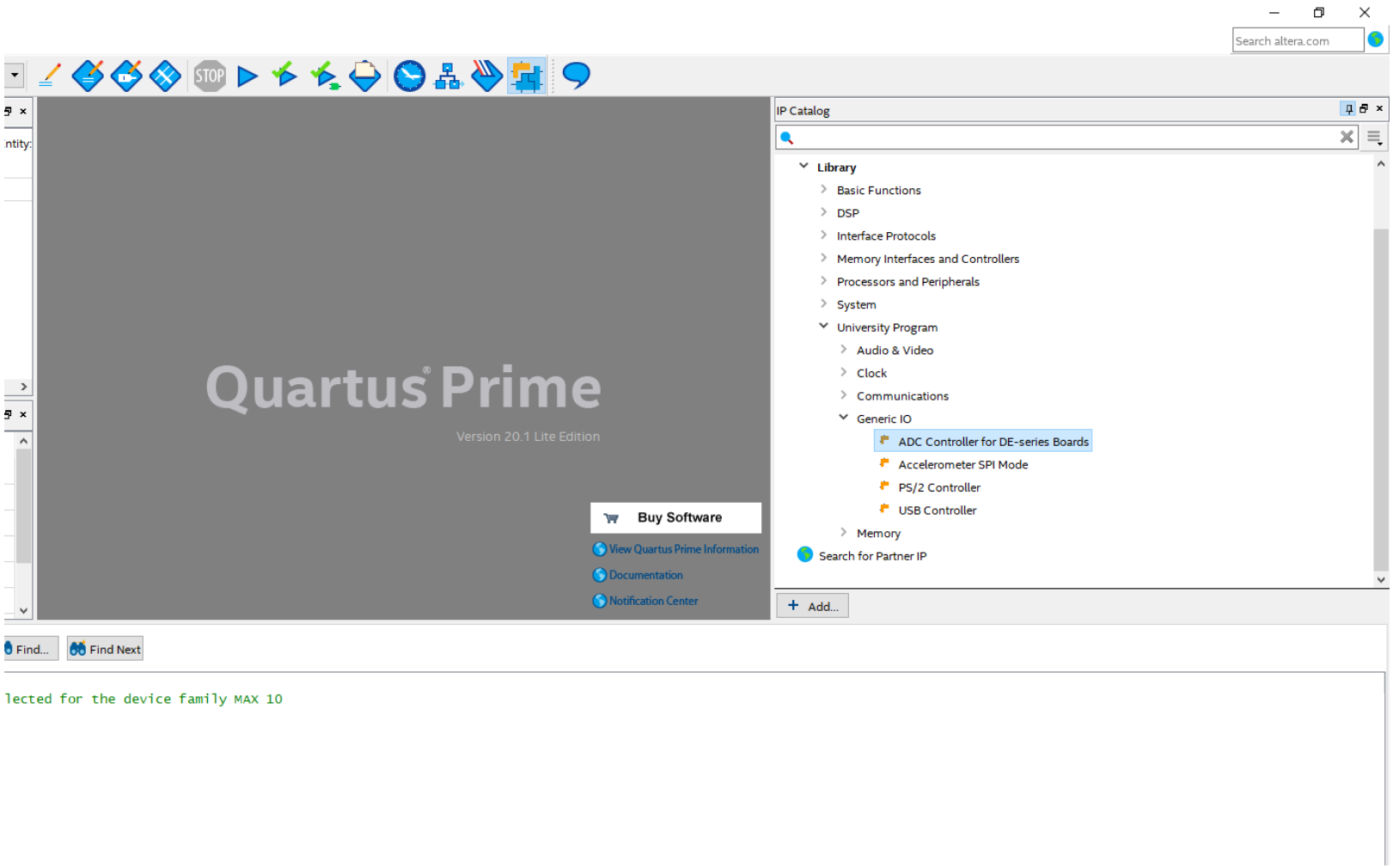
13) Double click on the IP catalog on "ADC Controller for DE-series Boards"



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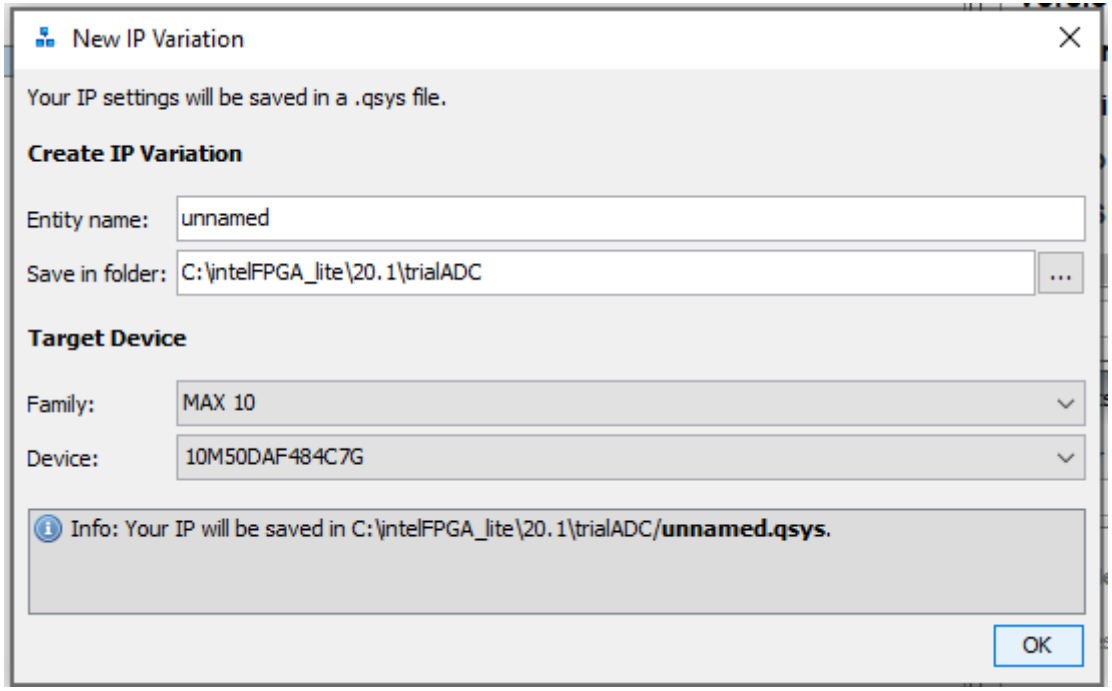
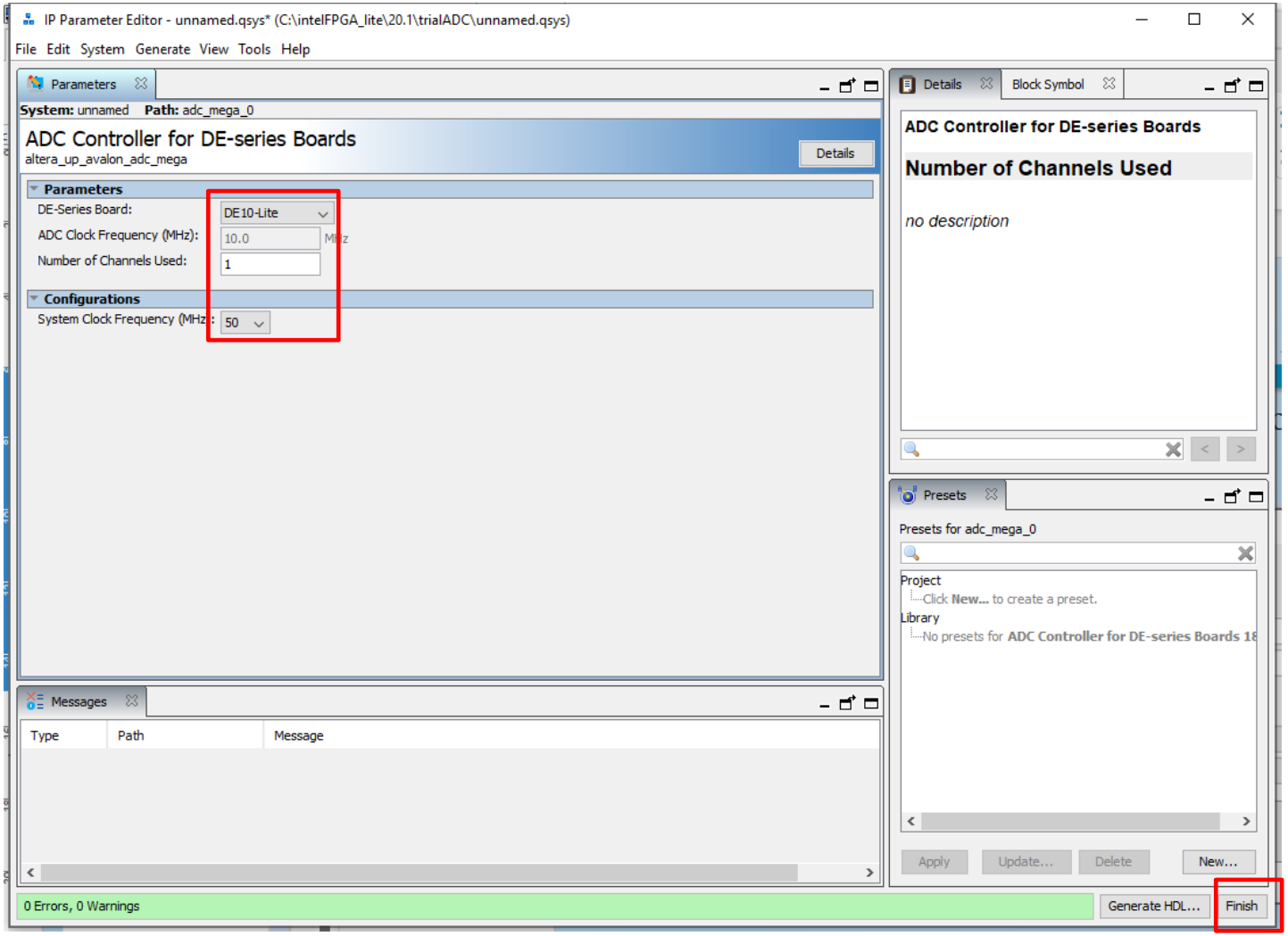
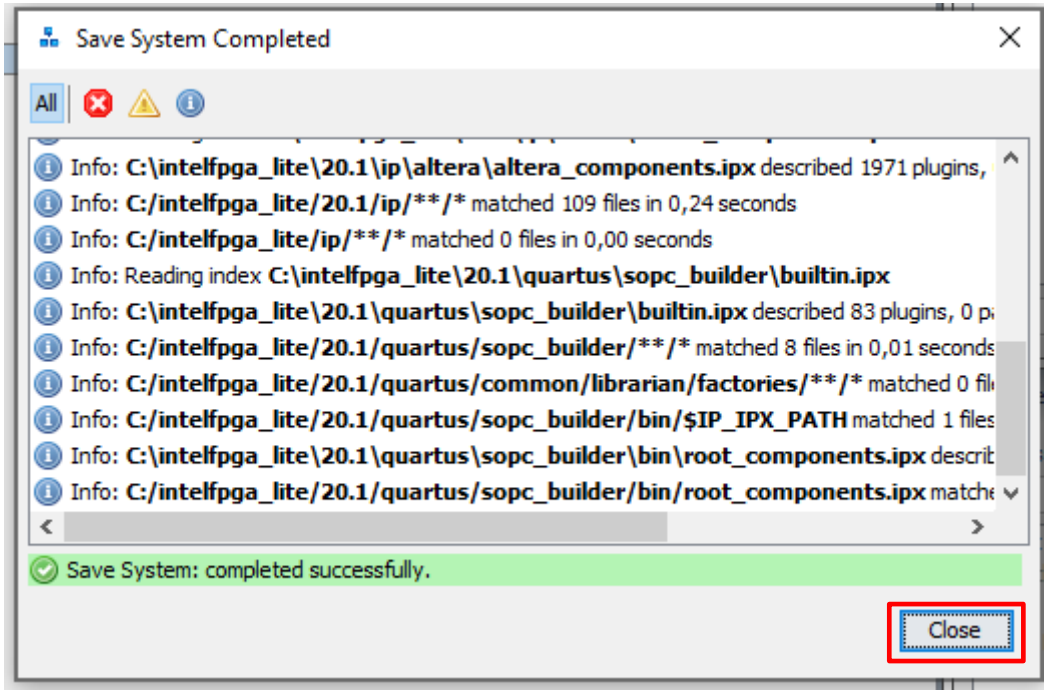
14) Press OK when asked to save

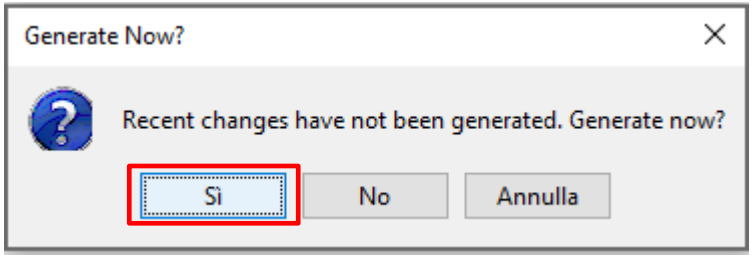


ADC with DE- series boards

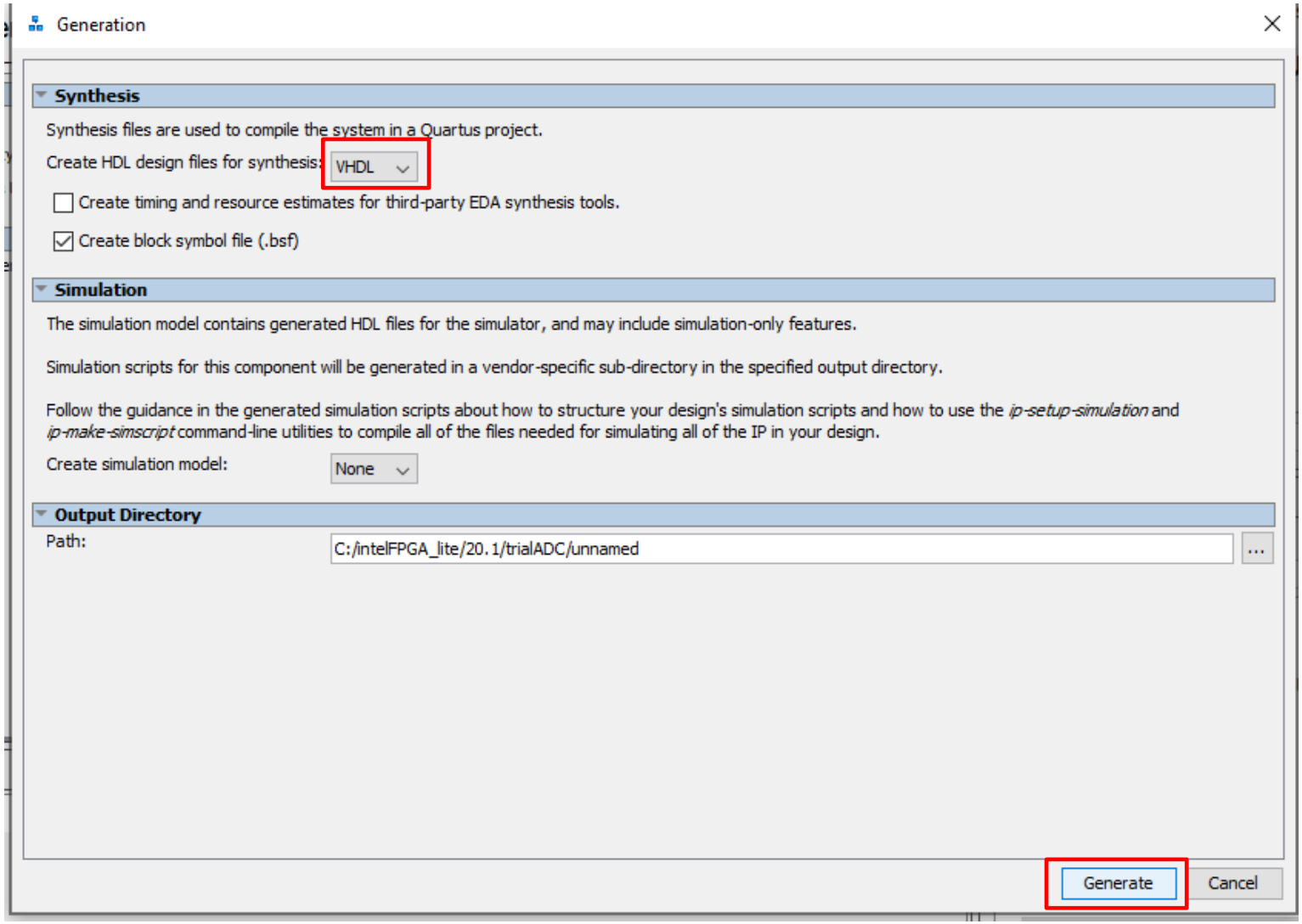


ADC with DE- series boards

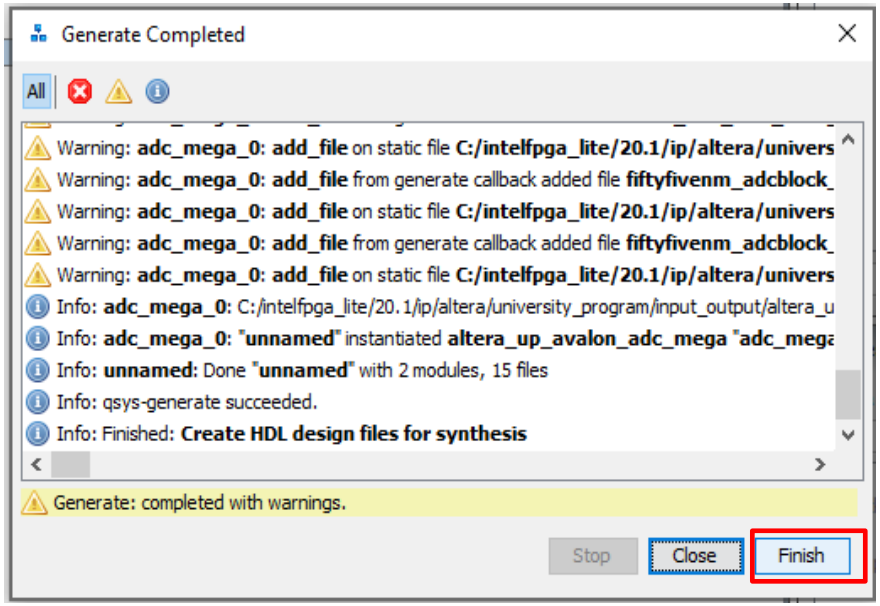


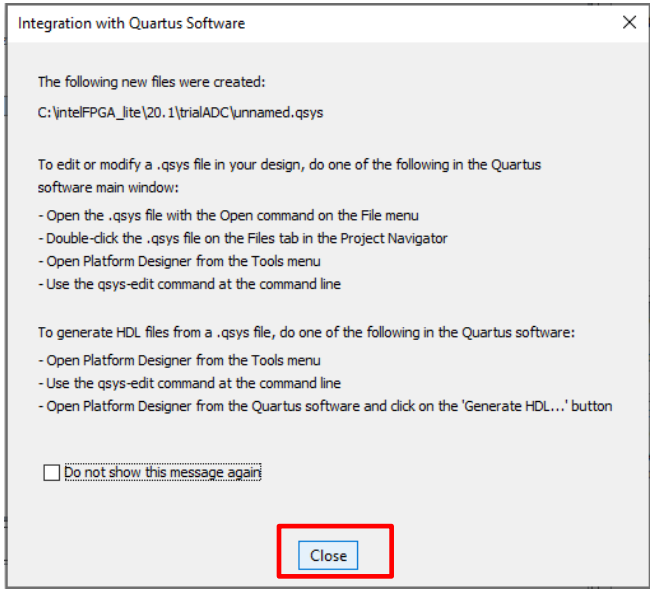


ADC with DE- series boards



ADC with DE- series boards





15) Click on Finish, Close and then Ok

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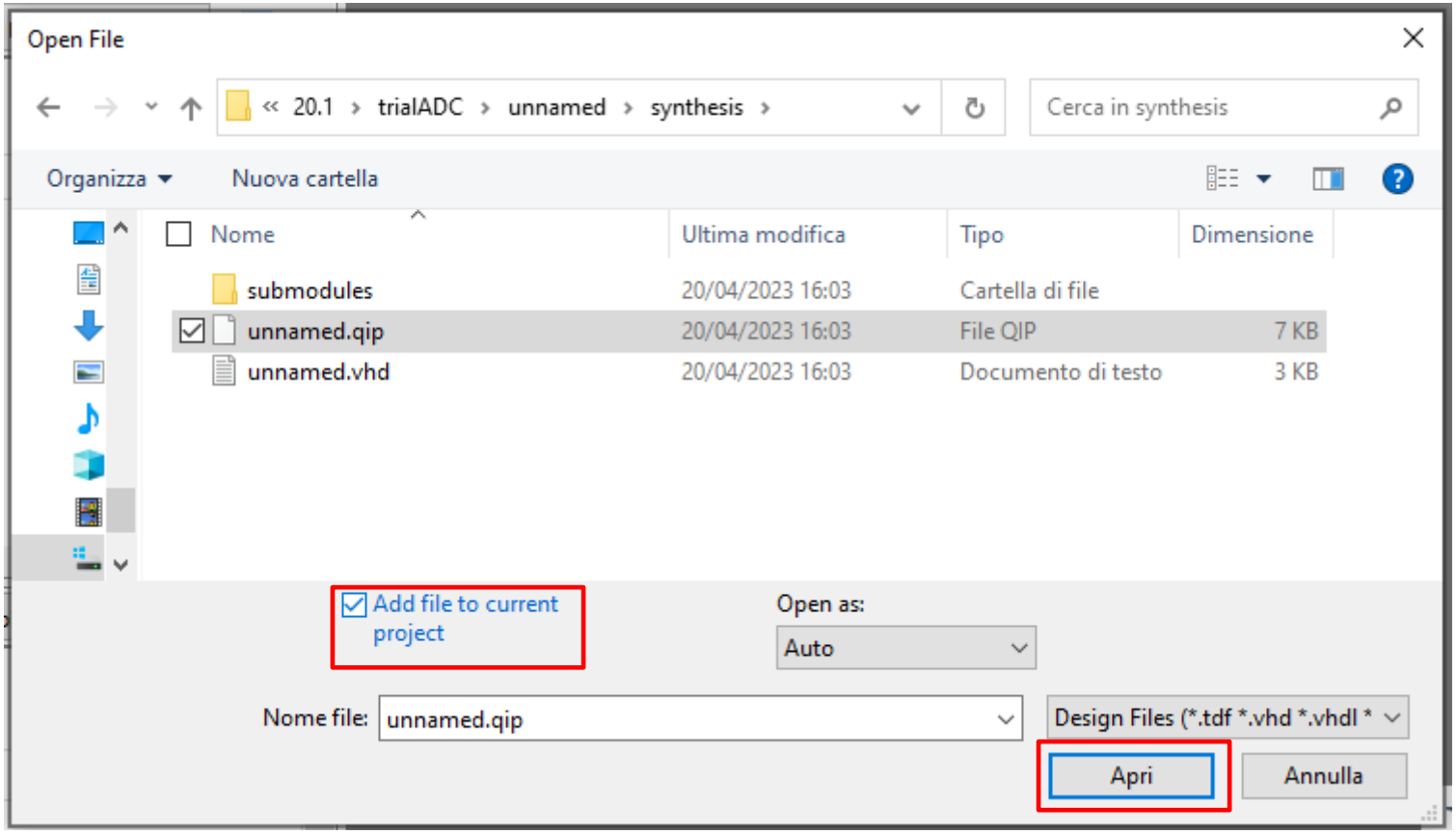
16) Open the .qip file just created (…unnamed/synthesis/unnamed.qip)

ADD it to the project!



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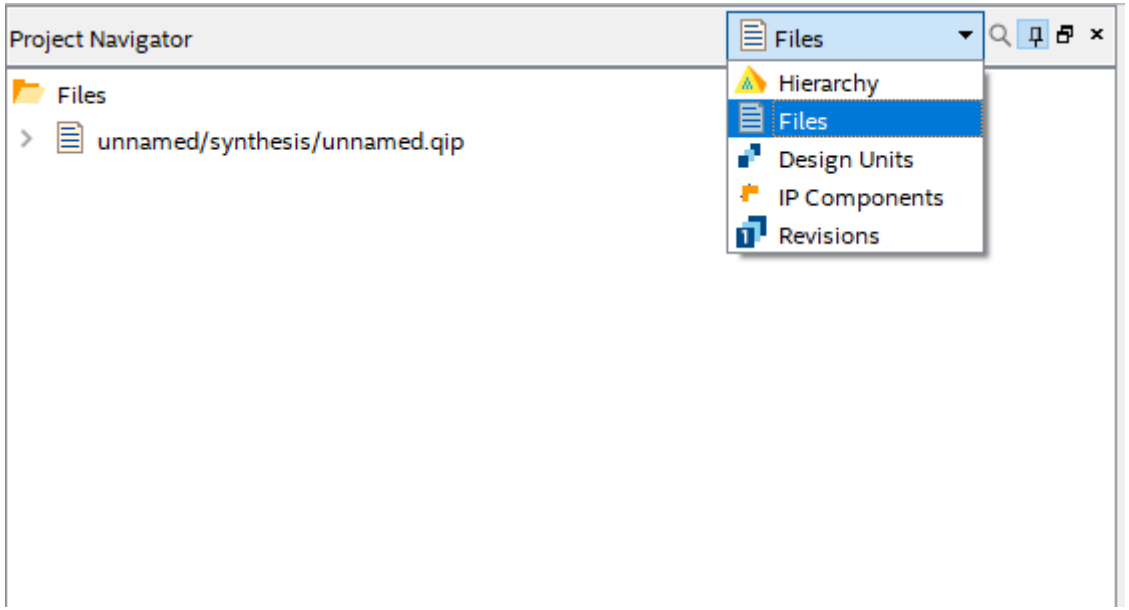
17) Go On Files view in the Project Navigator



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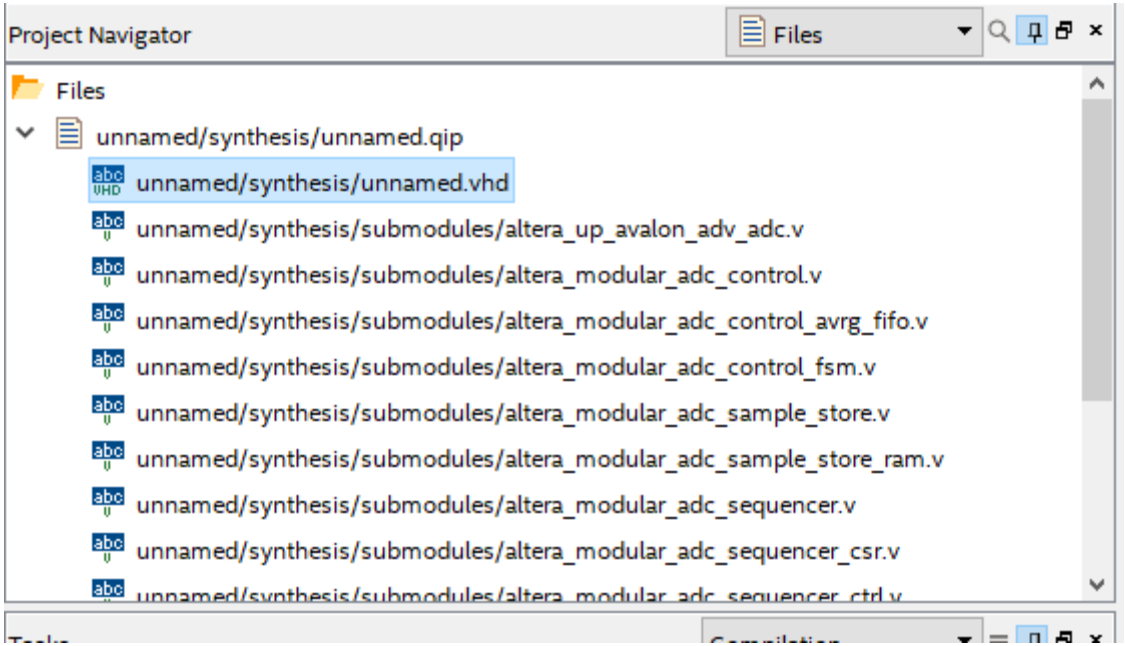
18) Open the unnamed.vhd file



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19) Open the unnamed.vhd file

```
-- unnamed.vhd

-- Generated using ACDS version 20.1 720

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity unnamed is
    port (
        CLOCK : in  std_logic                     := '0'; --       clk.clk
        CH0   : out std_logic_vector(11 downto 0);        -- readings.CH0
        CH1   : out std_logic_vector(11 downto 0);        --          .CH1
        CH2   : out std_logic_vector(11 downto 0);        --          .CH2
        CH3   : out std_logic_vector(11 downto 0);        --          .CH3
        CH4   : out std_logic_vector(11 downto 0);        --          .CH4
        CH5   : out std_logic_vector(11 downto 0);        --          .CH5
        CH6   : out std_logic_vector(11 downto 0);        --          .CH6
        CH7   : out std_logic_vector(11 downto 0);        --          .CH7
        RESET : in  std_logic                     := '0'  --     reset.reset
    );
end entity unnamed;
```

20) Now you can use it to place a component in your VHDL code