Computer Hardware

2018 Session 1

Lecture Serial
I have seen the future, and it is serial.

Serial Links

We have seen that parallel links have multiple problems. These problem increase as we try to push more data through a link, as the bit rate increases. Instead we have found that serial links are better for high speed data transmission.

This use of serial links occurs at several points in the hardware design of a computer. Between systems we are now using serial links, and within systems we are using serial links. We will investigate various serial links and describe how they are implemented and used.

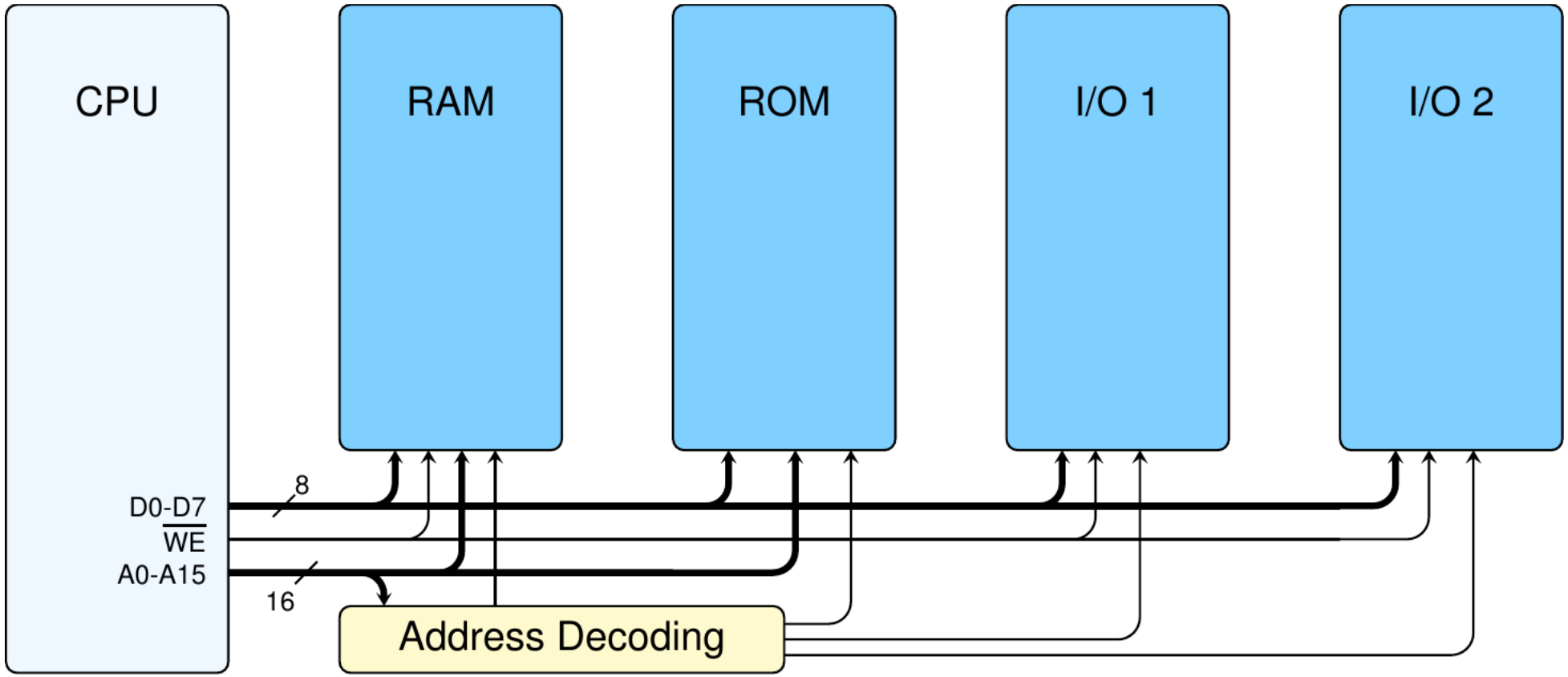
Historically....

26 pins were used to communicate between the (8 bit) CPU and peripheral devices

- 8 bit Data Bus
- 16 bit Address Bus
- Read/$\overline{\text{Write}}$ flag
- Ready Signal

Routing these 26+ lines across the circuit board is difficult and expensive in board real estate.

Traditional Integrated Circuit Connections



SPI – Serial Peripheral Interconnect

- With the advent of 16 bit, 32 bit, or 64 bit processors more and more circuit board traces would be required.
- 64 bit processor with 56 address bits and 8 byte lane selects
  - Over 128 traces required to be routed
  - Signals need to be kept synchronised which limits bus speed
- Serial solution to problem of interconnecting peripheral devices
- Reduces number of traces to four

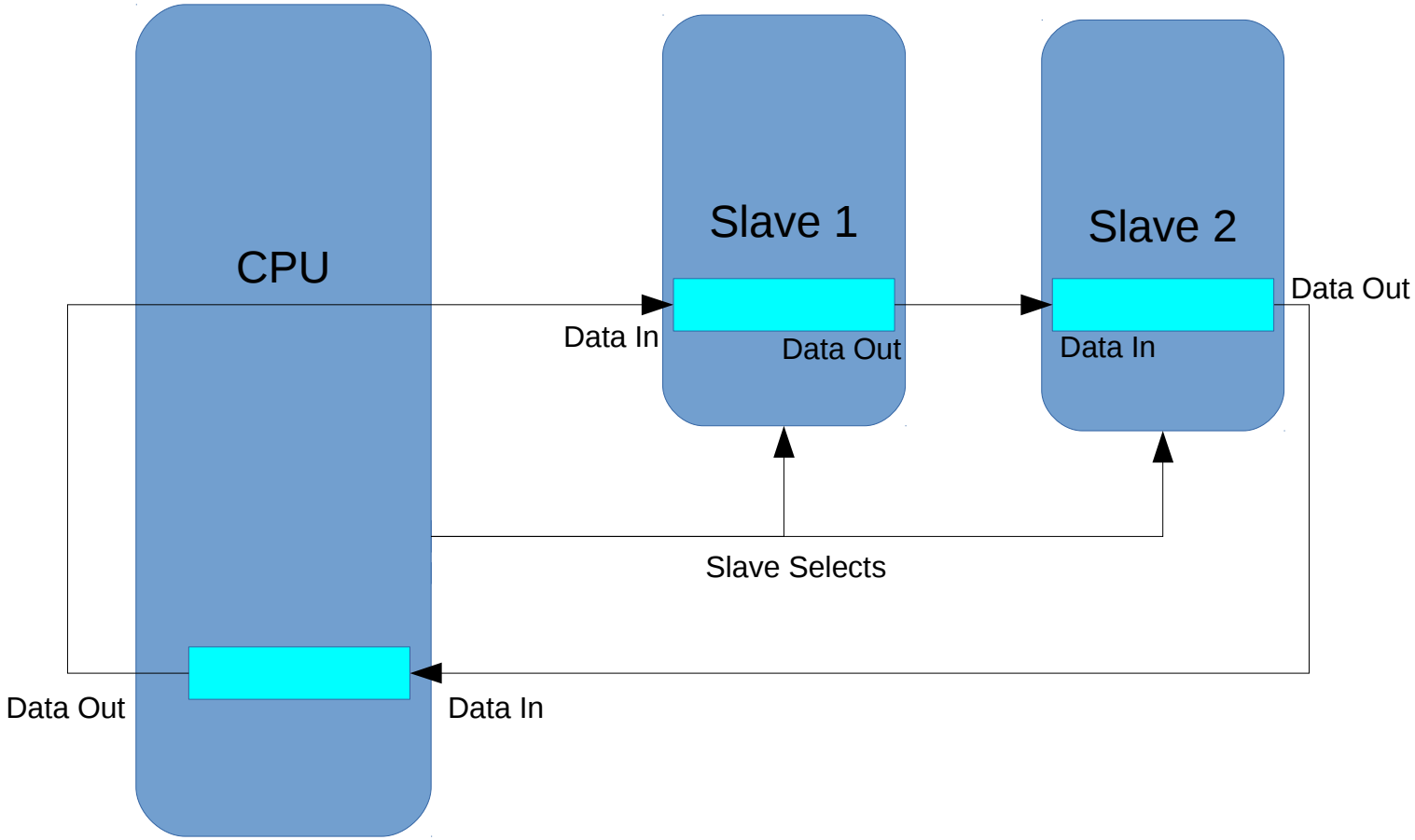
SPI Signals

- SPI uses four signals:
  - Clock
  - Data Out
  - Data In
  - (Optional) Slave Select
  - (Optional) Interrupt
- Speed is slower, but bus width is dramatically smaller
  - Easier to route
  - Easier to keep synchronised
  - Full Duplex

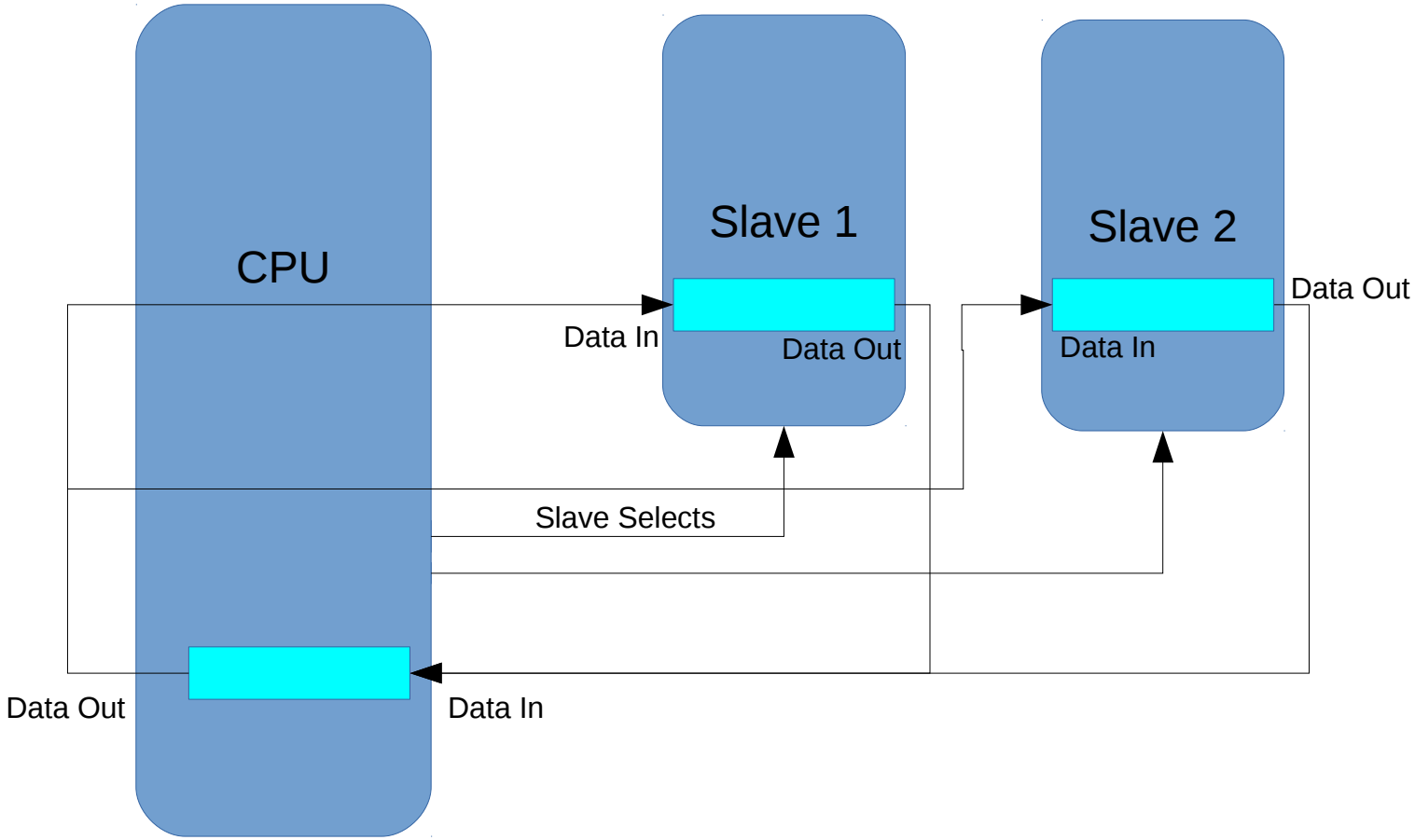
SPI Operation

- Master selects which slaves are in communication path
  - Slaves become part of large circular buffer
- Master sends data through data out line
  - Synchronised with master generated clock signal
- Slaves shift data into buffer.
  - Old data in buffer is shifted out
- Data shifted out from slaves is shifted into master
- Master stops when sufficient data has been moved

SPI Circular Buffer



SPI Shared Output



SPI Advantages

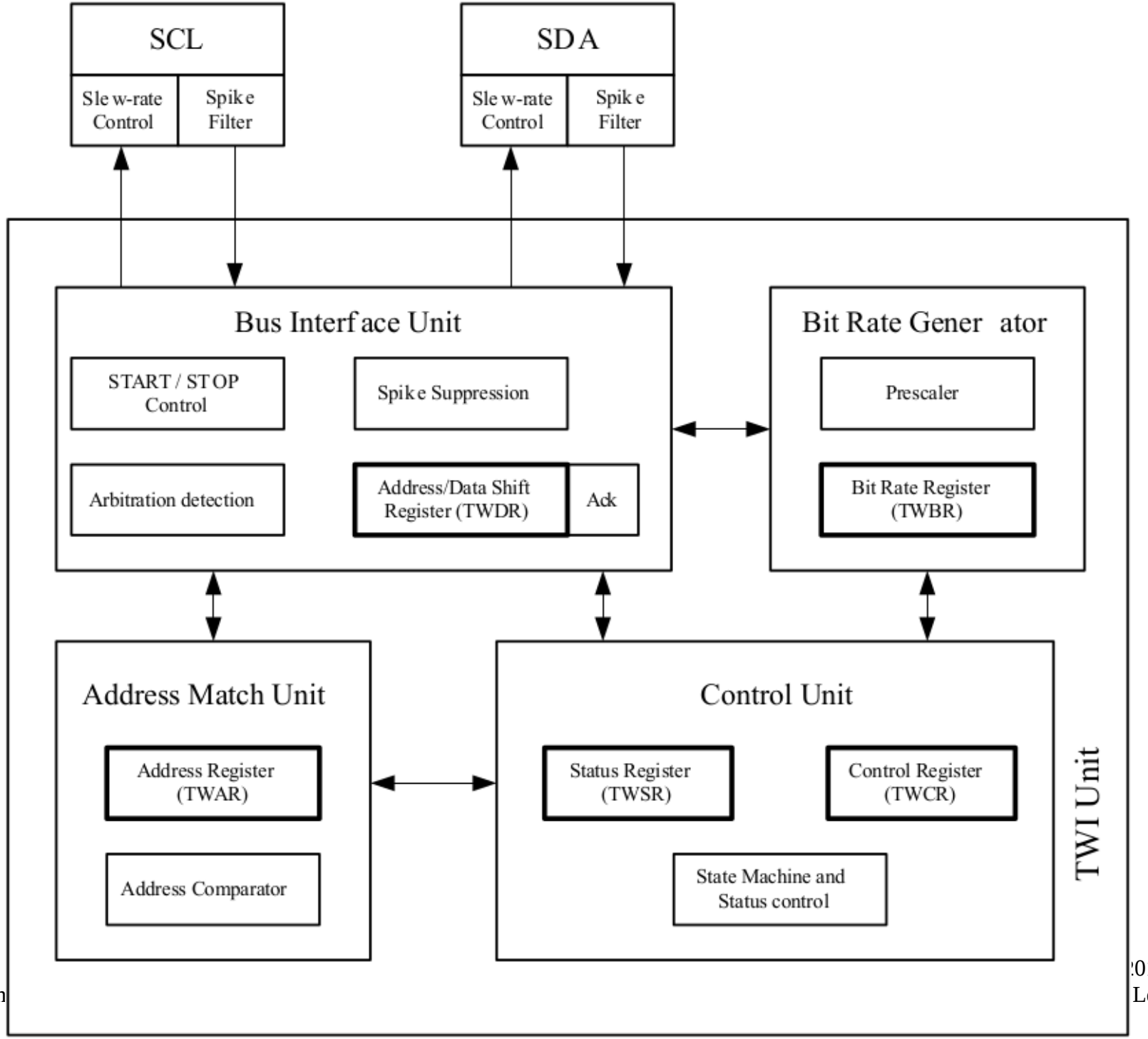
- Fewer circuit board traces
- Less signal skew means we can send shorter signals
- Advantage of Circular Buffer is all slaves controlled at once
  - We saw this arrangement with JTAG Boundary Scan
- Advantage of Shared Output is we only control the slave required
  - Less data transferred if we are only talking to one device

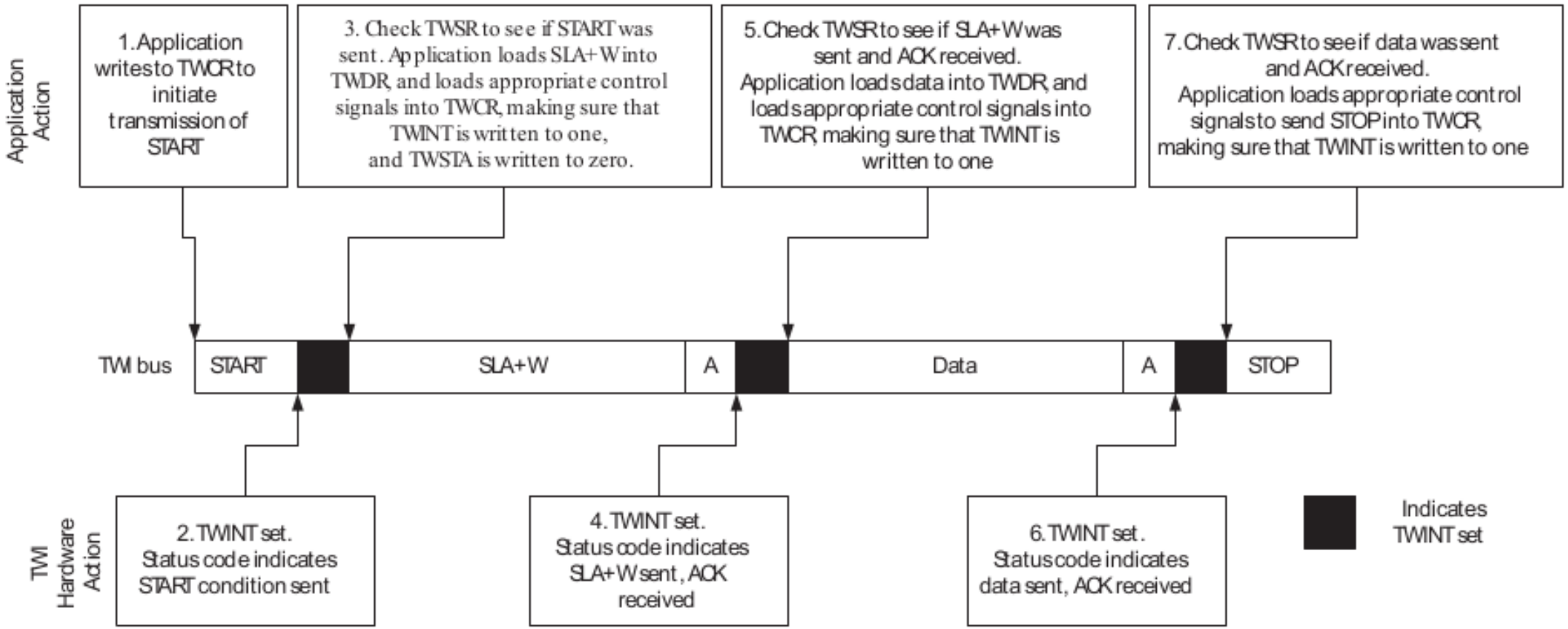
Inter-Integrated Circuit

- Also called:
  - I2C, I^2C, IIC, TWI
- Two wire interface
  - Shared Data and common Clock
  - Both signals are open collector:
    - an IC can force to LOW
    - floats to HIGH through pull-up resistors
    - Multiple drivers to LOW are not a problem, and are used for arbitration or clock stretching

- Addressable, network style interconnect between integrated circuits
  - Each slave chip has a 7 or 10 bit address
  - Master sends packetised data to one slave
  - Slave can be written to or read from in each transaction
    - Multiple data bytes in a transaction
    - Ack after the initial address and after each byte written or read
    - Transactions can be daisy-chained
  - Master is responsible for generating all clock signals
    - Slave can stretch clock by holding low if it needs more time to process request

- I2C transaction involves:
  - Master sends a start (S) sequence
  - Master sends slave address byte + read/write
    - Two bytes sent for 10 bit addresses
    - Slave acks each byte sent
  - Command byte or bytes
    - Slave acks each byte sent
  - Data byte or bytes
    - Slave acks each byte sent for write operation OR
    - Master acks each byte sent for a read operation
  - Master sends a stop (P) sequence to finish transaction
  - Master can send a restart instead of stop


SCL
Slew-rate Control
Spike Filter
SDA
Slew-rate Control
Spike Filter
Bus Interface Unit
START / STOP Control
Spike Suppression
Arbitration detection
Address/Data Shift Register (TWDR)
Ack
Bit Rate Generator
Prescaler
Bit Rate Register (TWBR)
Address Match Unit
Address Register (TWAR)
Address Comparator
Control Unit
Status Register (TWSR)
Control Register (TWCR)
State Machine and Status control
TWI Unit


Application Action
1. Application writes to TWCR to initiate transmission of START
3. Check TWSR to see if START was sent. Application loads SLA+W into TWDR, and loads appropriate control signals into TWCR, making sure that TWINT is written to one, and TWSTA is written to zero.
5. Check TWSR to see if SLA+W was sent and ACK received. Application loads data into TWDR, and loads appropriate control signals into TWCR, making sure that TWINT is written to one
7. Check TWSR to see if data was sent and ACK received. Application loads appropriate control signals to send STOP into TWCR, making sure that TWINT is written to one
TWI bus
START
SLA+W
A
Data
A
STOP
TWI Hardware Action
2. TWINT set. Status code indicates START condition sent
4. TWINT set. Status code indicates SLA+W sent, ACK received
6. TWINT set. Status code indicates data sent, ACK received
Indicates TWINT set

Multiple Master I2C

- Multiple masters can share a bus
- Each master senses if the bus is active and refrains from transmitting if the bus is active
- When transmitting the master checks the data is correct.
  - If another master is transmitting the data will be LOW rather than HIGH
  - on collision the master trying to transmit the HIGH will stop and wait

I2C Advantages and Disadvantages

Advantages:

- Only two circuit board traces required
- Multiple slaves can be addressed in a single transaction
- Multiple masters are allowed by the protocol

Disadvantages:

- Open collector, so data rate is relatively low
- Each slave requires unique address
- Master needs to know slave's addresses
- Half Duplex

Hardware v. Bit Banging

- Hardware support for the protocol reduces software complexity
- Hardware is more efficient, and can provide faster data speeds
  - Microcontroller can only change output signals once every instruction
- Software is cheaper
  - No per unit hardware cost (per microcontroller)
  - Incur Software development cost, but matched by no hardware development cost

- Software is not tied to a particular pin
  - On the ATmega328 the I2C interface use particular pins (A4 and A5)
  - Software implementations can use any general purpose I/O pin

Beyond...

- Both SPI and I2C are single circuit board interconnects.
- They are both single ended
- They suffer from noise and crosstalk
- Newer interconnects use differential signalling
  - Higher immunity to noise
  - Constant current
    - Reduces switching spikes on power supply
- Newer interconnects encode the clock with the data
  - No synchronisation between signals needed
- At even higher speed digital signals aren't

Double Data Rate

- We have looked at systems that send one data bit per clock pulse.
- Double data rate systems send a data bit on both the rising edge and the falling edge of the clock pulse.

Low Voltage Differential Signalling (LVDS)

- TIA/EIA-644 and later
- Pair of traces that use the difference in voltage on the traces to encode a 1 or a 0
- Receiver is terminated with a 100 ohm impedance
- Transmitter sends 3.5mA through the pair of traces
- LVDS does not describe the data framing or packetisation
  - Many different standards use LVDS transmission
  - PCIe
  - UltraSCSI
  - Hypertransport

JSED204(B)

- High speed interface (3.125Gbps), originally for connecting DACs and ADCs to FPGAs
- Rev B pushes data rate to 12.5Gbps
- Differential signals
- Multiple Lanes connecting two devices
  - Clocks can be uncoupled in each lane
  - 8b/10b encoding so no separate clock signal

Are we Digital or RF?

- At multi gigaHertz rates digital signals just aren't
- Square waves are limited by rising and falling edges
- We are effectively transmitting radio signals
- High speed signalling systems use RF transmission techniques instead
  - ADSL
  - 10Gb, 100Gb ethernet
  - Mobile Phones 4G, 5G, *beyond 5G*

RF Transmission of Digital Data

- We don't try to use square waves
- We take advantage of sine waves and encode the data in perturbations of the sine waves themselves
  - Frequency – FM
  - Amplitude – PAM
  - Phase – QAM
  - Polarisation, Spin, Momentum – ?
- Need to distinguish between Baud rate and Bit rate

Baud Rate v. Bit Rate

- We transmit information encoded as a set of symbols
- A symbol may encode one bit of information, it may take multiple symbols to encode one bit or a symbol may encode multiple bits
- The Baud rate is the number of symbols transmitted
- The Bit rate is the number of bits transmitted

Baud Rate = Bit Rate / Bits per Symbol

- Increases in bits per symbol means more information transmitted

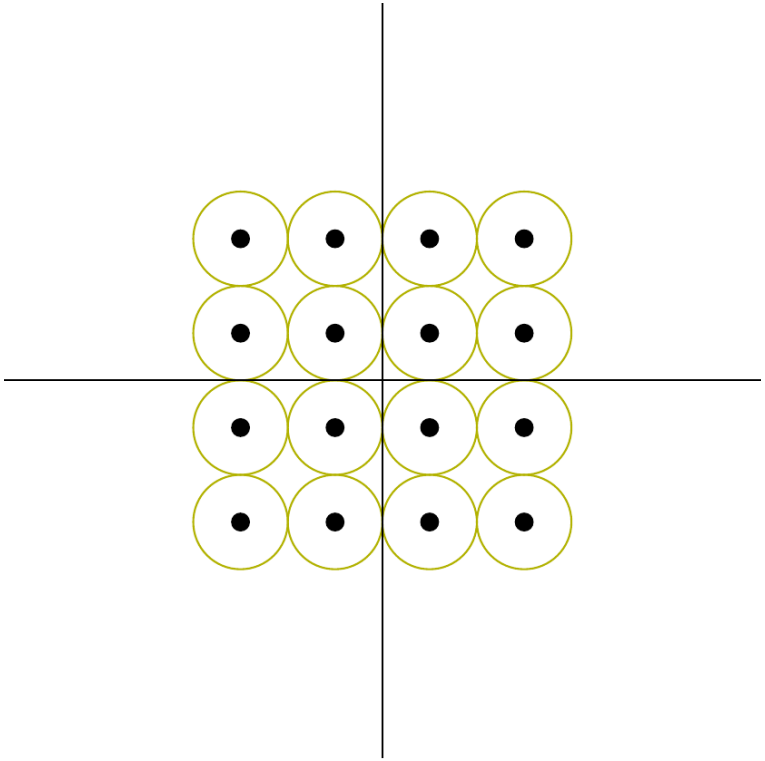
Pulse Amplitude Modulation – PAM

- We vary the amplitude of a series (possibly one) of pulses
- The change in amplitude is the encoded information
- Each symbol is a different amplitude
- The number of discrete amplitudes that can be generated and detected is the limit to the number of different symbols that can be used
- The number of pulses that need to be transmitted is the limit to the symbols that can be transmitted per time frame.
- Noise limits the number of discrete amplitudes we can utilise

Quadrature Amplitude Modulation – QAM

- Combines two signals at 90° phase shift
  - Normally called the I and Q signals
  - This is the Quadrature part of the name
- This allows us to generate different phases of output signal
- We can also vary the Amplitude of the signal
- The symbol information is the combination of
  - The phase of the transmitted signal
  - The amplitude of the transmitted symbol
- We represent this information as a constellation diagram

- Each point on the diagram represents a unique combination of phase and amplitude
- We wish to maximise the distance between any two points
  - Noise moves the signal away from the centre of a point
  - The receiver interprets a value as the closest point
- Common variants are 16-QAM and 64-QAM
- ADSL modems use two techniques:
  - Frequency division (up to 127 different bins)
  - 32768-QAM in each bin



16-QAM

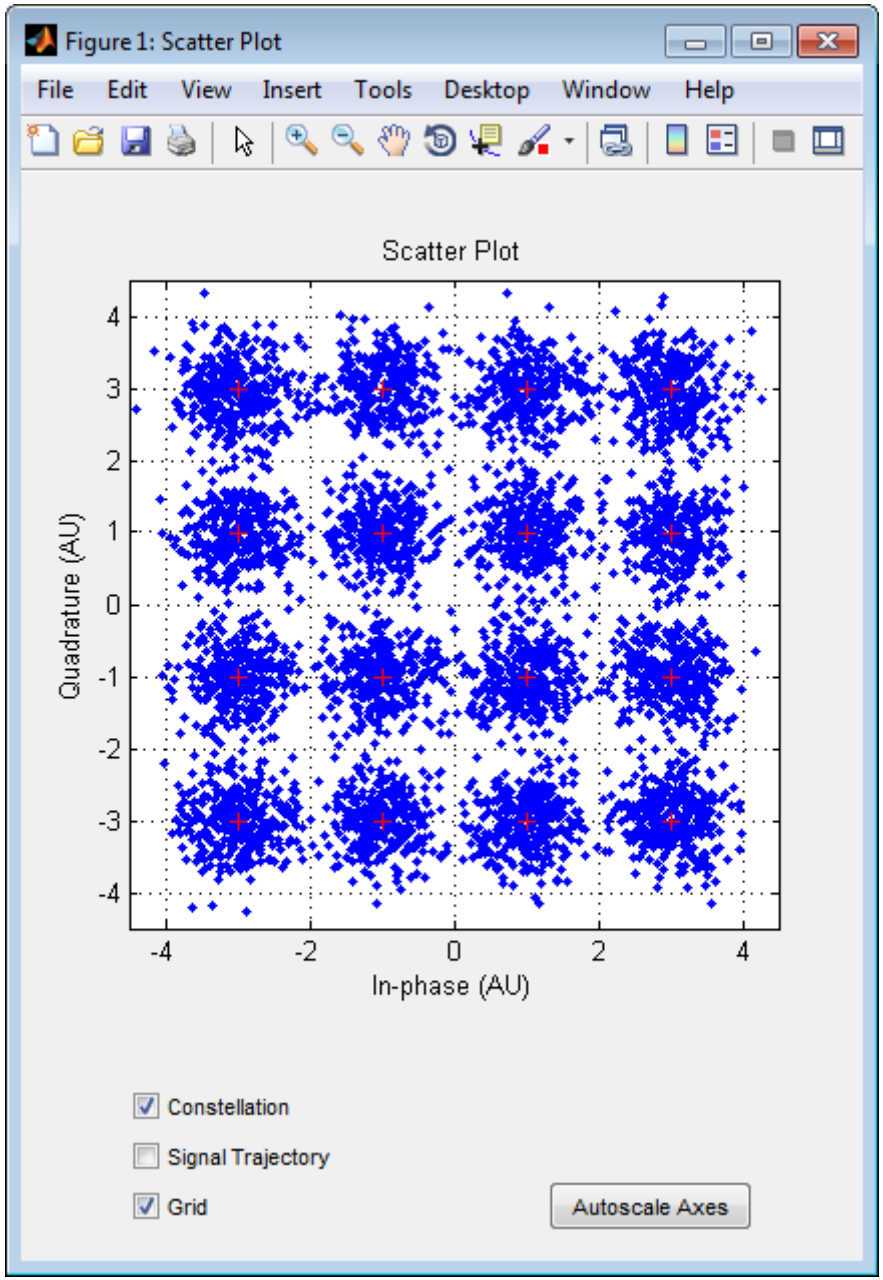
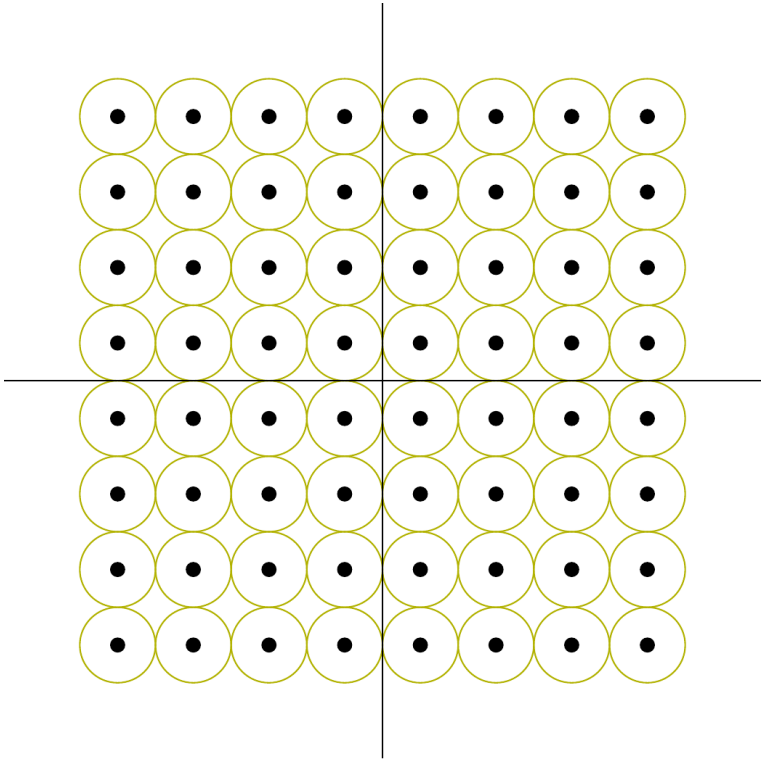
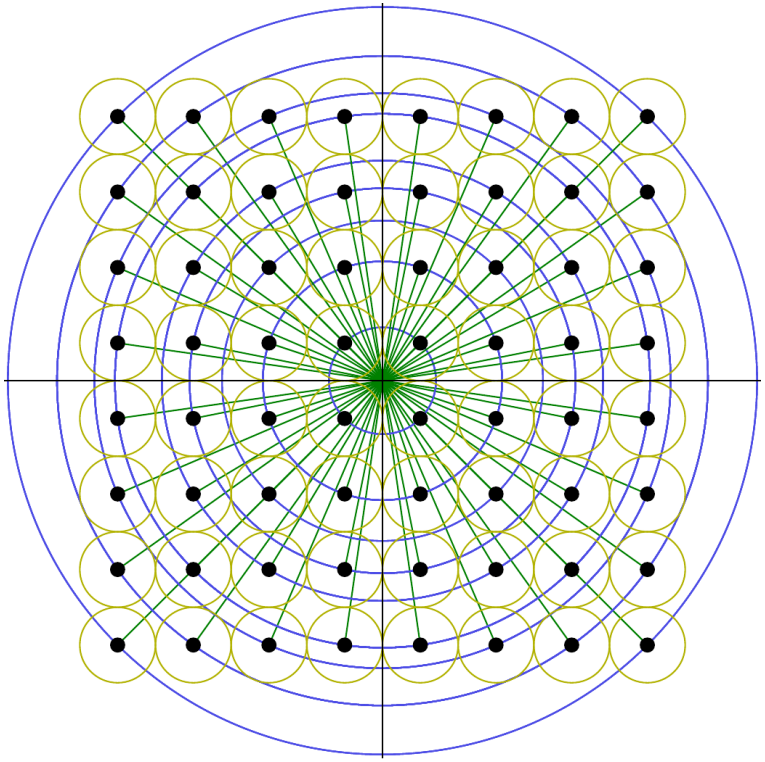


Figure 1: Scatter Plot
File Edit View Insert Tools Desktop Window Help
Scatter Plot
Quadrature (AU)
In-phase (AU)
4
3
2
1
0
-1
-2
-3
-4
-4
-2
0
2
4
Constellation
Signal Trajectory
Grid
Autoscale Axes





64-QAM: 9 Amplitudes, 52 Phases