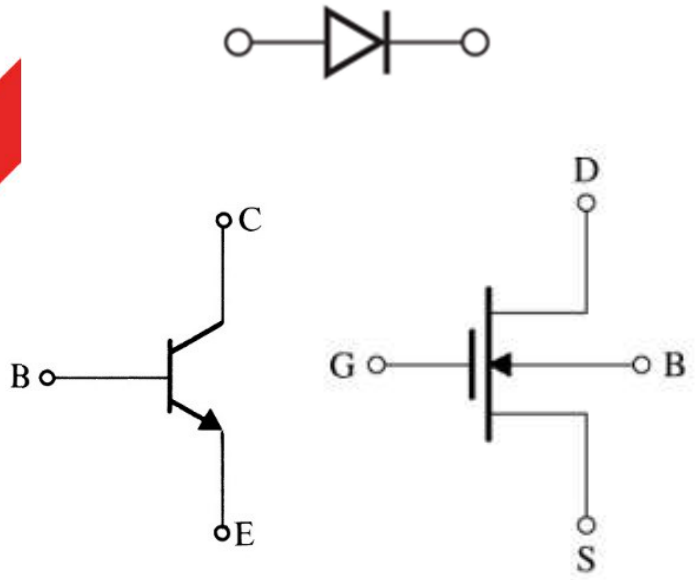
MACQUARIE University

ELEC2005
Electrical and Electronic Systems

MOSFETS– PART 1

DAVID PAYNE



In Today's Lecture

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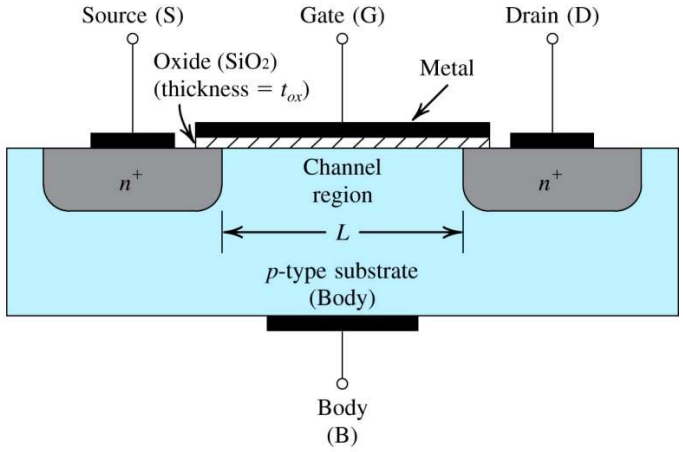
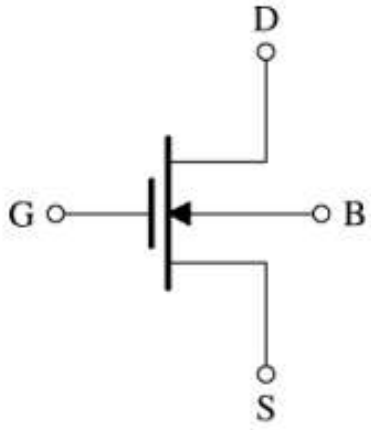
- Introduction to MOSFETS
- MOSFETS Vs. BJTs
- Device Structure
- Device Operation
- P and N channel MOSFETS
- Characteristics and Operating Modes





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Lecture 5

1. **Intro to MOSFETs**
2. Device Structure & Operation
3. Examples

Introduction to MOSFETS

WHAT ARE THEY?

- **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
- Very well established and widely used technology (especially in the IC industry)
- **Metal** - used for the contacts, though polycrystalline silicon can also be used
- **Oxide** - Unlike BJTs, in a MOSFET the gate is separated from the rest of the device by a thin insulating layer (usually **silicon dioxide**)
- **Semiconductor** - most commonly fabricated on **silicon** (though other semiconductors can be used, including compounds like SiGe)
- **Field effect** – Applying a voltage between the gate and body terminals creates an electric field which penetrates the oxide and creates an *inversion layer at* the semiconductor interface

Introduction to MOSFETS

MOSFETS VS BJTS

Q: What are two major types of three-terminal semiconductor devices?

- metal-oxide-semiconductor field-effect transistor (MOSFET)
- bipolar junction transistor (BJT)

Q: Why are MOSFET's more widely used?

- size (smaller)
- ease of manufacture
- lower power requirements

MOSFET are more widely used in implementation of modern electronic devices

Introduction to MOSFETS

MOSFETS VS BJTS

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MOSFET technology

- Allows placement of approximately 2 billion transistors on a single IC
- Backbone of very large scale integration (VLSI)
- Preferable to BJT technology for many applications (for example digital circuits).
- But NO simple equivalent circuit (such as the 0.7V-drop model)

MOSFET are more widely used in implementation of modern electronic devices

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Lecture 5

1. Intro to MOSFETs
2. **Device Structure & Operation**
3. Examples

Introduction to MOSFETS

DEVICE STRUCTURE

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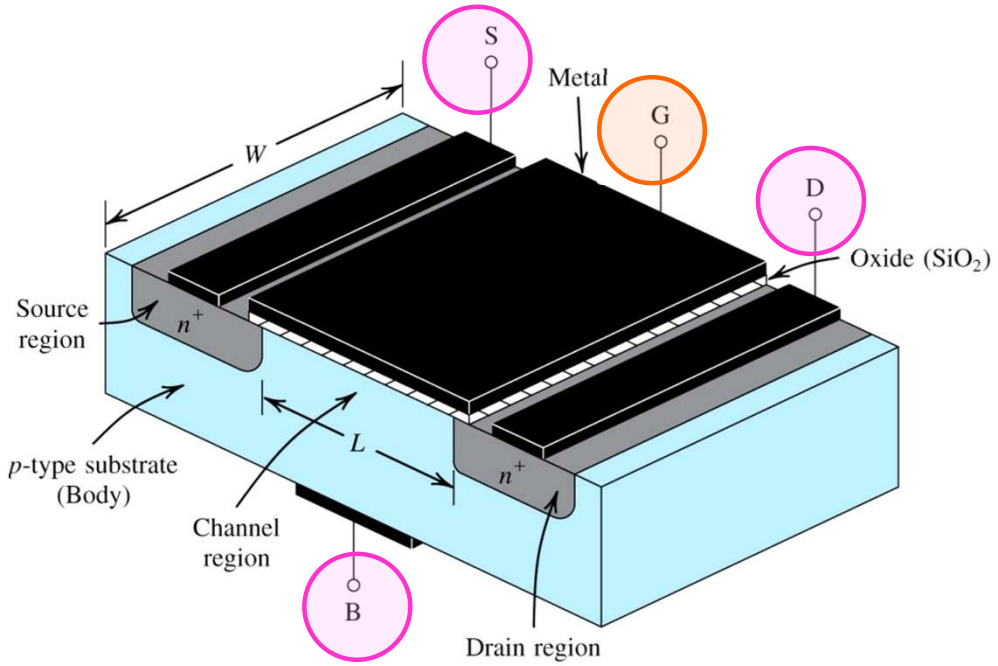
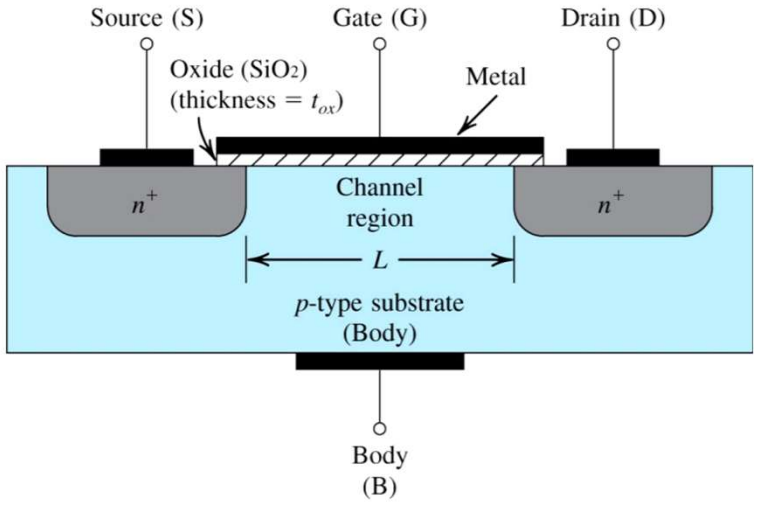
General structure of the n-channel MOSFET (nMOSFET):

See Sedra Chapter 5.1 for further information



(a)



(b)

Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view, **(b)** cross-section. Note that typically L = 0.03*um* to 1*um*, W = 0.1*um* to 100*um*, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10*nm*.

Introduction to MOSFETS

DEVICE STRUCTURE

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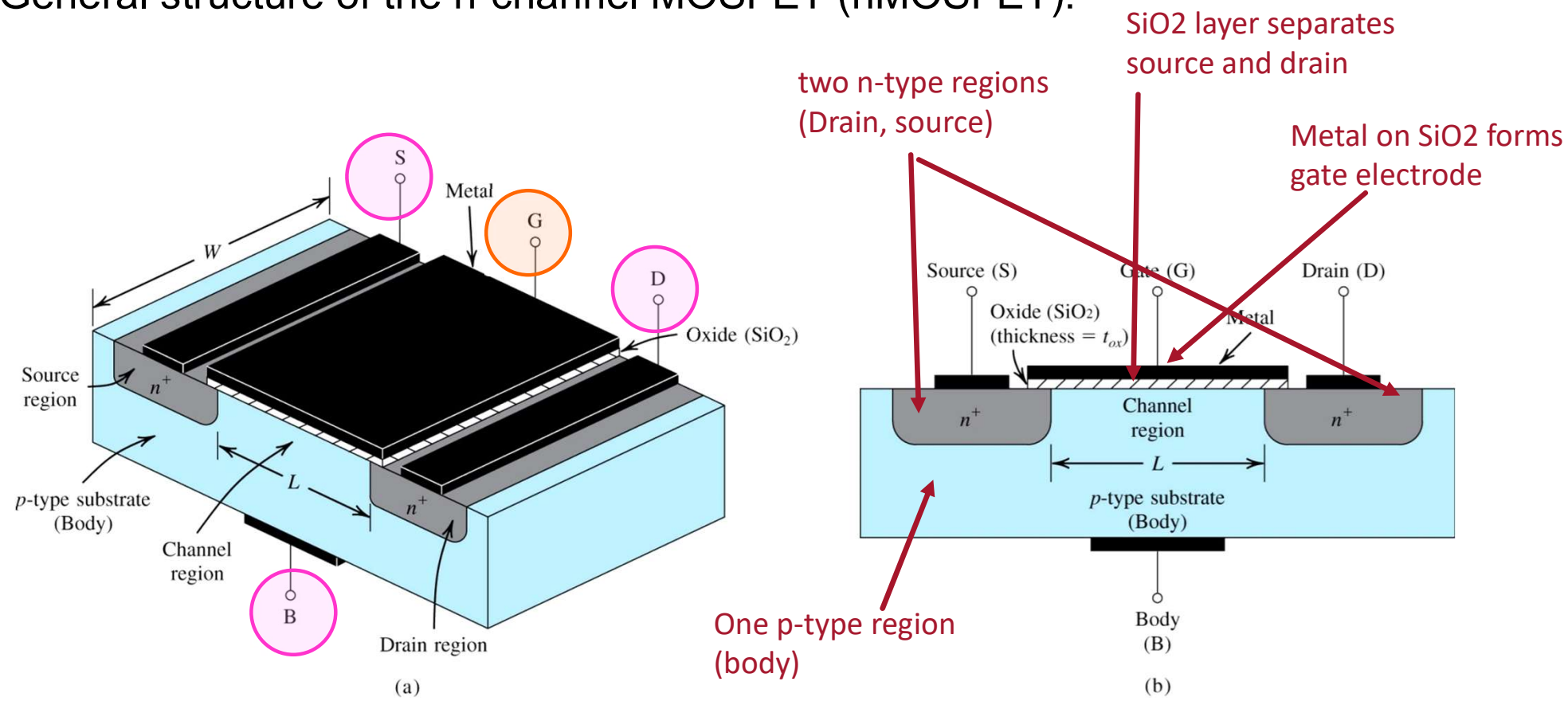
General structure of the n-channel MOSFET (nMOSFET):



Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view, **(b)** cross-section. Note that typically L = 0.03*um* to 1*um*, W = 0.1*um* to 100*um*, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10*nm*.

Introduction to MOSFETS

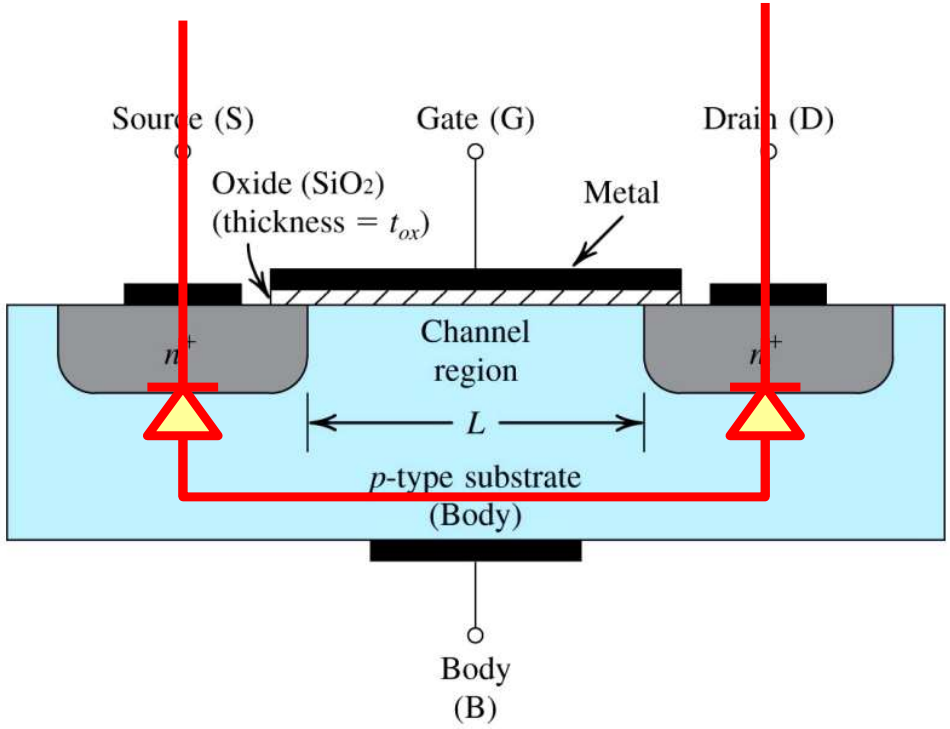
DEVICE STRUCTURE

- The MOSFET consists of two pn junctions

  - Essentially two back-to-back diodes

- Diodes between drain and source prevent current when voltage V_{DS} is applied

  - Yields very high resistance (10^{12} ohms!)



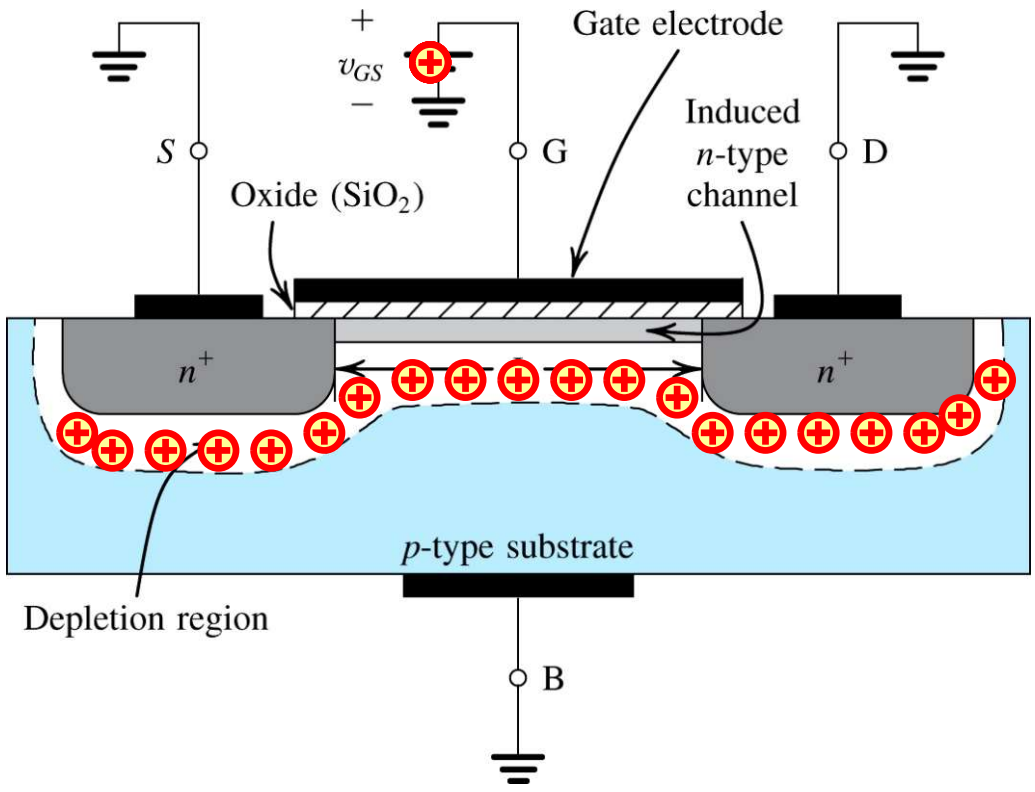
Device Operation

CREATING A CHANNEL

Q: What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate? *Refer to figure to right*

step #1: v_{GS} is applied to the gate terminal, causing a positive charge build up along metal electrode.

step #2: This "build up" causes free holes to be repelled from region of *p*-type substrate under gate.



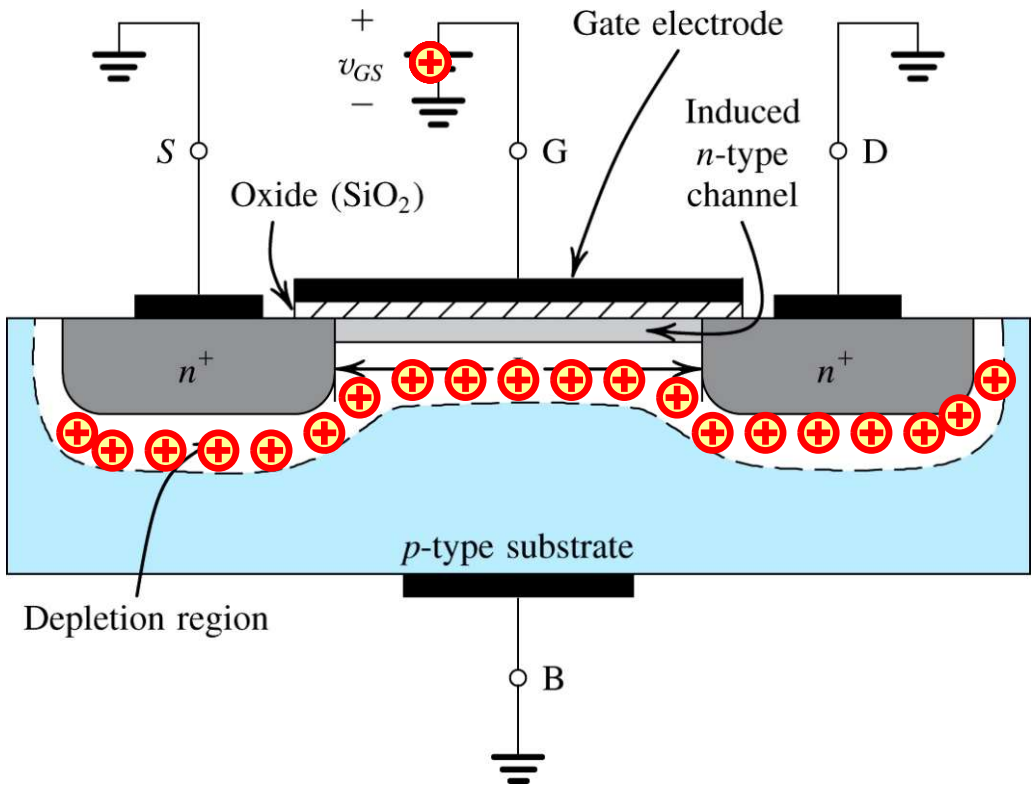
Device Operation

CREATING A CHANNEL

Q: What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate? *Refer to figure to right*

step #3: This 'migration' results in the uncovering of negative bound charges, originally neutralized by the free holes

step #4: The positive gate voltage also **attracts electrons from the n⁺ source** and drain regions into the channel



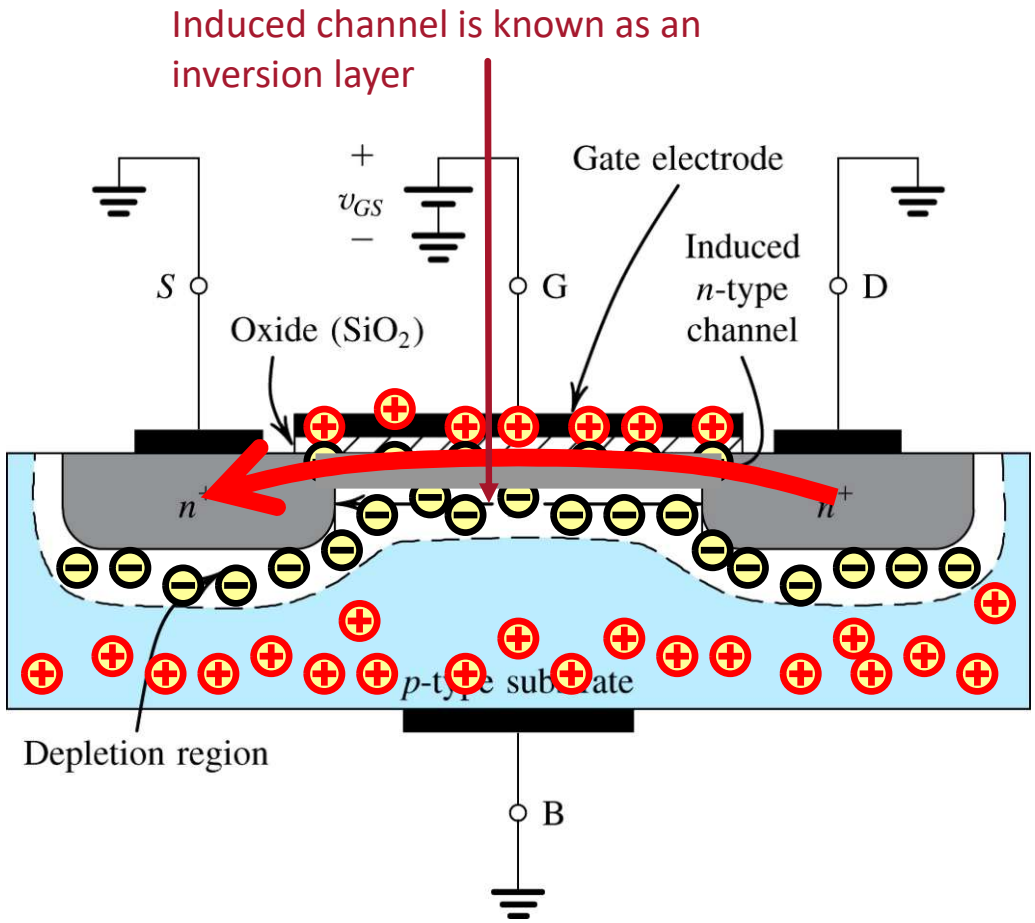
Device Operation

CREATING A CHANNEL

Q: What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate? *Refer to figure to right*

step #5: Once a sufficient number of these electrons accumulate, an n-region is made (connecting S and D!)

step #6: This provides a path for current flow between S and D



Device Operation

A CURRENT SOURCE WITH SQUARE-LAW DEPENDENCE

- Channel is induced when the gate source voltage exceeds the threshold voltage
- Additional voltage beyond the threshold point is the overdrive

$v_{GS} > V_t$ Threshold voltage

$v_{OV} = v_{GS} - V_t$ Overdrive voltage

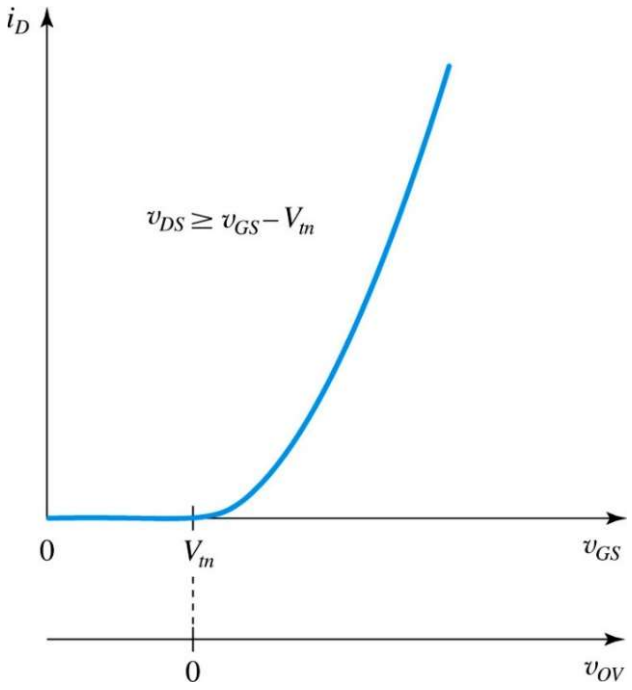
- Drain current has a square-law dependence on the overdrive voltage:

$$i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2$$

Constant

$$k_n = \mu_n C_{ox} \frac{W}{L}$$

Constant



Different constants for n and p channel MOSFETs

Class Exercise

OVERDRIVE VOLTAGE

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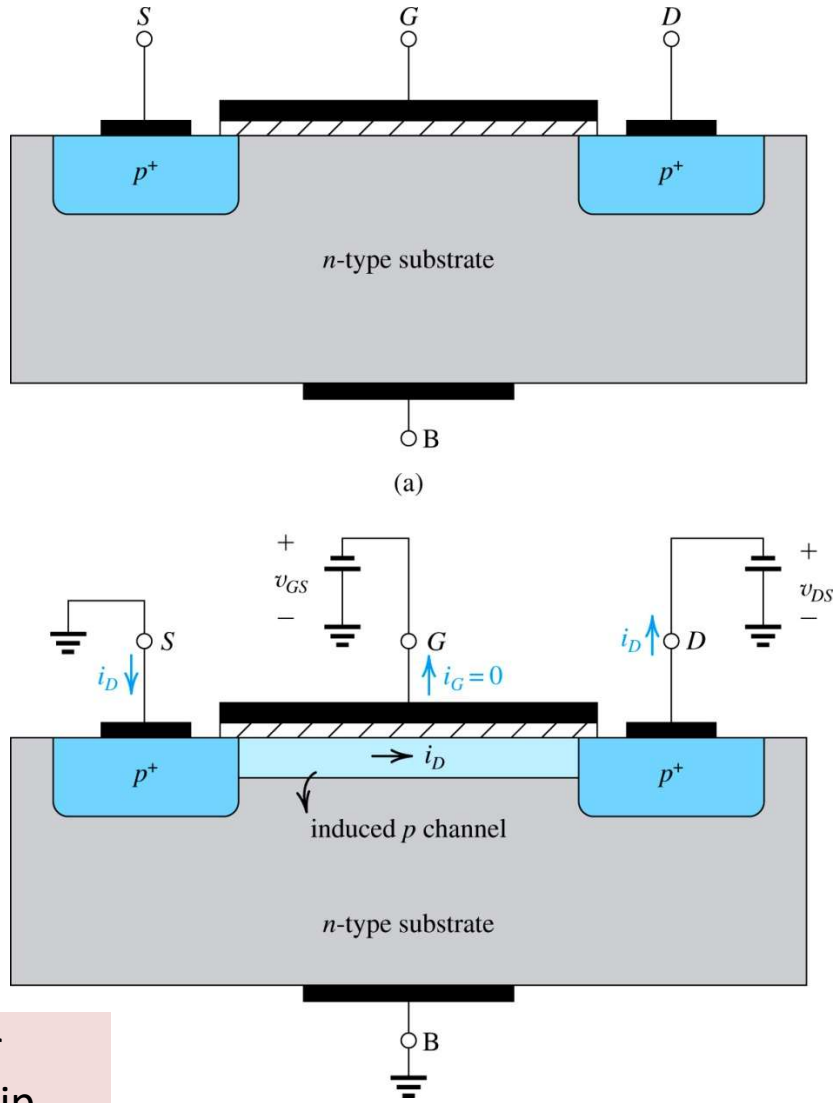
A MOSFET's threshold voltage is 0.5V. If you apply 2V between Gate and Source, what is the overdrive voltage?

P-Channel MOSFET

A CURRENT SOURCE WITH SQUARE-LAW DEPENDENCE

- P-Channel MOSFETs have a similar but opposite structure to n-channel
- They are complementary devices
- PMOS originally dominated the MOS field. but as manufacturing difficulties with NMOS were solved, NMOS took over
- Q: Why is NMOS advantageous?

  - Because electron mobility μ_n **is 2 – 4 times greater** than hole mobility μ_p

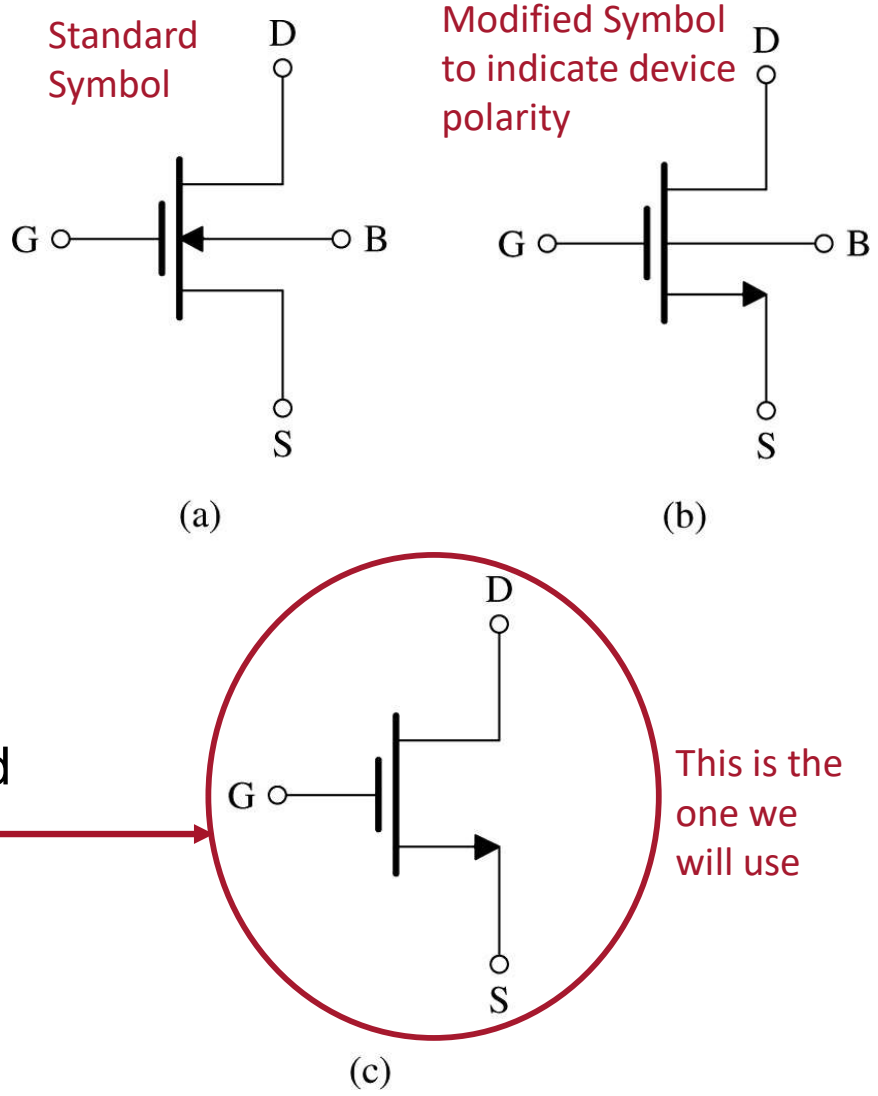


Complementary MOS (**CMOS**) is the technology for fabrication of both NMOS and PMOS on the same chip

nMOSFET

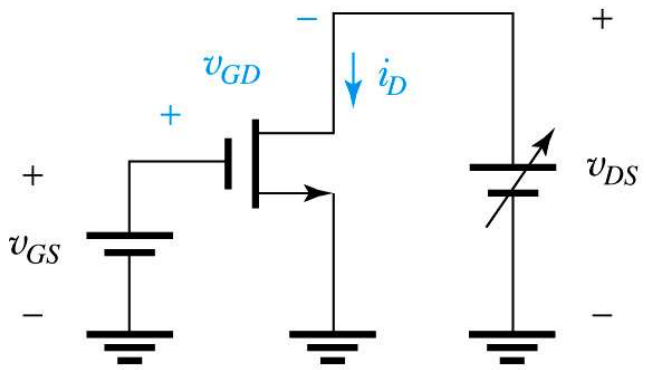
CIRCUIT SYMBOLS

- Numerous circuit symbols used
- There are four terminals:
  Drain (D), Gate (G), Body (B) and Source (S)
- Simplified circuit symbol for the case when body and source are connected or body effect can be ignored

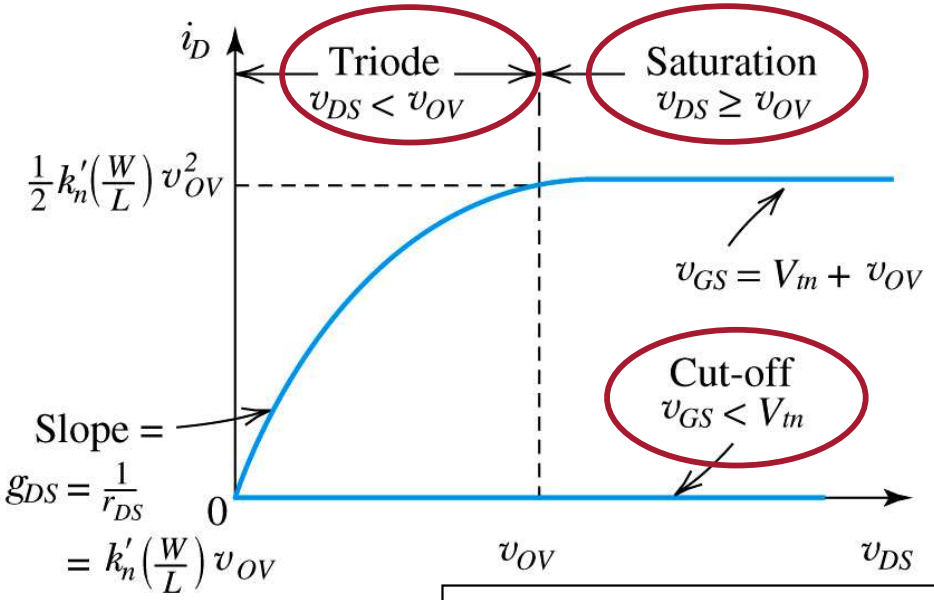


nMOSFET

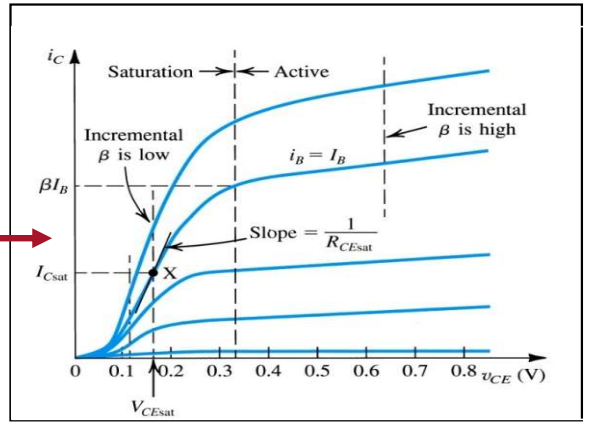
REGIONS OF OPERATION



Regions of Operation

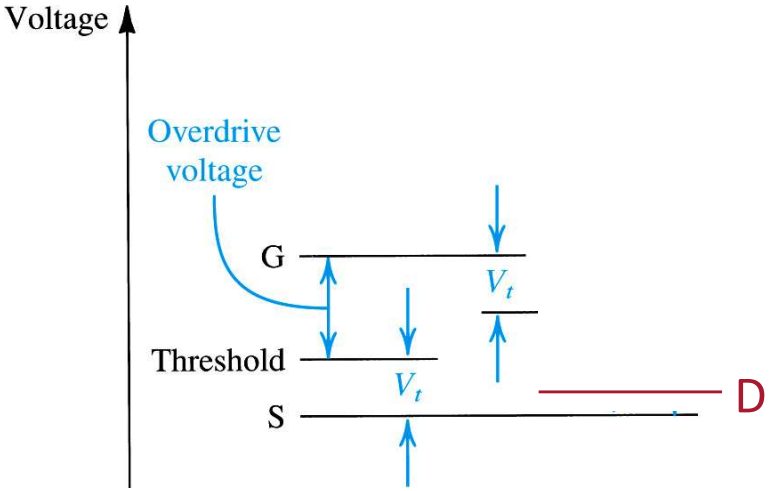


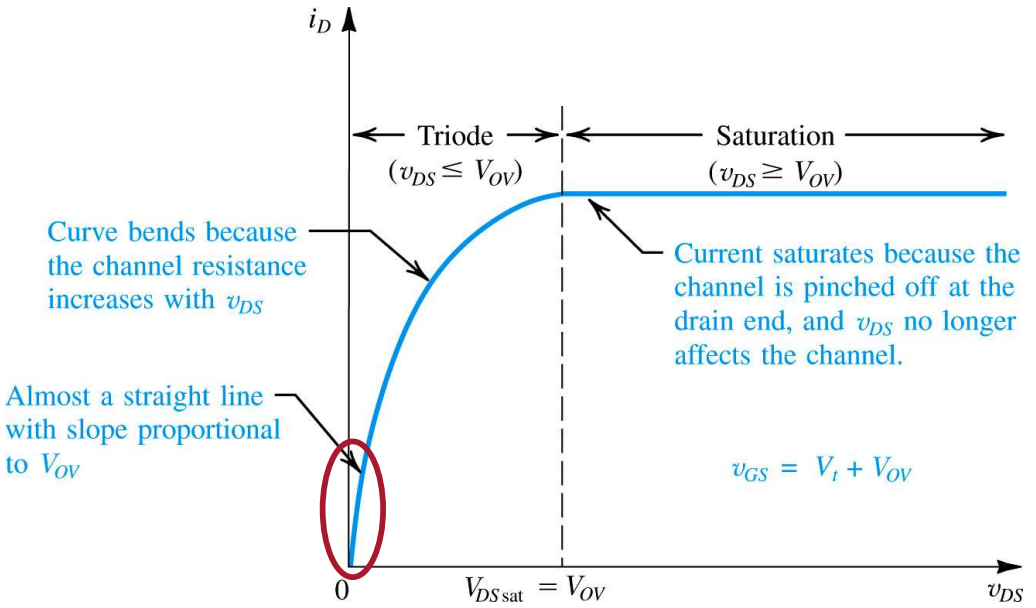
Note the differences and similarities with the BJT!

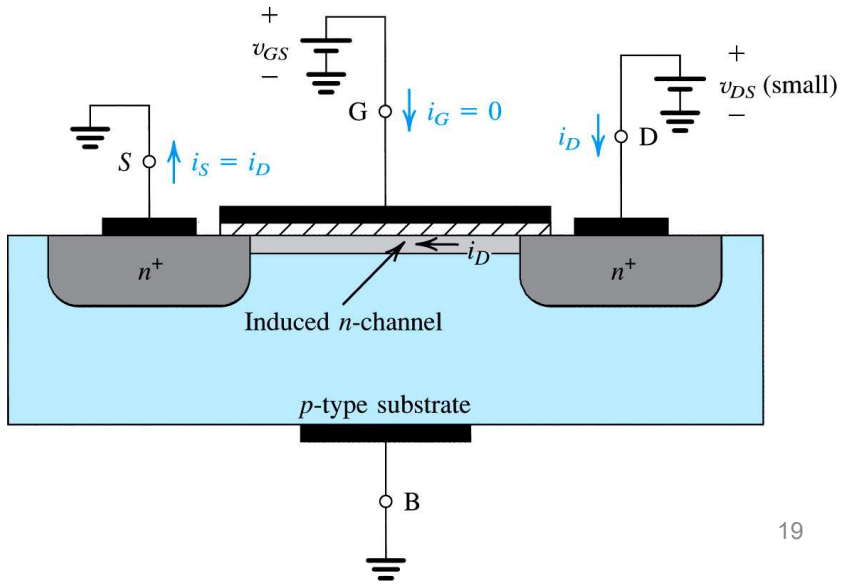


nMOSFET

REGIONS OF OPERATION

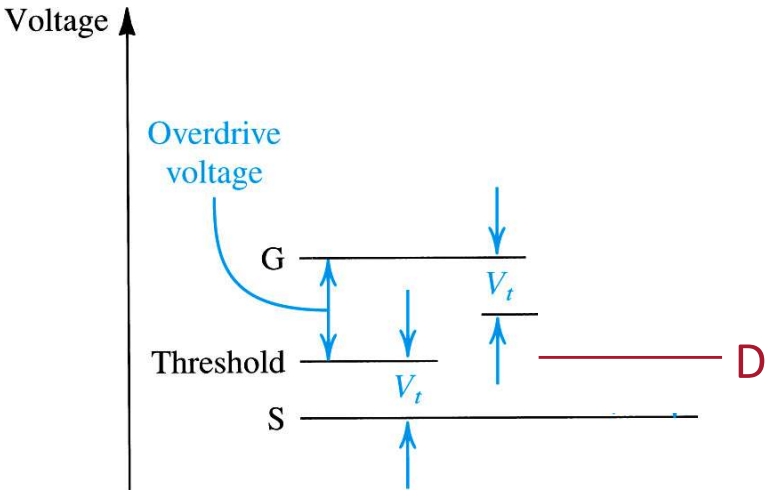


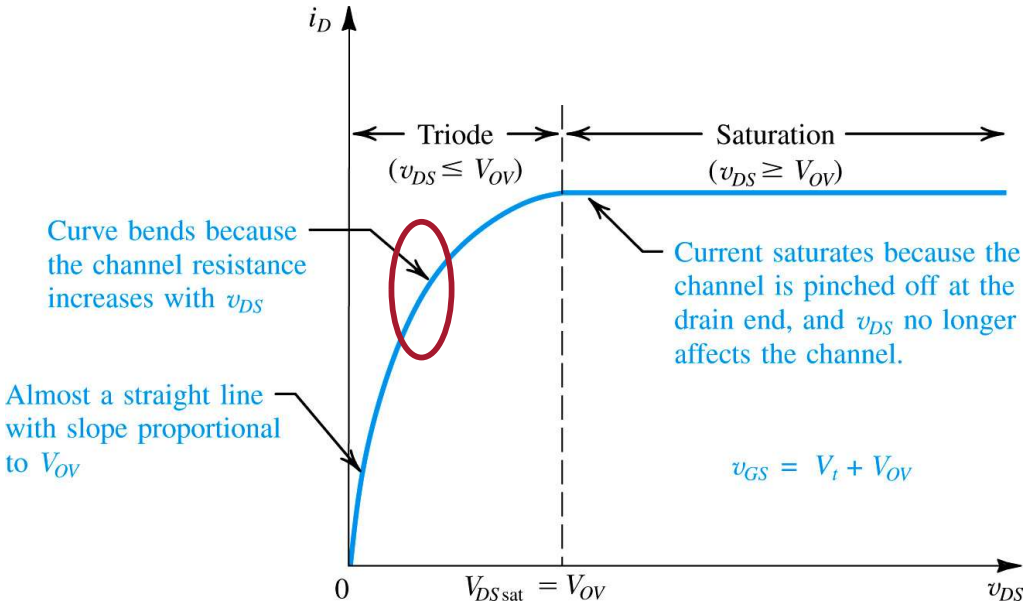


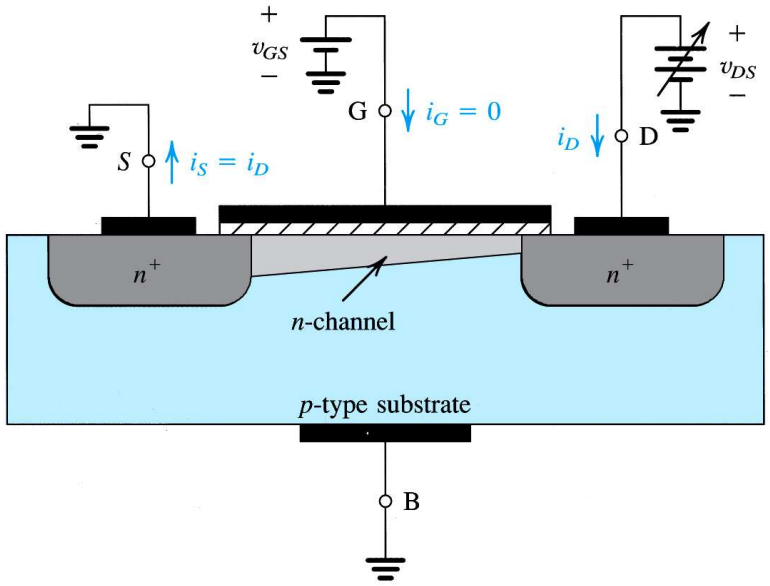


nMOSFET

REGIONS OF OPERATION

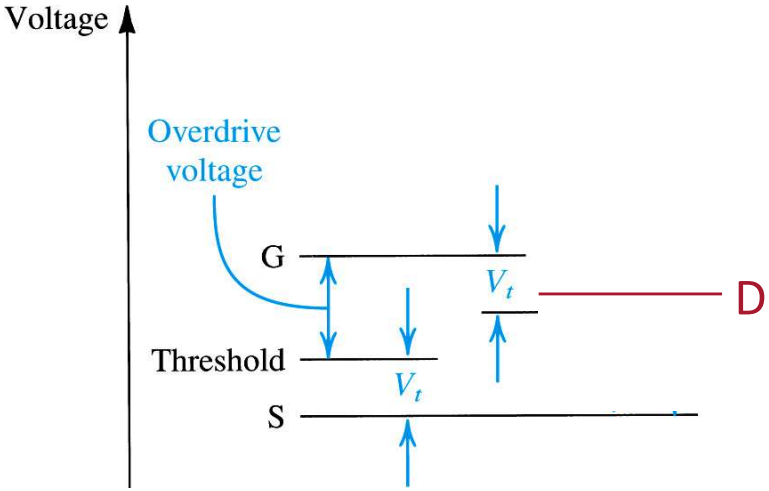


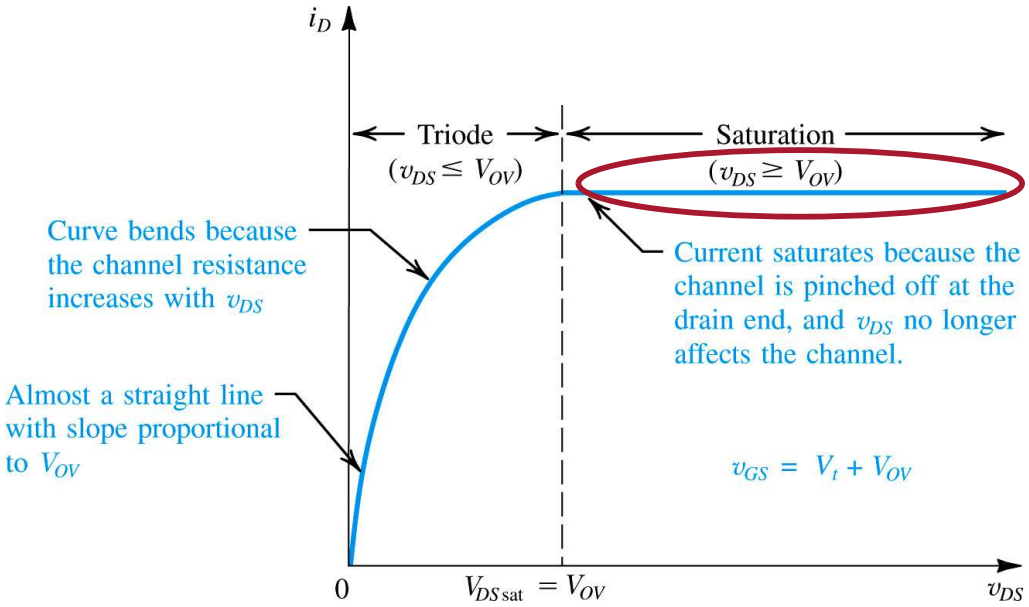


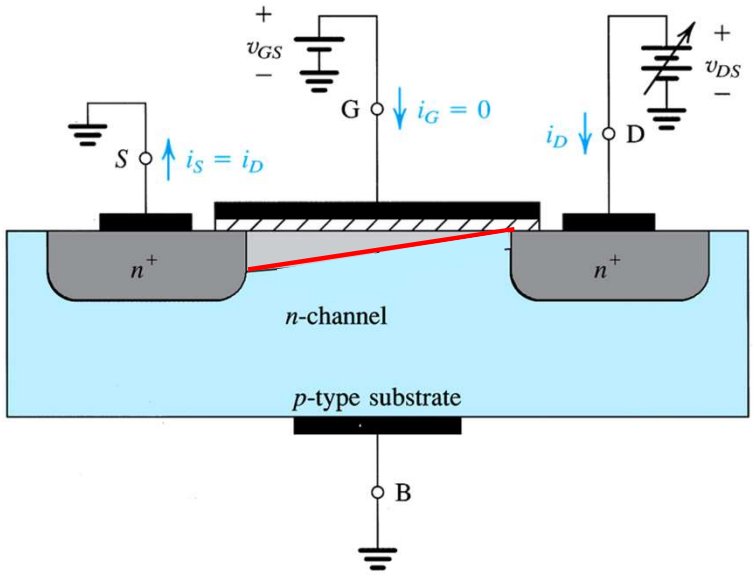


nMOSFET

REGIONS OF OPERATION

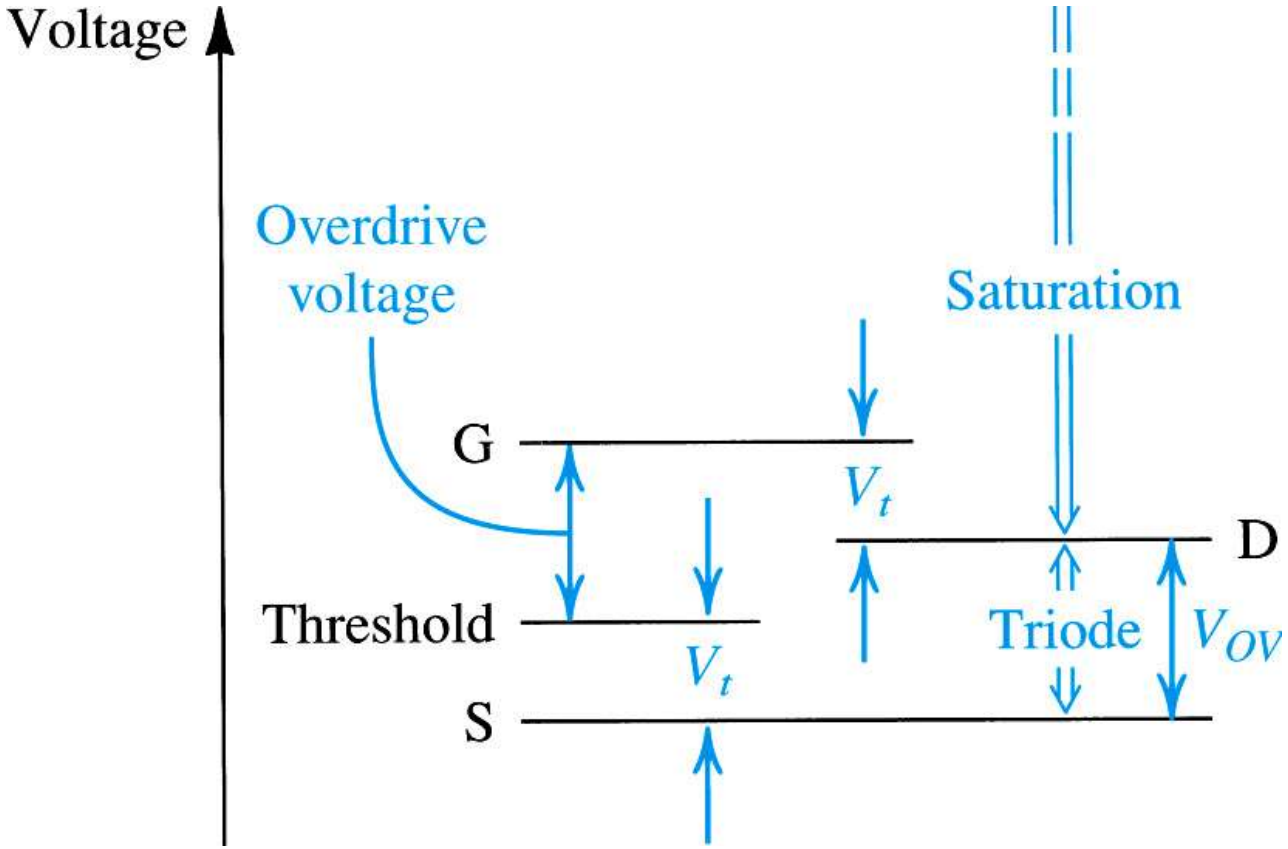






nMOSFET

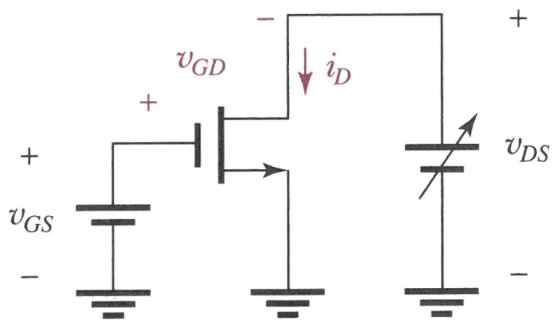
OPERATING MODE VOLTAGES



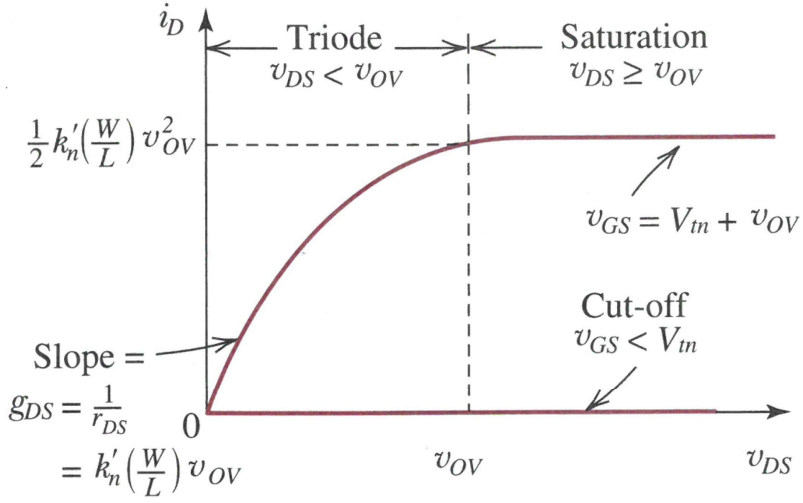
The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

nMOSFET

OPERATING MODE VOLTAGES



$V_{GS} < V_t$: no channel
in cut-off; $i_D=0$



$V_{GS} = V_t + V_{OV}$: channel induced :
in triode or saturation region, depending on state:

Triode Region

ontinuous channel, obtained by:

$$v_{GD} > V_{tn}$$

equivalently:

$$v_{DS} < v_{OV}$$

hen,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

nMOSFET

OPERATING MODE VOLTAGES

Triode mode when,

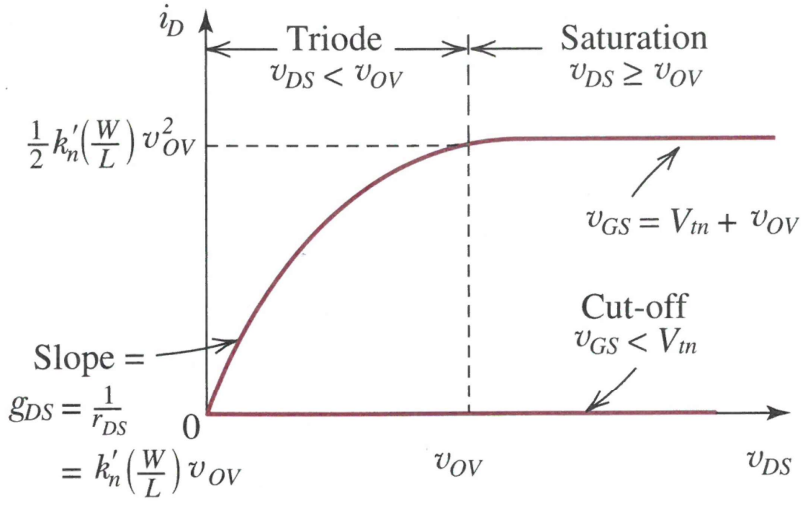
$V_{DS} < V_{OV}$

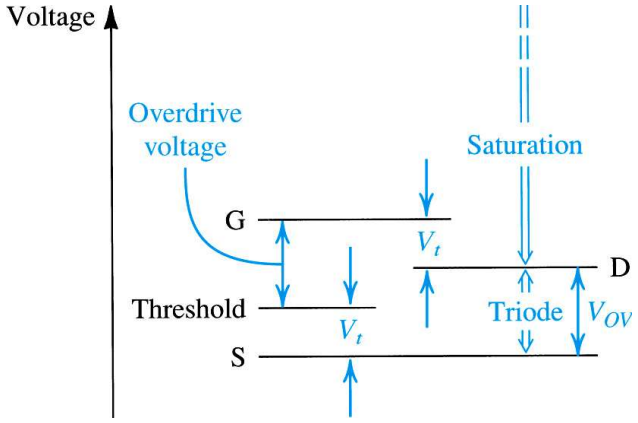
Saturation mode when,

$V_{DS} \geq V_{OV}$

MOSFET: Amplify in Saturation mode

BJT: Amplify in Active mode





MOSFET Example

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Consider an NMOS transistor fabricated in a 0.18-µm process with $L = 0.18$ µm and $W = 2$ µm. The process technology is specified to have $C_{ox} = 8.6$ fF/µm^2, $\mu_n = 450$ cm^2/V·s, and $V_{tn} = 0.5$ V.

(a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100$ µA.
(b) If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50$ µA.
(c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3$ V. Find the change in i_D resulting from v_{GS} changing from 0.7 V by +0.01 V and by –0.01 V.

Triode mode:

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(\upsilon_{GS} - V_t)\upsilon_{DS} - \frac{1}{2}\upsilon_{DS}^2\right]$$

Saturation:

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(\upsilon_{GS} - V_t)^2$$

Overdrive voltage: $\upsilon_{OV} = \upsilon_{GS} - V_t$

$$k_n' = C_{ox}\mu_n$$

See example 5.2 of Sedra for more details

MOSFET Example

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$C_{ox} = 8.6$ fF/μm², $\mu_n = 450$ cm²/V·s, and $V_{tn} = 0.5$ V.

$L = 0.18$ μm and $W = 2$ μm.

edge of saturation with $I_D = 100$ μA.

Triode mode:

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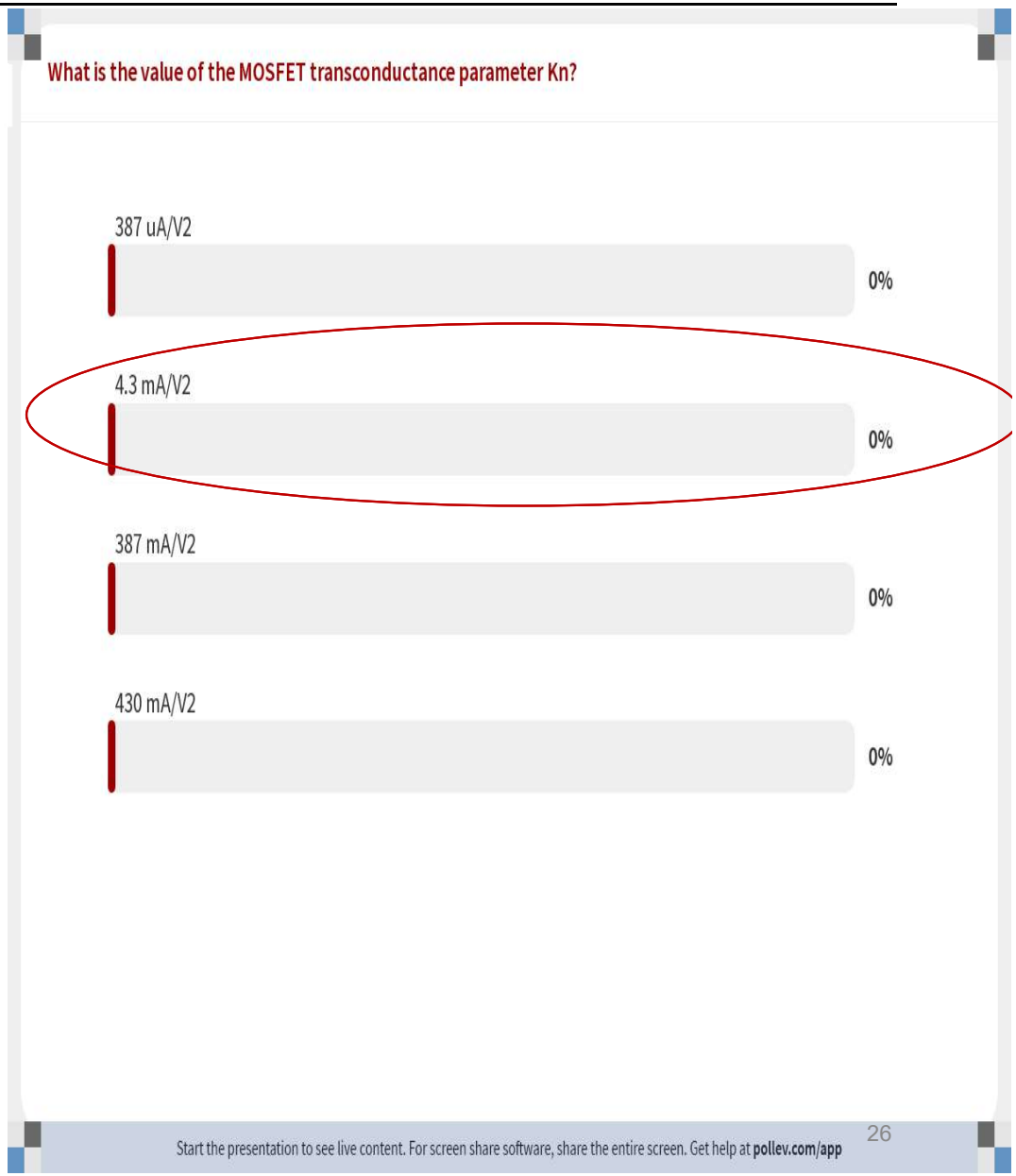

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Saturation:

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Overdrive voltage: $\upsilon_{OV} = \upsilon_{GS} - V_t$

$$k_n' = C_{ox}\mu_n$$

$$C_{ox}\mu_n\left(\frac{W}{L}\right) = 4.3 \times 10^{-3}\ \text{A/V}^2 = 4.3\ \text{mA/V}^2$$

Careful with the units!

See example 5.2 of Sedra for more details

MOSFET Example

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Triode mode:

$$i_D = k_n'\left(\frac{W}{L}\right)\left[\left(\upsilon_{GS} - V_t\right)\upsilon_{DS} - \frac{1}{2}\upsilon_{DS}^2\right]$$

Saturation:

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\left(\upsilon_{GS} - V_t\right)^2$$

Overdrive voltage: $\upsilon_{OV} = \upsilon_{GS} - V_t$

$$C_{ox}\mu_n\left(\frac{W}{L}\right) = 4.3\times10^{-3}\ \text{A/V}^2 = 4.3\ \text{mA/V}^2$$

a) Edge of saturation: $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\left(\upsilon_{GS} - V_t\right)^2 = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\upsilon_{OV}^2 = 100\ \mu A \Rightarrow$

$$\upsilon_{GS} = 0.71\ \text{V}$$
$$\upsilon_{DS} = 0.21\ \text{V}$$

MOSFET Example

Consider an NMOS transistor fabricated in a 0.18-µm process with $L = 0.18$ µm and $W = 2$ µm. The process technology is specified to have $C_{ox} = 8.6$ fF/µm^2, $\mu_n = 450$ cm^2/V·s, and $V_{tn} = 0.5$ V.

(a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100$ µA.
(b) If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50$ µA.
(c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3$ V. Find the change in i_D resulting from v_{GS} changing from 0.7 V by +0.01 V and by –0.01 V.

Triode mode:

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(\upsilon_{GS} - V_t)\upsilon_{DS} - \frac{1}{2}\upsilon_{DS}^2\right]$$

Saturation:

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(\upsilon_{GS} - V_t)^2$$

Overdrive voltage: $\upsilon_{OV} = \upsilon_{GS} - V_t$

$$C_{ox}\mu_n\left(\frac{W}{L}\right) = 4.3\times10^{-3}\ \text{A/V}^2 = 4.3\ \text{mA/V}^2$$

b) $\upsilon_{GS} = 0.71$ V $\quad i_D = 50\ \mu\text{A} < 100\ \mu\text{A}$ in triode mode

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(\upsilon_{GS} - V_t)\upsilon_{DS} - \frac{1}{2}\upsilon_{DS}^2\right] \quad \ldots \rightarrow \upsilon_{DS}^2 - 0.42\upsilon_{DS} + 0.023 = 0$$

$$\upsilon_{DS} = 0.35\ \text{V}$$

$$\upsilon_{DS} = 0.06\ \text{V}$$

Q: which solution do we pick?

MOSFET Example

MACQUARIE University

Consider an NMOS transistor fabricated in a 0.18-µm process with $L = 0.18$ µm and $W = 2$ µm. The process technology is specified to have $C_{ox} = 8.6$ fF/µm^2, $\mu_n = 450$ cm^2/V·s, and $V_{tn} = 0.5$ V.

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$$C_{ox}\mu_n\left(\frac{W}{L}\right) = 4.3\times10^{-3}\ \text{A/V}^2 = 4.3\ \text{mA/V}^2$$

c) $\upsilon_{DS} = 0.3$ V **Q:** which mode is the transistor in?

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(\upsilon_{GS} - V_t)^2$$

$\upsilon_{GS} = 0.71\ \text{V} \longrightarrow i_D = 94.8\ \mu\text{A}$, change $8.8\ \mu\text{A}$

$\upsilon_{GS} = 0.70\ \text{V} \longrightarrow i_D = 86\ \mu\text{A}$

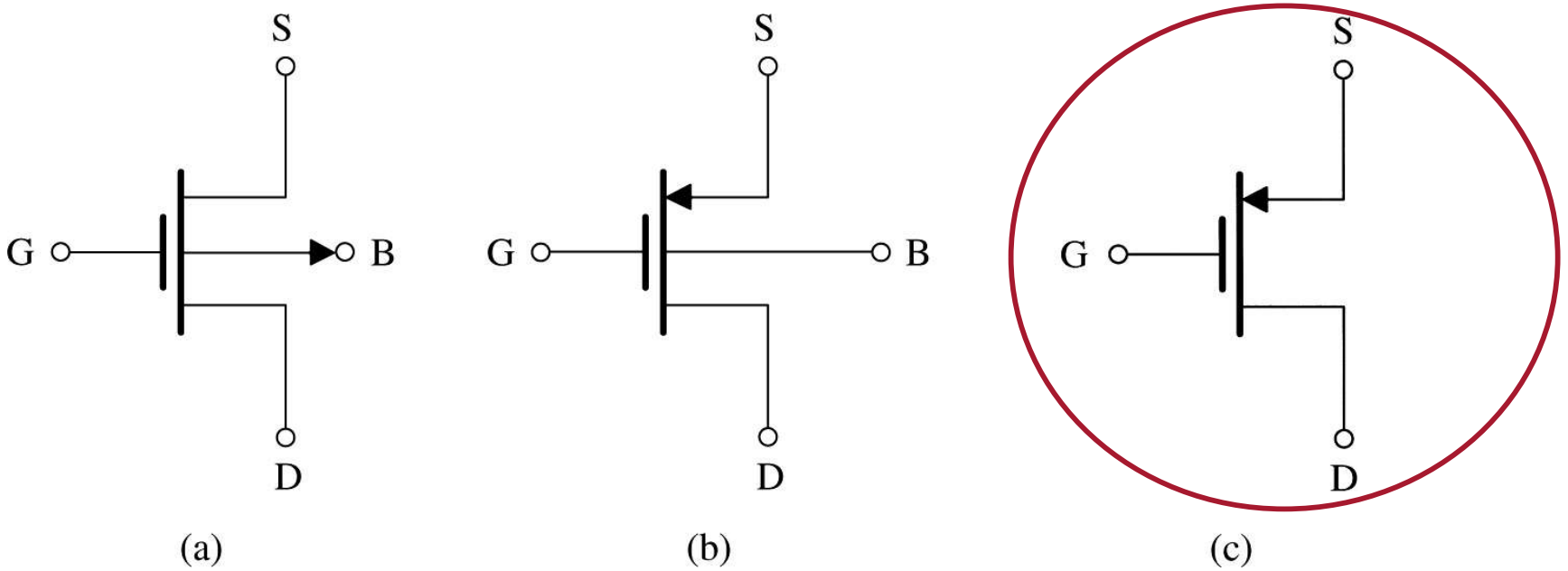
$\upsilon_{GS} = 0.69\ \text{V} \longrightarrow i_D = 77.6\ \mu\text{A}$, change $-8.4\ \mu\text{A}$

Q: is it a linear amplifier?

pMOSFET

CIRCUIT SYMBOLS

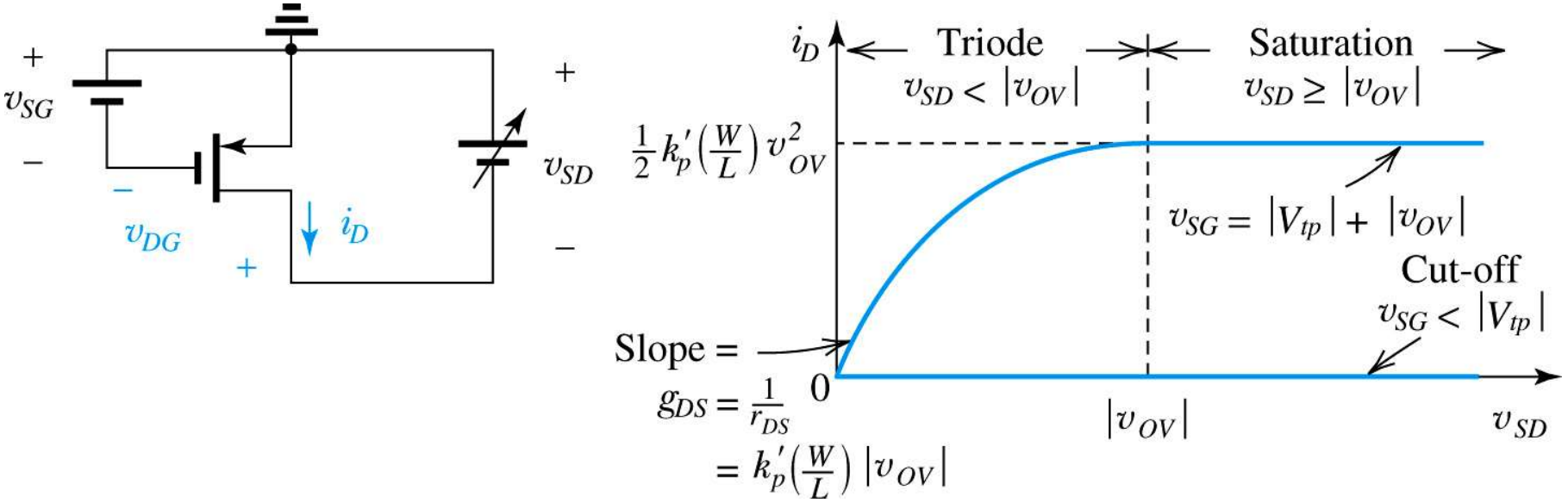
This is the one we will use



(a) Circuit symbol for the *p*-channel enhancement-type MOSFET. (b) Modified symbol with an arrowhead on the source lead. (c) Simplified circuit symbol for the case where the source is connected to the body.

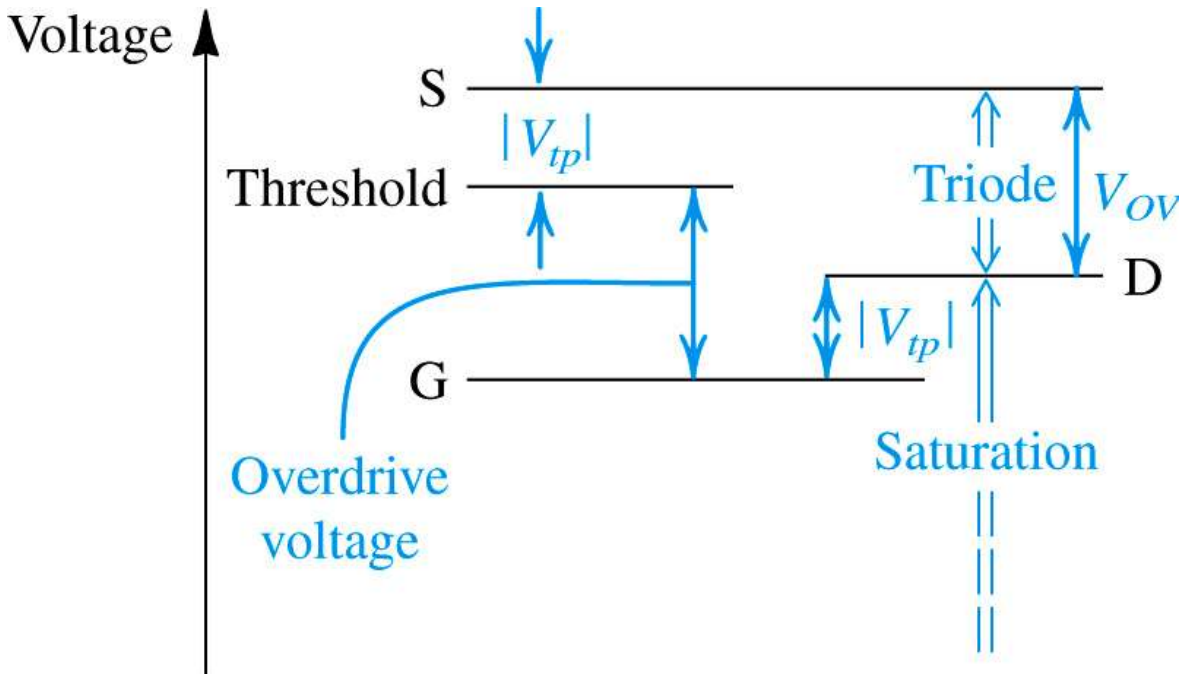
pMOSFET

COMMON SOURCE CHARACTERISTICS



pMOSFET

OPERATING MODE VOLTAGES



The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

Operating Modes

ON FORMULA SHEET

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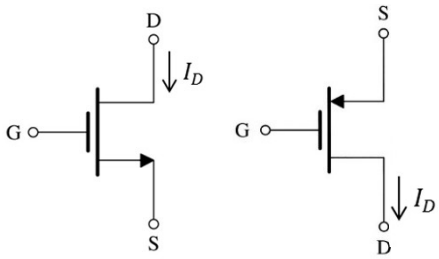
Large-signal modes of operation for nMOSFET

$V_t > 0 \quad V_{DS} > 0 \quad V_A = \infty \quad k_n = \mu_n C_{ox} \frac{W}{L}$

For pMOSFET use the same current equations but with reversed voltage polarities and $V_t < 0 \quad k_p = \mu_p C_{ox} \frac{W}{L}$

nMOSFET pMOSFET



V_{GS}	V_{GD}	V_{DS}	Mode	$I_D(V_{GS}, V_{DS})$
$< \lvert V_t \rvert$	$< \lvert V_t \rvert$	> 0	cut-off	$I_D = 0$
$> \lvert V_t \rvert$	$> \lvert V_t \rvert$	small $\ll V_{GS} - \lvert V_t \rvert$	triode (linear)	$I_D = k_n(V_{GS} - \lvert V_t \rvert)V_{DS}$
$> \lvert V_t \rvert$	$> \lvert V_t \rvert$	$< V_{GS} - \lvert V_t \rvert$	triode	$I_D = k_n\left[(V_{GS} - \lvert V_t \rvert)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
$> \lvert V_t \rvert$	$= \lvert V_t \rvert$	$= V_{GS} - \lvert V_t \rvert$	edge of triode and saturation	$I_D = \frac{1}{2}k_n(V_{GS} - \lvert V_t \rvert)^2$
$> \lvert V_t \rvert$	$< \lvert V_t \rvert$	$> V_{GS} - \lvert V_t \rvert$	saturation	$I_D = \frac{1}{2}k_n(V_{GS} - \lvert V_t \rvert)^2$

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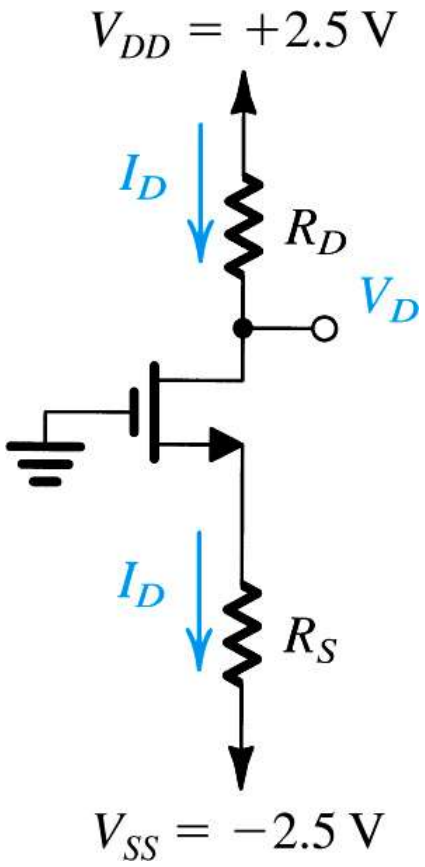
Lecture 5

1. Intro to MOSFETs
2. Device Structure & Operation
3. **Examples**

nMOSFET

EXAMPLE-1 (DC)

Design the circuit so that I_D=0.4 mA and V_D=+0.5 V.
Transistor parameters: V_t=0.7 V, $\mu_n C_{ox}$=100 µA/V^2, L=1µm, W=32 µm.



nMOSFET

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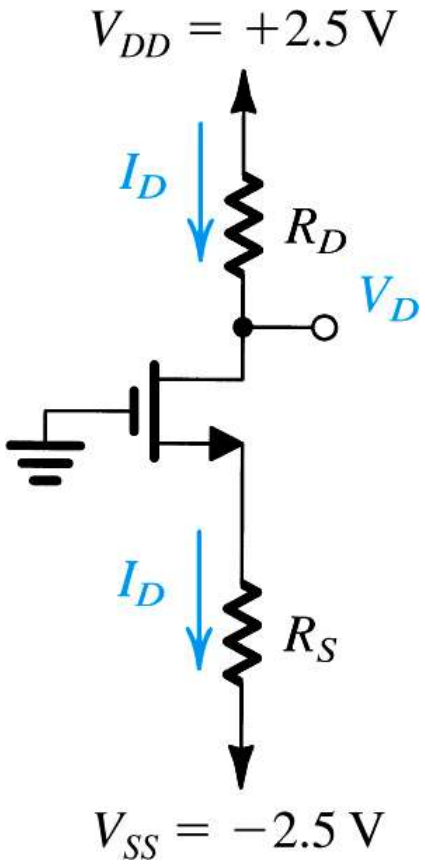

Step 1: R_D

$$R_D = \frac{V_{DD} - V_D}{I_D} = 5\ \text{k}\Omega$$

nMOSFET

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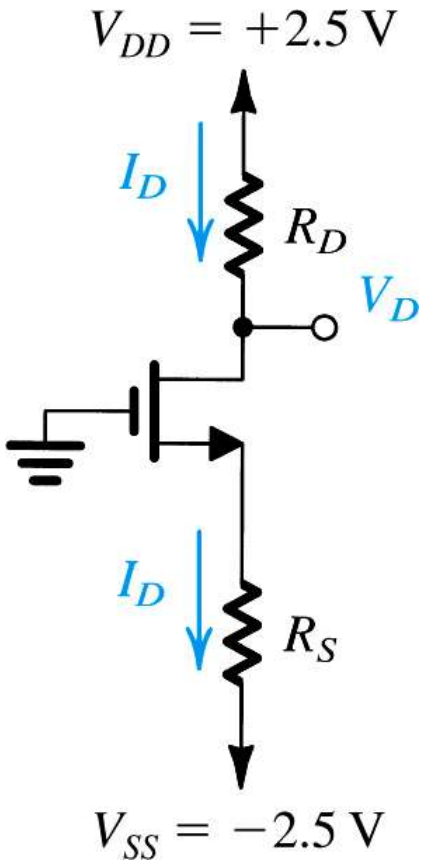

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Step 2: R_S

$$R_S = \frac{V_S - V_{SS}}{I_D}$$

nMOSFET

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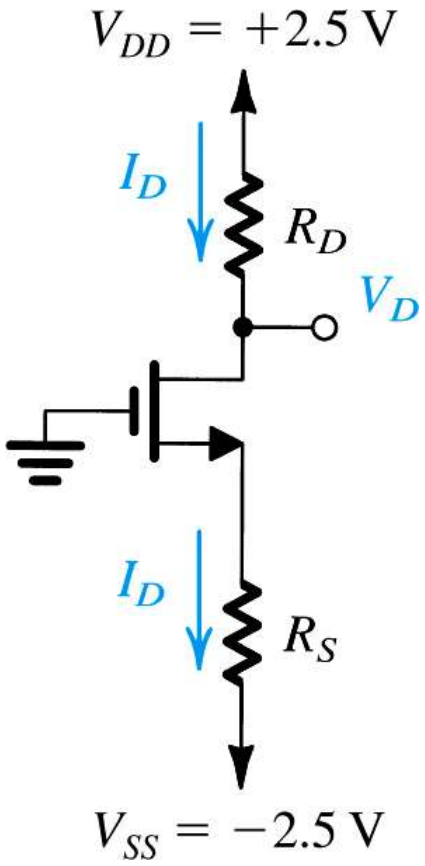

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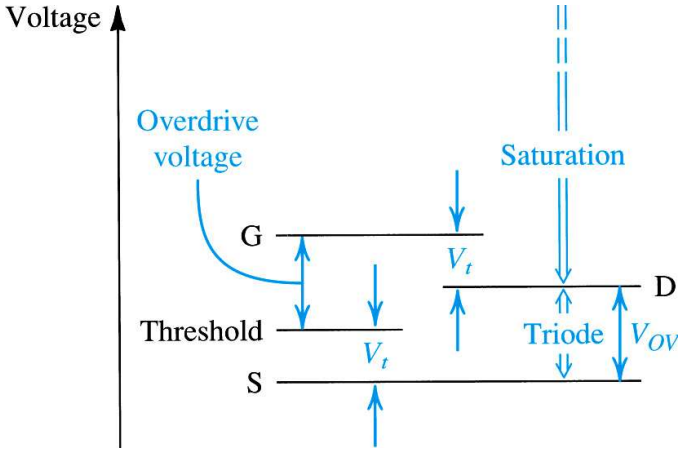
Step 2: R_S

$$R_S = \frac{V_S - V_{SS}}{I_D}$$

Q: which mode is the transistor in?

Need to find V_S



nMOSFET

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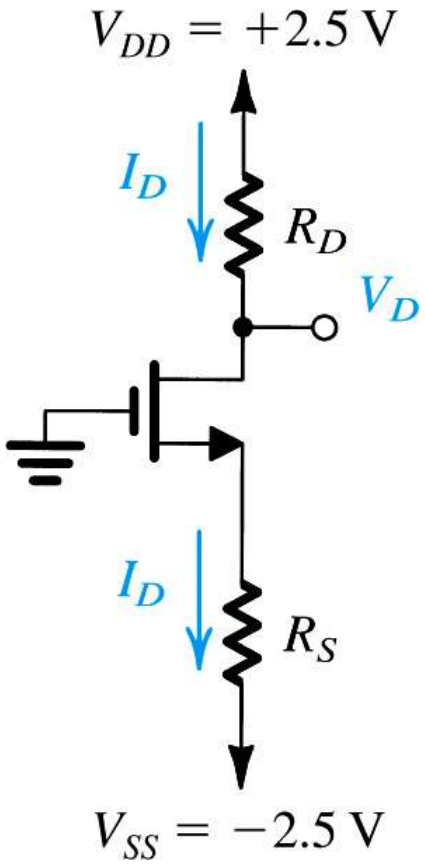

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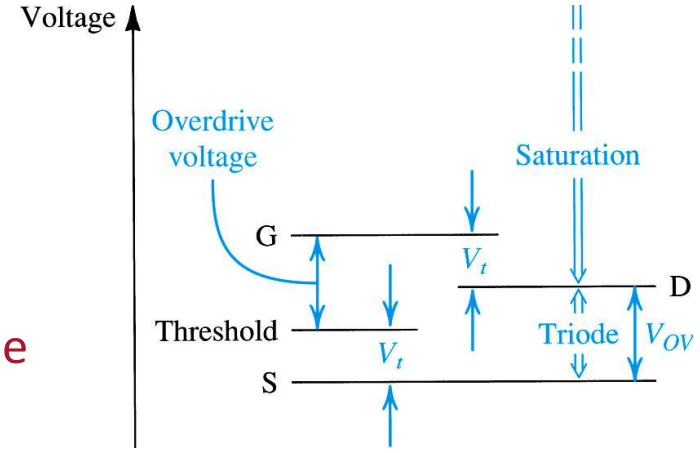
Need to find V_S



Q: which mode is the transistor in?

V_D>V_G, so saturation mode

Operating Modes

ON FORMULA SHEET

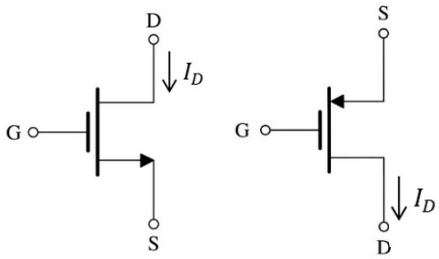
MACQUARIE University

Large-signal modes of operation for nMOSFET

$V_t > 0 \quad V_{DS} > 0 \quad V_A = \infty \quad k_n = \mu_n C_{ox} \frac{W}{L}$

For pMOSFET use the same current equations but with reversed voltage polarities and $V_t < 0 \quad k_p = \mu_p C_{ox} \frac{W}{L}$

nMOSFET pMOSFET



V_{GS}	V_{GD}	V_{DS}	Mode	$I_D(V_{GS}, V_{DS})$
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$> \lvert V_t \rvert$	$> \lvert V_t \rvert$	$< V_{GS} - \lvert V_t \rvert$	triode	$I_D = k_n\left[(V_{GS} - \lvert V_t \rvert)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
$> \lvert V_t \rvert$	$= \lvert V_t \rvert$	$= V_{GS} - \lvert V_t \rvert$	edge of triode and saturation	$I_D = \frac{1}{2}k_n(V_{GS} - \lvert V_t \rvert)^2$
$> \lvert V_t \rvert$	$< \lvert V_t \rvert$	$> V_{GS} - \lvert V_t \rvert$	saturation	$I_D = \frac{1}{2}k_n(V_{GS} - \lvert V_t \rvert)^2$

nMOSFET

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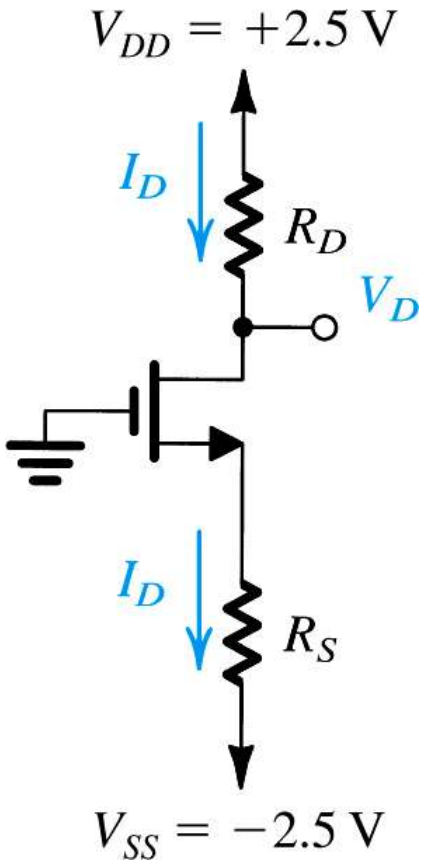

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Step 2: R_S

$$R_S = \frac{V_S - V_{SS}}{I_D}$$

Q: which mode is the transistor in?

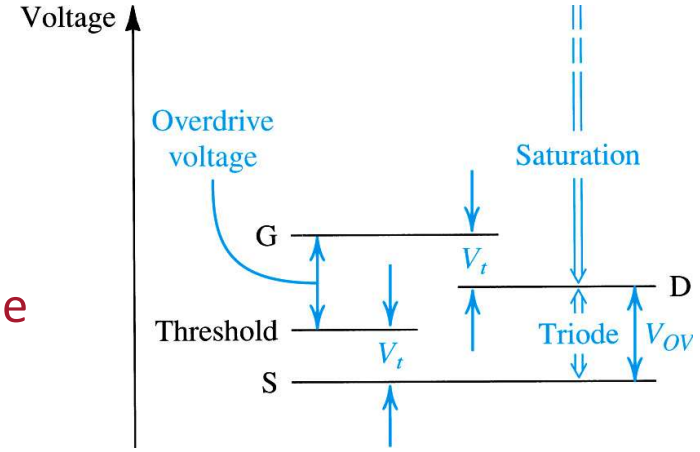
$V_D > V_G$, so saturation mode

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

Solve for V_{OV}: $V_{OV} = 0.5V$

$$V_{GS} = V_{OV} + V_t = 1.2V$$

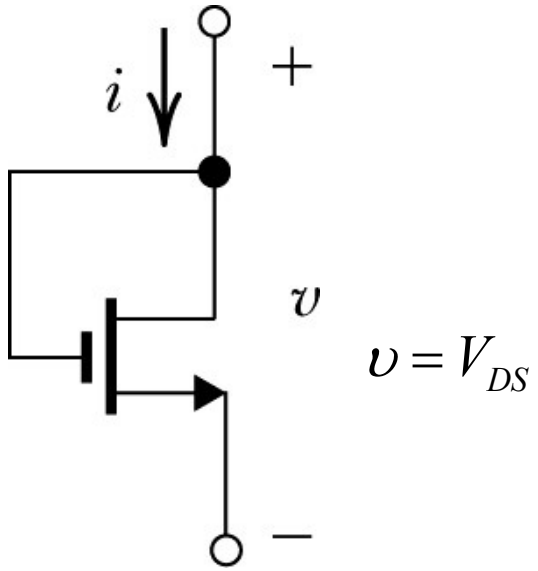
$$V_S = -1.2V \qquad R_S = \frac{V_S - V_{SS}}{I_D} = 3.25\ \text{k}\Omega$$



nMOSFET

EXAMPLE-2 (DC)

Find the i-v relationship of the following two-terminal device.
The transistor parameters, V_t, $\mu_n C_{ox}$, L and W are given.



nMOSFET

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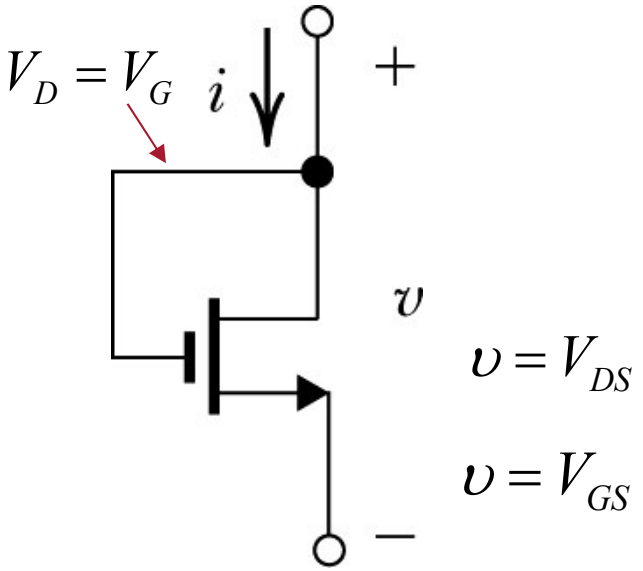
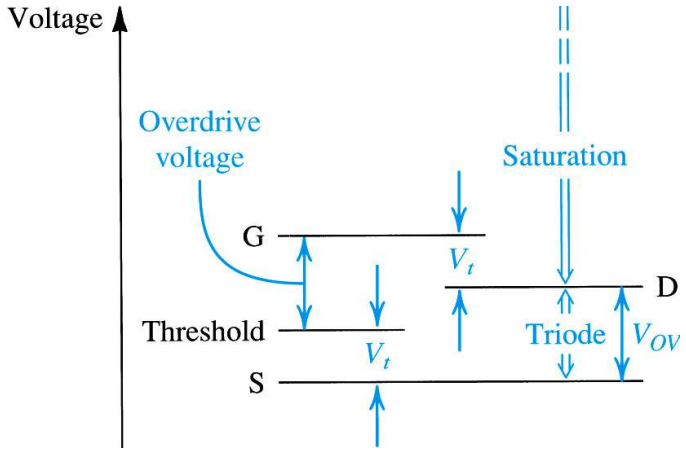


Q: Which mode is the transistor in?



nMOSFET

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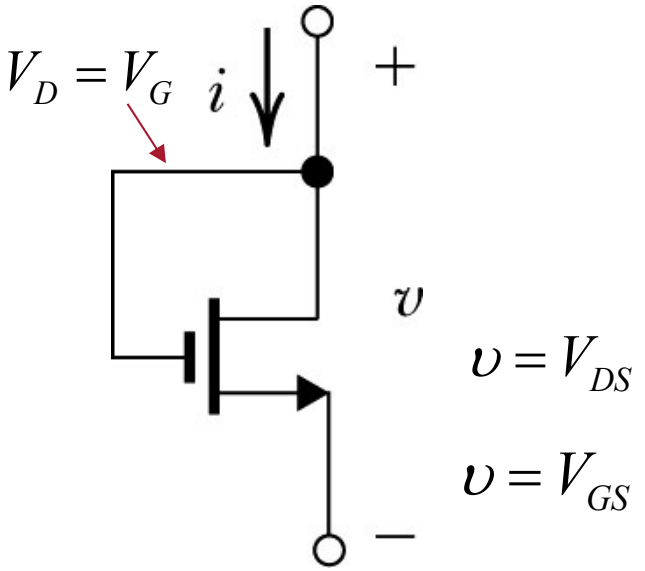

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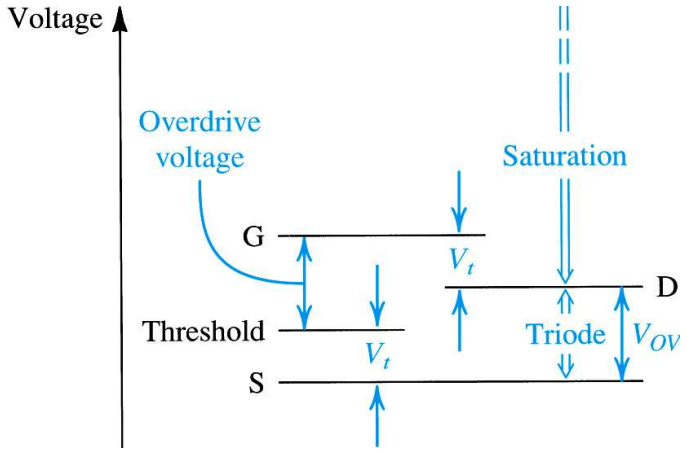


A1: Saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_t\right)^2$$

$$i = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\upsilon - V_t\right)^2$$

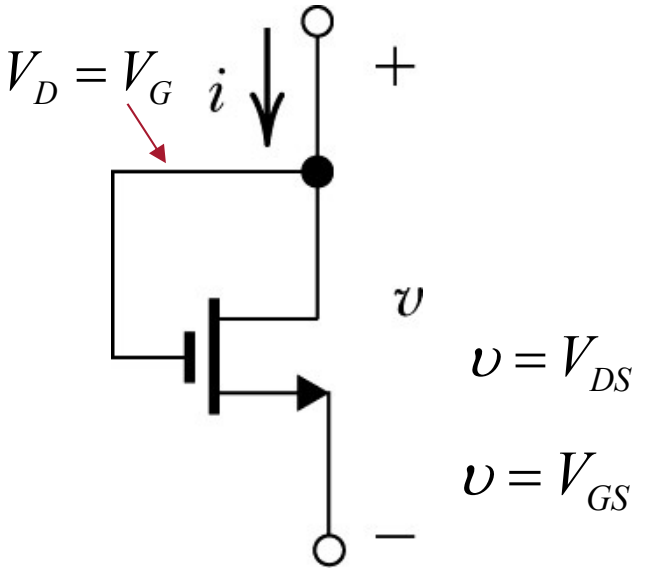
IF $V_{GS} > V_t$

$\upsilon > V_t$

nMOSFET

EXAMPLE-2 (DC)

Find the i-v relationship of the following two-terminal device.
The transistor parameters, V_t, $\mu_n C_{ox}$, L and W are given.



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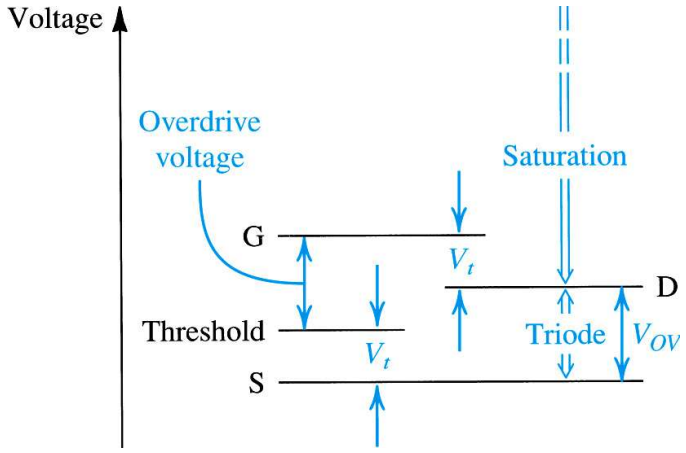

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$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_t\right)^2$$

$$i = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\upsilon - V_t\right)^2$$

IF $V_{GS} > V_t$

$\upsilon > V_t$

A2: Cutoff

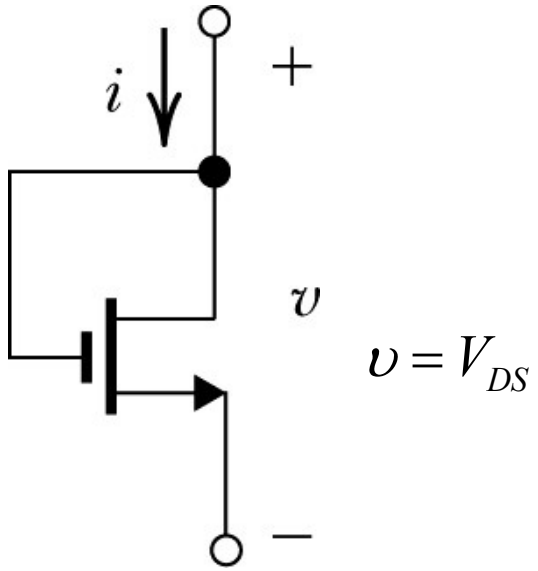
$V_{GS} < V_t$

$i = 0$ $\quad \upsilon < V_t$

nMOSFET

EXAMPLE-2 (DC)

Find the i-v relationship of the following two-terminal device.
The transistor parameters, V_t, $\mu_n C_{ox}$, L and W are given.



$\upsilon = V_{DS}$

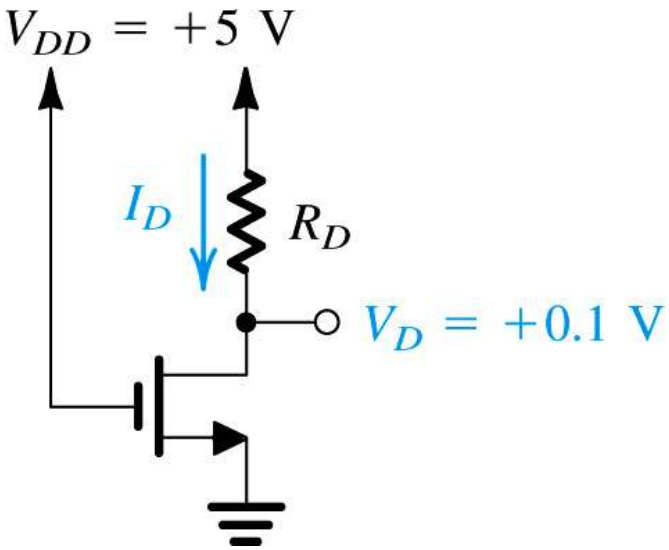
$$\upsilon \le V_t \qquad i = 0$$

$$\upsilon > V_t \qquad i = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\upsilon - V_t\right)^2$$

nMOSFET

EXAMPLE-3 (DC)

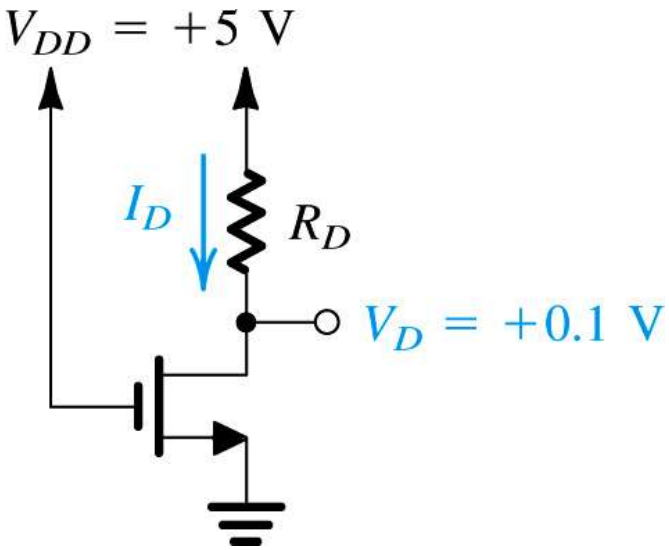
Which mode is this transistor in? V_t=1 V, $k_n'(W/L)$=1 mA/V^2

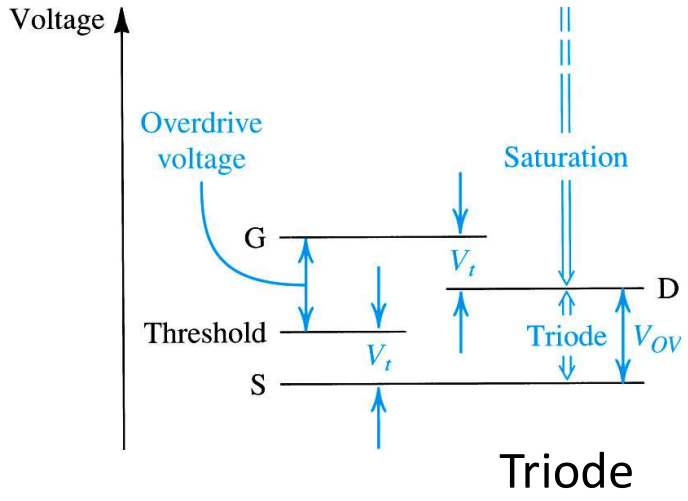


nMOSFET

EXAMPLE-3 (DC)

Which mode is this transistor in? V_t=1 V, $k_n'(W/L)$=1 mA/V^2

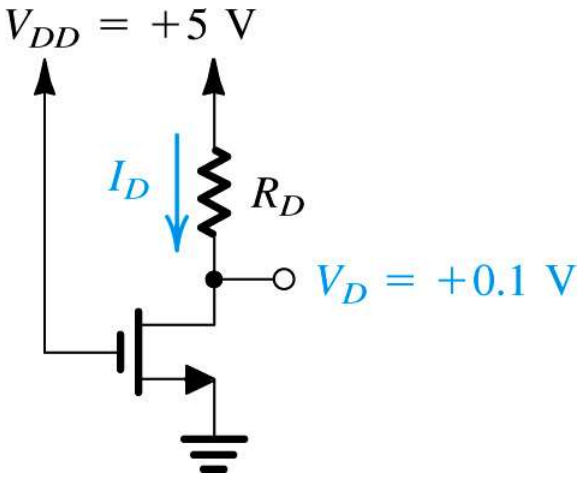




Triode

Operating Modes

ON FORMULA SHEET



V_t=1 V, $k_n'(W/L)$=1 mA/V²

I_D=0.395 mA

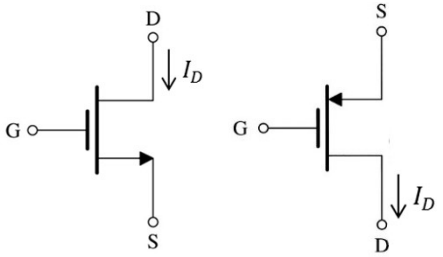
R_D=12.4 kΩ

Large-signal modes of operation for nMOSFET

$V_t > 0 \quad V_{DS} > 0 \quad V_A = \infty \quad k_n = \mu_n C_{ox} \frac{W}{L}$

For pMOSFET use the same current equations but with reversed voltage polarities and $V_t < 0 \quad k_p = \mu_p C_{ox} \frac{W}{L}$

nMOSFET pMOSFET

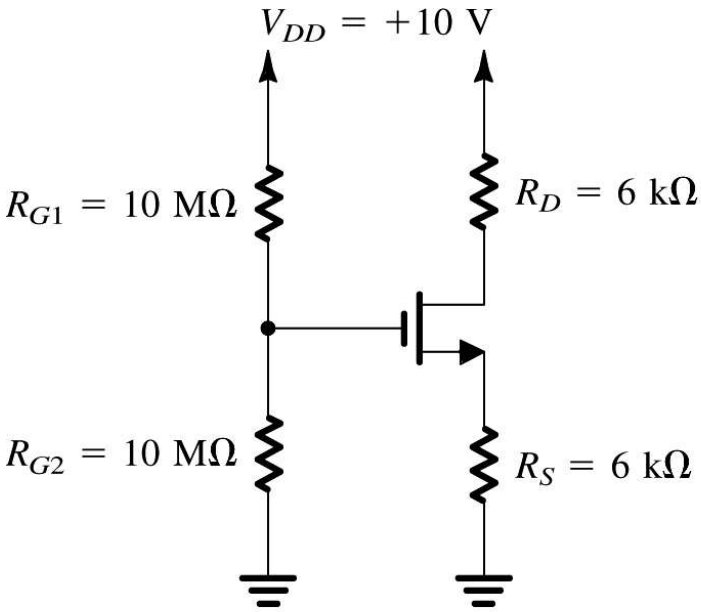


V_{GS}	V_{GD}	V_{DS}	Mode	$I_D(V_{GS}, V_{DS})$
$< \lvert V_t \rvert$	$< \lvert V_t \rvert$	> 0	cut-off	$I_D = 0$
$> \lvert V_t \rvert$	$> \lvert V_t \rvert$	small $\ll V_{GS} - \lvert V_t \rvert$	triode (linear)	$I_D = k_n(V_{GS} - \lvert V_t \rvert)V_{DS}$
$> \lvert V_t \rvert$	$> \lvert V_t \rvert$	$< V_{GS} - \lvert V_t \rvert$	triode	$I_D = k_n\left[(V_{GS} - \lvert V_t \rvert)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
$> \lvert V_t \rvert$	$= \lvert V_t \rvert$	$= V_{GS} - \lvert V_t \rvert$	edge of triode and saturation	$I_D = \frac{1}{2}k_n(V_{GS} - \lvert V_t \rvert)^2$
$> \lvert V_t \rvert$	$< \lvert V_t \rvert$	$> V_{GS} - \lvert V_t \rvert$	saturation	$I_D = \frac{1}{2}k_n(V_{GS} - \lvert V_t \rvert)^2$

nMOSFET

EXAMPLE-4 (DC)

Determine the voltages at all nodes and the current at all branches in the circuit below. V_t=1 V, $k_n'(W/L)$=1 mA/V^2.

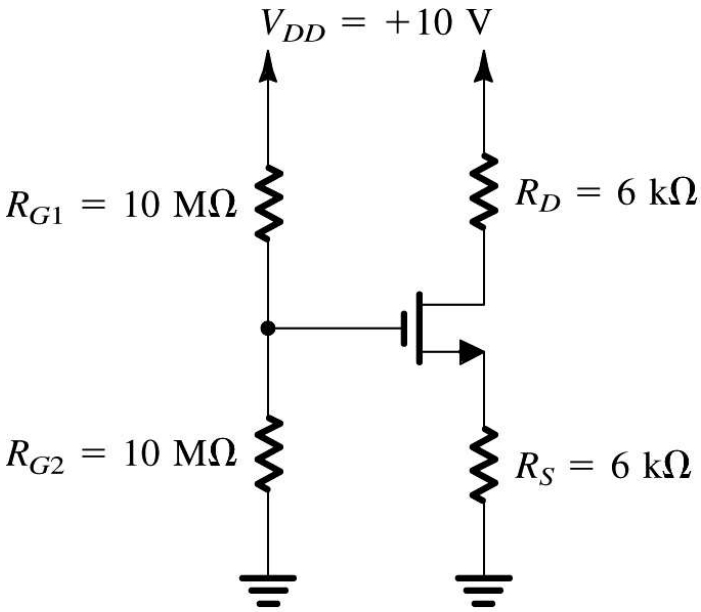


(a)

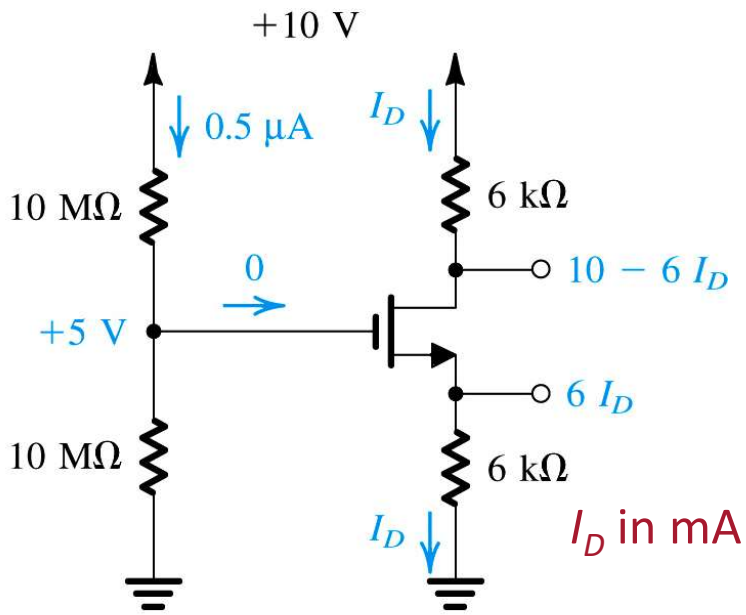
nMOSFET

EXAMPLE-4 (DC)

Determine the voltages at all nodes and the current at all branches in the circuit below. V_t=1 V, $k_n'(W/L)$=1 mA/V^2.



(a)

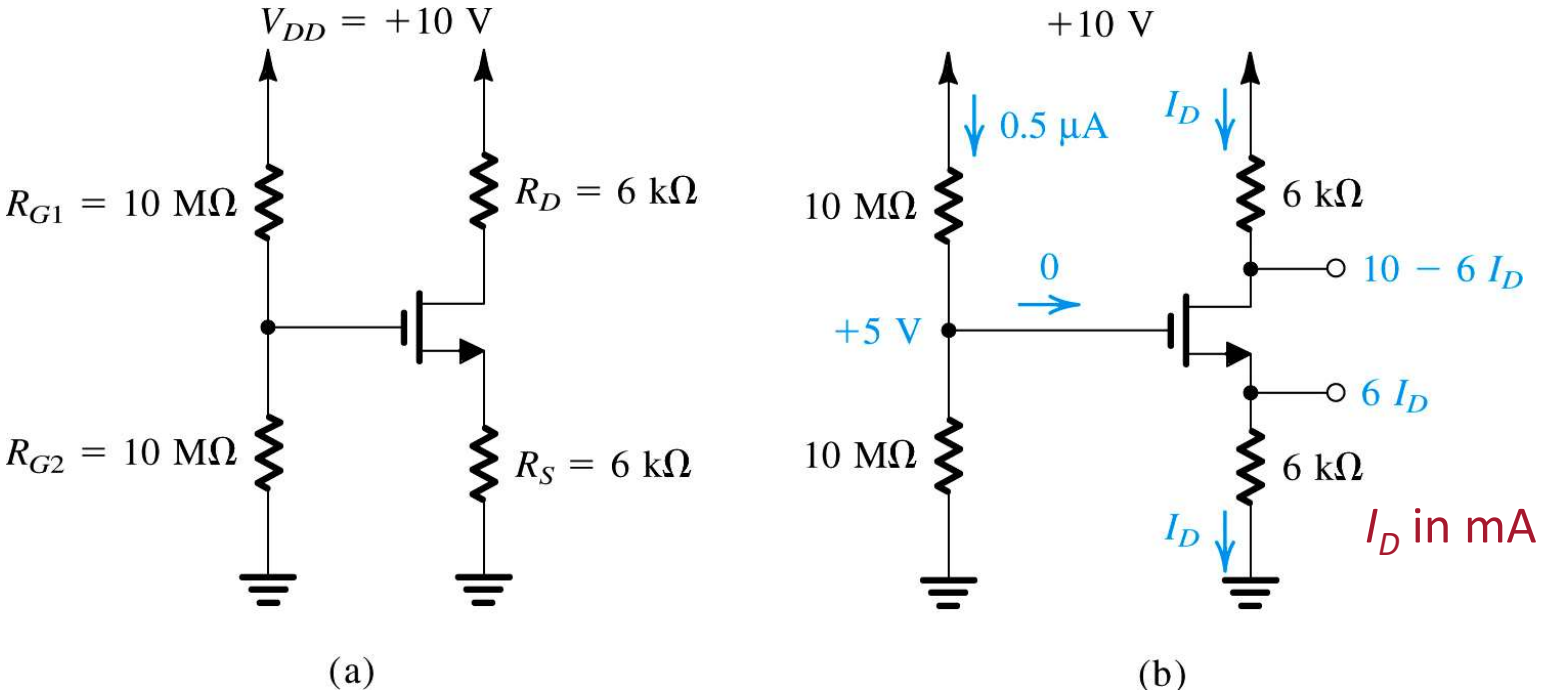


(b)

nMOSFET

EXAMPLE-4 (DC)

Determine the voltages at all nodes and the current at all branches in the circuit below. V_t=1 V, $k_n'(W/L)$=1 mA/V^2.



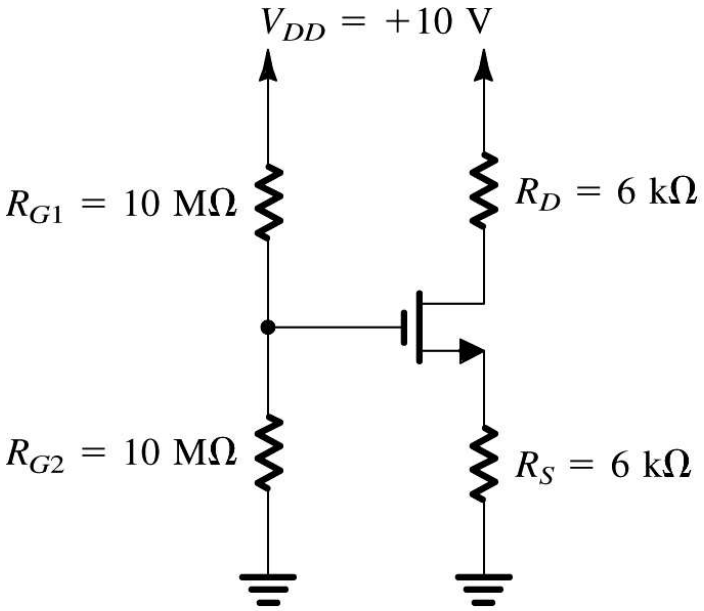
Assuming saturation mode:

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \xrightarrow{Expand} 18I_D^2 - 25I_D + 8 = 0$$

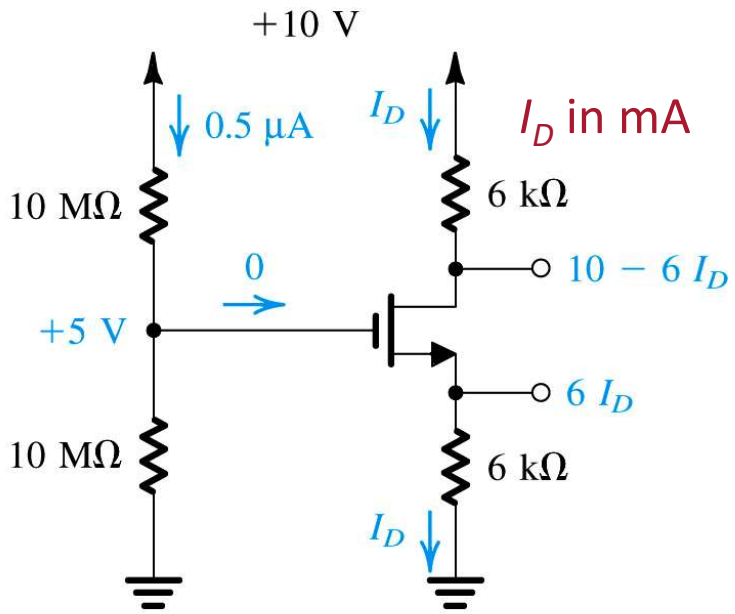
nMOSFET

EXAMPLE-4 (DC)

Determine the voltages at all nodes and the current at all branches in the circuit below. V_t=1 V, $k_n'(W/L)$=1 mA/V^2.



(a)



(b)

Assuming saturation mode: $I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2 \Rightarrow 18I_D^2 - 25I_D + 8 = 0$

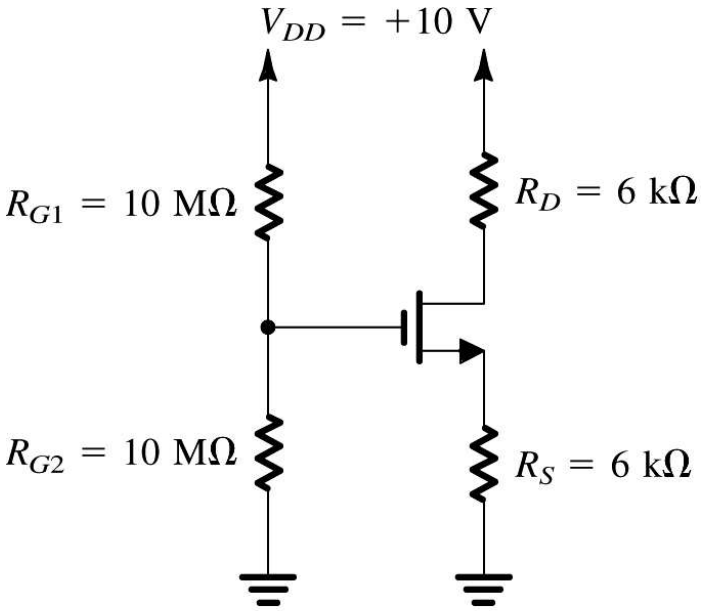
$I_D = 0.89mA$

$I_D = 0.5mA$

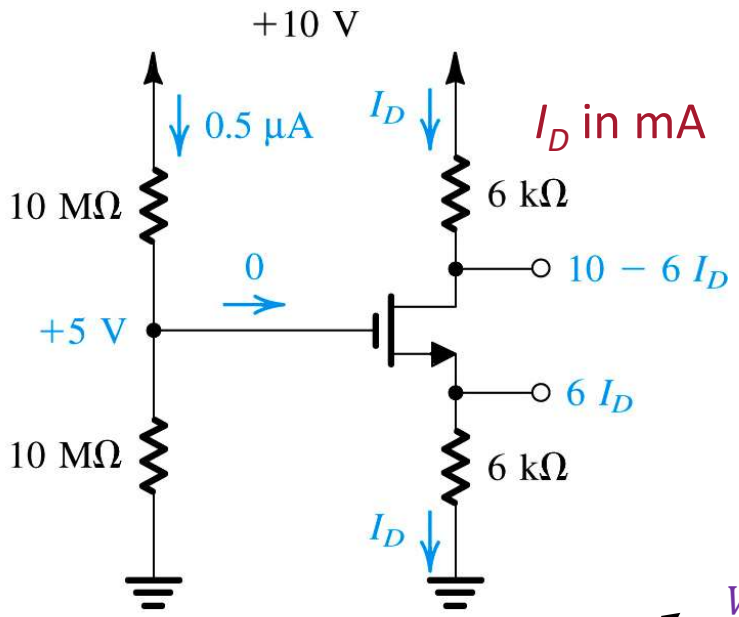
nMOSFET

EXAMPLE-4 (DC)

Determine the voltages at all nodes and the current at all branches in the circuit below. V_t=1 V, $k_n'(W/L)$=1 mA/V^2.



(a)



(b)

Assuming saturation mode: $I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_t)^2 \Rightarrow 18I_D^2 - 25I_D + 8 = 0$

$I_D = 0.89mA$ → $V_S = 5.34V$ ✗

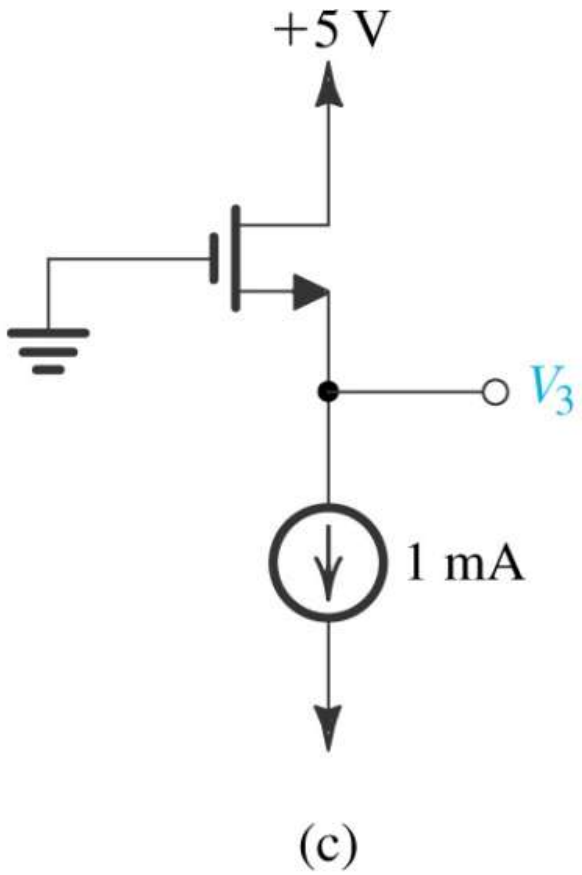
$I_D = 0.5mA$ → $V_S = 3V$

nMOSFET

EXAMPLE-5 (DC)

Determine the voltages at all nodes and the current at all branches in the circuit below. V_t=1 V, $k_n'(W/L)$=0.4 mA/V^2.

See Sedra P5.37c for more details



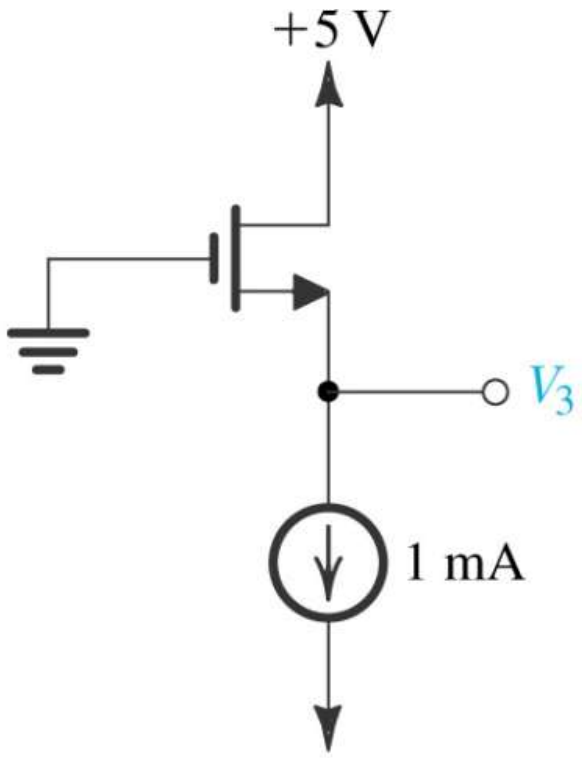
(c)

nMOSFET

EXAMPLE-5 (DC)

Determine the voltages at all nodes and the current at all branches in the circuit below in saturation. V_t=1 V, $k_n'(W/L)$=0.4 mA/V^2.

See Sedra P5.37c for more details



(c)

$$V_{GS} = -V_3$$

$$V_{DS} = 5 - V_3$$

$$V_D = 5V$$

$$V_G = 0V$$

$$1 = \frac{1}{2} 0.4\,(V_{GS} - 1)^2$$

$$V_{GS}^2 - 2V_{GS} - 4 = 0$$

$$V_{GS} = 3.235V \; or \; -1.235V$$

$$V_{GS} > V_t \xrightarrow{requires} V_{GS} = 3.235V \quad -1.235V$$

$$V_S = V_3 = -V_{GS} = -3.235V$$

This week

LAB + FIRST ASSIGNMENT

MACQUARIE University

BJT Lab:

- The worksheet is available on iLearn
- You will use the AD2 and your kit to make a BJT amplifier with biasing
- Complete as much of the lab as you can before attending the support session (prelab part is the minimum requirement)

First Assignment!

- The first assignment is available now.
- An iLearn quiz on the topics of diodes and BJTs
- Submission is due by midnight Friday 25th