Exploring weaker atomic instructions for latch-free data structures

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1. INTRODUCTION

Since the rise of multi-core architectures, multi-threaded concurrent programming quickly become the technique for further improving program performances.

The biggest problem in concurrent programming is to synchronize access of shared memories. There are generally two ways of synchronization mechnisms. The first one is blocking through locks. Before accessing an area of shared memories, a thread must first aquire a lock. If the lock is currently held by another thread, the aquiring thread will yield the CPU and wait for the lock. The second one is non-blocking synchronization through special atomic instructions. The de facto atomic instruction is the Compare-and-Swap (CAS). Most commonly, when a thread wants to access a shared memory block, it first uses an atomic instruction to atomically change a small piece of memory to an expected state. Other threads see the change and so won't break the thread's operations.

Atomic instruction based non-blocking synchronization has the advantage of low system overhead comparing with blocking synchronizations. Recently, a lot of research efforts have been put into developing latch-free data structures. However, most of them are based on the strongest atomic instruction, i.e. CAS. For example, OpenJDK 9 uses only CAS to implement all its atomic functionalities (The java.util.concurrent.atomic).

Except for CAS, there are several weaker atomic instructions, as listed in Table 1. CAS is the strongest atomic instruction. It is able to implement all other instructions. What it does is (this is how X86 implemented it) given a memory word m_1, compare the value of it with another value c, if the two matches, replace the value of m_1 to a new value m_2.

The problem of CAS is that it can fail. The typical usage of CAS is using a while loop such as the following simple code block:

```
while (CAS fail) { ... }
```

It basically means keeping doing CAS until it succeeds.

Table 1: Atomic instructions provided by various platforms

	Compare-and-Swap	Swap	Test-and-Set	Fetch
ARM	LL/SC	deprecated	no	
POWER	LL/SC	no	no	
SPARC	yes	deprecated	yes	
x86	yes	yes	yes	

This can result in poor performances if the number of threads concurrently doing CAS is big.

On the other hand, the weaker atomic instructions succeed every time. This difference may result in highly efficient algorithms for some concurrent problems. For example, for an atomic integer ID generator, Fetch-and-Add should be able to outperform Compare-and-Swap a lot in high contention situations. Recently, Morrison et. al. designed a new FIFO queue using Fetch-and-Add [1] which dramatically outperforms CAS based and blocking locking based FIFO queues in high contention situations.

2. MILESTONES

Week 1 2: Add weak atomic instruction support to OpenJDK 9. And test the performance

Week 3 4: Find a data structure that is suitable for implementation using weaker atomic instructions.

Week 5 : Implement the chosen data structure.

3. REFERENCES

[1] A. Morrison and Y. Afek. Fast concurrent queues for x86 processors. In *Proceedings of the 18th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, PPoPP '13, pages 103–112, New York, NY, USA, 2013. ACM.