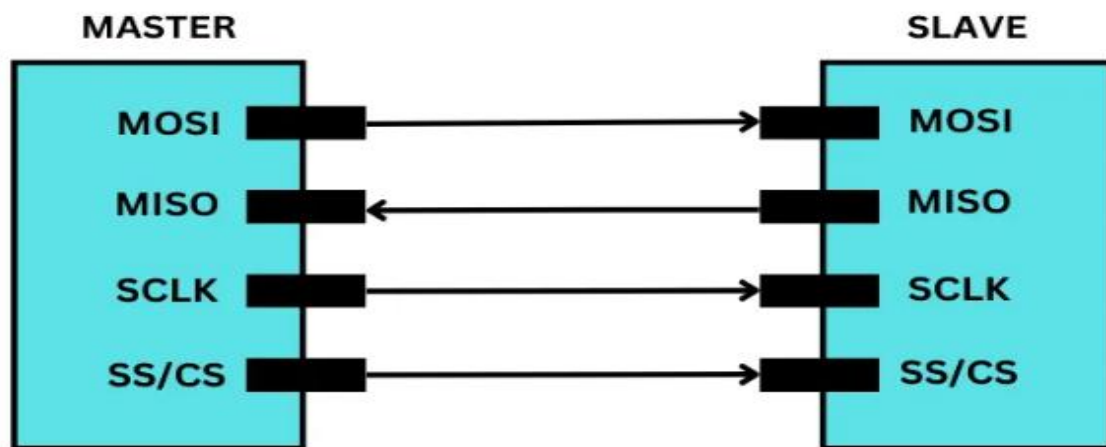


*Created  
By*

Ismail Raafat Fawzy

## SPI\_Interface



## Introduction to SPI Communication Protocol:

The Serial Peripheral Interface (SPI) is a synchronous serial communication protocol developed by Motorola, widely used for short-distance communication in embedded systems. SPI allows for high-speed data transfer between a master device and one or more peripheral devices. It is particularly valued for its simplicity, efficiency, and low pin count, making it an essential protocol in digital design and embedded systems.

## Definition of SPI Communication Protocol

SPI operates in a master-slave configuration, where the master device initiates communication and controls the clock signal. The key signals in SPI communication are:

- **MOSI (Master Out Slave In):** Data line for transmission from master to slave.
- **MISO (Master In Slave Out):** Data line for transmission from slave to master.
- **SCLK (Serial Clock):** Clock signal generated by the master to synchronize data transfer.
- **SS (Slave Select):** Control line for selecting the slave device.

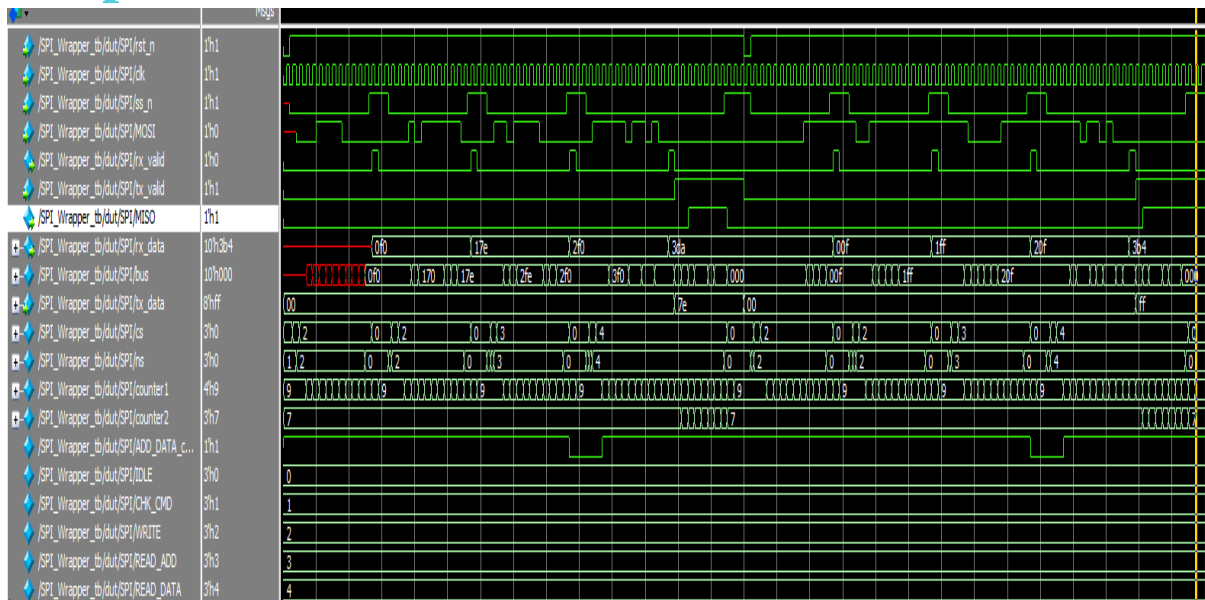
Data transfer in SPI is full-duplex, meaning data can be sent and received simultaneously. The protocol supports different modes of operation, determined by the clock polarity (CPOL) and clock phase (CPHA) settings, allowing flexibility in communication.

## Importance of SPI Communication Protocol

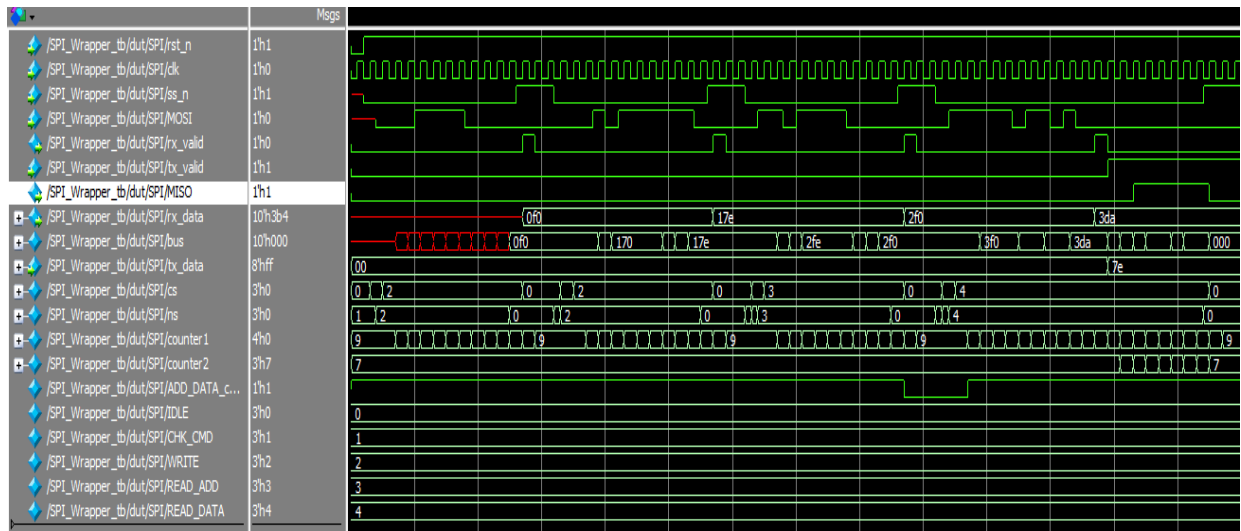
SPI is crucial in embedded systems and digital design for several reasons:

1. **Speed:** SPI supports high-speed data transfers, making it suitable for applications requiring quick data exchanges, such as sensors, memory devices, and display controllers.
2. **Simplicity:** The protocol's straightforward design and minimal overhead make it easy to implement and debug, reducing development time and complexity.
3. **Efficiency:** SPI's full-duplex communication and streamlined signal lines contribute to efficient data transmission, minimizing latency and maximizing throughput.
4. **Scalability:** SPI can connect multiple slave devices to a single master, using individual slave select lines, allowing for scalable and expandable system designs.
5. **Versatility:** SPI is compatible with a wide range of devices, from simple sensors to complex microcontrollers, making it a versatile choice for various applications.

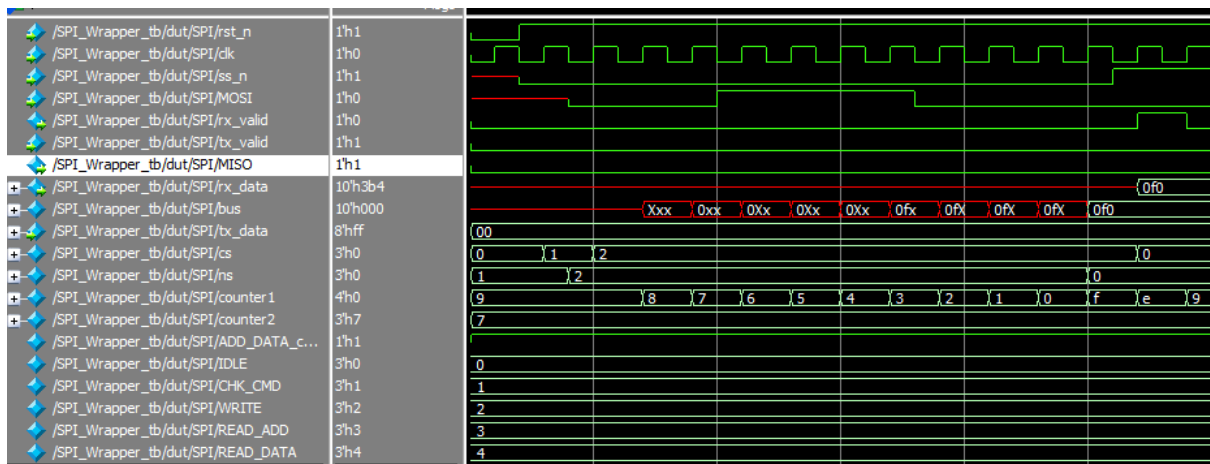
## Snapshot of the whole wave form:



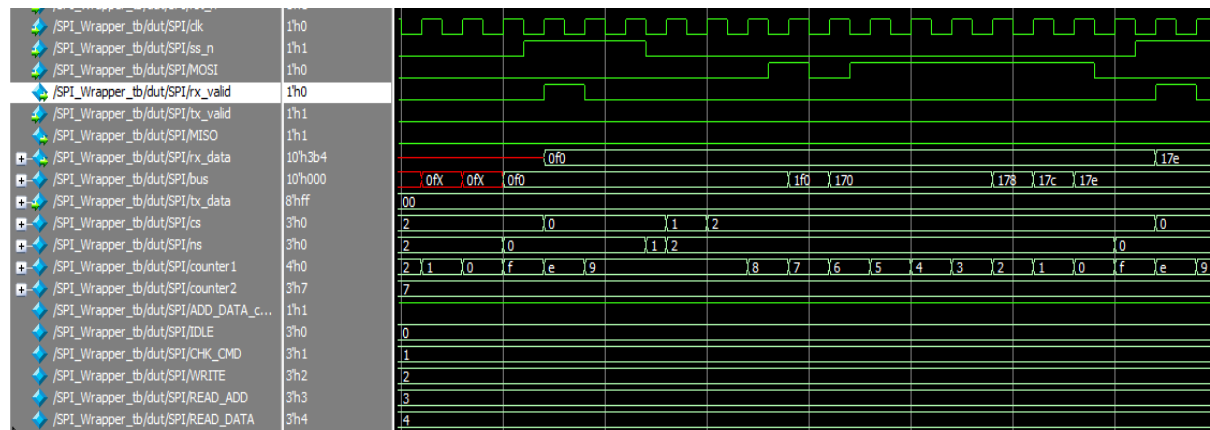
# First scenario:



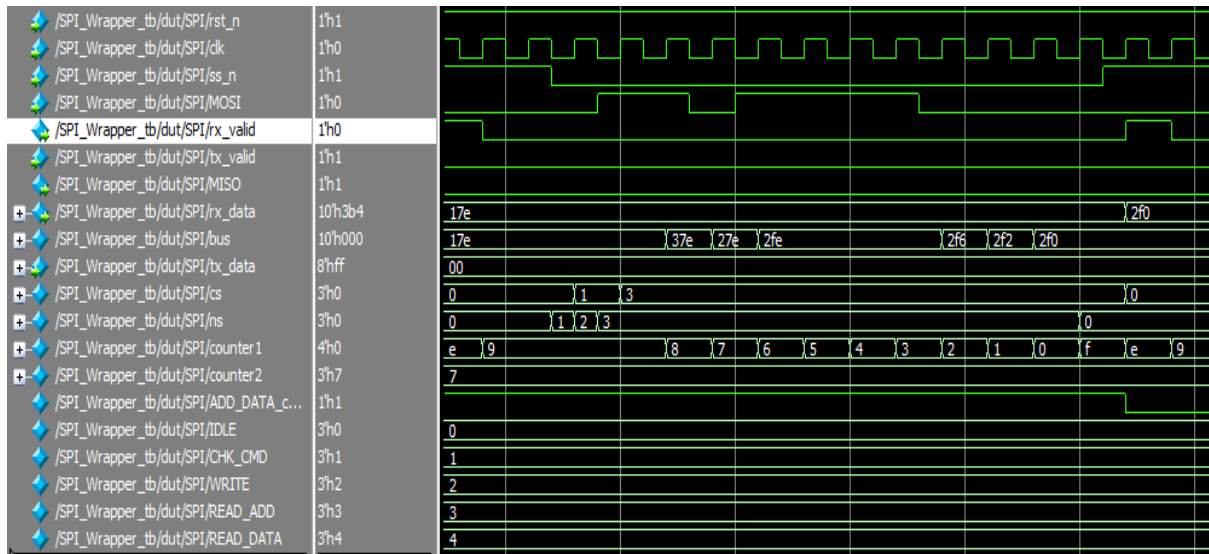
## • WRITE state (Address):



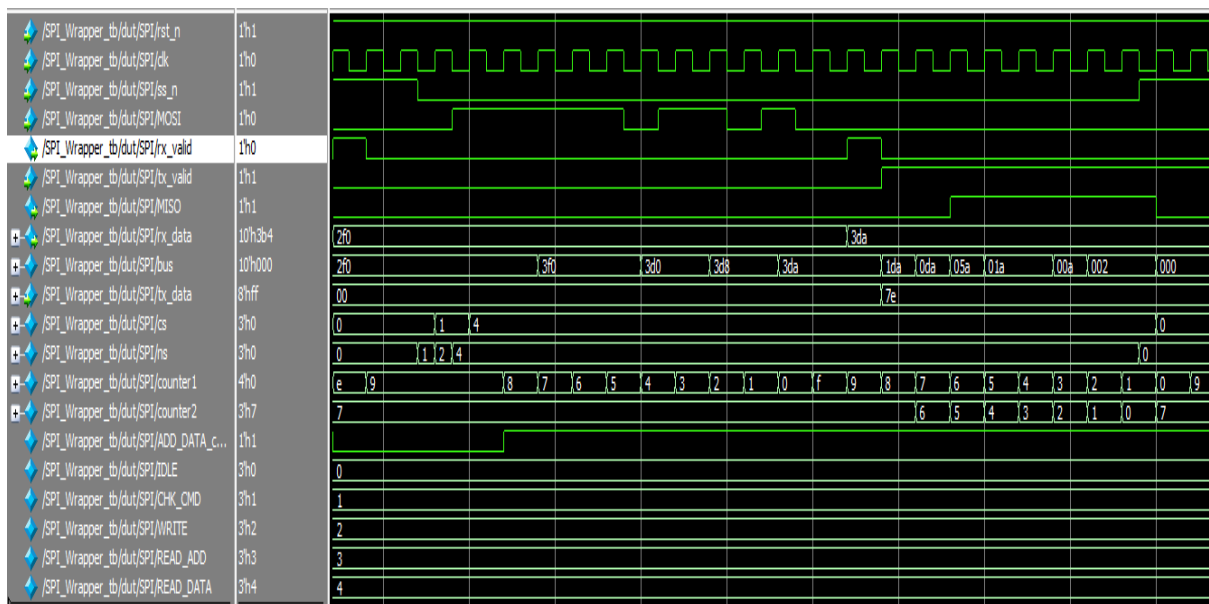
## • WRITE state (Data):



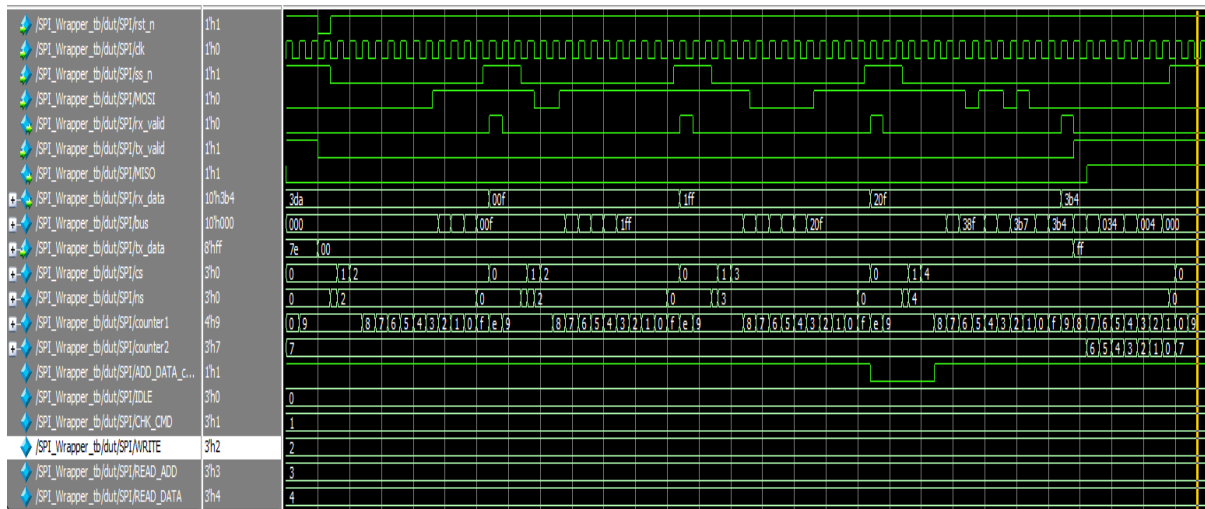
## • READ\_ADD state:



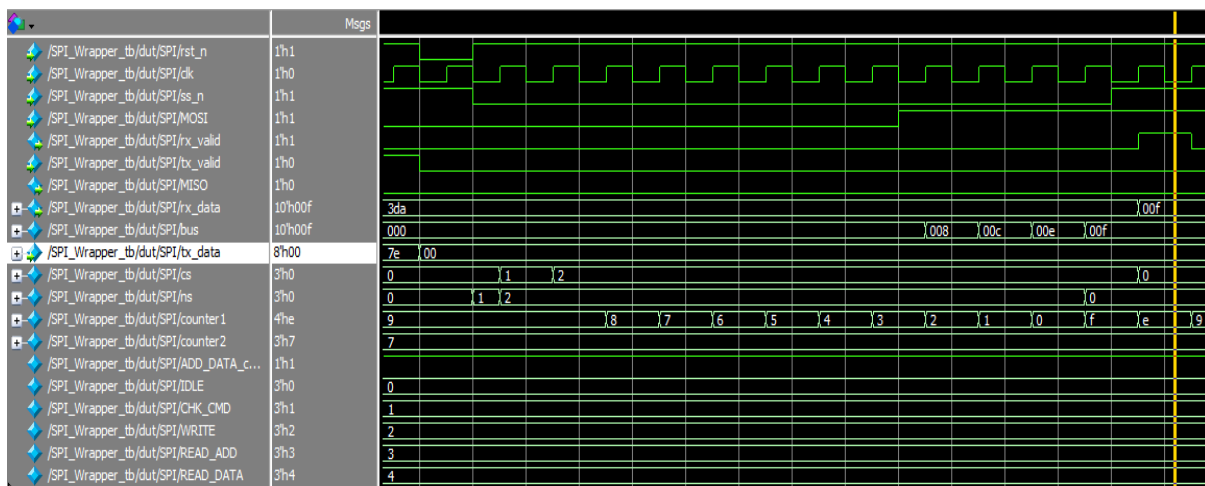
## • READ\_DATA state:



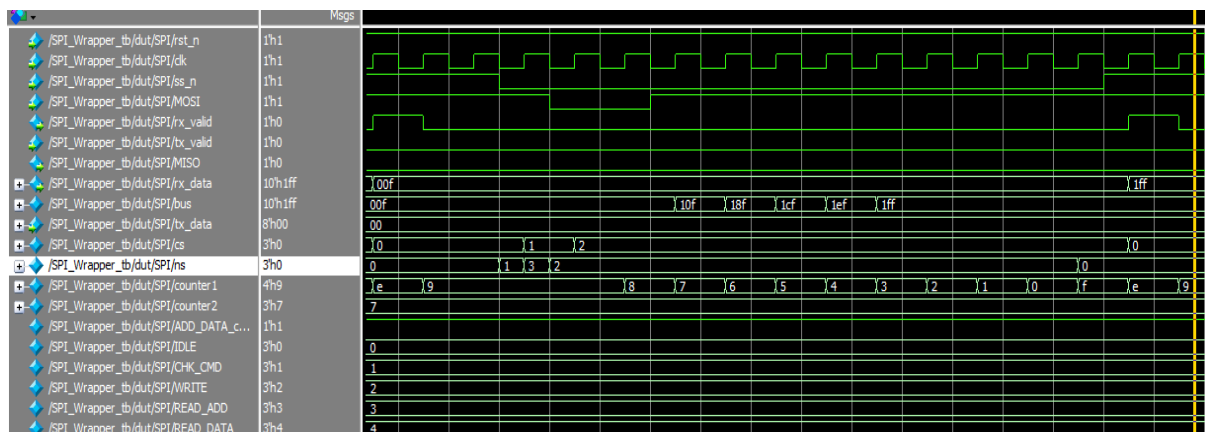
## Second scenario:



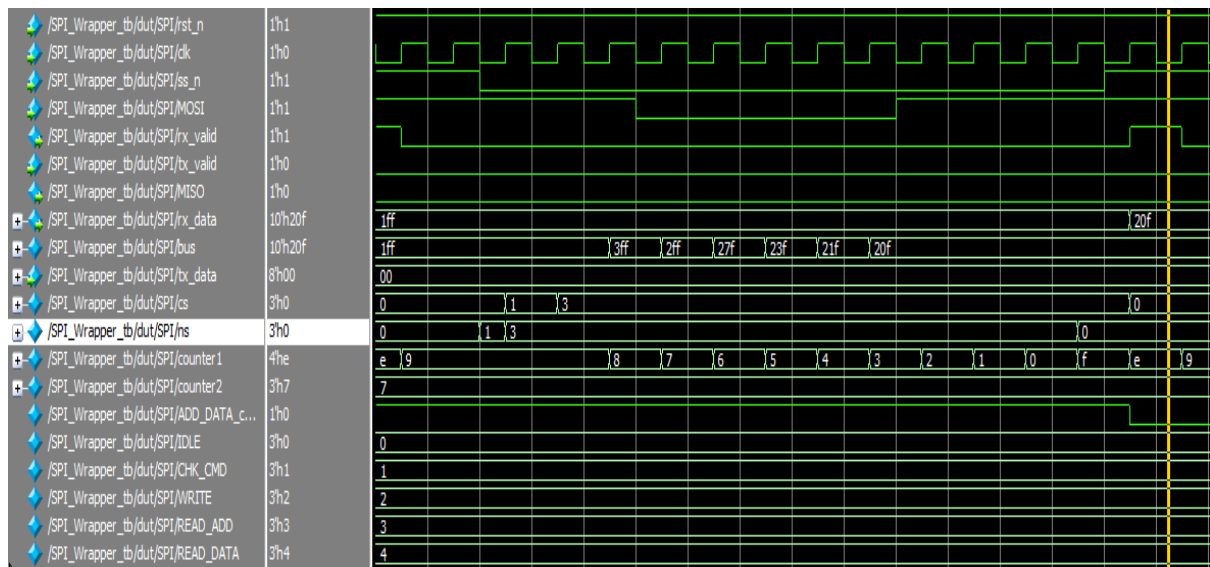
### • WRITE state (Address):



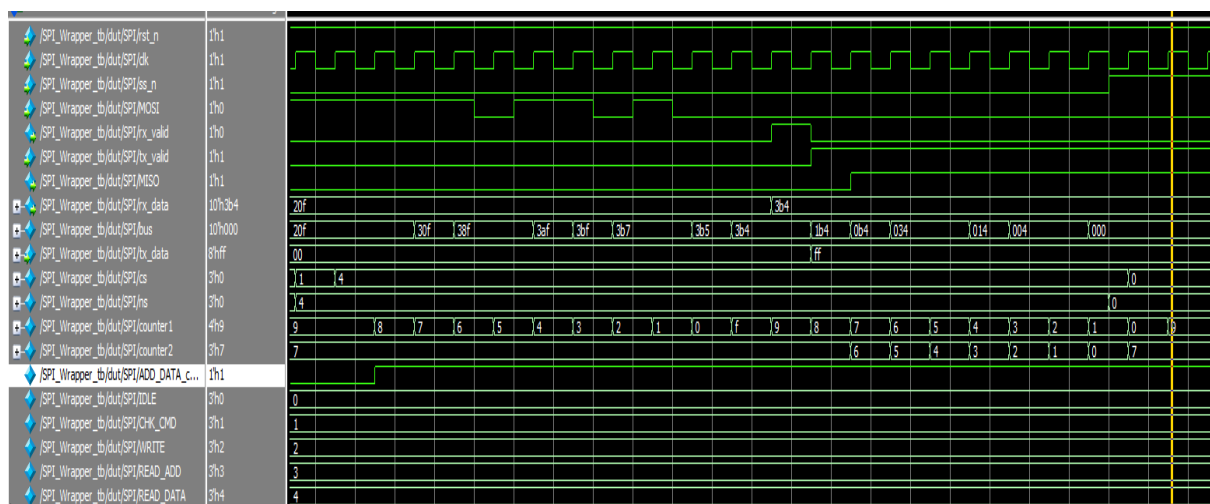
### • WRITE state (Data):



## • READ\_ADD state:

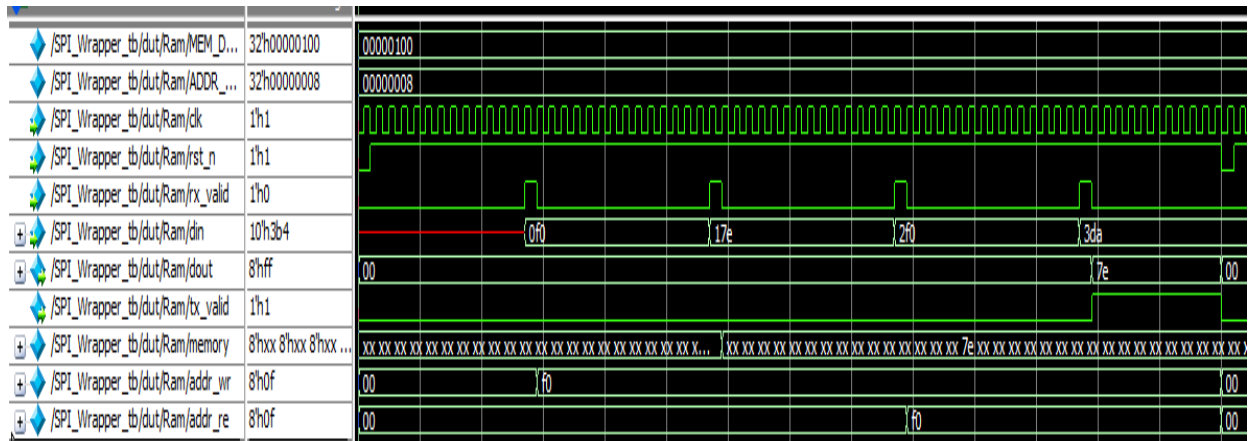


## • READ\_DATA state:

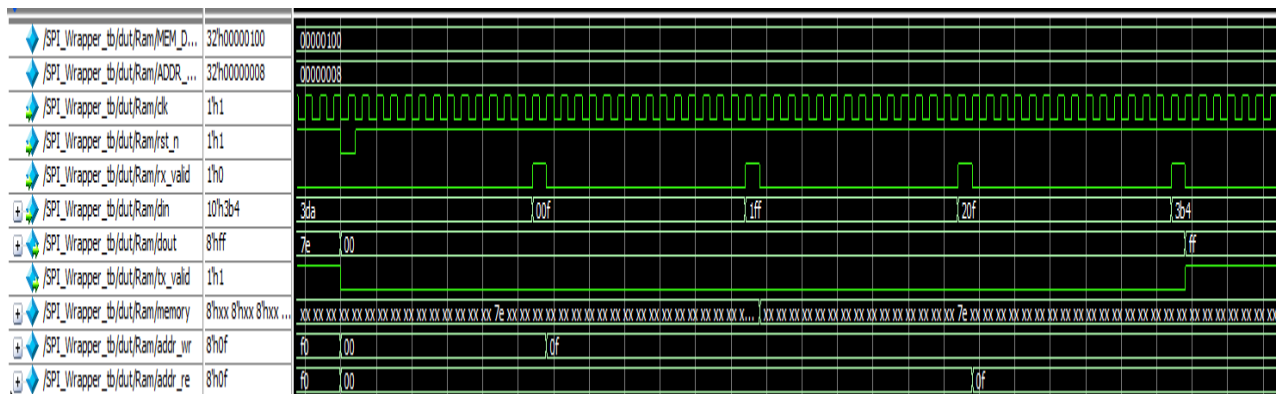


## Snapshots of RAM:

- First scenario:



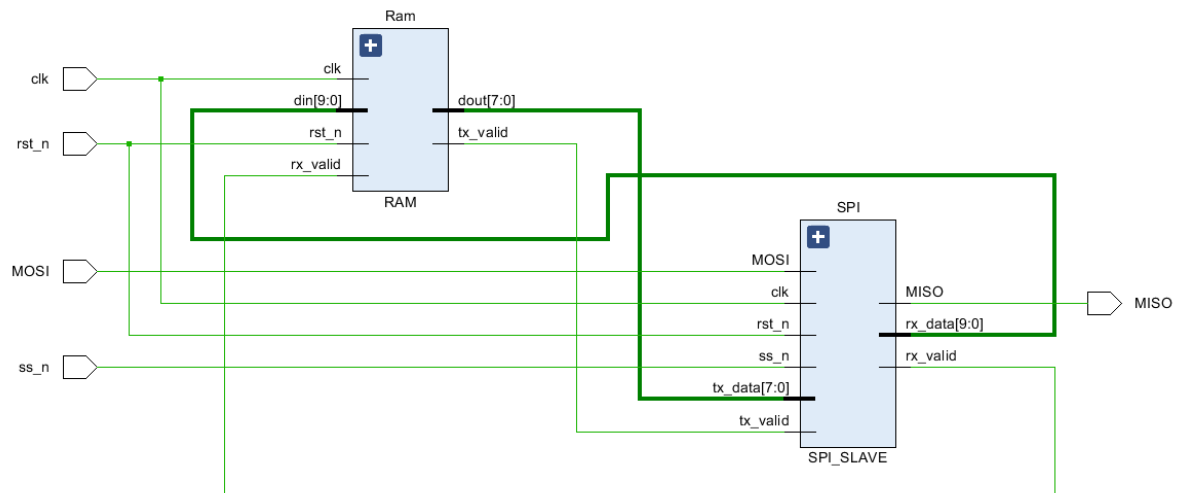
- Second scenario:



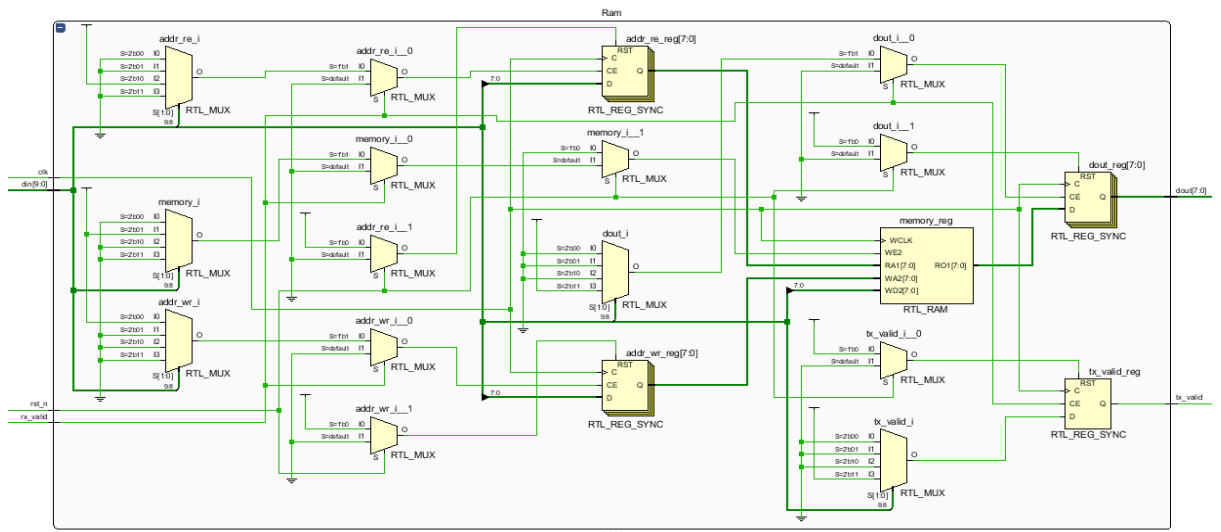
# Vivado:

- Elaboration:

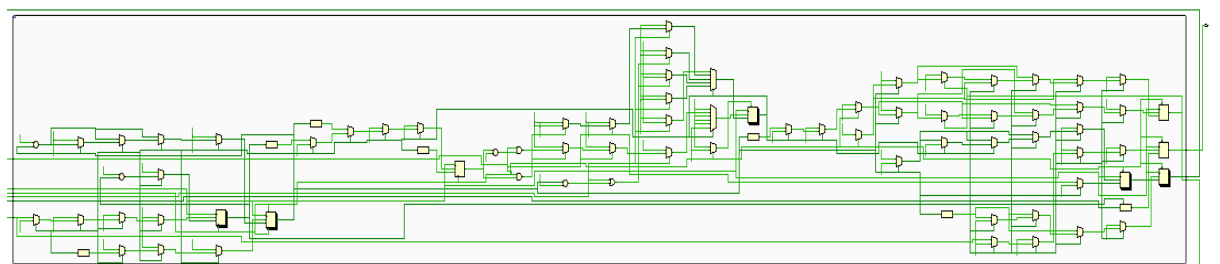
- System:



- Ram:



- SPI:



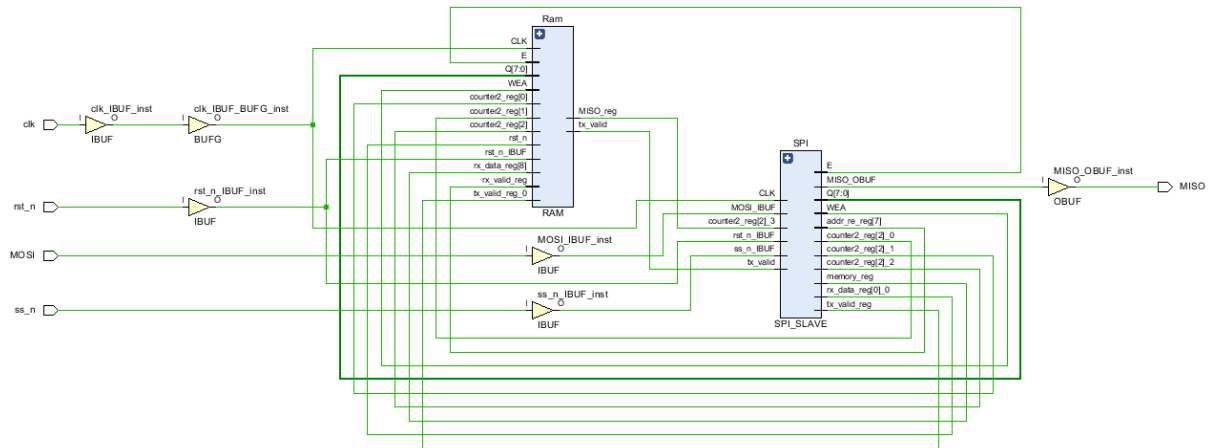


- **Synthesis:**

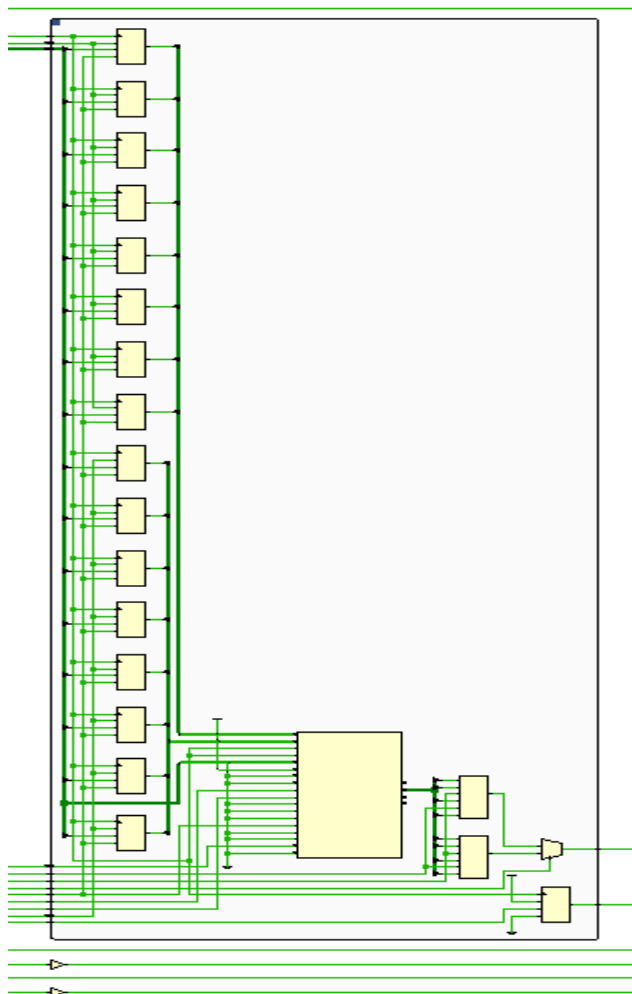
- **Seq:**

- **Schematic:**

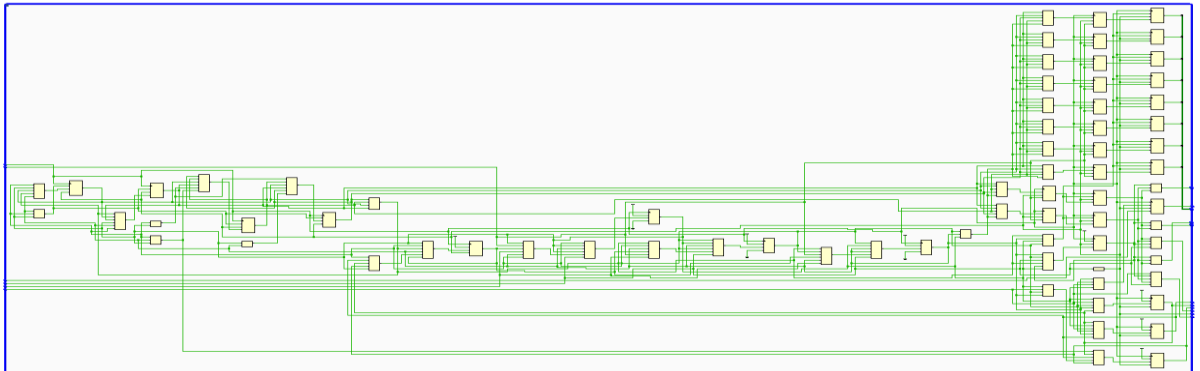
- **System:**



- **Ram:**



- SPI:



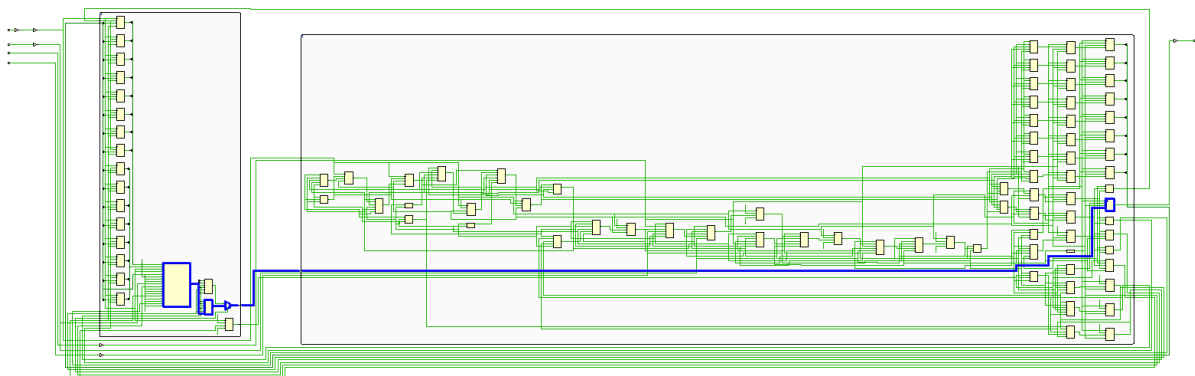
- Encoding Report:

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	011
READ_DATA	100	100

- Timing Summary:

Timing			
Design Timing Summary			
Worst Negative Slack (WNS):	6.261 ns	Worst Hold Slack (WHS):	0.146 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	108	Total Number of Endpoints:	108
All user specified timing constraints are met.			

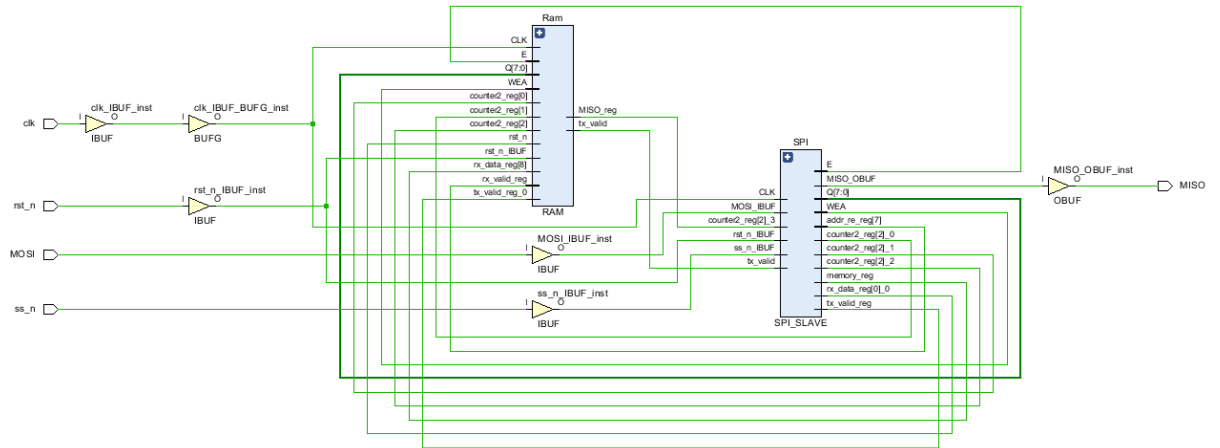
- Critical Path:



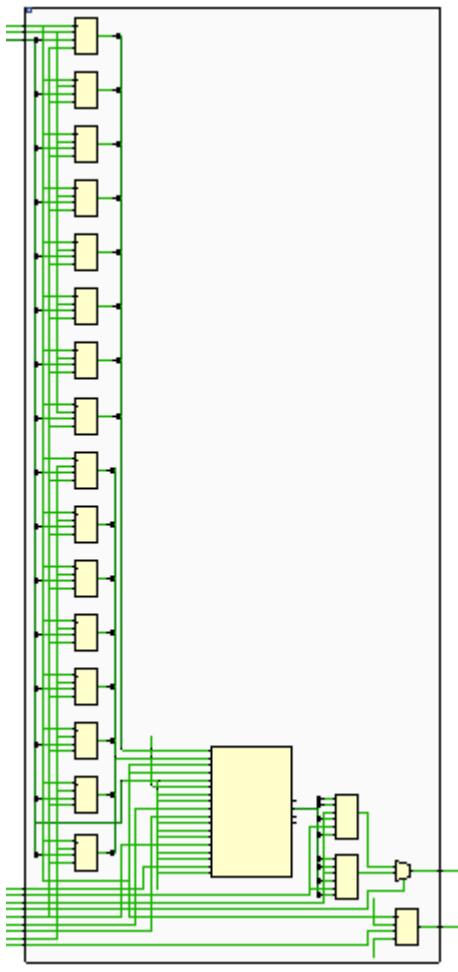
## ○ Gray:

### ■ Schematic:

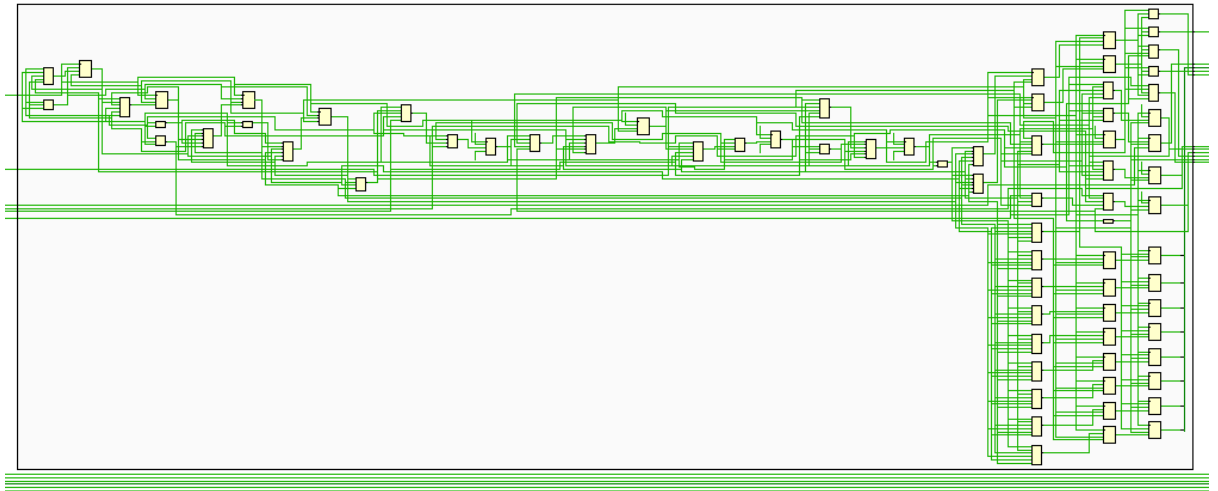
#### ● System:



#### ● Ram:



- SPI:



- Encoding Report:

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	011
READ_DATA	111	100

- Timing Summary:

Timing

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (4)

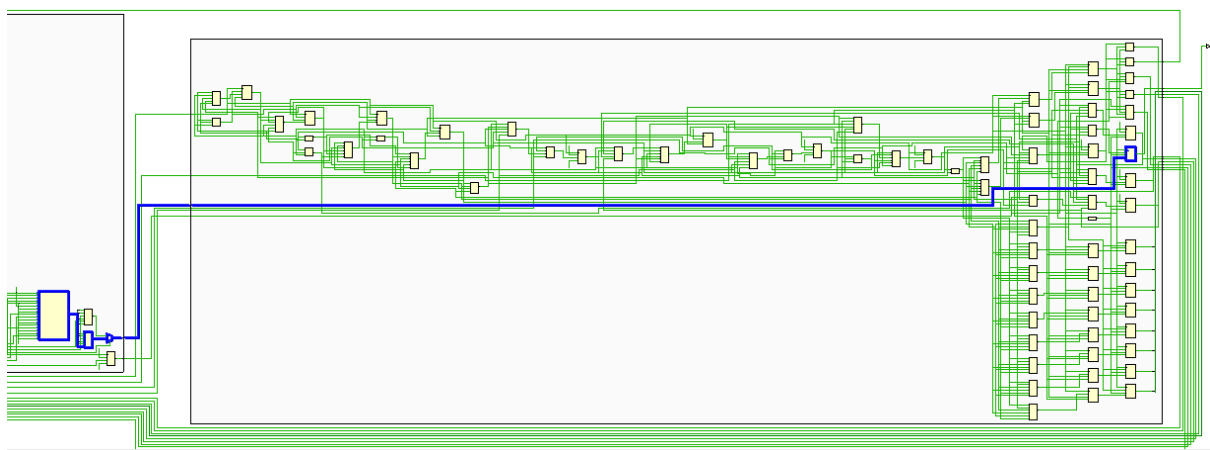
Intra-Clock Paths

Design Timing Summary

Worst Negative Slack (WNS):	6.261 ns	Worst Hold Slack (WHS):	0.146 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	108	Total Number of Endpoints:	108	Total Number of Endpoints:	53

All user specified timing constraints are met.

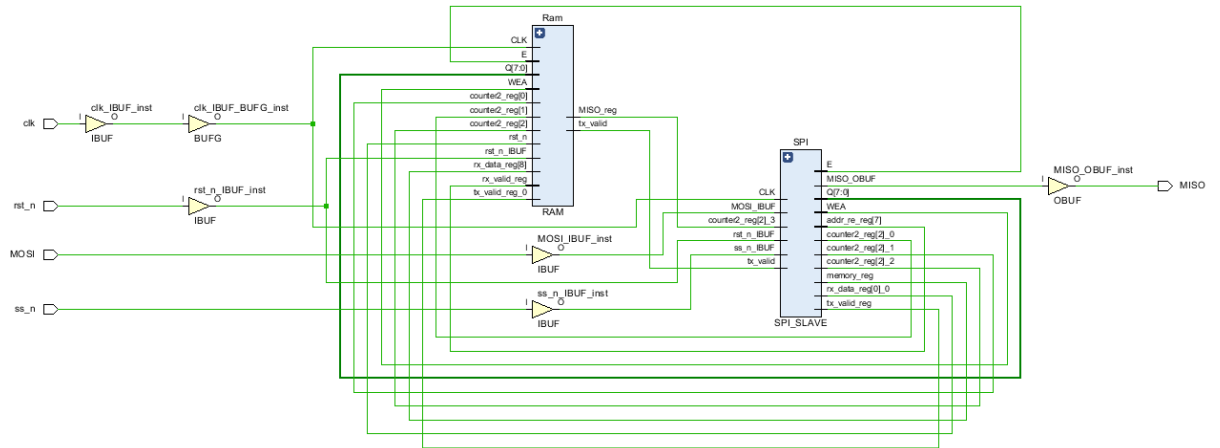
- Critical Path:



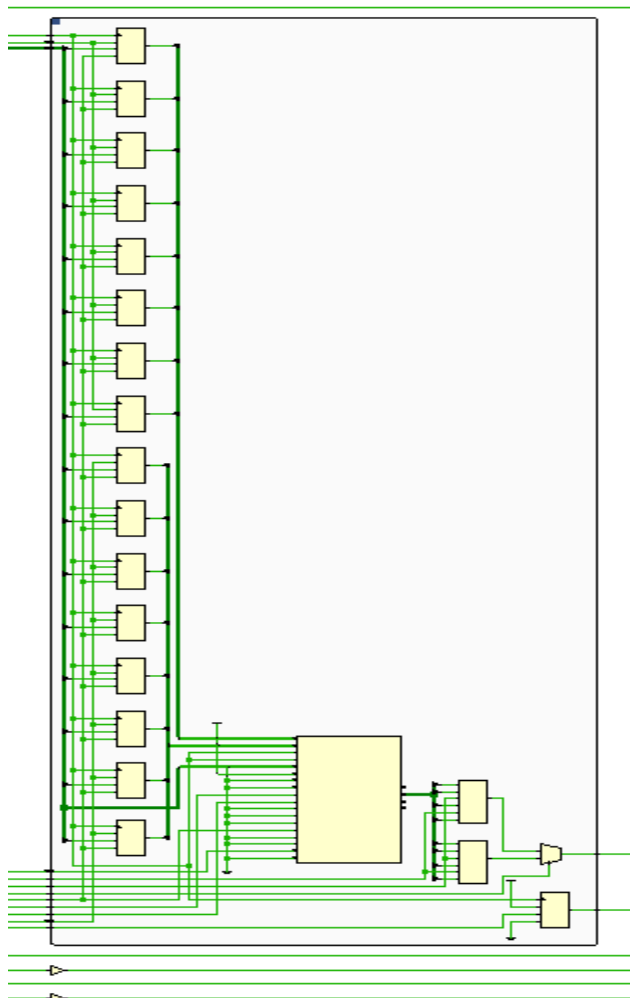
## ○ One\_Hot:

### ■ Schematic:

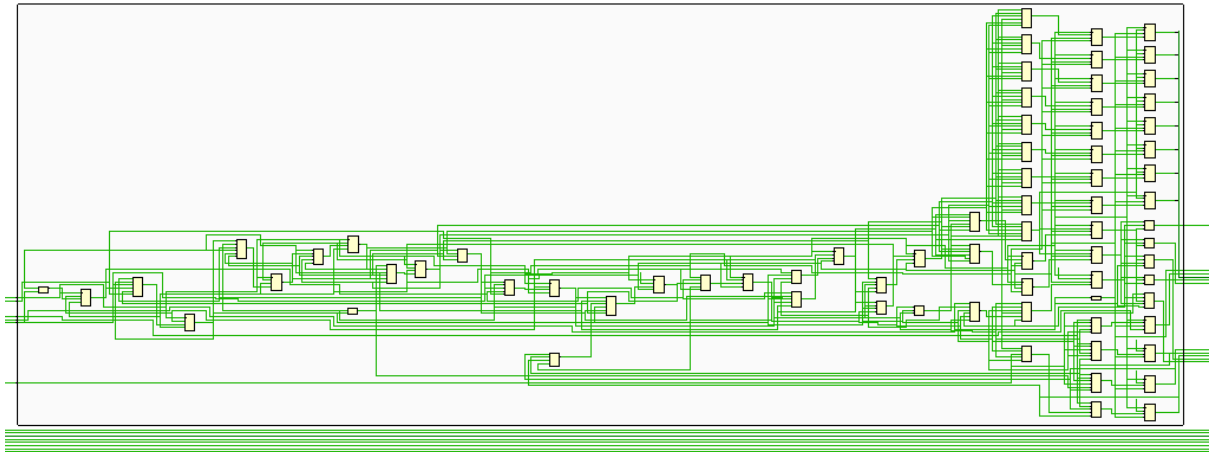
#### ● System:



#### ● Ram:



- SPI:



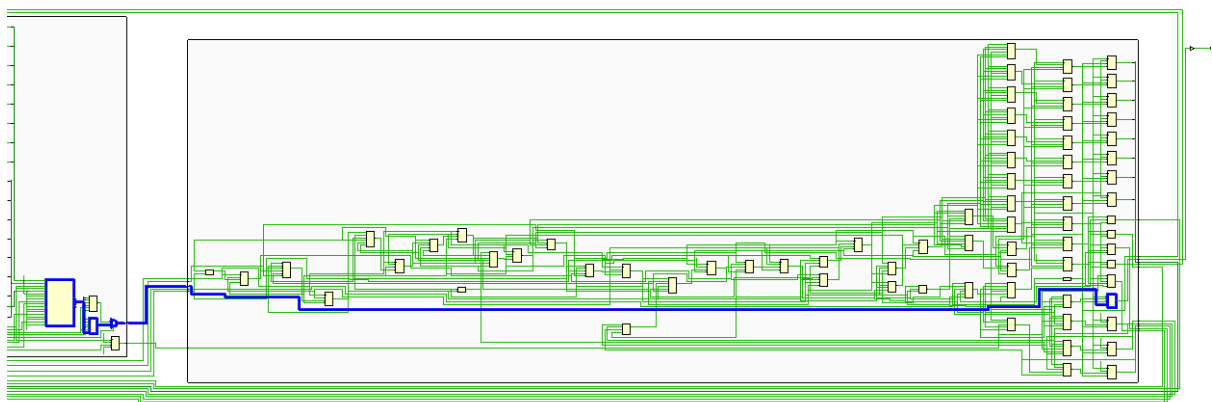
- Encoding Report:

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	011
READ_DATA	10000	100

- Timing Summary:

<div>Timer Settings</div> <div>Design Timing Summary</div> <div>Clock Summary (1)</div> <div>&gt; Check Timing (4)</div> <div>✓ Intra-Clock Paths</div> <div>    ✓ sys_clk_pin</div> <div>        Setup 6.261 ns (10)</div>	<div>Setup</div> <div>Worst Negative Slack (WNS): 6.261 ns</div> <div>Total Negative Slack (TNS): 0.000 ns</div> <div>Number of Failing Endpoints: 0</div> <div>Total Number of Endpoints: 115</div>	<div>Hold</div> <div>Worst Hold Slack (WHS): 0.148 ns</div> <div>Total Hold Slack (THS): 0.000 ns</div> <div>Number of Failing Endpoints: 0</div> <div>Total Number of Endpoints: 115</div>	<div>Pulse Width</div> <div>Worst Pulse Width Slack (WPWS): 4.500 ns</div> <div>Total Pulse Width Negative Slack (TPWS): 0.000 ns</div> <div>Number of Failing Endpoints: 0</div> <div>Total Number of Endpoints: 55</div>
	All user specified timing constraints are met.		

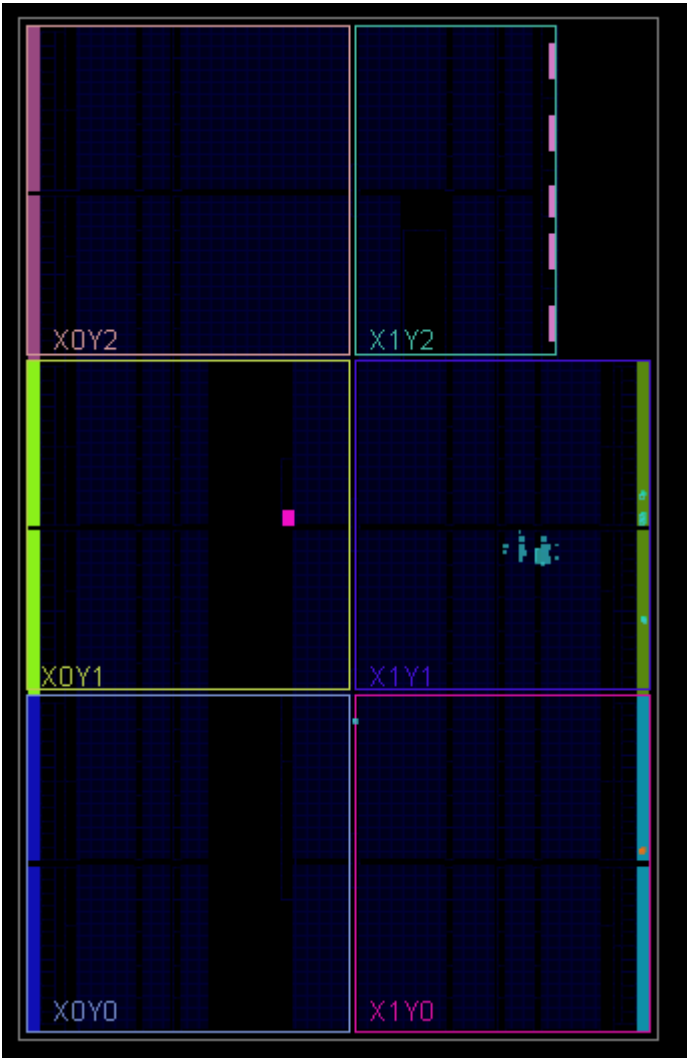
- Critical Path:



- Implementation:

- Seq:

- Schematic:



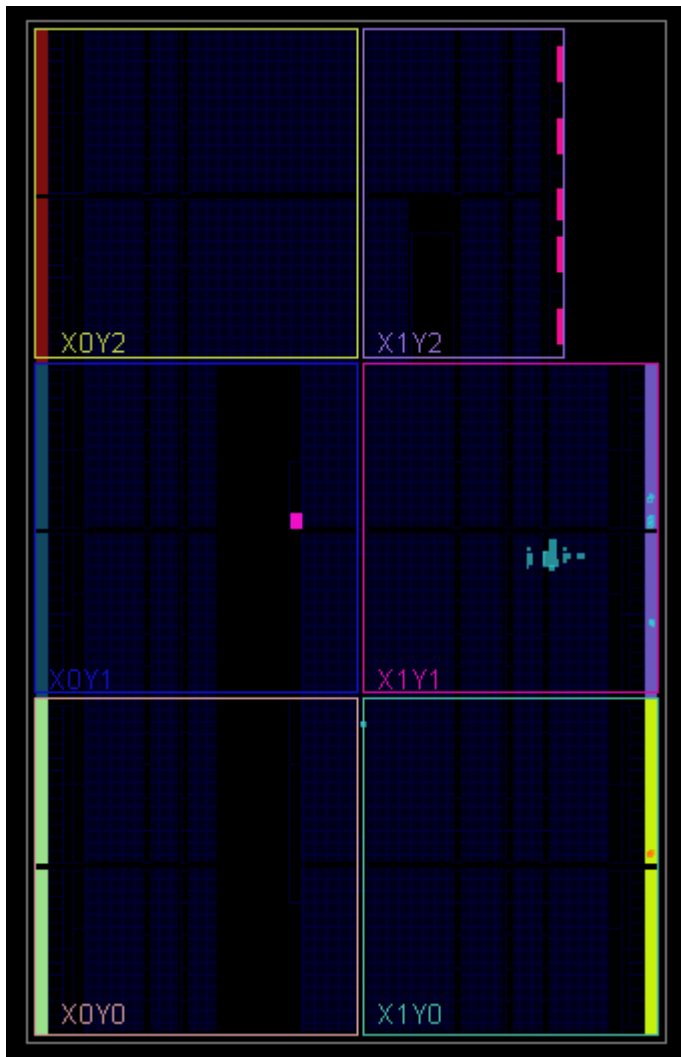
- Timing:

Design Timing Summary			
Setup		Hold	Pulse Width
Worst Negative Slack (WNS): 6.118 ns		Worst Hold Slack (WHS): 0.098 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0		Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 109		Total Number of Endpoints: 109	Total Number of Endpoints: 53
All user specified timing constraints are met.			

- Utilization:

Hierarchy		Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
Summary											
▼ Slice Logic											
▼ Slice LUTs (<1%)											
LUT as Logic (<1%)		▼ N SPL_Wrapper	42	50	1	24	42	13	0.5	5	1
F7 Muxes (<1%)		▼ Ram (RAM)	3	17	1	6	3	0	0.5	0	0
▼ Slice Registers (<1%)		▼ SPI (SPI_SLAVE)	39	33	0	21	39	12	0	0	0

- Gray:
- Schematic:



- Timing:

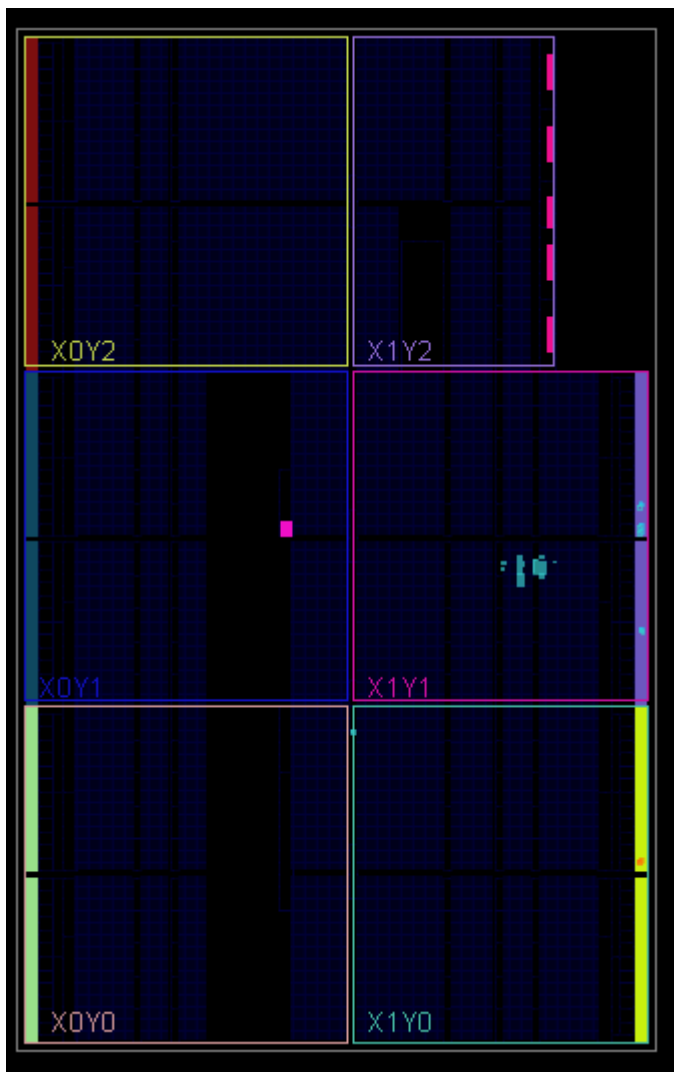
General Information			Setup			Hold			Pulse Width		
Timer Settings			Worst Negative Slack (WNS):			Worst Hold Slack (WHS):			Worst Pulse Width Slack (WPWS):		
Design Timing Summary			Total Negative Slack (TNS):			Total Hold Slack (THS):			Total Pulse Width Negative Slack (TPWS):		
Clock Summary (1)			Number of Failing Endpoints:			Number of Failing Endpoints:			Number of Failing Endpoints:		
Check Timing (4)			Total Number of Endpoints:			Total Number of Endpoints:			Total Number of Endpoints:		
Intra-Clock Paths			All user specified timing constraints are met.								
Inter-Clock Paths											
Other Path Groups											

- Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_Wrapper	44	50	1	21	44	13	0.5	5	1
Ram (RAM)	3	17	1	5	3	0	0.5	0	0
SPI (SPI_SLAVE)	41	33	0	18	41	12	0	0	0



- One\_Hot:
  - Schematic:



- Timing:

Design Timing Summary			
General Information	Setup	Hold	Pulse Width
Timer Settings	Worst Negative Slack (WNS): 5.954 ns	Worst Hold Slack (WHS): 0.050 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Design Timing Summary	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Clock Summary (1)	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
> Check Timing (4)	Total Number of Endpoints: 116	Total Number of Endpoints: 116	Total Number of Endpoints: 55
> Intra-Clock Paths	All user specified timing constraints are met.		
> sys_clk_pin			
Inter-/Intra Paths			

- Utilization:

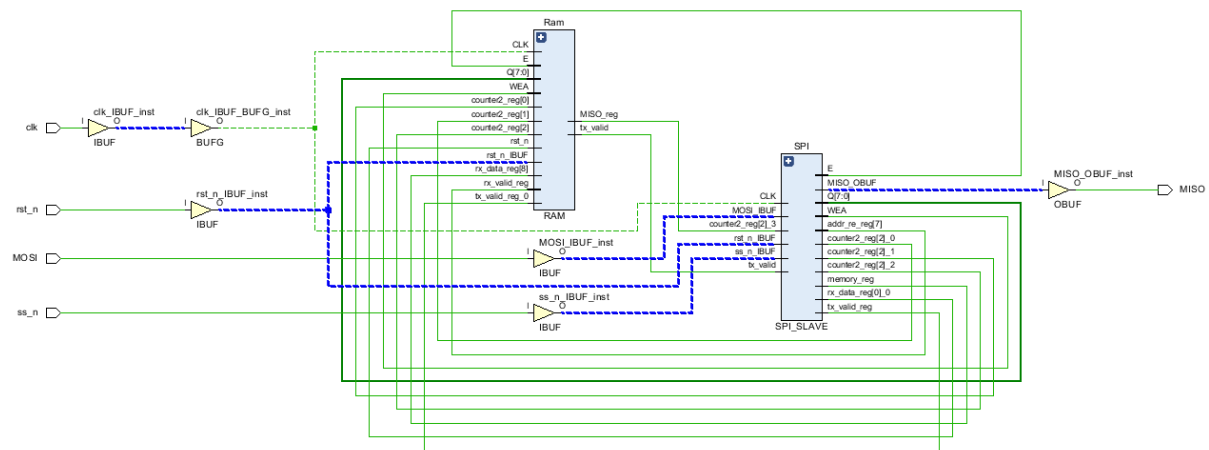
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPL_Wrapper	42	52	1	21	42	15	0.5	5	1
I Ram (RAM)	3	17	1	5	3	0	0.5	0	0
I SPI (SPI_SLAVE)	39	35	0	19	39	14	0	0	0

From the results we found that the best encoding is **seq.**

- Messages:



- Debugged Design:



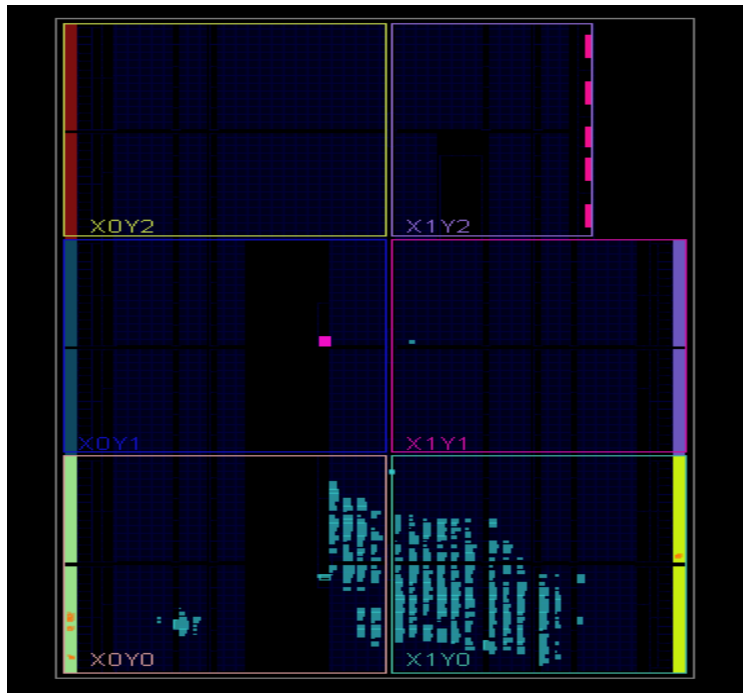
- Timing after debug:

General Information			
Timer Settings			
Design Timing Summary			
Clock Summary (2)			
Check Timing (4)			
Intra-Clock Paths			
Inter-Clock Paths			
Other Path Groups			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 2.745 ns	Worst Hold Slack (WHS): 0.041 ns	Worst Pulse Width Slack (WPWS): 3.750 ns	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Total Number of Endpoints: 3894	Total Number of Endpoints: 3878	Total Number of Endpoints: 2153	
All user specified timing constraints are met.			

- Messages after debug:



- **Implementation of Device after Debug:**



- **Bitstream Successfull:**

